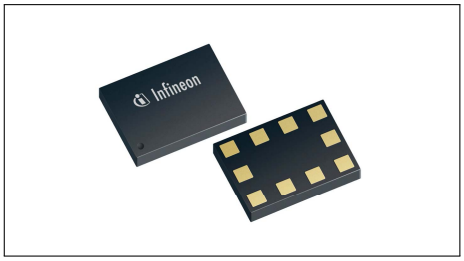
BGSA143GL10

Low Resistance Antenna Tuning Switch

Features

- Designed for high-linearity antenna tuning switching and RF tuning applications
- Ultra low R_{ON} resistance of 1.15 Ω at each port in ON state
- Low C_{OFF} capacitance of 140 fF at each port in OFF state
- High RF operating peak voltage handling of 42 V in OFF state
- Resonance-Stopper Antenna Tuning
- Low harmonic generation
- 3 GPIO pins control interface
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



1.1 x 1.5 mm^2

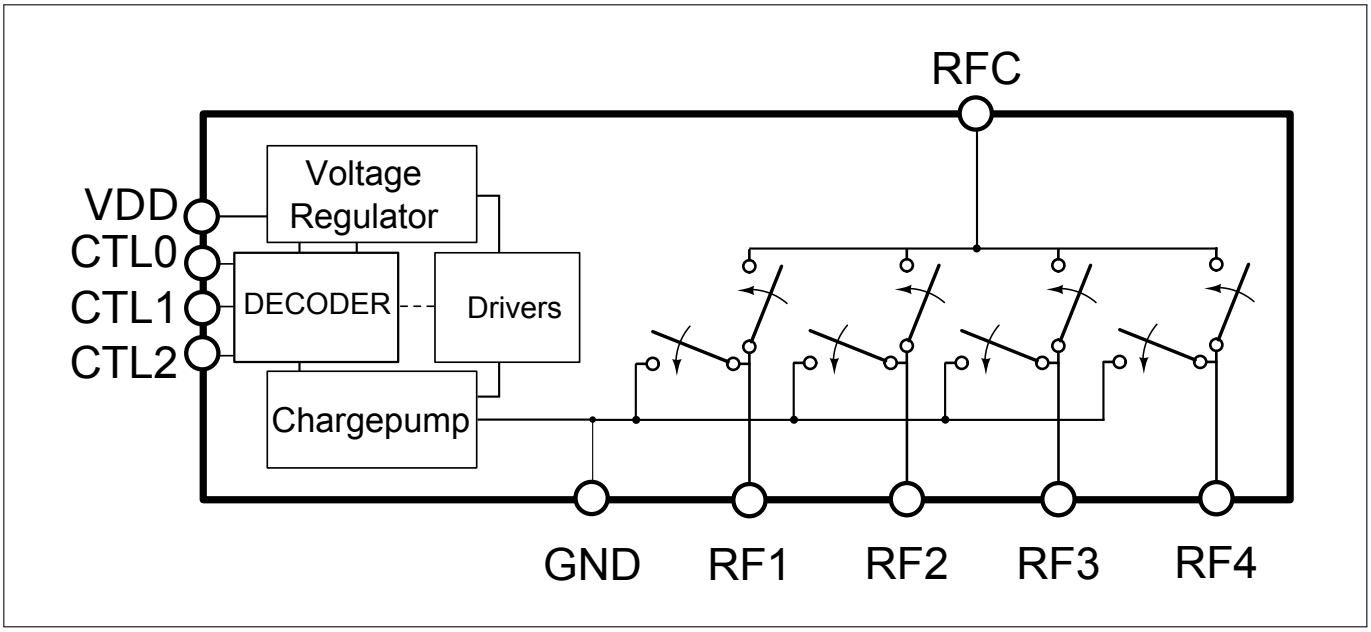
Application

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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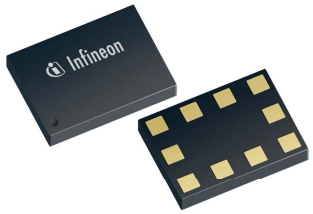
1 Features



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RoHS Halogen-Free Lead-Free Green

Description

The BGSA143GL10 is a small and versatile Single-Pole Quad Throw (SP4T) RF switch optimized for low C_{off} as well as low R_{on} enabling applications up to 6.0 GHz. GPIO digital control lines offer the possibility to adopt SP4T, SPDT along with SPST topology for an optimum flexibility in RF Front-end designs.

The BGSA143GL10 is ideal for high Q tuning applications. This single supply chip integrates on-chip CMOS logic control. It can be driven by 2 or 3 CMOS or TTL compatible control input signals. Due to its high RF voltage ruggedness and OFF RF ports reflective short feature, it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses, also mitigating or even eradicating unwanted parasitic RF resonances.

Product Name	Marking	Package
BGSA143GL10	K9	TSLP-10-2

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	–	GHz	[1]
Supply voltage [2]	V_{DD}	-0.5	–	6.0	V	Only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_max}	–	–	40	dBm	Pulsed RF input power, duty cycle of 25 % with T_period= 4620 μs, ON-state, setup as of Fig. 2
RF peak voltage	V_{RF_max}	–	–	50	V	Short term peaks (1μs, duty cycle 0.1%), Isolation mode, test setup acc. Fig. 1 and exceeding typical linearity, R_{ON} and C_{OFF} parameters
ESD capability, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD capability, HBM [4]	$V_{ESD_{HBM}}$	-0.6	–	+0.6	kV	
ESD capability, system level (RF port) [5]	$V_{ESD_{ANT}}$	-8	–	+8	kV	RFx vs system GND, with 27 nH shunt inductor on tested port
Junction temperature	T_j	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	–	43	K/W	–
Control Voltage Levels	V_{Ctrl}	-0.7	–	V_{Ctrl}+0.7 (max. 3.6)	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{IO}. A high RF ripple at the V_{IO} can exceed the maximum ratings by $V_{Ctrl} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002 Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

Maximum Ratings

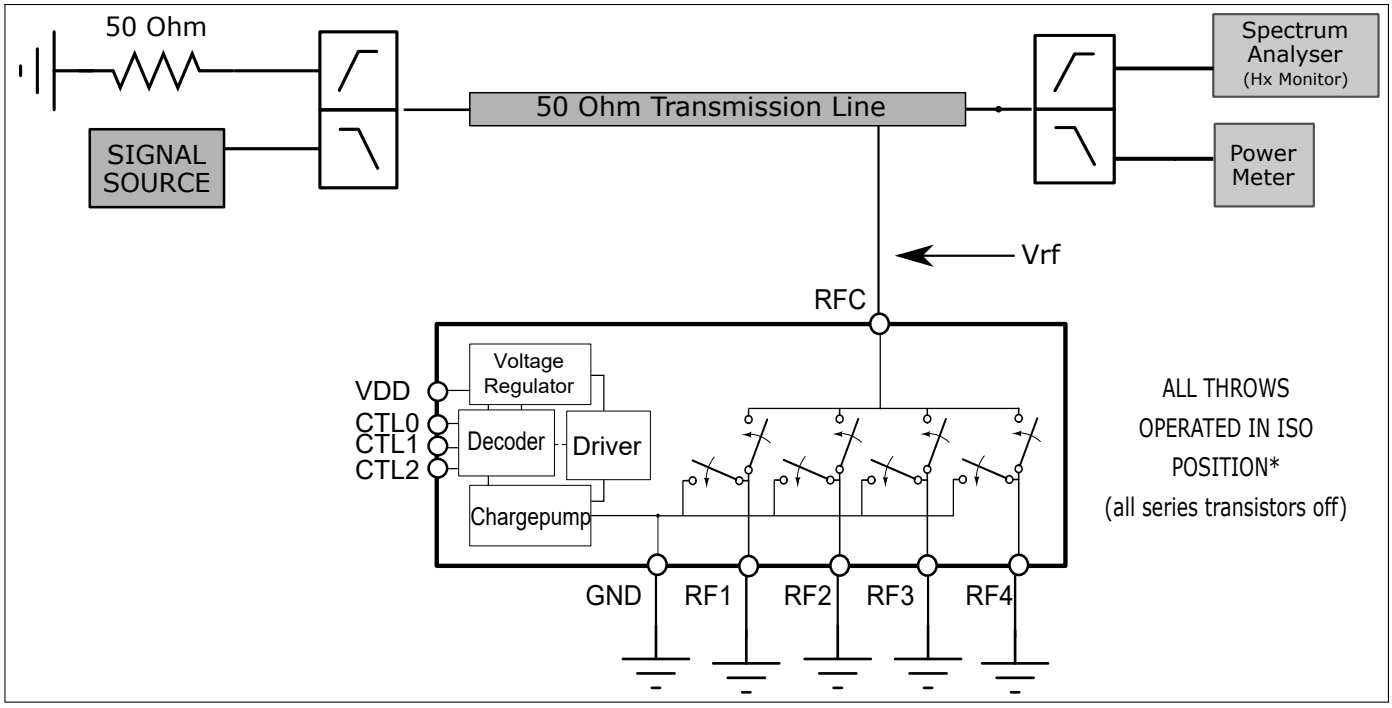

Figure 1: RF operating voltage measurement configuration - OFF mode

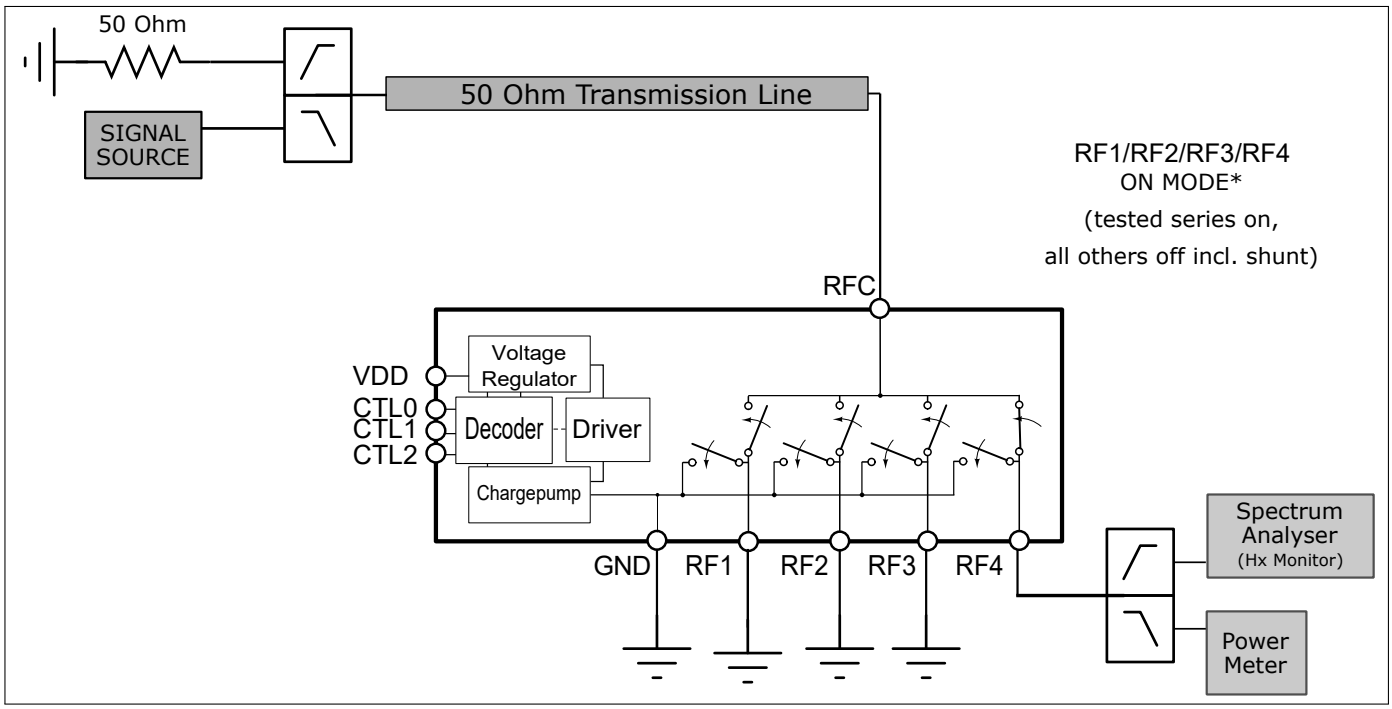

Figure 2: RF operating and Harmonics generation measurement configuration - RFx ON mode

3 DC Characteristics

Table 2: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.65	2.8	3.6	V	–
Supply current	I_{DD}	45	60	200[1]	µA	[1] T_A = 85 °C, P_{IN} = 36 dBm, ON mode
Control voltage low	$V_{Ctrl,low}$	0	–	0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} < V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	µA	–
Control current high	$I_{Ctrl,high}$	-1	0	4	µA	$V_{Ctrl,high} < V_{DD}$ 1 MΩ Pull-Down resistor at Control Pins
Ambient temperature	T_A	-40	25	85	°C	–
Power Up Settling Time	t_{Pup}	–	10	25	µs	Time from V_{DD} Min. power level to 90 % RF-signal
Switching Time	t_{ST}	–	5	8	µs	Time between RF states in active mode $V_{Ctl,high}$ Min. or $V_{Ctl,low}$ Max. level to 90 % RF-signal
RF Rise Time	t_{RT}	–	1	5	µs	Time between 10 % to 90 % RF-signal

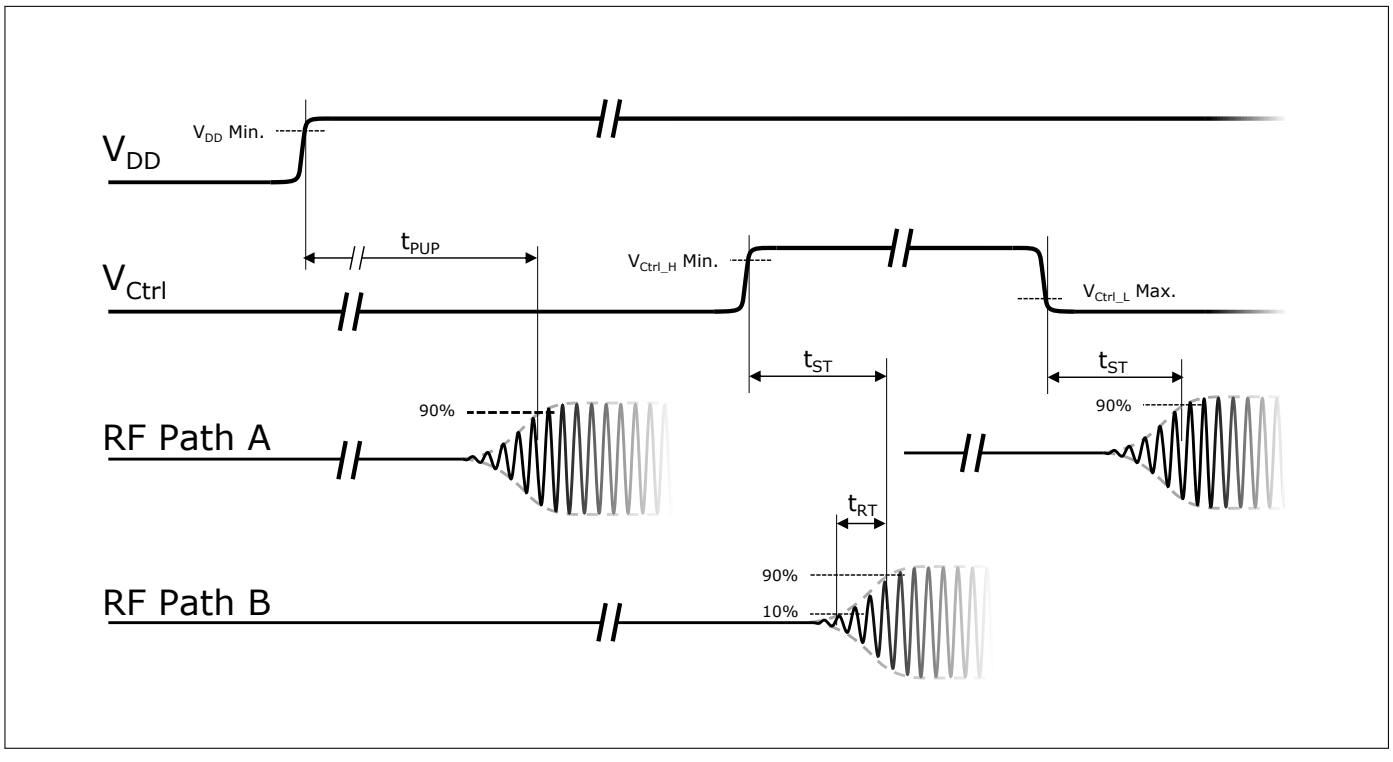

Figure 3: BGSA143GL10 Switching Time Behavior

4 RF Small Signal Characteristics

Table 3: Parametric specifications

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Frequency range	f	0.4		6.0	GHz	$T_A = -40\,°C... + 85\,°C$, $Z_0 = 50\,\Omega$
RFx to RFc ON DC resistance	R_{ON}		1.15		Ω	
RFx to RFc OFF DC resistance	R_{OFF}	–	200	–	kΩ	
RFx to GND ON DC resistance	$R_{ON,Shunt}$		5.9		Ω	
RFx to GND OFF DC resistance	$R_{OFF,Shunt}$	–	200	–	kΩ	
RFx to RFc[1] OFF capacitance	C_{OFF}	–	140	–	fF	

[1] C_{OFF} represents the series capacitance RFx to GND. It is fitting to the Isolation Values for OPEN Shunts.

Table 4: RF electrical parameters

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Insertion Loss: RF1 to RFc, RF2 to RFc, RF3 to RFc or RF4 to RFc [1,2,3,4]						
698 - 960 MHz	IL_{SP4T}		0.18	0.3	dB	Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz			0.35	0.6	dB	
1981 - 2169 MHz			0.40	0.7	dB	
2170 - 2690 MHz			0.50	0.9	dB	
3400 - 3800 MHz			0.95	1.4	dB	
5000 - 6000 MHz			2.05	3.2	dB	
Return Loss: RF1, RF2, RF3 or RF4 [1,2,3,4]						
698 - 960 MHz	RL_{SP4T}	15	24		dB	Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		11	16		dB	
1981 - 2169 MHz		10	15		dB	
2170 - 2690 MHz		9.6	13		dB	
3400 - 3800 MHz		7.1	10		dB	
5000 - 6000 MHz		5.0	7.3		dB	
Isolation: All RF OFF[1,2,3,4]						
698 - 960 MHz	ISO_{OFF}	32	38		dB	Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		22	27		dB	
1981 - 2169 MHz		21	26		dB	
2170 - 2690 MHz		17	24		dB	
3400 - 3800 MHz		14	19		dB	
5000 - 6000 MHz		10	14		dB	

[1] Valid for all RF power levels, no compression behavior
[2] Network analyser input power: P_{IN} = −20 *dBm*
[3] On application board without any matching components
[4] OFF port shunts switches closed

5 RF large signal parameter

Table 5: RF large signal specifications at T_A = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF Operating Voltage	V_{RF_opr}			42	V	In Isolation mode, test condition schematic in Fig. 1 for H2/H3 <-42 dBm @50 Ω
Harmonic Generation up to 12.75 GHz						
All RF Ports - Second Order Harmonics	P_{H2}	–	-86	–	dBm	25 dBm, 50 Ω, f_0 = 698 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-91	–	dBm	25 dBm, 50 Ω, f_0 = 698 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	-67	–	dBm	35 dBm, 50 Ω, f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-63	–	dBm	35 dBm, 50 Ω, f_0 = 824 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	-65	–	dBm	33 dBm, 50 Ω, f_0 = 1960 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-66	–	dBm	33 dBm, 50 Ω, f_0 = 1960 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	-75	–	dBm	25 dBm, 50 Ω, f_0 = 2500 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-85	–	dBm	25 dBm, 50 Ω, f_0 = 2500 MHz
All RF Ports	P_{Hx}	-80	–	–	dBm	25 dBm, 50 Ω
Intermodulation Distortion IMD2						
IIP2, low	$IIP2, l$	–	120	–	dBm	IIP2 conditions Tab. 6
IIP2, high	$IIP2, h$	–	130	–	dBm	
Intermodulation Distortion IMD3						
IIP3	$IIP3$	–	78	–	dBm	IIP3 conditions Tab. 7

RF large signal parameter

Table 6: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 7: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

6 Logic Truth Table

Table 8: Modes of Operation

State	Mode	CTL2	CTL1	CTL0
1	RF1 to RFc on [1]	0	0	0
2	RF2 to RFc on [1]	0	0	1
3	RF3 to RFc on [1]	0	1	0
4	RF4 to RFc on [1]	0	1	1
5	RFc isolated from all RFx all RFx ports shunt to GND	1	0	0
6	RF1 to RFc on, RF4 to RFc on [1]	1	0	1
7	RF2 to RFc on, RF3 to RFc on [1]	1	1	0
8	all RFx to RFc on	1	1	1

[1] all other RFx ports Shunt to GND

7 Application Information

Pin Configuration and Function

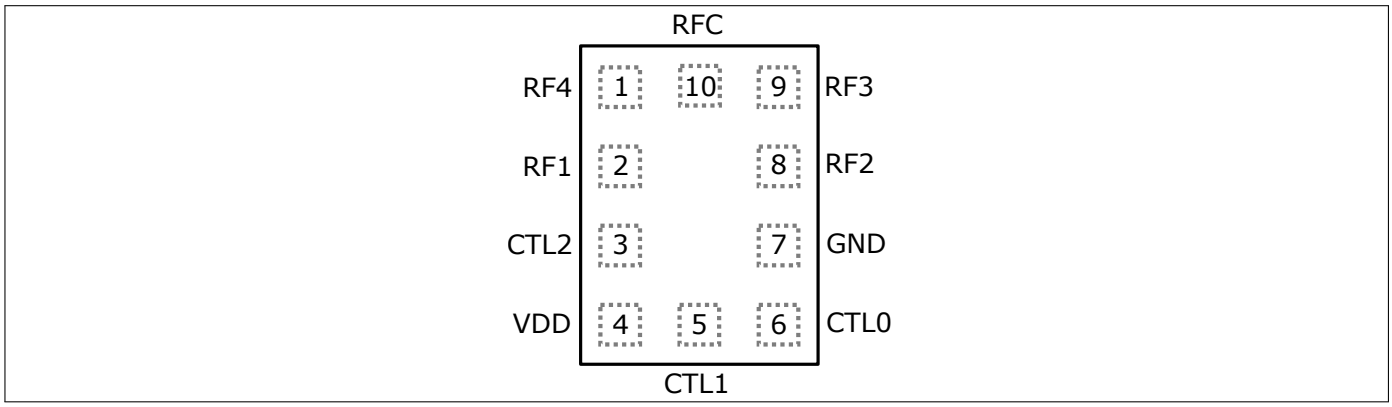

Figure 4: BGSA143GL10 Pin Configuration (top view)

Table 9: Pin definition and function

Pin No.	Name	Function
1	RF4	RF4 Port
2	RF1	RF1 Port
3	CTL2	GPIO Control
4	VDD	Power Supply
5	CTL1	GPIO Control
6	CTL0	GPIO Control
7	GND	Ground
8	RF2	RF2 Port
9	RF3	RF3 Port
10	RFC	Common RF Port

8 Package Information

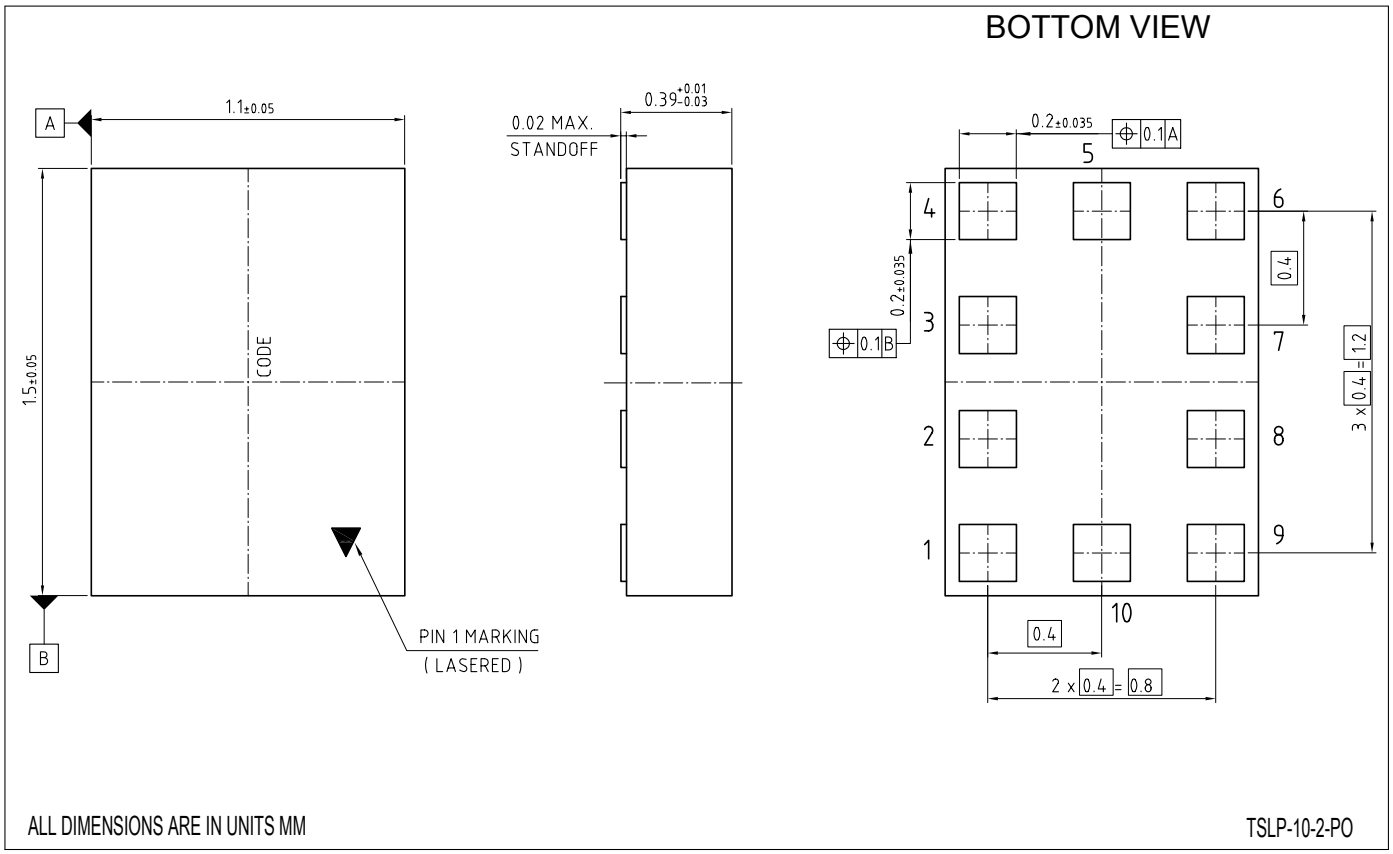

Figure 5: TSLP-10-2 Package Outline (top, side and bottom views)

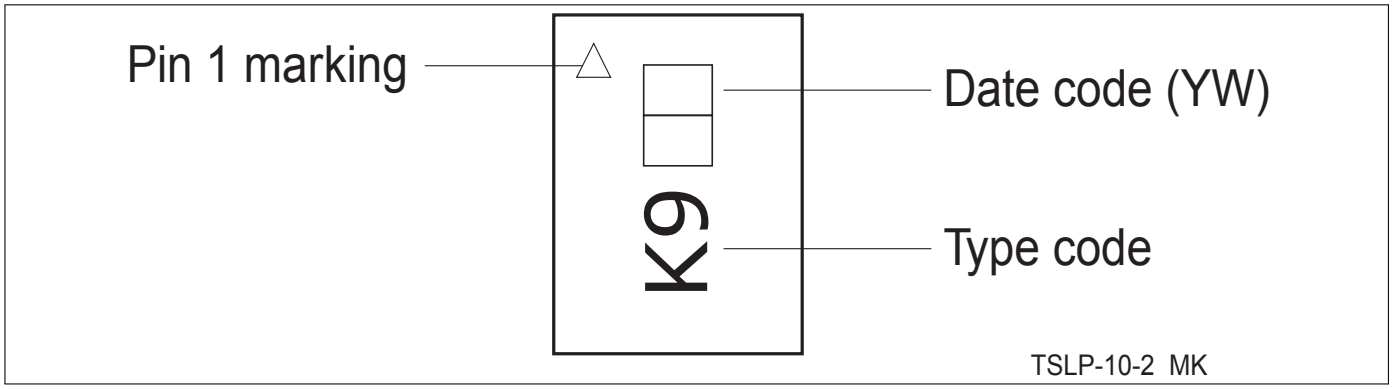

Figure 6: Marking Specification (top view): Date code digits Y and W defined in Table 10/11

Table 10: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

Table 11: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

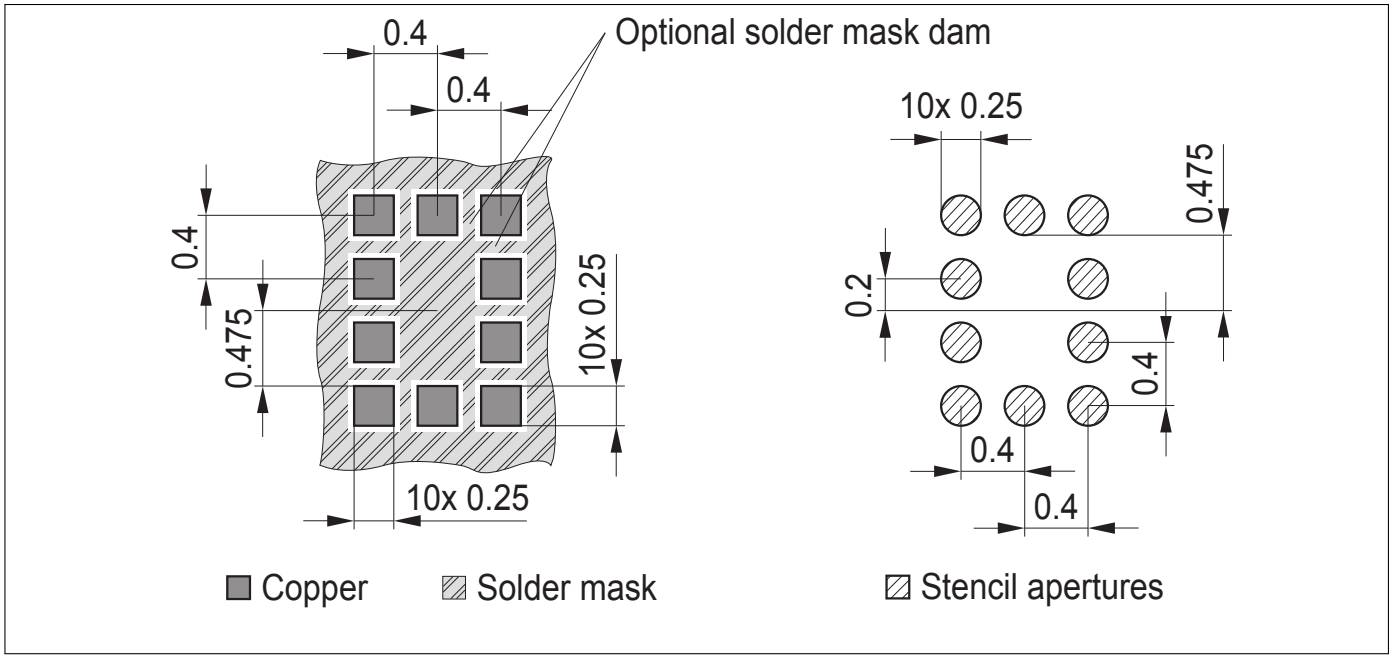

Figure 7: Footprint Recommendation

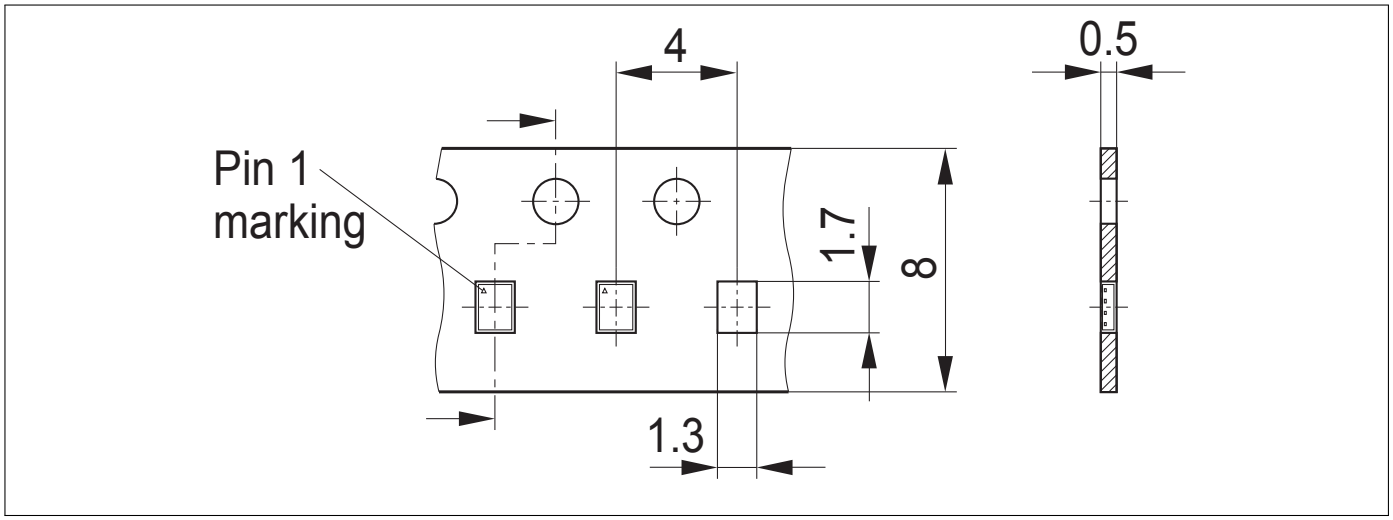

Figure 8: TSLP-10-2 Carrier Tape

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.2, 2025-04-22	
Revision 2.2	Marking update

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