

BGF106

SIM Card Interface Filter and ESD Protection

Small Signal Discretes



Never stop thinking

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BGF106

Revision History: 2008-02-19, V2.2

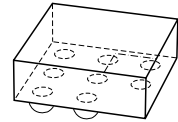
Previous Version: 2007-12-19, V2.1

Page	Subjects (major changes since last revision)
5	Figure 2 updated

BGF106

Features

- ESD protection circuit and interface filter for SIM cards
- Integrated ESD protection of external pins up to 15 kV contact discharge according to IEC61000-4-2
- Wafer level package with SnAgCu solder balls
- 400 μm solder ball pitch
- RoHS and WEEE compliant package



WLP-8-8-N-3D



Description

The BGF106 is an ESD protection circuit and filtering interface for SIM cards. The external pins are protected against ESD up to 15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green leadfree package with a size of only 1.2 mm x 1.2 mm and a total height of 0.6 mm

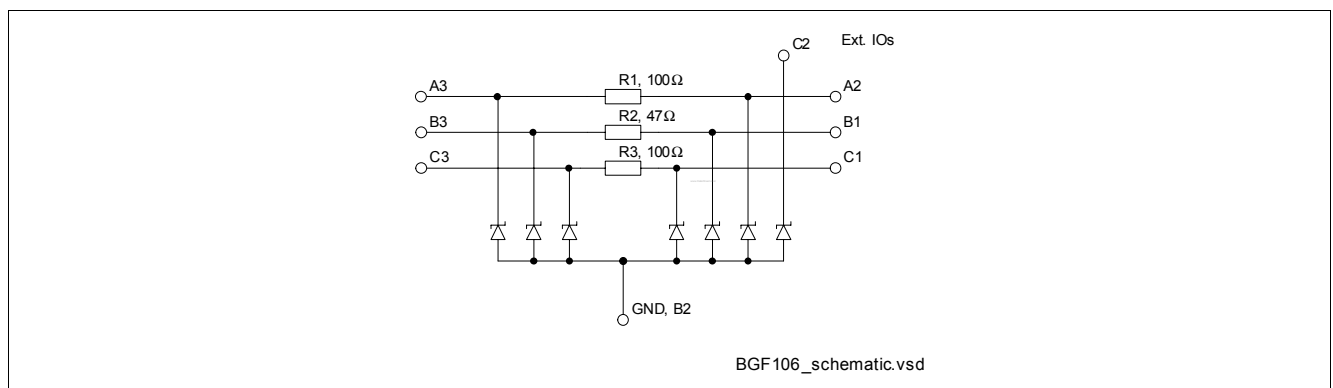


Figure 1 Schematic

Type	Package	Marking	Chip
BGF106	WLP-8-8	GF106	N0727

Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_P	0	—	5	V	—
Operating temperature range	T_{OP}	-40	—	+85	°C	—
Storage temperature range	T_{STG}	-65	—	+150	°C	—
Summed up into power for all pins	P_{in}	—	—	60	mW	$T_S < 70\text{ °C}$

Electrostatic Discharge According to IEC61000-4-2

Contact discharge at internal pins A3, B3, C3	V_{ESD}	-2	—	2	kV	—
Contact discharge at external pins A2, B1, C1, C2	V_{ESD}	-15	—	15	kV	—

Table 2 **Electrical Characteristics**¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistors R_1, R_3	$R_{1,3}$	80	100	120	Ω	–
Resistor R_2	R_2	37.6	47	56.4	Ω	–
Reverse current of ESD protection diodes	I_R	–	1	100	nA	$V = 3 \text{ V}$
			2	1000	nA	$V = 5 \text{ V}$
Breakdown voltage of ESD diodes	$V_{(BR)}$	6.5	7.8	–	V	$I_{(BR)} = 1 \text{ mA}$
Line capacitance Capacitance of all lines to GND	C_T	–	16.5	20	pF	$V = 0 \text{ V}$

1) at $T_A = 25^\circ\text{C}$

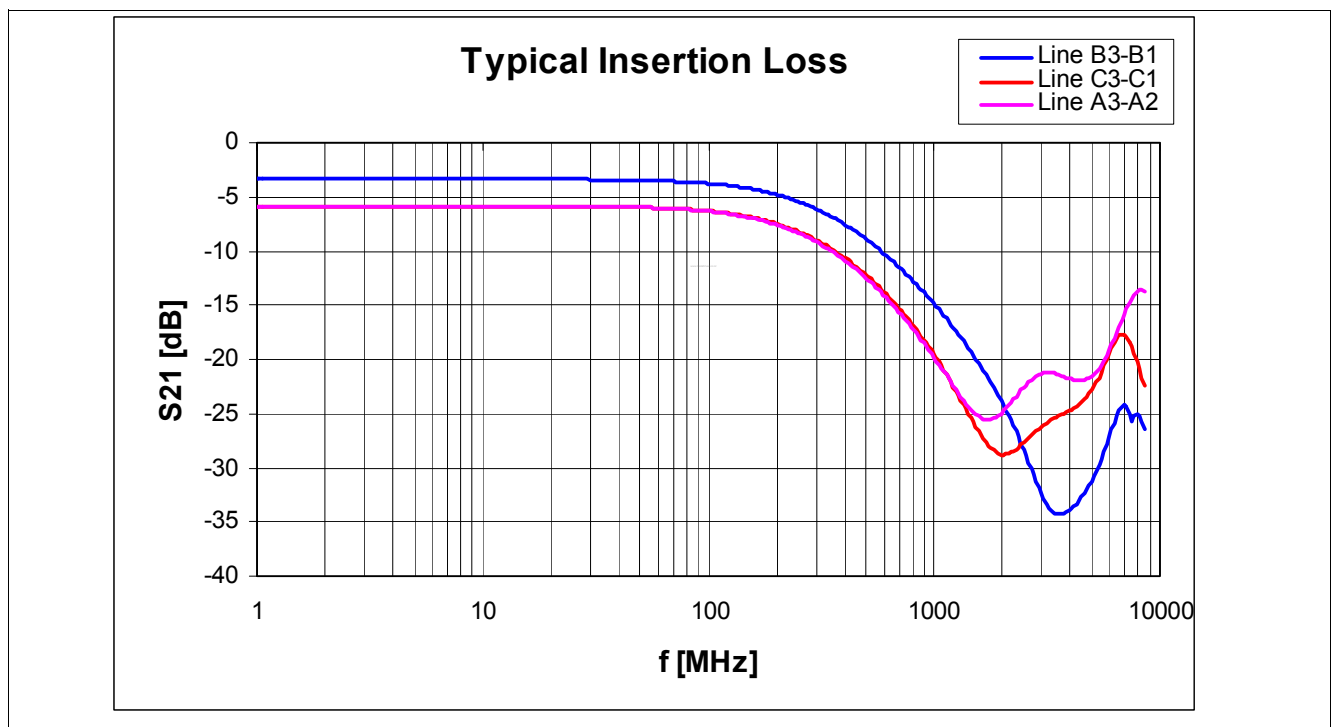


Figure 2 **Insertion Loss**

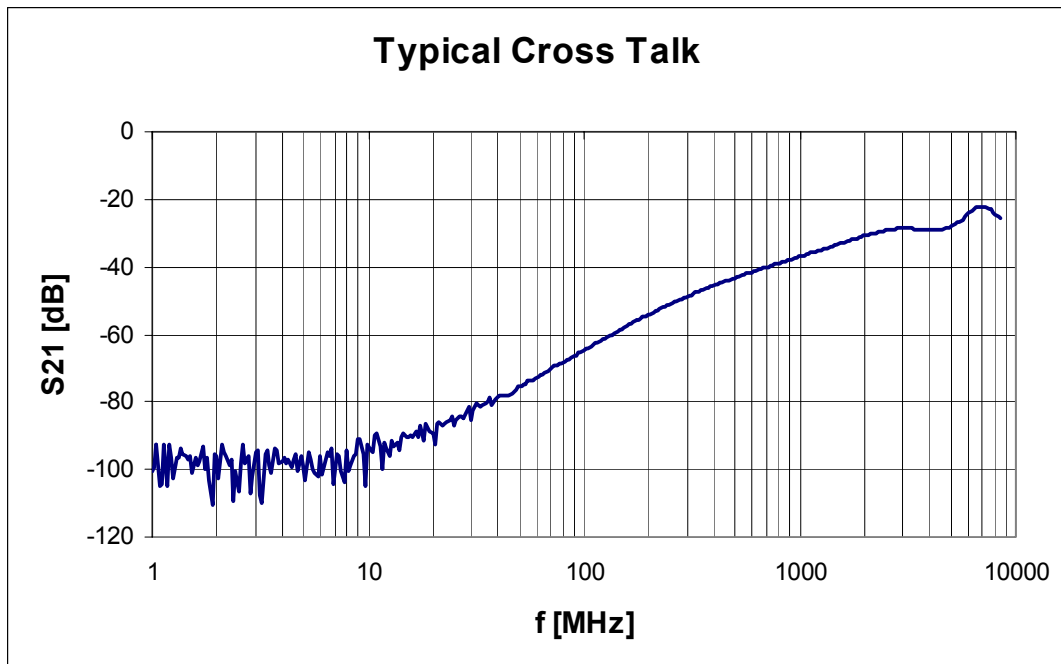


Figure 3 Cross Talk

Package Outlines

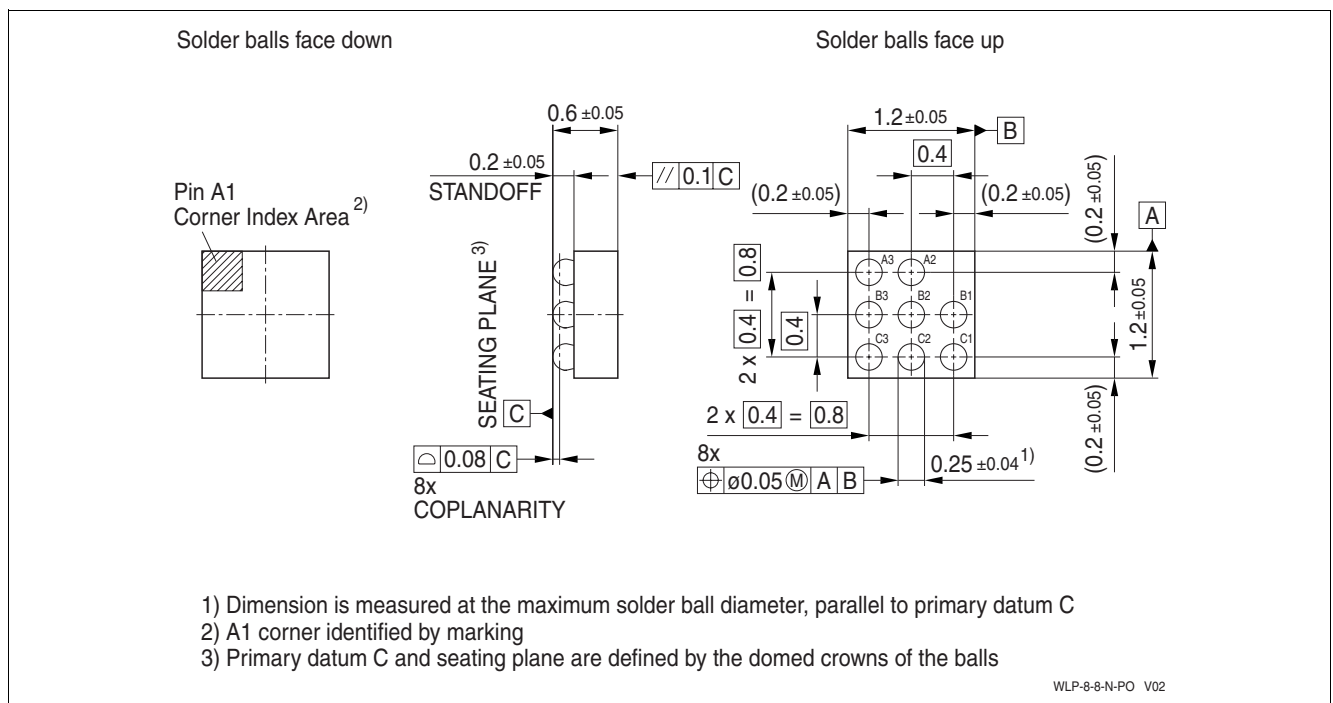


Figure 4 WLP-8-8 (Wafer Level Package)

Tape for BGF106

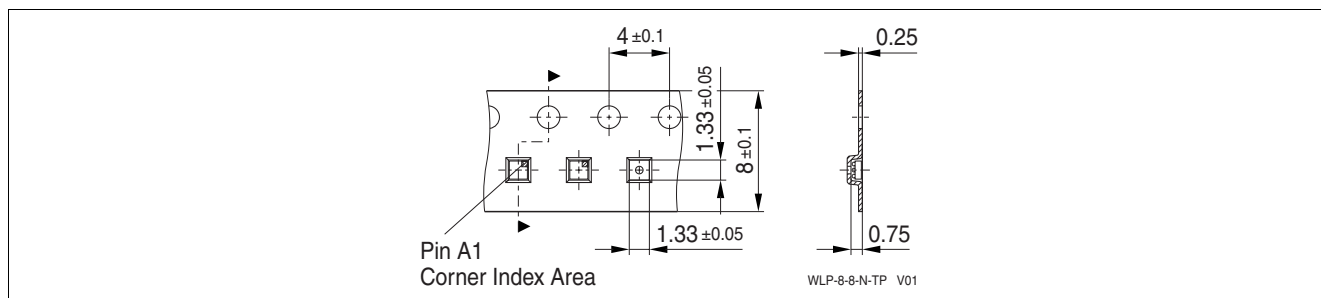


Figure 5 Tape for BGF106 / WLP-8-8

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