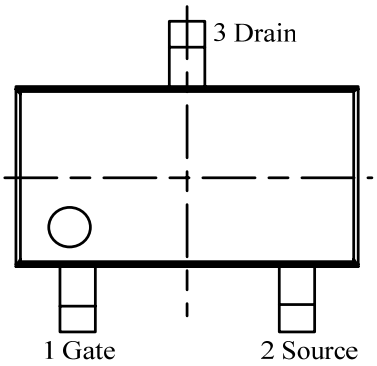
BYD Microelectronics Co., Ltd.

BF9035SNZ-M

30V N-Channel MOSFET

General Description

The BF9035SNZ-M is a Single N-channel MOS Field Effect Transistor, which uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This is applied to electronic systems as a power switch.

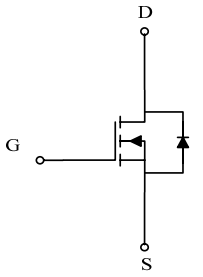


SOT23-3

Features

- V_{DS}=30 V
- I_D=4A
- Low on-state resistance
  $R_{DS\ (on)}$ <65mΩ (V_{GS}=10V，I_D=2.0A)
  $R_{DS\ (on)}$ < 80mΩ (V_{GS}=4.5V，I_D=2.0A)
  $R_{DS\ (on)}$ < 95mΩ (V_{GS}=3.0V，I_D=2.0A)
- Lead Pb-free and Halogen-free

EQUIVALENT CIRCUIT



N-Channel MOSFET

Absolute Maximum Ratings(T_C = 25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	30	V
I_D	Drain Current(continuous)at Tc=25℃	4	A
I_{DM}	Drain Current (pulsed) (Note a)	16	A
V_{GS}	Gate-Source Voltage	±12	V
P_D	Power Dissipation T_C = 25°C	2.0	W
T_J,Tstg	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum Lead Temperature for Soldering Purpose	150	℃

Ordering Information

Part Number	Package	Packaging
BF9035SNZ-M	SOT23-3	3000pcs Tape & Reel

Electrical Characteristics (T_c = 25℃)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DS}	Drain-source Breakdown Voltage	I_D=250uA,V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =24V, V_{GS} =0V			1	uA
I_{GSS}	Gate-body Leakage Current	V_{GS}=±12V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.6	1	1.4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS}=3.0V,I_D=2A		80	95	mΩ
		V_{GS}=4.5V,I_D=2A		65	80	
		V_{GS}=10.0V,I_D=2A		55	65	
C_{iss}	Input Capacitance	V_{DS}=15V,f=1MHz,V_{GS}=0V		300		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			50		pF
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V,I_D=2A, V_{GS}=10V, R_G=4.7Ω (Note b,c)		15		ns
t_r	Rise Time			20		ns
$t_{d(off)}$	Turn-off Delay Time			50		ns
t_f	Fall Time			12		ns
Q_g	Total Gate Charge	V_{DS}=15V,I_D=4A,V_{GS}=4.5V (Note b,c)		3.8		nC
Q_{gs}	Gate-source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			1.4		nC
V_{SD}(*)	Forward On Voltage	V_{GS}=0V,I_F=1A		0.8	1	V

Notes
a: Repetitive Rating : Pulse width limited by maximum junction temperature
b: Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
c: Essentially independent of operating temperature
(*)Pulsed: Pulse duration

Caution: These values must not be exceeded under any conditions.

Typical characteristics (25℃ unless noted)

Figure 1 Output Characteristics

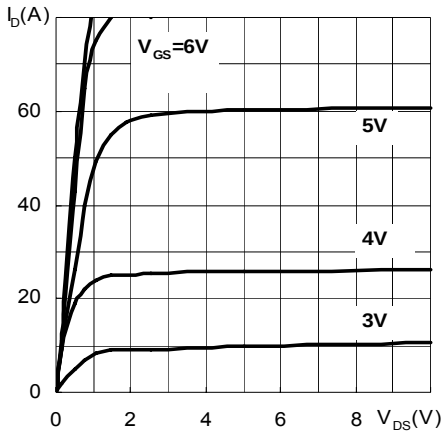


Figure 2 Transfer Characteristics

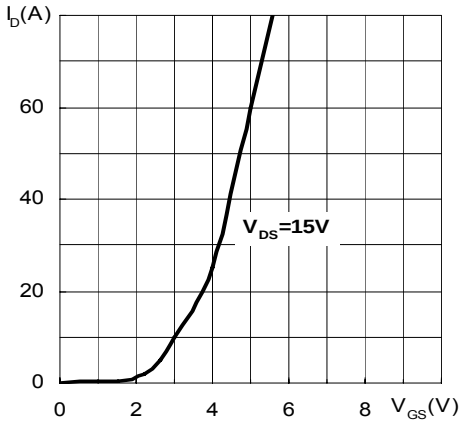


Figure 3 Vth vs. Temperature

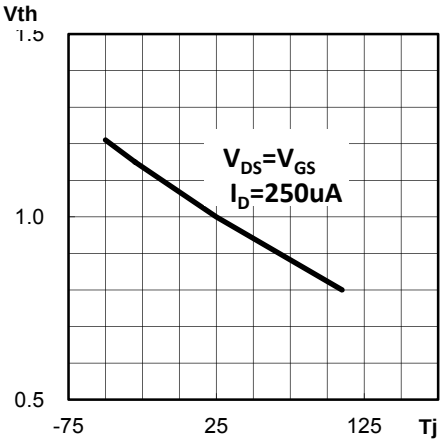


Figure 4 Normalized BV_{DSS} vs. Temperature

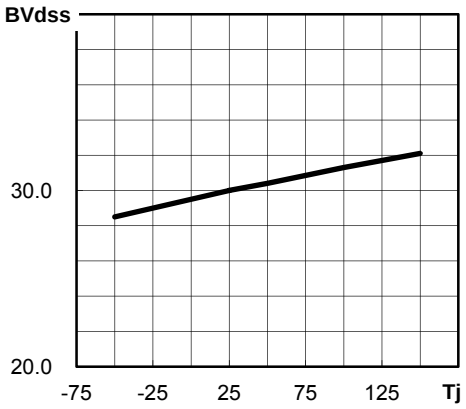


Figure 5 R_{DSON} vs. Temperature

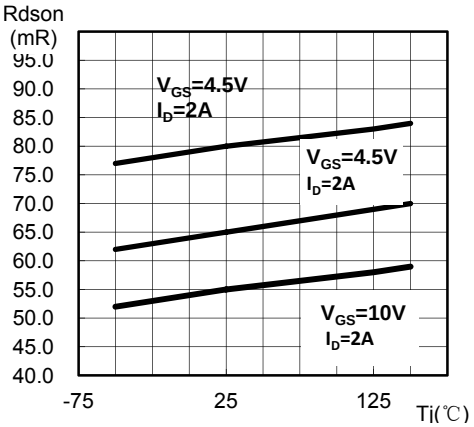


Figure 6 I_{GSS} vs Environment Temperature

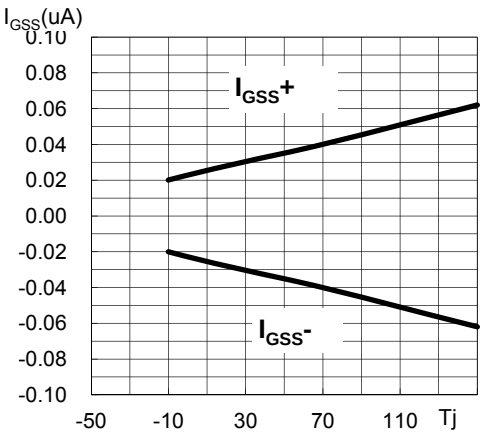


Figure 7 Capacitance

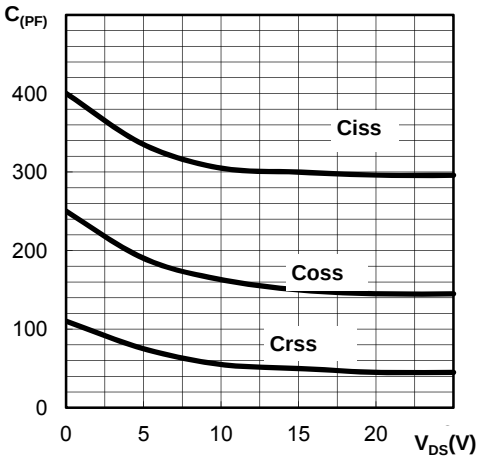


Figure 8 Gate Charge

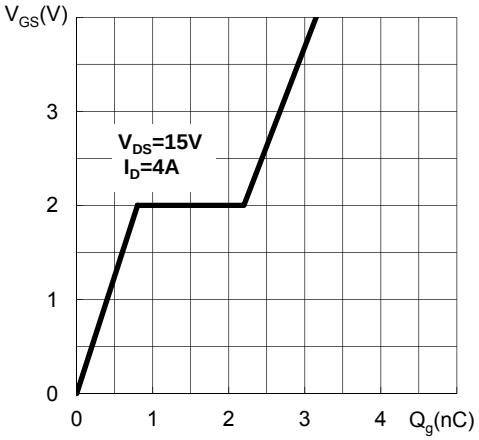


Figure 9 Safe Operating Area

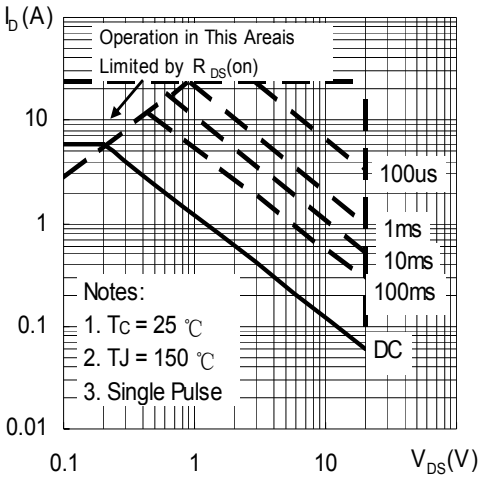


Figure 10 Maximum I_{DSS} vs. Case Temperature

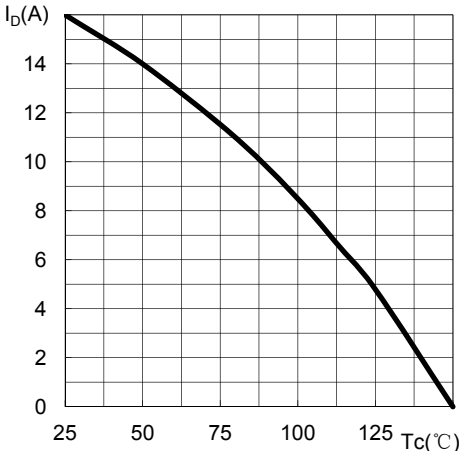


Figure 11 Rdson vs. V_{GS}

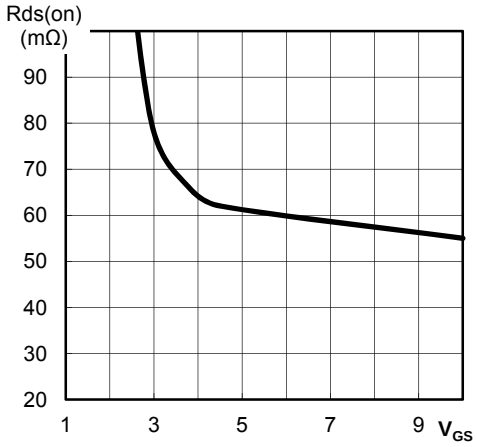


Figure 12 Gate-Current vs.Gate-Source Voltage

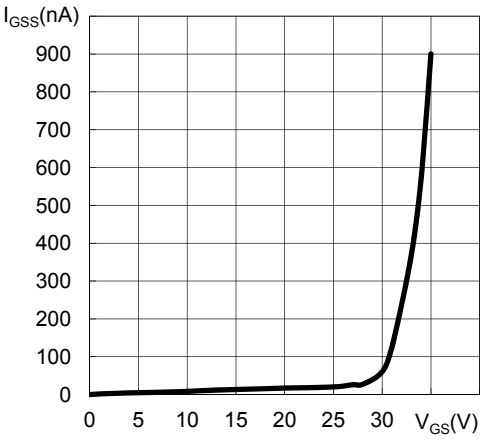
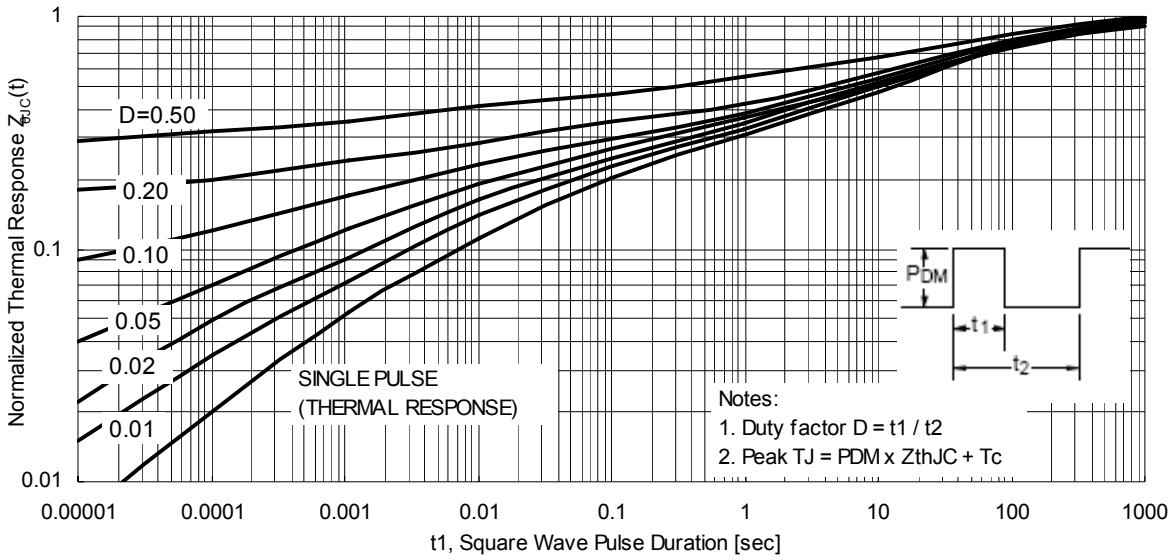
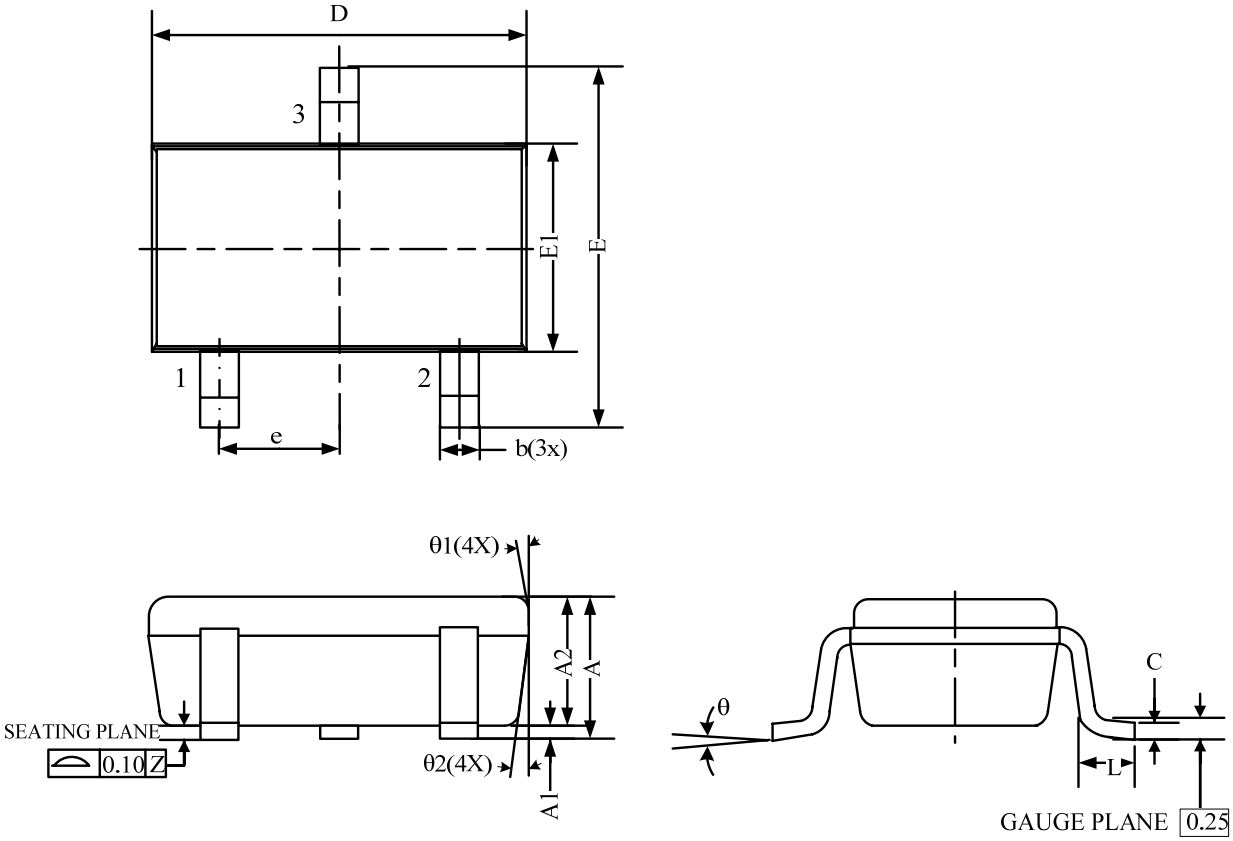


Figure 13 Maximum Transient Thermal Impedance



Package Drawing



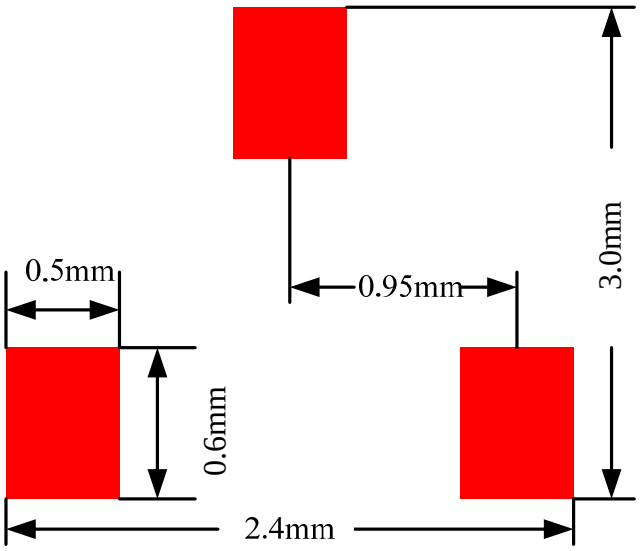
Dimensions

DIM.		A	A1	A2	b	C	D	E	E1	e	L	θ	θ1	θ2
mm	MIN.	1.00	0.03	1.00	0.30	0.10	2.80	2.60	1.50	0.95BSC	0.30	0°	5°	6°
	NOM.	1.15	0.09	1.10	0.40	0.15	2.90	2.80	1.60		0.45	4°	6°	8°
	MAX.	1.30	0.15	1.20	0.50	0.20	3.00	3.00	1.70		0.60	8°	7°	10°

Note:

1. Dimension D does not include mold flash, protrusions or gate burrs. mold flash, protrusions or gate burrs shall not exceed 0.10mm per side.
2. Dimension E1 does not include inter-lead flash or protrusion. Inter-lead flash or protrusion shall not exceed 0.1mm per side.

PCB Layout Guide



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