BYD Microelectronics Co., Ltd.

BF9028DND-GE

20V N-Channel MOSFET

General Description

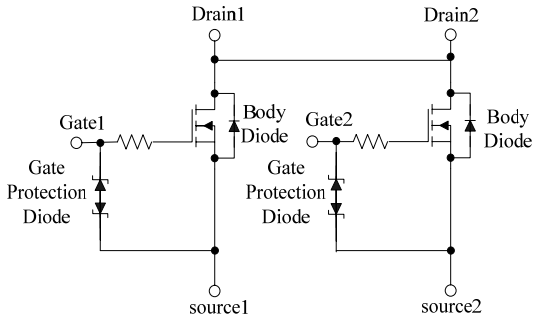
The BF9028DND-GE is a dual N-channel MOS Field Effect Transistor, which is applied to electronic systems as a power switch. This device has ESD-protection and low resistance characteristics.

1, 2 Source1 ； 3 Gate1 ；
4 Gate2 ； 5, 6 Source2 ；
Backside pad is Drain

Features

- V_{DS}=24 V
- I_D=6 A
- Low on-state resistance
  $R_{DS\ (on)}$ < 19.5 mΩ (V_{GS}=4.5V)
  $R_{DS\ (on)}$ < 20 mΩ (V_{GS}=3.8V)
  $R_{DS\ (on)}$ < 26 mΩ (V_{GS}=3.0V)
  $R_{DS\ (on)}$ < 30 mΩ (V_{GS}=2.5V)

EQUIVALENT CIRCUIT



Absolute Maximum Ratings(T_C = 25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	24	V
I_D	Drain Current(continuous)at Tc=25℃	6	A
I_{DM}	Drain Current (pulsed) (Note a)	24	A
V_{GS}	Gate-Source Voltage	±10	V
P_D	Power Dissipation T_C = 25°C	2.0	W
T_J,Tstg	Operating and Storage Temperature Range	-55 to +150	℃

Ordering Information

Part Number	Package	Packaging
BF9028DND-GE	DFN2*5-6L	Tape&Reel

Electrical Characteristics (T_c = 25℃)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source Breakdown Voltage	I_D=250uA,V_{GS}=0V	24			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =24V, V_{GS} =0V			10	uA
I_{GSS}	Gate-body Leakage Current	V_{GS}=±10V,V_{DS}=0V			±10	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.5	0.8	1.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS}=4.5V,I_D=3A	14	18.5	19.5	mΩ
		V_{GS}=3.8V, I_D=3A	15	19	20	
		V_{GS}=3.0V, I_D=3A	16	19.5	26	
		V_{GS}=2.5V, I_D=3A	17	21	30	
C_{iss}	Input Capacitance	V_{DS}=10V,f=1MHz,V_{GS}=0V		800		pF
C_{oss}	Output Capacitance			280		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=12V,I_D=3A, V_{GS}=4.5V,R_G=4.7Ω (Note b,c)		680		ns
t_r	Rise Time			1640		ns
$t_{d(off)}$	Turn-off Delay Time			3040		ns
t_f	Fall Time			2280		ns
Q_g	Total Gate Charge	V_{DS}=19V,I_D=6A, V_{GS}=4.5V (Note b,c)		12		nC
Q_{gs}	Gate-source Charge			2.5		nC
Q_{gd}	Gate-Drain Charge			3.5		nC
V_{SD}(*)	Forward On Voltage	V_{GS}=0V,I_F=6A		0.7		V

Electrical Characteristics (T_c =-30~80℃)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source Breakdown Voltage	I_D=250uA,V_{GS}=0V	24			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =24V, V_{GS} =0V			10	uA
I_{GSS}	Gate-body Leakage Current	V_{GS}=±10V,V_{DS}=0V			±10	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250uA	0.3	0.75	1.8	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS}=4.5V,I_D=3A	12	18.5	22.5	mΩ
		V_{GS}=3.8V, I_D=3A	13	19	22	
		V_{GS}=3.0V, I_D=3A	14.5	19.5	30	
		V_{GS}=2.5V, I_D=3A	16	21	32	
C_{iss}	Input Capacitance	V_{DS}=10V,f=1MHz,V_{GS}=0V		800		pF
C_{oss}	Output Capacitance			280		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=12V,I_D=3A, V_{GS}=4.5V,R_G=4.7Ω (Note b,c)		680		ns
t_r	Rise Time			1640		ns
$t_{d(off)}$	Turn-off Delay Time			3040		ns
t_f	Fall Time			2280		ns
Q_g	Total Gate Charge	V_{DS}=19V,I_D=6A,V_{GS}=4.5V (Note b,c)		12		nC
Q_{gs}	Gate-source Charge			2.5		nC
Q_{gd}	Gate-Drain Charge			3.5		nC
V_{SD}(*)	Forward On Voltage	V_{GS}=0V,I_F=6A		0.7		V

Notes
a: Repetitive Rating : Pulse width limited by maximum junction temperature
b: Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
c: Essentially independent of operating temperature
(*)Pulsed: Pulse duration

Caution: These values must not be exceeded under any conditions.

Remark: The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Typical characteristics (25℃ unless noted)

Figure 1 Output Characteristics

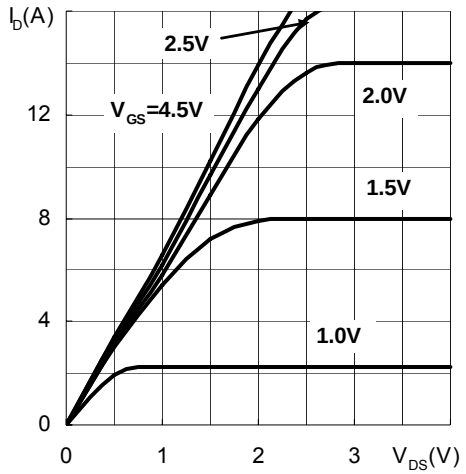


Figure 2 Transfer Characteristics

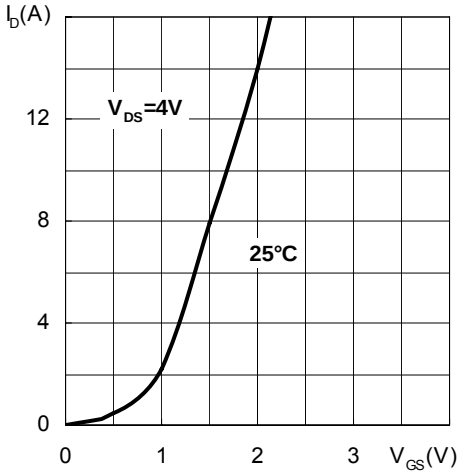


Figure 3 Normalized Vth vs. Temperature

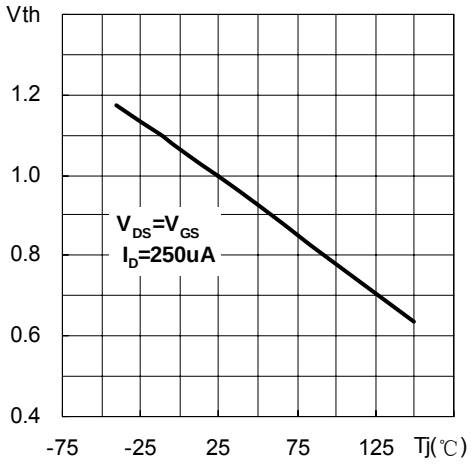


Figure 4 Normalized BV_{DSS} vs. Temperature

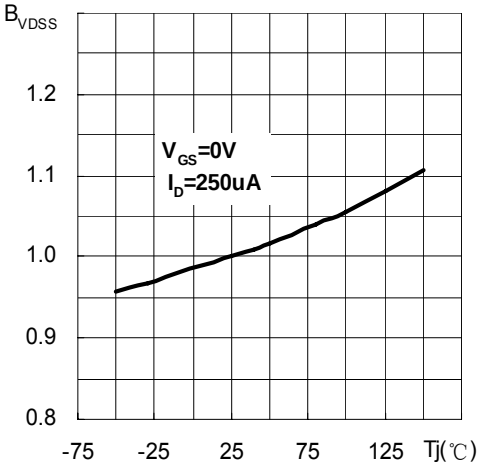


Figure 5 R_{DSON} vs. Temperature

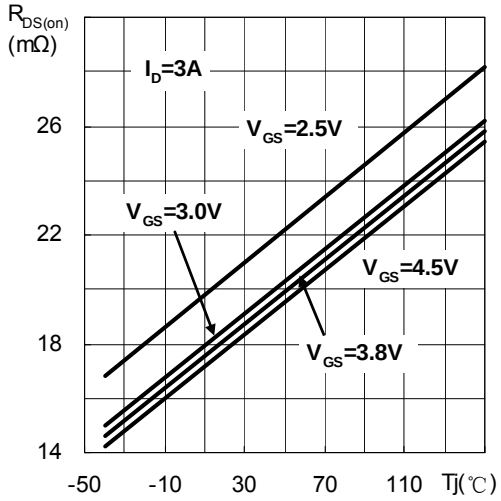


Figure 6 I_{GSS} vs. Temperature

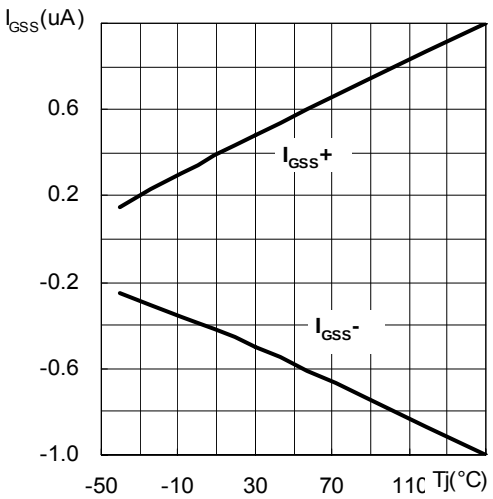


Figure 7 Capacitance

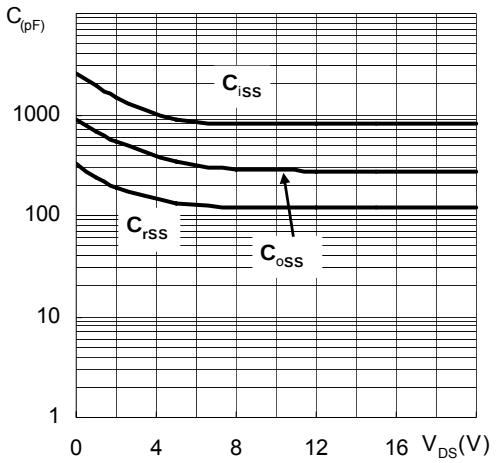


Figure 8 Gate Charge

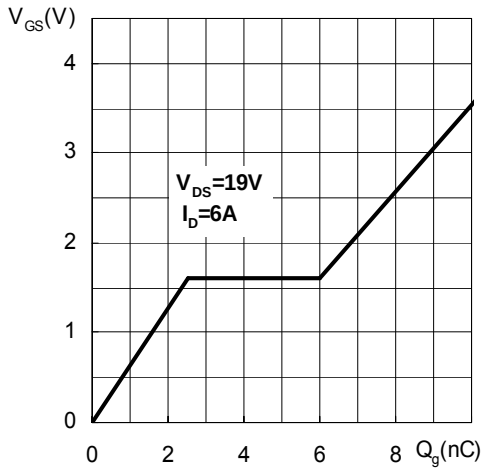


Figure 9 Safe Operating Area

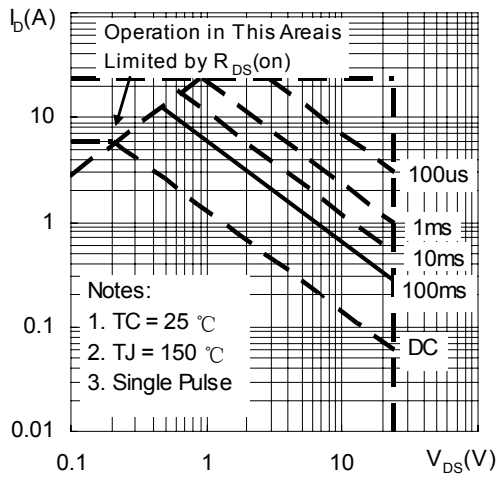


Figure 10 Maximum I_{DSS} Vs. Case Temperature

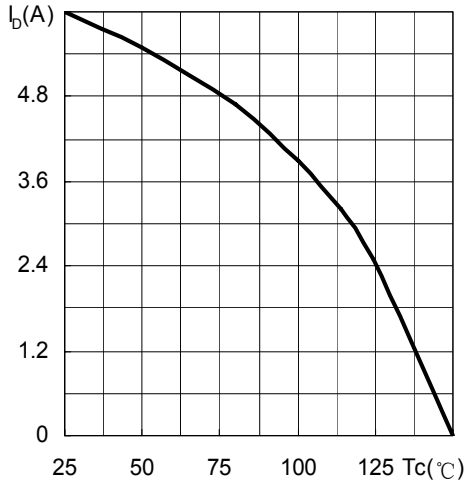


Figure 11 Rdson vs. V_{GS}

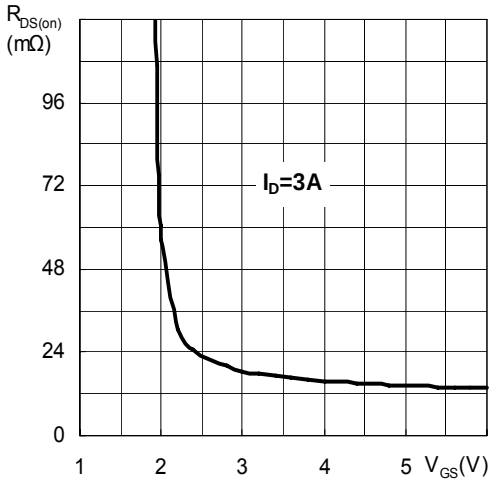
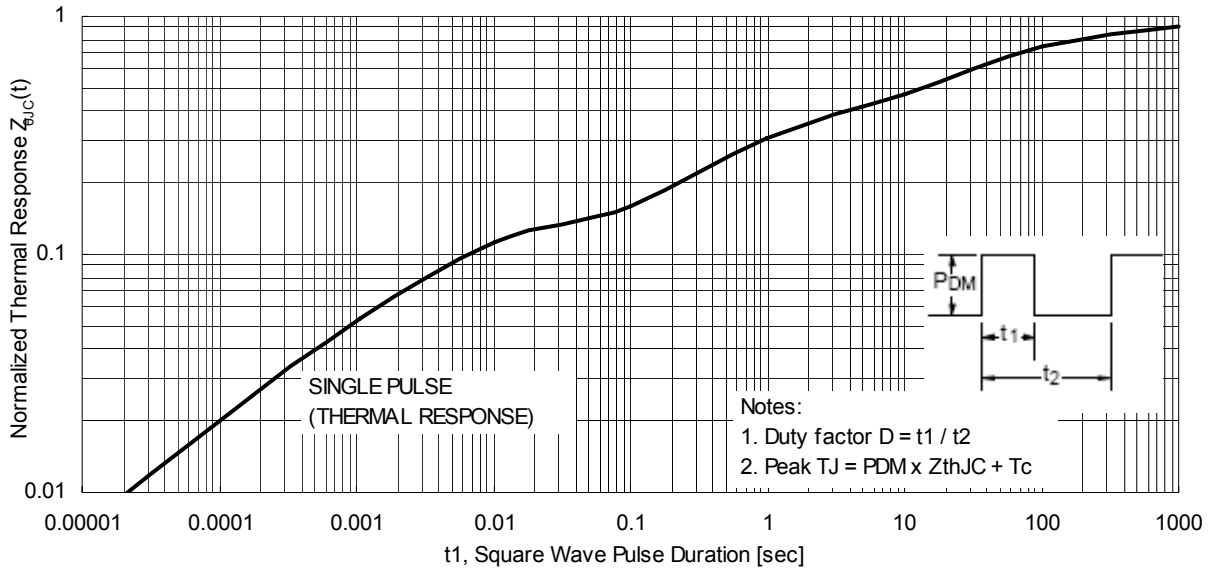
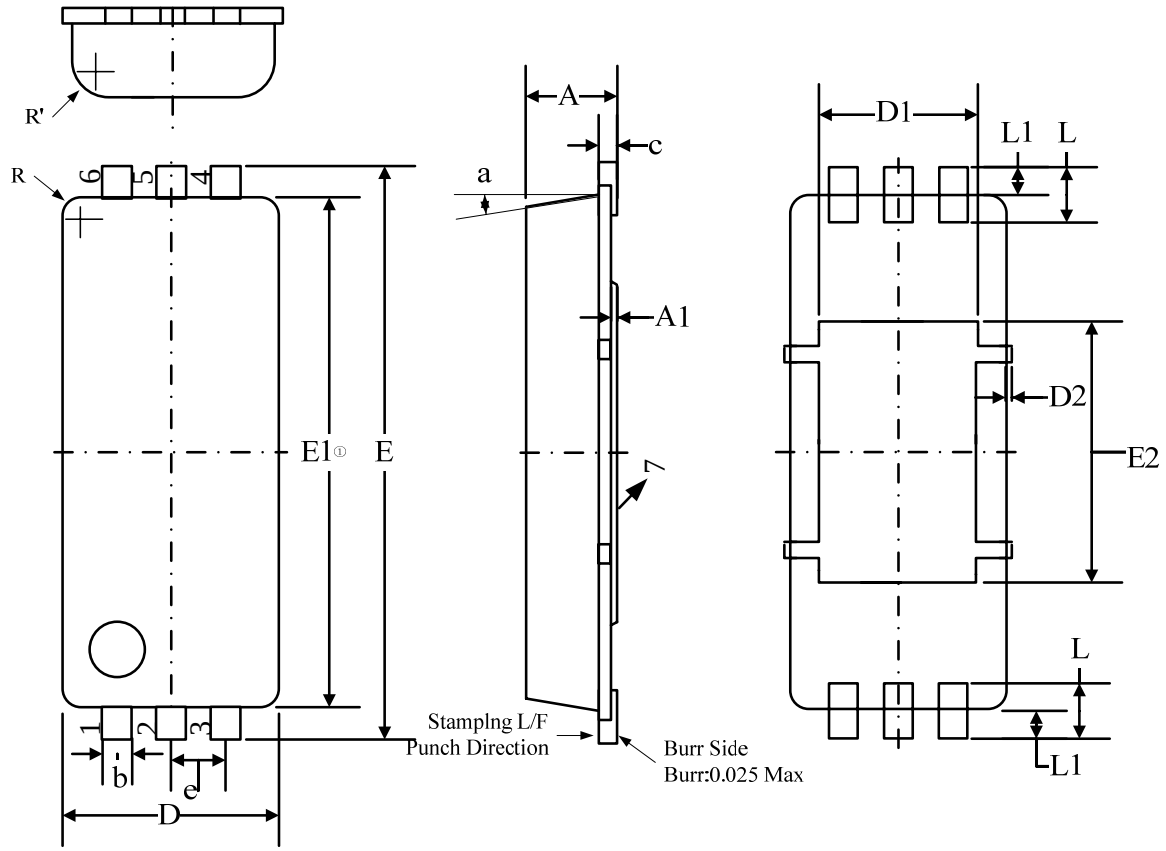


Figure 12 Normalized Maximum Transient Thermal Impedance



Package Drawing:



1,2 Source1；3 Gate1；
4 Gate2；5,6 Source2；7 Drain

NOTE:

1) All Dimensions Are In mm.

DIM	A	A1	b	c	D	D1	D2	E	E1	E2	e	L	L1	R	R′	a
Min.	0.70	0.00	0.18	0.10	1.85	1.25	0.00	4.90	4.30	2.30	0.50 BSC	0.37	0.23	0.15	0.10 (Ref)	10^0
Nom.	0.75	-	0.21	0.15	2.00	1.40	-	5.00	4.40	2.625		0.50	0.30			
Max.	0.80	0.05	0.33	0.20	2.15	1.55	0.10	5.10	4.50	2.95		0.63	0.37			

2) Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs, Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.

3) Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash ,Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.

4) The Package Top May Be Smaller Than The Package Bottom.

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