LED Drivers for LCD Backlights

White LED Diver for Backlight of Medium/Large-sized LCDs

BD9271KUT

General Description

BD9271KUT is a white LED diver used on backlight of Medium/Large-sized LCDs. This IC can achieve dimming function by SPI control. And through the SPI correspondence, it can set the ON/OFF of each switch, analog dimming and etc. The signals of PWM dimming can set the frequency, ON time and delay of PWM by inputting the external signals to the register.
BD9271KUT has equipped several protection functions to deal with the abnormal states, including LED OPEN protection, LED SHORT protection, external current setting resistance SHORT protection, external MOS transistor SHORT protection, etc. So it can be used in a wide output voltage range and various load conditions.

Features

- 16-ch constant current driver (external FET(NMOS)is equipped.)
- LED voltage can be set externally.
- PWM dimming and Analogue dimming can be controlled by SPI.
- LED Abnormal operation detection circuit (OPEN protection/ SHORT protection) is equipped.
- LED SHORT protection detection voltage is adjustable (LSP terminal)
- LED SHORT protection detection CH
- FAIL INDICATION function is equipped by ERR_DET terminal.
- 3 lines serial interface
- Package: TQFP64U

Key Specifications

- VCC power supply range : 9.0V～35.0V
- DVDD power supply range : 3.0V～3.6V
- CLK frequency setting range: 100～10000kHz
- Operating Circuit current range : 2.4mA(typ.)
- Operating temperature range : -40℃～+85℃

Package

	W(Typ.) D(Typ.) H(Max.)
TQFP64U	9.00mm×9.00mm×1.20mm
Pin Pitch	0.4mm

Figure 1. TQFP64U

Applications

TV, PC display
Other LCD backlight

Typical Application Circuit

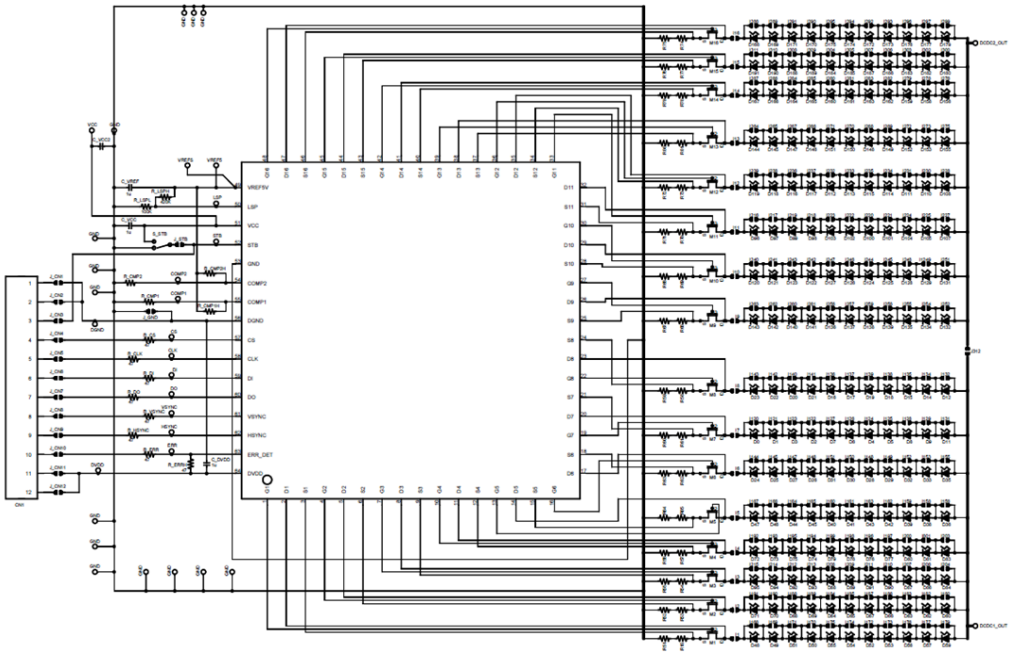


Figure 2. Typical Application Circuit

Absolute Maximum Ratings（Ta=25℃）

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	VCC	36	V
Power Supply Voltage at digital part	DVDD	4.5	V
STB Terminal Voltage	VSTB	VCC	V
D1～16 Terminal Voltage	VD1～VD16	40	V
ERR_DET Terminal Voltage	VERR_DET	VCC	V
S1～S16, G1～G16, VREF5V, LSP, COMP1, COMP2 Terminal Voltage	VS1～S16, VG1～VG16,VREF5V,VLSP, VCOMP1,VCOMP2	7	V
CS, CLK, DI, DO, VSYNC, HSYNC Terminal Voltage	VCS,VCLK,VDI,VDO,VVSYNC,VHSYNC	4.5	V
Power Dissipation	Pd	1.37(Note 1)	W
Operating Temperature Range	Topr	-40～+85	℃
Storage temperature range	Tstg	-55～+150	℃
Junction temperature	Tjmax	150	℃

(Note 1)When Ta = 25°C or higher, power dissipation is down with 11.0mW/°C (when a 70 mm x 70 mm x 16 mm 1-layer glass epoxy board is mounted).

Operation range（Ta=25℃）

Parameter	Symbol	Limits	Unit
Power source voltage	VCC	9.0～35.0	V
Power Supply Voltage at digital part	DVDD	3.0～3.6	V
CLK oscillation frequency setting range	fCLK	100～10000	kHz
VSYNC input oscillation frequency range	fVSYNC	80 ～ 1000	Hz
LSP terminal input voltage	VLSP	0.8 ～ 3.0	V

The operating ranges above are acquired by evaluating the IC separately. Please take care when set the IC in applications.

External Components Recommended Range

Parameter	Symbol	Range	Unit
VCC pin connection capacitance	CVCC	1～10	uF
VREF5V pin connection capacitance	CREF	0.1～10	uF

The operating ranges above are acquired by evaluating the IC separately. Please take care when set the IC in applications.

Block diagram

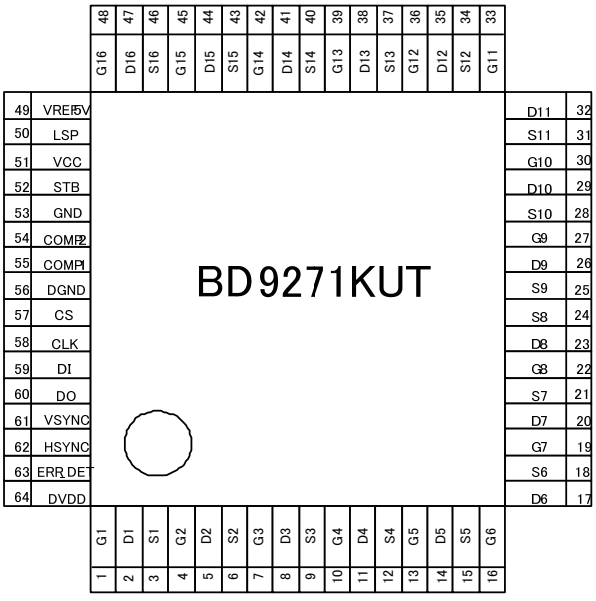


Figure 3. Pin Configuration

Package outline drawing

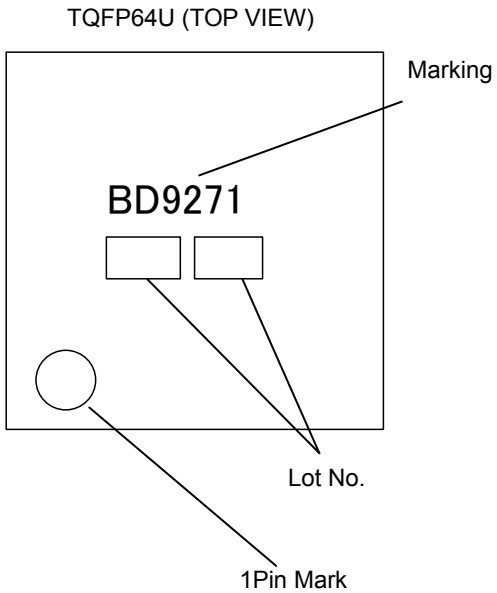


Figure 4. Marking Diagram

Electrical characteristics (unless otherwise specified, Ta = 25°C, VCC = 12V, STB=3V)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
【Whole device】						
Operating circuit current	Icc	—	2.4	5.0	mA	LED1-16 OFF
Stand-by circuit current	IST	—	200	500	μA	STB=0V
【VREF5V block】						
VREF5V output voltage	VREF5	4.95	5.00	5.05	V	IO=0mA
VREF5V Maximum output current	IREF5	15	—	-	mA	
【Error amplifier block】						
COMP1,COMP2 terminal sink current	ICOMPSINK	300	-	-	μA	VCOMP=0.5V
LED control voltage	VLED	270	300	330	mV	
【UVLO block】						
Operation power source voltage(VCC)	VUVLO_VCC	6.0	7.0	8.0	V	VCC=SWEEP UP
hysteresis voltage（VCC）	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
【LED DRIVER block】						
LED terminal current accuracy	⊿ILED	-1.5	-	1.5	%	ILED=100mA
OPEN detection voltage	VOPEN	0.05	0.10	0.15	V	VD=SWEEP DOWN
SHORT detection voltage	VSHORT	4.5	5.0	5.5	V	VD=SWEEP UP
Upper resistance of divided LSP terminal resistance	RupLSP	1000	-	-	kΩ	LSP=0V
Lower resistance of divided LSP terminal resistance	RdownLSP	250	-	-	kΩ	LSP=5V
Error detection of current detection resistance	VRESSH	0.10	0.15	0.20	V	LEDREF default
【STB block】						
STB terminal HIGH voltage	STBH	2.0	-	VCC	V	
STB terminal LOW voltage	STBL	-0.3	-	0.8	V	
STB terminal Pull Down resistance	REN	600	1000	1800	kΩ	VIN=3V(STB)
【FAIL block】						
ERR_DET terminal ON resistance	RFAIL	55	110	220	Ω	IERR_DET=5mA
【LOGIC input (CS, CLK, DI, HSYNC, VSYNC)】						
Input High voltage	VINH	0.7× DVDD	-	DVDD +0.3	V	
Input Low voltage	VINL	-0.3	-	0.3× DVDD	V	
Input inflow current	IIN1	-5	0	5	μA	VIN=3.3V
【LOGIC output (DO) 】						
Output High voltage	VOUTH	DVDD -0.6	DVDD -0.3	-	V	IOL=-1mA
Output Low voltage	VOUTL	-	0.19	0.60	V	IOL=1mA

Terminal No., Name, and Function

No.	Terminal	Function	No.	Terminal	Function	No.	Terminal	Function	No.	Terminal	Function
1	G1	CH1 NMOS gate terminal	17	D6	CH6 NMOS drain terminal	33	G11	CH11 NMOS gate terminal	49	VREF5V	5V regulator output terminal
2	D1	CH1 NMOS drain terminal	18	S6	CH6 NMOS source terminal	34	S12	CH12 NMOS source terminal	50	LSP	SHORT detection setting terminal
3	S1	CH1 NMOS source terminal	19	G7	CH7 NMOS gate terminal	35	D12	CH12 NMOS drain terminal	51	VCC	Power source terminal
4	G2	CH2 NMOS gate terminal	20	D7	CH7 NMOS drain terminal	36	G12	CH12 NMOS gate terminal	52	STB	Enable terminal
5	D2	CH2 NMOS drain terminal	21	S7	CH7 NMOS source terminal	37	S13	CH13 NMOS source terminal	53	GND	GND terminal
6	S2	CH2 NMOS source terminal	22	G8	CH8 NMOS gate terminal	38	D13	CH13 NMOS drain terminal	54	COMP2	ERROR AMP output (CH9～16)
7	G3	CH3 NMOS gate terminal	23	D8	CH8 NMOS drain terminal	39	G13	CH13 NMOS gate terminal	55	COMP1	ERROR AMP output (CH1～8)
8	D3	CH3 NMOS drain terminal	24	S8	CH8 NMOS source terminal	40	S14	CH14 NMOS source terminal	56	DGND	Digital GND terminal
9	S3	CH3 NMOS source terminal	25	S9	CH9 NMOS source terminal	41	D14	CH14 NMOS drain terminal	57	CS	Chip select terminal
10	G4	CH3 NMOS gate terminal	26	D9	CH9 NMOS drain terminal	42	G14	CH14 NMOS gate terminal	58	CLK	Clock input terminal
11	D4	CH4 NMOS drain terminal	27	G9	CH9 NMOS gate terminal	43	S15	CH15 NMOS source terminal	59	DI	DATE input terminal
12	S4	CH4 NMOS source terminal	28	S10	CH10 NMOS source terminal	44	D15	CH15 NMOS drain terminal	60	DO	DATE output terminal
13	G5	CH5 NMOS gate terminal	29	D10	CH10 NMOS drain terminal	45	G15	CH15 NMOS gate terminal	61	VSYNC	VSYNC signal terminal
14	D5	CH5 NMOS drain terminal	30	G10	CH10 NMOS gate terminal	46	S16	CH16 NMOS source terminal	62	HSYNC	HSYNC signal terminal
15	S5	CH5 NMOS source terminal	31	S11	CH11 NMOS source terminal	47	D16	CH16 NMOS drain terminal	63	ERR_DET	Abnormal detection output terminal
16	G6	CH6 NMOS gate terminal	32	D11	CH11 NMOS drain terminal	48	G16	CH16 NMOS gate terminal	64	DVDD	Digital Power source terminal

Internal Equivalent Circuit Diagram

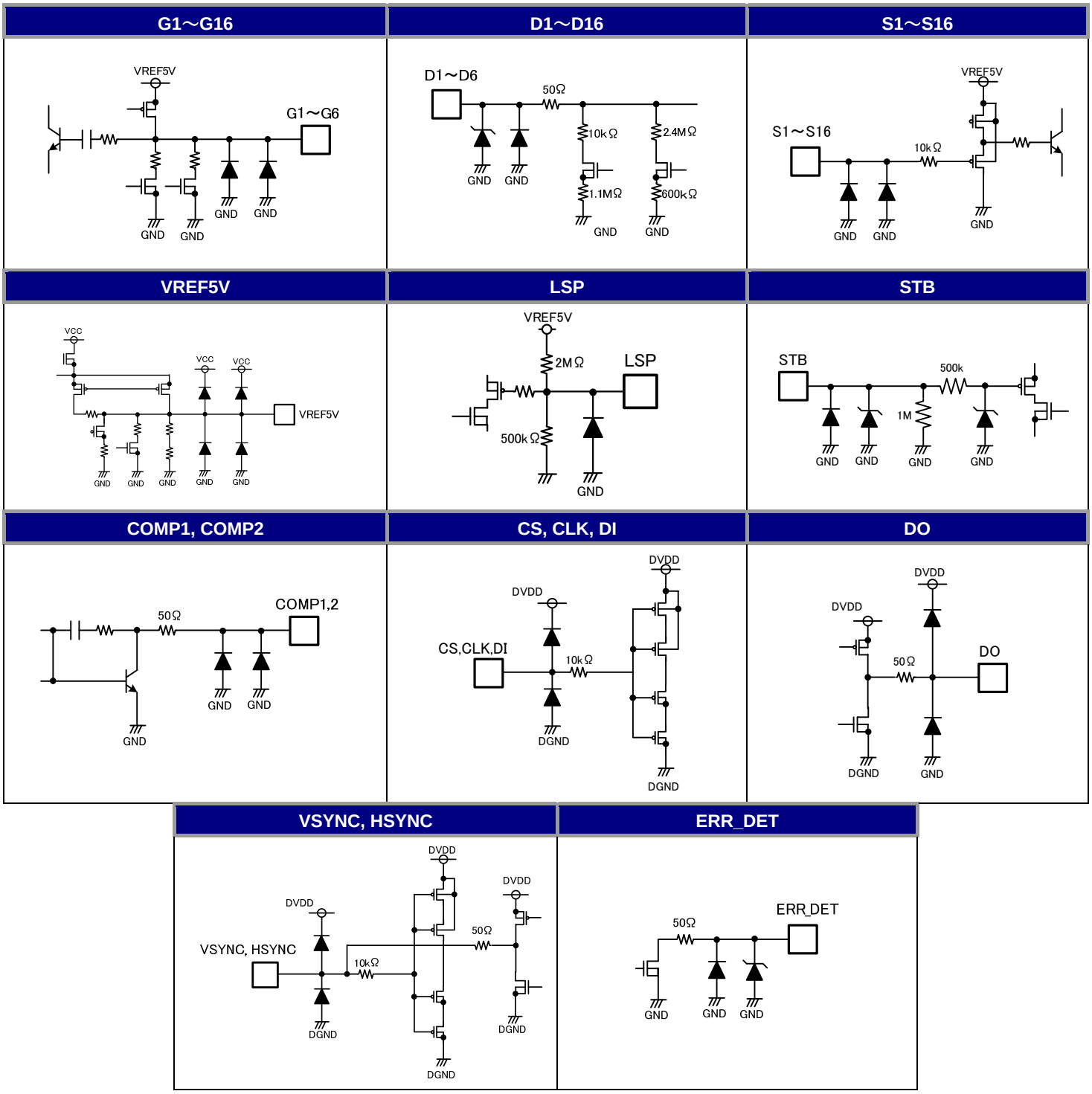


Figure 5. Pin ESD Type

Block Diagram

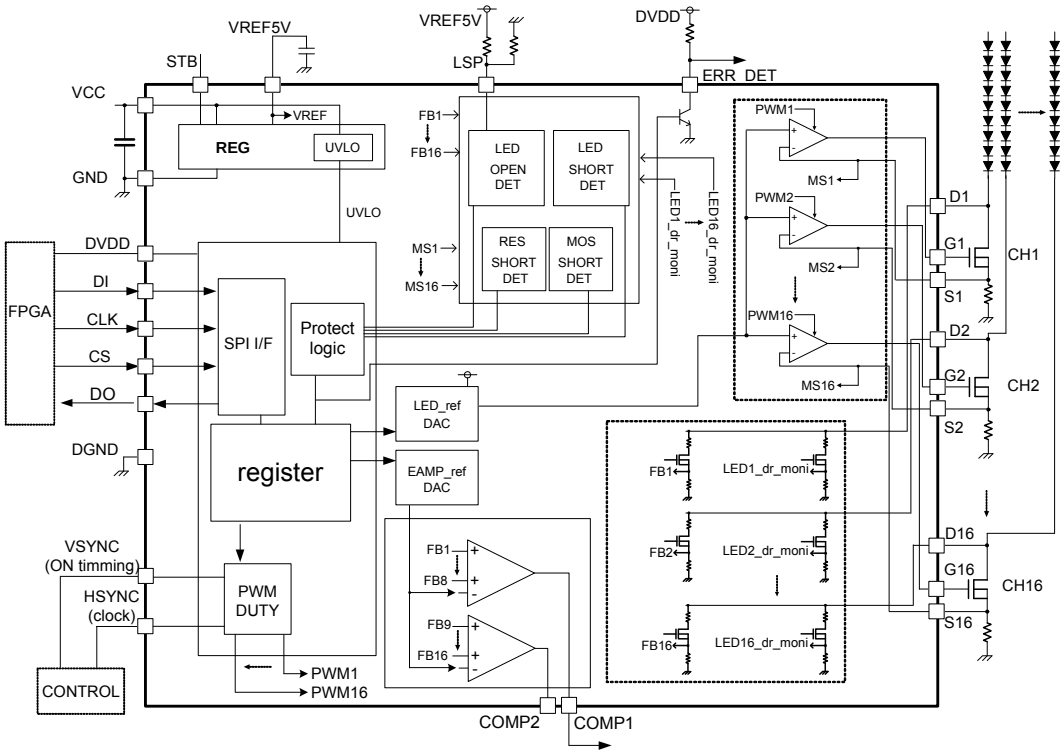


Figure 6. Block Diagram

Typical Performance Curves

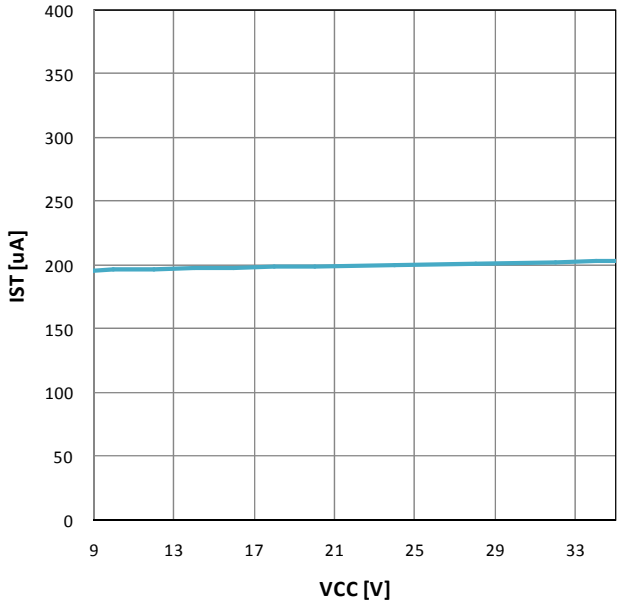


Figure 7. Stand-by Current (IST) [µA] vs. VCC[V]

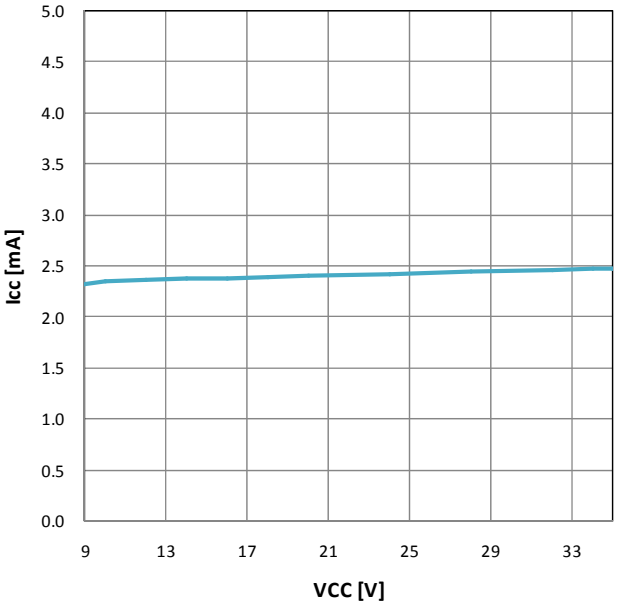


Figure 8. Operating Current (Icc) [mA] vs. VCC[V] (LED1-16 OFF)

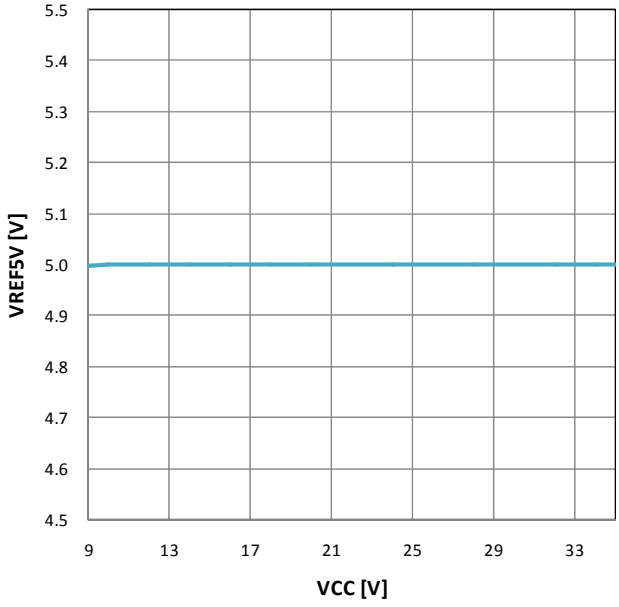


Figure 9. VREF5V[V] vs. VCC[V]

Pin Function Descriptions

○G1-G16 (1,4,7,10,13,16,19,22,27,30,33,36,39,42,45,48PIN)

External FET gate driving terminal of LED constant current driver, operating range : 0～5V.

○S1-S16 (3,6,9,12,15,18,21,24,25,28,31,34,37,40,43,46PIN)

Connect to external FET's source terminal of LED constant current driver. Through the operations of constant current driver, all CHs of S1-S16 terminals are outputted the set voltages at addresses of 02h, 03h, and S1-S16 proceed the constant current operation.
By monitoring the voltage of this terminal, the external resistance SHORT detection of each CH and external MOS SHORT during Drain-Source detection proceed.
When Dimming＝HIGH, external resistance SHORT detection proceeds, and output the errors.
When Dimming＝LOW, external MOS Drain-Source SHORT detection proceeds, and output the errors.

The detection voltage of Sx pin for RESSHORT, MOSSHORT protection corresponds to the register value of 02h, 03h LEDREF (the normal operation voltage of Sx pin). Please refer to the condition of protections.

LEDREF[11:0]	Abnormal detection voltage	Normal operation voltage
000h - 0CDh	0.05V	0.1V
800h - FFFh	0.50V	1.0V
266h(default)	0.15V	0.3V

○D1-D16 (2,5,8,11,14,17,20,23,26,29,32,35,38,41,44,47PIN)

At output terminal of LED constant current driver, drain of external FET is connected. By monitoring the voltage of this terminal, LED OPEN detection and LED SHORT detection of each terminal proceed.
When Dimming＝HIGH, if LED is in SHORT mode or OPEN mode, error signals are outputted.
LED OPEN protection detected voltage ・・・0.1V(typ.)
LED SHORT protection detected voltage・・・5.0V(typ.)・・・(It can be changed by setting the LSP terminal. Details are given in LSP Pin Description.)

When Dimming＝LOW, the abnormal state when Dimming＝HIGH just before continues. In other words, when Dimming=HIGH and the abnormal state is detected, the error signal is still outputted even turned to Dimming＝LOW.
To prevent the mistake of detection caused by the time change of state, abnormal detection mask can be set at address of 04h.

At D1～16 pin
① LED OPEN detection（when PWM=H）
② LED SHORT detection（when PWM=H）

At S1～16 pin
③ RESISTOR SHORT detection（when PWM=H）
④ MOS SHORT detection（when PWM=L）

are detected, then the error signals are outputted.

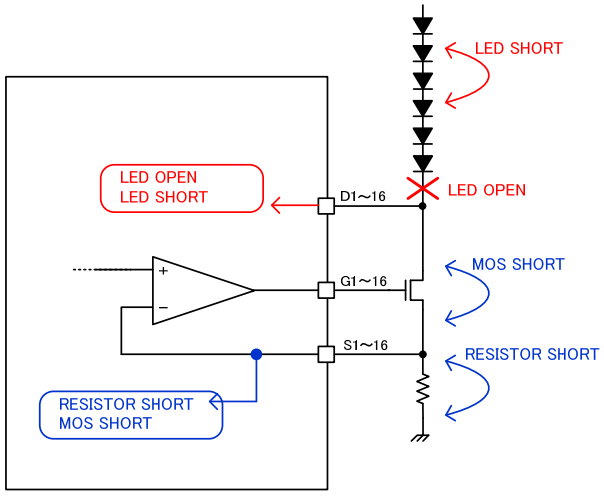


Figure 10. LED Protected operation

○VREF5V (49PIN)

The VREF5V pin is used to output power (5V) to the internal block of the IC and serves as a main power supply for the internal circuit of the IC. Install a ceramic capacitor as close to this pin as possible in order to stabilize the power supply voltage.

○LSP (50PIN)

A pin used for setting the LED SHORT protection detecting voltage. When LSP pin is in OPEN state, the voltage in inward of IC is 1V typ.（Set it in range of 0.8V~3.0V）

When LED is lighting, if the voltage of D1～16 pin is higher than

「Voltage of LSP x 5 (V) 」（default 5V）

the abnormal state of IC is detected.

Because this pin has a high impedance, please connect a capacitor about 1000pF to remove the noise basically.

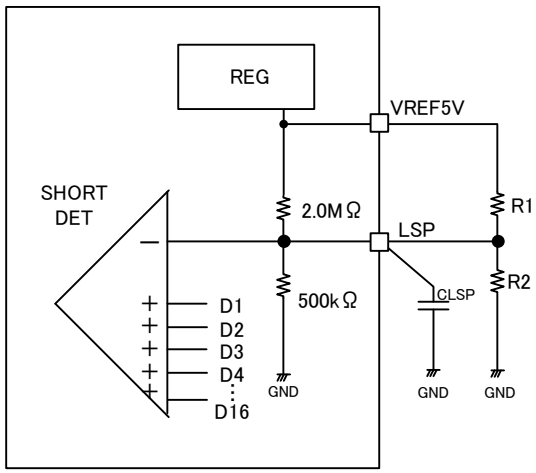


Figure 11. LSP Pin Internal Equivalent Circuit Diagram

In case of outputting a voltage to LSP by using the resistor divider circuit, REF5V

$$LED_{SHORT} = 5 \times \frac{(500k\Omega \;//\; R2)}{(2.0M\Omega \;//\; R1) + (500k\Omega \;//\; R2)} \times 5V\ [V]$$

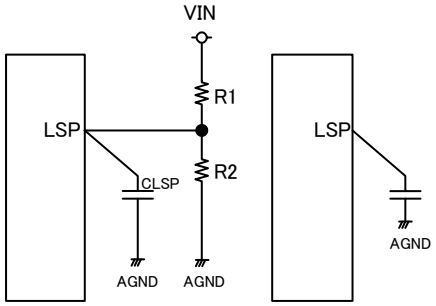


Figure 12. Setting for LSP

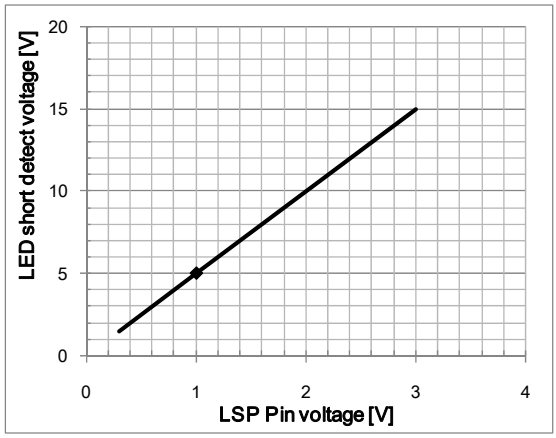


Figure 13. LED SHORT detect Voltage [V] vs. LSP [V]

○VCC (51PIN)

The VCC pin is used to supply power for the IC in the range of 9 to 35V. If the VCC pin voltage reaches 7.0V (Typ.) or more, the IC will initiate operation. If it reaches 6.7V (Typ.) or less, the IC will be shut down. Basically, insert a resistor of approx. 10 ohms in resistance between the VCC pin and the external power supply and install a ceramic capacitor of approx. 1uF in capacitance in the vicinity of the IC.

○STB (52PIN)

The STB pin is used to make setting of turning ON and OFF the IC and allowed for use to reset the IC from shutdown.

Note: Set the STB pin voltage below the VCC pin voltage.

Note: The IC state is switched (i.e., the IC is switched between ON and OFF state) according to voltages input in the STB pin. Avoid using the STB pin between two states (0.8 to 2.0V).

○GND (53PIN)

The GND pin is an analog circuit ground pin of the IC. Set the ground pattern as close as possible to that of resistors connected to the S1 to S16 pins.

○COMP1(55PIN)

The COMP1 pin is used to feed back the state of voltage to the external power supply in order to optimize the power supply voltage for the LED layer.

Positive feedback voltage is output to a pin having the lowest voltage out of the D1 to D8 pins. If the lowest voltage of the D1 to D8 pins is higher than 0.6V typical voltage, the COMP1 pin will become open-circuited. If the lowest voltage of these pins is lower than 0.6V typical voltage, the internal NPN transistor of the COMP1 pin will turn ON. The COMP1 pin is intended to connect to the output voltage monitor pin of the DC/DC converter.

○*COMP2(54PIN)*

The COMP2 pin is used to feed back the state of voltage to the external power supply in order to optimize the power supply voltage for the LED layer.
Positive feedback voltage is output to a pin having the lowest voltage out of the D9 to D16 pins. If the lowest voltage of the D9 to D16 pins is higher than 0.6V typical voltage, the COMP2 pin will become open-circuited. If the lowest voltage of these pins is lower than 0.6V typical voltage, the internal NPN transistor of the COMP2 pin will turn ON. The COMP2 pin is intended to connect to the output voltage monitor pin of the DC/DC converter.

○*CS(57PIN), CLK(58PIN,) DI(59PIN), DO(60PIN)*

These pins are used to control the IC with the CS, CLK, DI, and DO serial interfaces. Input levels are determined by the DVDD power supply of the digital block. For data input format and timing, refer to the description of Logic block to be hereinafter provided.

Input State	Input Level
High-level input	DVDD×0.7~ DVDD+0.3[V]
Low-level input	-0.3~DVDD×0.3 [V]

○*VSYNC(61PIN), HSYNC(62PIN)*

The VSYNC and HSYNC input signals enable the PWM light modulation signal to make setting of PWM frequency, PWM ON time, and PWM delay time. For data input format and timing, refer to the description of Logic block to be hereinafter provided.

○*ERR_DET(63PIN)*

The ERR_DET pin is used to output an IC error detection signal and provides the N-MOS open-drain output function. If this pin is pulled up to the DVDD voltage of the IC or else, it will be set to output High voltage for normal operation. If any error is detected, the internal NMOS of the IC will be put into ON state, setting the pin to output Low voltage.

State	FAIL Signal Output
Normal operation	OPEN
LED error detection	GND Level

When the ERR_DET pin is put into the GND Level, the LED has already caused an error. In this case, reading the registers located at addresses 05h to 0Ch makes it possible to recognize what channel is in what type of error state. (For detail, refer to the description of registers to be hereinafter provided.)

○*DGND(56PIN)*

The DGND pin is a digital circuit ground pin of the IC. Lay out the DGND pin using interconnect independent of that for the GND pin wherever possible.

○*DVDD(64PIN)*

The DVDD pin is used to input power in the digital block of the IC in the range of 3.0 to 3.6V. When the DVDD pin voltage reaches 3.3V (typ.), the IC will start operating. Insert a ceramic capacitor of approx. 1uF in capacitance between the DVDD and DGND pins in the vicinity of the IC.

Functions of Logic Block

Serial interface block

This IC is controlled with the CS, CLK, DI, and DO serial interfaces.
The following section describes data input format and timing.

◆WRITE MODE

・To write 1 byte of data:

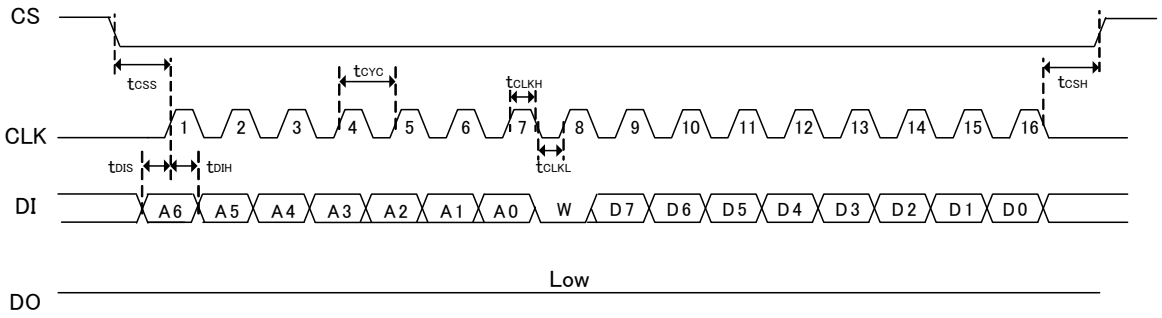


Figure 14. WRITE MODE (for 1byte)

・Write consecutive 32 bytes of data:

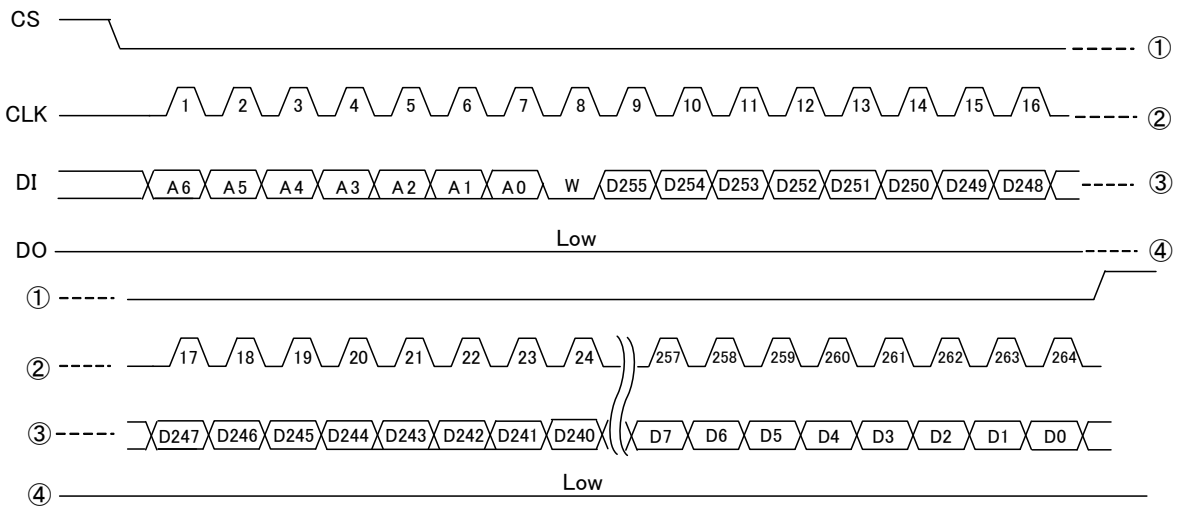


Figure 15. WRITE MODE (for 32byte)

Addresses are automatically counted up in increments of 1 address by 8 bits after the first set value.

◆**READ MODE**

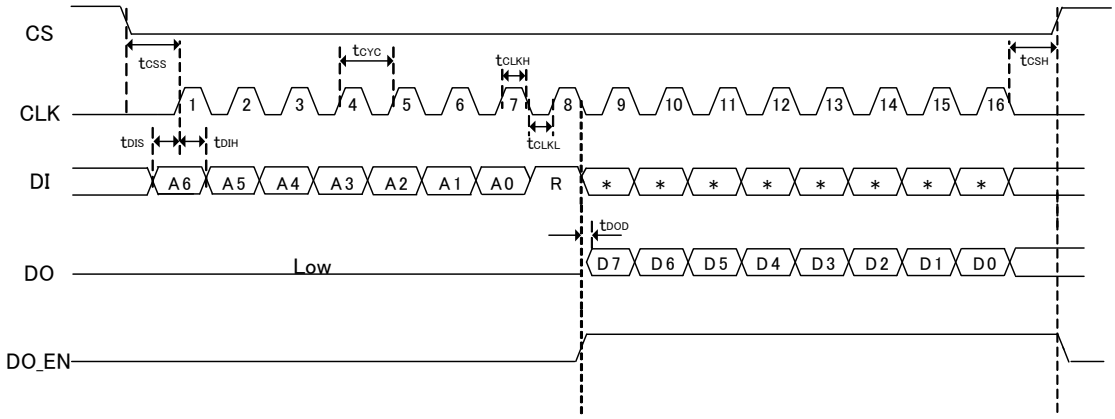


Figure 16. READ MODE

AC electrical characteristics:

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
CLK cycle	t_{CYC}	100	-	-	ns
CLK high level range	t_{CLKH}	35	-	-	ns
CLK low level range	t_{CLKL}	35	-	-	ns
DI input setup time	t_{DIS}	50	-	-	ns
DI input hold time	t_{DIH}	50	-	-	ns
CS input setup time	t_{CSS}	50	-	-	ns
CS input hold time	t_{CSH}	50	-	-	ns
DO output delay time	t_{DOD}	-	-	40	ns

(Output load capacitance: 15pF)

◆**HSYNC, VSYNC**

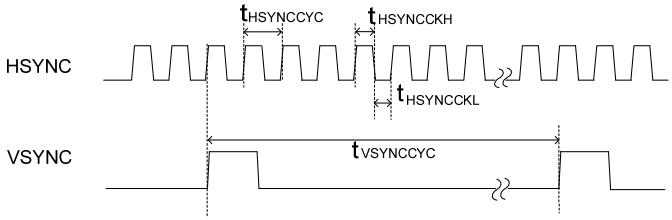


Figure 16-2. HSYNC VSYNC timing

・VSYNC SETUP/HOLD time

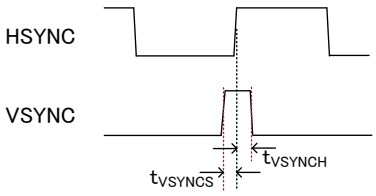


Figure 16-3. VSYNC SETUP/HOLD time

AC electrical characteristics:

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max	
HSYNC cycle	$t_{HSYNCCYC}$	244	-	-	ns
HSYNC high level range	$t_{HSYNCCKH}$	122	-	-	ns
HSYNC low level range	$t_{HSYNCCKL}$	122	-	-	ns
VSYNC cycle	$t_{VSYNCCYC}$	1000	-	-	us
VSYNC setup time	t_{VSYNCS}	20	-	-	ns
VSYNC hold time	t_{VSYNCH}	20	-	-	ns

(Output load capacitance: 15pF)

◆Register map（1/2）

The data in every register is updated in 3 ways which are showed below.

①Updated to the newest data immediately when the data is written.
②Updated to the newest data when the next VSYNC or VSYNC_REG signal rises up (positive-edge trigger).
③Updated to the newest data when the next PWM signal rises up (positive-edge trigger).

Address	R/W	Default	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
00h	R/W	FFh	LEDENA	LEDEN[7]	LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]	LEDEN[0]	Ch1 to Ch8 LED Enable
			Update Timing	①	①	①	①	①	①	①	①	
01h	R/W	FFh	LEDENB	LEDEN[15]	LEDEN[14]	LEDEN[13]	LEDEN[12]	LEDEN[11]	LEDEN[10]	LEDEN[9]	LEDEN[8]	Ch9～Ch16 LED Enable
			Update Timing	①	①	①	①	①	①	①	①	
02h	R/W	66h	LEDREFL	LEDREF[7]	LEDREF [6]	LEDREF [5]	LEDREF[4]	LEDREF [3]	LEDREF [2]	LEDREF[1]	LEDREF[0]	Analog light modulation (Low 8 bits)
			Update Timing	①	①	①	①	①	①	①	①	
03h	R/W	02h	LEDREFM	–	–	–	–	LEDREF[11]	LEDREF[10]	LEDREF [9]	LEDREF [8]	Analog light modulation (High 4 bits)
			Update Timing	–	–	–	–	①	①	①	①	
04h	R/W	02h	MASKSET	–	–	–	–	–	–	ERRMSK[1]	ERRMSK[0]	Mask time setting
			Update Timing	–	–	–	–	–	–	②	②	
05h	R	00h	ERRLEDOPA	ERLOP_08	ERLOP_07	ERLOP_06	ERLOP_05	ERLOP_04	ERLOP_03	ERLOP_02	ERLOP_01	Ch1 to Ch8 ERR pin monitor (LEDOP)
			Update Timing	①	①	①	①	①	①	①	①	
06h	R	00h	ERRLEDOPB	ERLOP_16	ERLOP_15	ERLOP_14	ERLOP_13	ERLOP_12	ERLOP_11	ERLOP_10	ERLOP_09	Ch9 to Ch16ERROR pin monitor (LEDOP)
			Update Timing	①	①	①	①	①	①	①	①	
07h	R	00h	ERRLEDSHA	ERLSH_08	ERLSH_07	ERLSH_06	ERLSH_05	ERLSH_04	ERLSH_03	ERLSH_02	ERLSH_01	Ch1 to Ch8ERR pin monitor (LEDSH)
			Update Timing	①	①	①	①	①	①	①	①	
08h	R	00h	ERRLEDSHB	ERLSH_16	ERLSH_15	ERLSH_14	ERLSH_13	ERLSH_12	ERLSH_11	ERLSH_10	ERLSH_09	Ch9 to Ch16ERRO pin monitor (LEDSH)
			Update Timing	①	①	①	①	①	①	①	①	
09h	R	00h	ERRRESSHA	ERRSH_08	ERRSH_07	ERRSH_06	ERRSH_05	ERRSH_04	ERRSH_03	ERRSH_02	ERRSH_01	Ch1 to Ch8ERR pin monitor (RESSH)
			Update Timing	①	①	①	①	①	①	①	①	
0Ah	R	00h	ERRRESHB	ERRSH_16	ERRSH_15	ERRSH_14	ERRSH_13	ERRSH_12	ERRSH_11	ERRSH_10	ERRSH_09	Ch9 to Ch16ERROR pin monitor (RESSH)
			Update Timing	①	①	①	①	①	①	①	①	
0Bh	R	00h	ERRMOSSHA	ERMSH_08	ERMSH_07	ERMSH_06	ERMSH_05	ERMSH_04	ERMSH_03	ERMSH_02	ERMSH_01	Ch1 to Ch8ERR pin monitor (MOSSH)
			Update Timing	①	①	①	①	①	①	①	①	
0Ch	R	00h	ERRMOSSHB	ERMSH_16	ERMSH_15	ERMSH_14	ERMSH_13	ERMSH_12	ERMSH_11	ERMSH_10	ERMSH_09	Ch9 to Ch16ERROR pin monitor (MOSSH)
			Update Timing	①	①	①	①	①	①	①	①	
0Dh	R/W	01h	DUMMY	DMY08	DMY07	DMY06	DMY05	DMY04	DMY03	DMY02	DMY01	Dummy register
			Update Timing	①	①	①	①	①	①	①	①	
0Eh	R/W	60h	SYSCONFIG	EAMPREFC	EAMPREFB	EAMPREFA	VSYNCDIS	MOSSHDIS	RESSHDIS	LEDSHDIS	LEDOPDIS	Setting register
			Update Timing	②	②	②	①	②	②	②	②	
0Fh	R/W	00h	VSYNCREG	–	–	–	–	–	–	–	VSNC_REG	VSYNC signal input with register
			Update Timing	–	–	–	–	–	–	–	①	
10h	R/W	0Ch	SSMSKSET	SSMASK[7]	SSMASK[6]	SSMASK[5]	SSMASK[4]	SSMASK[3]	SSMASK[2]	SSMASK[1]	SSMASK[0]	Mask section setting for soft start
			Update Timing	②	②	②	②	②	②	②	②	
11h	R/W	00h	DTYCNT01L	DTY01[7]	DTY01[6]	DTY01[5]	DTY01[4]	DTY01[3]	DTY01[2]	DTY01[1]	DTY01[0]	LED1 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
12h	R/W	00h	DTYCNT01M	–	–	–	–	DTY01[11]	DTY01[10]	DTY01[9]	DTY01[8]	LED1 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
13h	R/W	00h	DTYCNT02L	DTY02[7]	DTY02[6]	DTY02[5]	DTY02[4]	DTY02[3]	DTY02[2]	DTY02[1]	DTY02[0]	LED2 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
14h	R/W	00h	DTYCNT02M	–	–	–	–	DTY02[11]	DTY02[10]	DTY02[9]	DTY02[8]	LED2 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
15h	R/W	00h	DTYCNT03L	DTY03[7]	DTY03[6]	DTY03[5]	DTY03[4]	DTY03[3]	DTY03[2]	DTY03[1]	DTY03[0]	LED3 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
16h	R/W	00h	DTYCNT03M	–	–	–	–	DTY03[11]	DTY03[10]	DTY03[9]	DTY03[8]	LED3 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
17h	R/W	00h	DTYCNT04L	DTY04[7]	DTY04[6]	DTY04[5]	DTY04[4]	DTY04[3]	DTY04[2]	DTY04[1]	DTY04[0]	LED4 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
18h	R/W	00h	DTYCNT04M	–	–	–	–	DTY04[11]	DTY04[10]	DTY04[9]	DTY04[8]	LED4 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
19h	R/W	00h	DTYCNT05L	DTY05[7]	DTY05[6]	DTY05[5]	DTY05[4]	DTY05[3]	DTY05[2]	DTY05[1]	DTY05[0]	LED5 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
1Ah	R/W	00h	DTYCNT05M	–	–	–	–	DTY05[11]	DTY05[10]	DTY05[9]	DTY05[8]	LED5 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
1Bh	R/W	00h	DTYCNT06L	DTY06[7]	DTY06[6]	DTY06[5]	DTY06[4]	DTY06[3]	DTY06[2]	DTY06[1]	DTY06[0]	LED6 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
1Ch	R/W	00h	DTYCNT06M	–	–	–	–	DTY06[11]	DTY06[10]	DTY06[9]	DTY06[8]	LED6 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
1Dh	R/W	00h	DTYCNT07L	DTY07[7]	DTY07[6]	DTY07[5]	DTY07[4]	DTY07[3]	DTY07[2]	DTY07[1]	DTY07[0]	LED7 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
1Eh	R/W	00h	DTYCNT07M	–	–	–	–	DTY07[11]	DTY07[10]	DTY07[9]	DTY07[8]	LED7 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
1Fh	R/W	00h	DTYCNT08L	DTY08[7]	DTY08[6]	DTY08[5]	DTY08[4]	DTY08[3]	DTY08[2]	DTY08[1]	DTY08[0]	LED8 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
20h	R/W	00h	DTYCNT08M	–	–	–	–	DTY08[11]	DTY08[10]	DTY08[9]	DTY08[8]	LED8 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
21h	R/W	00h	DTYCNT09L	DTY09[7]	DTY09[6]	DTY09[5]	DTY09[4]	DTY09[3]	DTY09[2]	DTY09[1]	DTY09[0]	LED9 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
22h	R/W	00h	DTYCNT09M	–	–	–	–	DTY09[11]	DTY09[10]	DTY09[9]	DTY09[8]	LED9 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
23h	R/W	00h	DTYCNT10L	DTY10[7]	DTY10[6]	DTY10[5]	DTY10[4]	DTY10[3]	DTY10[2]	DTY10[1]	DTY10[0]	LED10 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
24h	R/W	00h	DTYCNT10M	–	–	–	–	DTY10[11]	DTY10[10]	DTY10[9]	DTY10[8]	LED10 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
25h	R/W	00h	DTYCNT11L	DTY11[7]	DTY11[6]	DTY11[5]	DTY11[4]	DTY11[3]	DTY11[2]	DTY11[1]	DTY11[0]	LED11 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
26h	R/W	00h	DTYCNT11M	–	–	–	–	DTY11[11]	DTY11[10]	DTY11[9]	DTY11[8]	LED11 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
27h	R/W	00h	DTYCNT12L	DTY12[7]	DTY12[6]	DTY12[5]	DTY12[4]	DTY12[3]	DTY12[2]	DTY12[1]	DTY12[0]	LED12 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	

◆Register map（2/2）

The data in every register is updated in 3 ways which are showed below.

①Updated to the newest data immediately when the data is written.
②Updated to the newest data when the next VSYNC or VSYNC_REG signal rises up (positive-edge trigger).
③Updated to the newest data when the next PWM signal rises up (positive-edge trigger).

Address	R/W	Default	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
28h	R/W	00h	DTYCNT12M	–	–	–	–	DTY12[11]	DTY12[10]	DTY12[9]	DTY12[8]	LED12 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
29h	R/W	00h	DTYCNT13L	DTY13[7]	DTY13[6]	DTY13[5]	DTY13[4]	DTY13[3]	DTY13[2]	DTY13[1]	DTY13[0]	LED13 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
2Ah	R/W	00h	DTYCNT13M	–	–	–	–	DTY13[11]	DTY13[10]	DTY13[9]	DTY13[8]	LED13 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
2Bh	R/W	00h	DTYCNT14L	DTY14[7]	DTY14[6]	DTY14[5]	DTY14[4]	DTY14[3]	DTY14[2]	DTY14[1]	DTY14[0]	LED14 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
2Ch	R/W	00h	DTYCNT14M	–	–	–	–	DTY14[11]	DTY14[10]	DTY14[9]	DTY14[8]	LED14 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
2Dh	R/W	00h	DTYCNT15L	DTY15[7]	DTY15[6]	DTY15[5]	DTY15[4]	DTY15[3]	DTY15[2]	DTY15[1]	DTY15[0]	LED15 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
2Eh	R/W	00h	DTYCNT15M	–	–	–	–	DTY15[11]	DTY15[10]	DTY15[9]	DTY15[8]	LED15 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
2Fh	R/W	00h	DTYCNT16L	DTY16[7]	DTY16[6]	DTY16[5]	DTY16[4]	DTY16[3]	DTY16[2]	DTY16[1]	DTY16[0]	LED16 PWM ON range setting (Low 8 bits)
			Update Timing	③	③	③	③	③	③	③	③	
30h	R/W	00h	DTYCNT16M	–	–	–	–	DTY16[11]	DTY16[10]	DTY16[9]	DTY16[8]	LED16 PWM ON range setting (High 4bit)
			Update Timing	–	–	–	–	③	③	③	③	
31h	R/W	00h	DLYCNT01L	DLY01[7]	DLY01[6]	DLY01[5]	DLY01[4]	DLY01[3]	DLY01[2]	DLY01[1]	DLY01[0]	LED1 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
32h	R/W	00h	DLYCNT01M	–	–	–	–	DLY01[11]	DLY01[10]	DLY01[9]	DLY01[8]	LED1 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
33h	R/W	00h	DLYCNT02L	DLY02[7]	DLY02[6]	DLY02[5]	DLY02[4]	DLY02[3]	DLY02[2]	DLY02[1]	DLY02[0]	LED2 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
34h	R/W	00h	DLYCNT02M	–	–	–	–	DLY02[11]	DLY02[10]	DLY02[9]	DLY02[8]	LED2 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
35h	R/W	00h	DLYCNT03L	DLY03[7]	DLY03[6]	DLY03[5]	DLY03[4]	DLY03[3]	DLY03[2]	DLY03[1]	DLY03[0]	LED3 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
36h	R/W	00h	DLYCNT03M	–	–	–	–	DLY03[11]	DLY03[10]	DLY03[9]	DLY03[8]	LED3 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
37h	R/W	00h	DLYCNT04L	DLY04[7]	DLY04[6]	DLY04[5]	DLY04[4]	DLY04[3]	DLY04[2]	DLY04[1]	DLY04[0]	LED4 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
38h	R/W	00h	DLYCNT04M	–	–	–	–	DLY04[11]	DLY04[10]	DLY04[9]	DLY04[8]	LED4 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
39h	R/W	00h	DLYCNT05L	DLY05[7]	DLY05[6]	DLY05[5]	DLY05[4]	DLY05[3]	DLY05[2]	DLY05[1]	DLY05[0]	LED5 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
3Ah	R/W	00h	DLYCNT05M	–	–	–	–	DLY05[11]	DLY05[10]	DLY05[9]	DLY05[8]	LED5 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
3Bh	R/W	00h	DLYCNT06L	DLY06[7]	DLY06[6]	DLY06[5]	DLY06[4]	DLY06[3]	DLY06[2]	DLY06[1]	DLY06[0]	LED6 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
3Ch	R/W	00h	DLYCNT06M	–	–	–	–	DLY06[11]	DLY06[10]	DLY06[9]	DLY06[8]	LED6 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
3Dh	R/W	00h	DLYCNT07L	DLY07[7]	DLY07[6]	DLY07[5]	DLY07[4]	DLY07[3]	DLY07[2]	DLY07[1]	DLY07[0]	LED7 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
3Eh	R/W	00h	DLYCNT07M	–	–	–	–	DLY07[11]	DLY07[10]	DLY07[9]	DLY07[8]	LED7 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
3Fh	R/W	00h	DLYCNT08L	DLY08[7]	DLY08[6]	DLY08[5]	DLY08[4]	DLY08[3]	DLY08[2]	DLY08[1]	DLY08[0]	LED8 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
40h	R/W	00h	DLYCNT08M	–	–	–	–	DLY08[11]	DLY08[10]	DLY08[9]	DLY08[8]	LED8 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
41h	R/W	00h	DLYCNT09L	DLY09[7]	DLY09[6]	DLY09[5]	DLY09[4]	DLY09[3]	DLY09[2]	DLY09[1]	DLY09[0]	LED9 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
42h	R/W	00h	DLYCNT09M	–	–	–	–	DLY09[11]	DLY09[10]	DLY09[9]	DLY09[8]	LED9 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
43h	R/W	00h	DLYCNT10L	DLY10[7]	DLY10[6]	DLY10[5]	DLY10[4]	DLY10[3]	DLY10[2]	DLY10[1]	DLY10[0]	LED10 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
44h	R/W	00h	DLYCNT10M	–	–	–	–	DLY10[11]	DLY10[10]	DLY10[9]	DLY10[8]	LED10 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
45h	R/W	00h	DLYCNT11L	DLY11[7]	DLY11[6]	DLY11[5]	DLY11[4]	DLY11[3]	DLY11[2]	DLY11[1]	DLY11[0]	LED11 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
46h	R/W	00h	DLYCNT11M	–	–	–	–	DLY11[11]	DLY11[10]	DLY11[9]	DLY11[8]	LED11 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
47h	R/W	00h	DLYCNT12L	DLY12[7]	DLY12[6]	DLY12[5]	DLY12[4]	DLY12[3]	DLY12[2]	DLY12[1]	DLY12[0]	LED12 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
48h	R/W	00h	DLYCNT12M	–	–	–	–	DLY12[11]	DLY12[10]	DLY12[9]	DLY12[8]	LED12 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
49h	R/W	00h	DLYCNT13L	DLY13[7]	DLY13[6]	DLY13[5]	DLY13[4]	DLY13[3]	DLY13[2]	DLY13[1]	DLY13[0]	LED13 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
4Ah	R/W	00h	DLYCNT13M	–	–	–	–	DLY13[11]	DLY13[10]	DLY13[9]	DLY13[8]	LED13 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
4Bh	R/W	00h	DLYCNT14L	DLY14[7]	DLY14[6]	DLY14[5]	DLY14[4]	DLY14[3]	DLY14[2]	DLY14[1]	DLY14[0]	LED14 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
4Ch	R/W	00h	DLYCNT14M	–	–	–	–	DLY14[11]	DLY14[10]	DLY14[9]	DLY14[8]	LED14 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
4Dh	R/W	00h	DLYCNT15L	DLY15[7]	DLY15[6]	DLY15[5]	DLY15[4]	DLY15[3]	DLY15[2]	DLY15[1]	DLY15[0]	LED15 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
4Eh	R/W	00h	DLYCNT15M	–	–	–	–	DLY15[11]	DLY15[10]	DLY15[9]	DLY15[8]	LED15 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	
4Fh	R/W	00h	DLYCNT16L	DLY16[7]	DLY16[6]	DLY16[5]	DLY16[4]	DLY16[3]	DLY16[2]	DLY16[1]	DLY16[0]	LED16 PWM delay time setting (Low 8 bits)
			Update Timing	②	②	②	②	②	②	②	②	
50h	R/W	00h	DLYCNT16M	–	–	–	–	DLY16[11]	DLY16[10]	DLY16[9]	DLY16[8]	LED16 PWM delay time setting (High 4 bits)
			Update Timing	–	–	–	–	②	②	②	②	

◆Description of registers

●ADDR=00h
LEDENA (Ch1 to Ch8 LED Enable control register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	LEDEN[7]	LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]	LEDEN[0]
Default	1	1	1	1	1	1	1	1

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=01h
LEDENB (Ch9 to Ch16 LED enable control register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	LEDEN[15]	LEDEN[14]	LEDEN[13]	LEDEN[12]	LEDEN[11]	LEDEN[10]	LEDEN[9]	LEDEN[8]
Default	1	1	1	1	1	1	1	1

LEDEN	Enable control
0	Disable
1	Enable

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=02h
LEDREFA (Analog light modulation setting register - Low 8 bits -: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	LEDREF[7]	LEDREF[6]	LEDREF[5]	LEDREF[4]	LEDREF[3]	LEDREF[2]	LEDREF[1]	LEDREF[0]
Default	0	1	1	0	0	1	1	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=03h
LEDREFB (Analog light modulation setting register - High 4 bits -: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	-	-	LEDREF[11]	LEDREF[10]	LEDREF[9]	LEDREF[8]
Default	-	-	-	-	0	0	1	0

LEDREF[11：0] (Register output)	LED_REF_12～LED_REF_01（to analog）
000h～0CDh	0CDh
0CEh～7FFh	0CEh～7FFh
800h～FFFh	800h

LED_REF_12 to LED_REF_01 signals to analog are used with the maximum voltage of 1.0V and the minimum voltage of 0.1V, they are converted with the decoder listed above.

Minimum value (0.1V): 0.1 / 2 * 4095 = 0CDh
Maximum value (1.0V): 1 / 2 * 4095 = 800h
Default value (0.3V): 0.3 / 2 * 4095 = 266h
Note: Reg02h and 03h are synchronized with the leading edge of VSYNC input signal.

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=04h
MASKSET (Error signal output mask time setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	-	-	-	-	ERRMSK[1]	ERRMSK[0]
Default	-	-	-	-	-	-	1	0

Decoder

ERRMSK[1]	ERRMSK[0]	ERROR MASK Count Value	ERROR MASK TIME
0	0	02h(2d)	HSYNC : 2～5 clks
0	1	04h(4d)	HSYNC : 4～7 clks
1	0	08h(8d)	HSYNC : 8～11 clks
1	1	10 h (16d)	HSYNC : 16～19 clks

Note: For counting values, a counter that counts one every four HSYNC signals is used.
Default : set08h(8d) to 8 counts
Due to there are 4 types of ERRSTATE, the mask time from PWM=H to ERRDET=L is HSYNC8～11 clks.

The data in register is update to the newest data when the next VSYNC signal rises up (positive-edge trigger).

●ADDR=05h
ERRLEDOPA (LED1 to LED8 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRLEDOP_08	ERRLEDOP_07	ERRLEDOP_06	ERRLEDOP_05	ERRLEDOP_04	ERRLEDOP_03	ERRLEDOP_02	ERRLEDOP_01
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=06h
ERRLEDOPB (LED9 to LED16 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRLEDOP_16	ERRLEDOP_15	ERRLEDOP_14	ERRLEDOP_13	ERRLEDOP_12	ERRLEDOP_11	ERRLEDOP_10	ERRLEDOP_09
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=07h
ERRLEDSHA (LED1 to LED8 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRLEDSH_08	ERRLEDSH_07	ERRLEDSH_06	ERRLEDSH_05	ERRLEDSH_04	ERRLEDSH_03	ERRLEDSH_02	ERRLEDSH_01
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=08h
ERRLEDB (LED9 to LED16 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRLEDSH_16	ERRLEDSH_15	ERRLEDSH_14	ERRLEDSH_13	ERRLEDSH_12	ERRLEDSH_11	ERRLEDSH_10	ERRLEDSH_09
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=09h
ERRRESSHA (LED1 to LED8 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRRESSH_08	ERRRESSH_07	ERRRESSH_06	ERRRESSH_05	ERRRESSH_04	ERRRESSH_03	ERRRESSH_02	ERRRESSH_01
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=0Ah
ERRRESSHB (LED9 to LED16 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRRESSH_16	ERRRESSH_15	ERRRESSH_14	ERRRESSH_13	ERRRESSH_12	ERRRESSH_11	ERRRESSH_10	ERRRESSH_09
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=0Bh
ERRMOSSHA (LED1 to LED8 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRMOSSH_08	ERRMOSSH_07	ERRMOSSH_06	ERRMOSSH_05	ERRMOSSH_04	ERRMOSSH_03	ERRMOSSH_02	ERRMOSSH_01
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=0Ch

ERRMOSSHB (LED9 to LED16 ERROR pin monitor: Read)

Bit	7	6	5	4	3	2	1	0
Register Name	ERRMOSSH_16	ERRMOSSH_15	ERRMOSSH_14	ERRMOSSH_13	ERRMOSSH_12	ERRMOSSH_11	ERRMOSSH_10	ERRMOSSH_09
Default	0	0	0	0	0	0	0	0

ERR	ERR monitor
0	Normal
1	ERROR

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=0Dh

DUMMY (Dummy register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	DMY08	DMY07	DMY06	DMY05	DMY04	DMY03	DMY02	DMY01
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

●ADDR=0Eh

SYSCONFIG (Dummy register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	EAMPREFC	EAMPREFB	EAMPREFA	VSYNCDIS	MOSSHDIS	RESSHDIS	LEDSHDIS	LEDOPDIS
Default	0	1	1	0	0	0	0	0

LEDOPDIS	LED Open Disable control
0	LED open detection is enabled
1	LED open detection is disabled

LEDSHDIS	LED Short Disable control
0	LED short detection is enabled
1	LED short detection is disabled

RESSHDIS	RES Short Disable control
0	Resistor short detection is enabled
1	Resistor short detection is disabled

MOSSHDIS	MOS Short Disable control
0	MOS short detection is enabled
1	MOS short detection is disabled

VSNCDIS	VSYNC Disable control
0	External VSYNC is enabled.
1	External VSYNC is disenabled.

When VSYNCDIS=1 (disable VSYNC), the written data is not reflected.
When VSYNCDIS=0 (enable VSYNC), the written data is updated when VSYNC signal rises up.

The register LEDOPDIS, LEDSHDIS, RESSHDIS, MOSSHDIS is update to the newest data when the next VSYNC signal rises up (positive-edge trigger) after CS positive edge.
The register VSNCDIS is updated to the newest data immediately when the new data is written.

Decoder

EAMPREFC	EAMPREFB	EAMPREFA	EAMP Ref. Voltage Setting	EAMP_DAC_11～EAMP_DAC_01
0	0	0	0.3V	0F5h(245d)
0	0	1	0.4V	147h(327d)
0	1	0	0.5V	199h(409d)
0	1	1	0.6V	1EBh(491d)
1	0	0	0.8V	28Fh(655d)
1	0	1	1.0V	333h(819d)
1	1	0	1.2V	3E7h(999d)
1	1	1	1.5V	4CCh(1228d)

DAC output voltages to analog are converted with the decoders listed above.

0.3V: 0.3 / 5 * 4095 = 0F5h
0.4V: 0.4 / 5 * 4095 = 147h
0.5V: 0.5 / 5 * 4095 = 199h
0.6V: 0.6 / 5 * 4095 = 1EBh
0.8V: 0.8 / 5 * 4095 = 28Fh
1.0V: 1.0 / 5 * 4095 = 333h
1.2V: 1.2 / 5 * 4095 = 3E7h
1.5V: 1.5 / 5 * 4095 = 4CCh

The data in register EAMPREF is update to the newest data when the next VSYNC signal rises up (positive-edge trigger).

●ADDR=0Fh
VSYNCREG (VSYNCREG control register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	-	-	-	-	-	VSNC_REG
Default	-	-	-	-	-	-	-	0

VSNC_REG	VSYNCREG control
0	OFF
1	ON

If VSYNC is not used, the register can be controlled by turning ON/OFF VSYNCREG instead of VSYNC.
The data in register is updated to the newest data immediately when the new data is written.

●ADDR=10h
SSMASKSET (Soft start mask register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	SSMASK[7]	SSMASK[6]	SSMASK[5]	SSMASK[4]	SSMASK[3]	SSMASK[2]	SSMASK[1]	SSMASK[0]
Default	0	0	0	0	1	1	0	0

This register is used to make mask interval setting of abnormal protection (in sync with VSYNC) for the startup of power supply.

This count starts up from VSYNC pulse input. The count value is not relation with the STB pin signal or the register LEDEN. Please refer to the timing chart (soft start mask) in detail.

Decoder

SSMASK[7:0]	SS mask interval
“0000 0000”	No mask time
“0000 0001”	VSYNC 2clks
“0000 0010”	VSYNC 3clks
“0000 0011”	VSYNC 4clks
-	-
“1111 1101”	VSYNC 254clks
“1111 1110”	VSYNC 255clks
“1111 1111”	VSYNC 256clks

The data in register is updated to the newest data when the next VSYNC (positive-edge trigger).

●ADDR=11h
DTYCNT01L (LED1 PWM duty setting register - Low 8 bits -: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	DTY01[7]	DTY01[6]	DTY01[5]	DTY01[4]	DTY01[3]	DTY01[2]	DTY01[1]	DTY01[0]
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data when the next PWM signal rises up (positive-edge trigger).

●ADDR=12h
DTYCNT01M (LED1 PWM duty setting register - High 4 bits -: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	–	–	–	–	DTY01[11]	DTY01[10]	DTY01[9]	DTY01[8]
Default	–	–	–	–	0	0	0	0

This register is used to make setting of pulse duty for PWM light modulation in a total of 12 bits, i.e., Bit7-0 when ADDR=11h and Bit3-0 when ADDR=12h.

DTY01[11 : 0]	LED Pulse Width
“0000 0000 0000”	Normally set to Low (default)
“0000 0000 0001”	HSYNC 2 clock width
“0000 0000 0010”	HSYNC 3 clock width
“0000 0000 0011”	HSYNC 4 clock width
to	to
“1111 1111 1100”	HSYNC 4093 clock width
“1111 1111 1101”	HSYNC 4094 clock width
“1111 1111 1110”	HSYNC 4095 clock width
“1111 1111 1111”	HSYNC 4096 clock width

The data in register is updated to the newest data when the next PWM signal rises up (positive-edge trigger).

●ADDR=13h～30h

This register is used to make setting of PWM pulse width for LED2 to LED16. The setting procedure is the same as that for LED1 with ADDR set to 11h and 12h.

The data in register is updated to the newest data when the next PWM signal rises up (positive-edge trigger).

●ADDR=31h

DLYCNT01L (LED1 PWM Delay setting register – Low 8bit-: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	DLY01[7]	DLY01[6]	DLY01[5]	DLY01[4]	DLY01[3]	DLY01[2]	DLY01[1]	DLY01[0]
Default	0	0	0	0	0	0	0	0

The data in register is updated to the newest data when the next VSYNC signal rises up (positive-edge trigger).

●ADDR=32h

DLYCNT01M (LED1 PWM Delay setting register–High 4bit-: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	—	—	—	—	DLY01[11]	DLY01[10]	DLY01[9]	DLY01[8]
Default	—	—	—	—	0	0	0	0

This register is used to make setting of delay width for PWM light modulation in a total of 12 bits, i.e., Bit7-0 when ADDR=31h and Bit3-0 when ADDR=32h.

DLY01[11 : 0]	LED Delay Width
“0000 0000 0000”	HSYNC0 clock width
“0000 0000 0001”	HSYNC1 clock width
“0000 0000 0010”	HSYNC 2 clock width
“0000 0000 0011”	HSYNC 3 clock width
to	to
“1111 1111 1100”	HSYNC 4092 clock width
“1111 1111 1101”	HSYNC 4093 clock width
“1111 1111 1110”	HSYNC 4094 clock width
“1111 1111 1111”	HSYNC 4095 clock width

The data in register is updated to the newest data when the next VSYNC signal rises up (positive-edge trigger).

●ADDR=33h～50h

This register is used to make PWM delay width setting for LED2 to LED16. The setting procedure is the same as that for LED1 with ADDR set to 31h and 32h.

The data in register is updated to the newest data when the next VSYNC signal rises up (positive-edge trigger).

◆Timing chart

●PWM Delay and ON Duty setting procedure

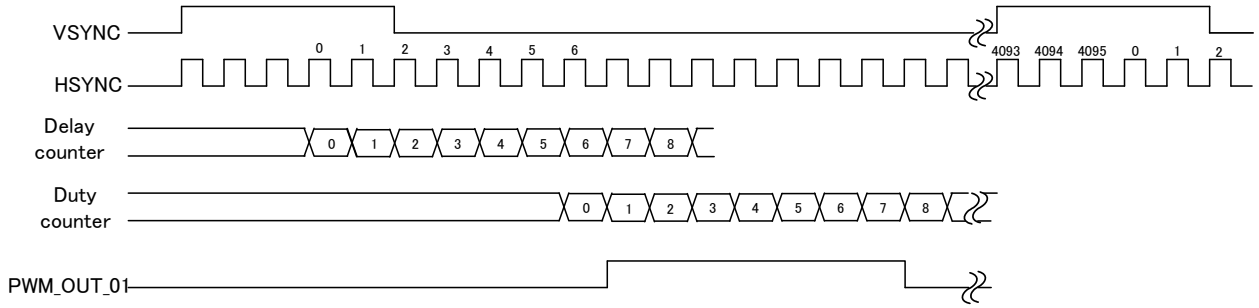


Figure 17. Setting for PWM Delay and ON Duty

By making register setting, PWM output delay and ON duty time counts of CH1 to CH16 can be controlled.
The above timing chart shows an example for CH1.
(To make delay time count setting, write 06h in address 31h. To make ON duty time count setting, write 07h in address 11h.)

The delay counter starts counting after counting three from the leading edge of VSYNC signal. When the counter reaches the set delay count value (06h), the duty counter will start counting simultaneously when the PWM_OUT_01 signal is set to “H”. Subsequently, when the duty counter reaches the set duty count value (07h), the PWM_OUT_01 signal will be set to ”L”. Since then, the said sequence is continuously repeated.
The same control is also carried out for CH2 to CH16.

The delay counter counts up to FFCh. Even if the set value exceeds this maximum value, it will also count up to FFCh.

●oft-start masking function

A value set at address 10h serves as the pulse number of the VSYNC signal and masks the error signal control in the relevant section.

(Example) When ADDR=10h and DATA=02h:

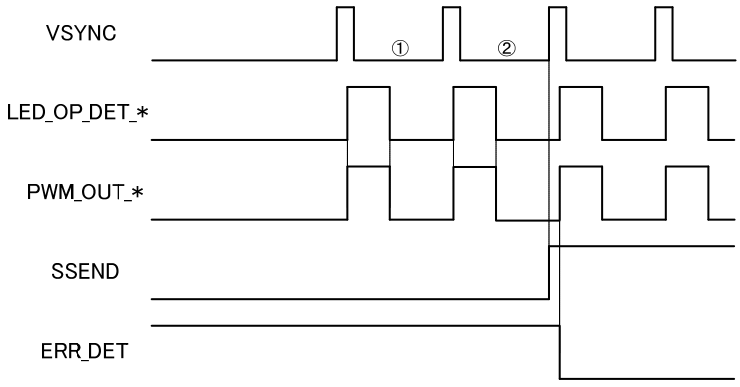


Figure 18. In case of ADDR:10h and DATA:02h

● ERROR control

There are the following four types of ERROR detection signals:

(1) LED OPEN, (2) LED SHORT, (3) REGISTER SHORT, and (4) MOS SHORT

The following section shows timing charts with the setting below:

LED OPEN
LED SHORT, REGISTER SHORT are in the same way.
(example) ERRMSK[1:0]＝10b (ERR MASK count：08d)

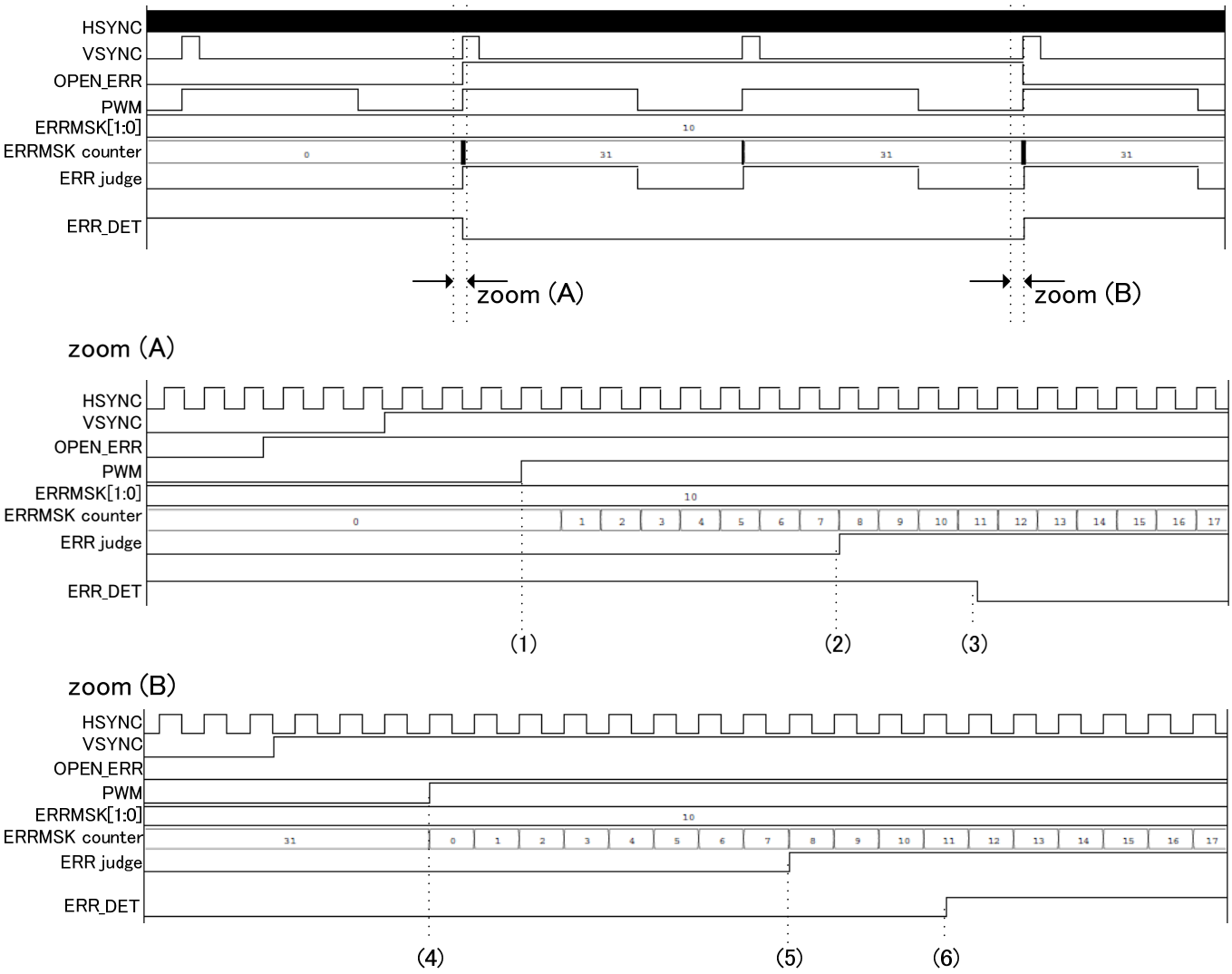


Figure 19-1. Timing Chart for Error detection 1

Zoom (A) is the operation of ERROR detection.
(1)…When the abnormal signal OPEN_ERR(internal signal) is detected, and PWM=H, the abnormal condition is detected, ERRMSK counter starts.
(2)…When ERRMSK counter reaches to the register ERRMSK[1:0]=10b, the condition is judged to the abnormal. The internal signal ERR_judge=H.
(3)…The external pin ERR_DET turns to ERR_DET=L within 4 clks of HSYNC.

Zoom (B) is the operation of ERROR release.
(4)…When the abnormal signal is released (OPEN_ERR=L) and PWM=H, ERRMSK counter starts.
(5)…When ERRMSK counter reaches to the register ERRMSK[1:0] =10b, the condition is judged to the normal. The internal signal ERR_judge=H.
(6)…The external pin ERR_DET turns to ERR_DET=HiZ (High as pulled up) within 4 clks of HSYNC.

MOSSHORT
(example) ERRMSK[1:0]＝10b (ERR MASK count：08d)

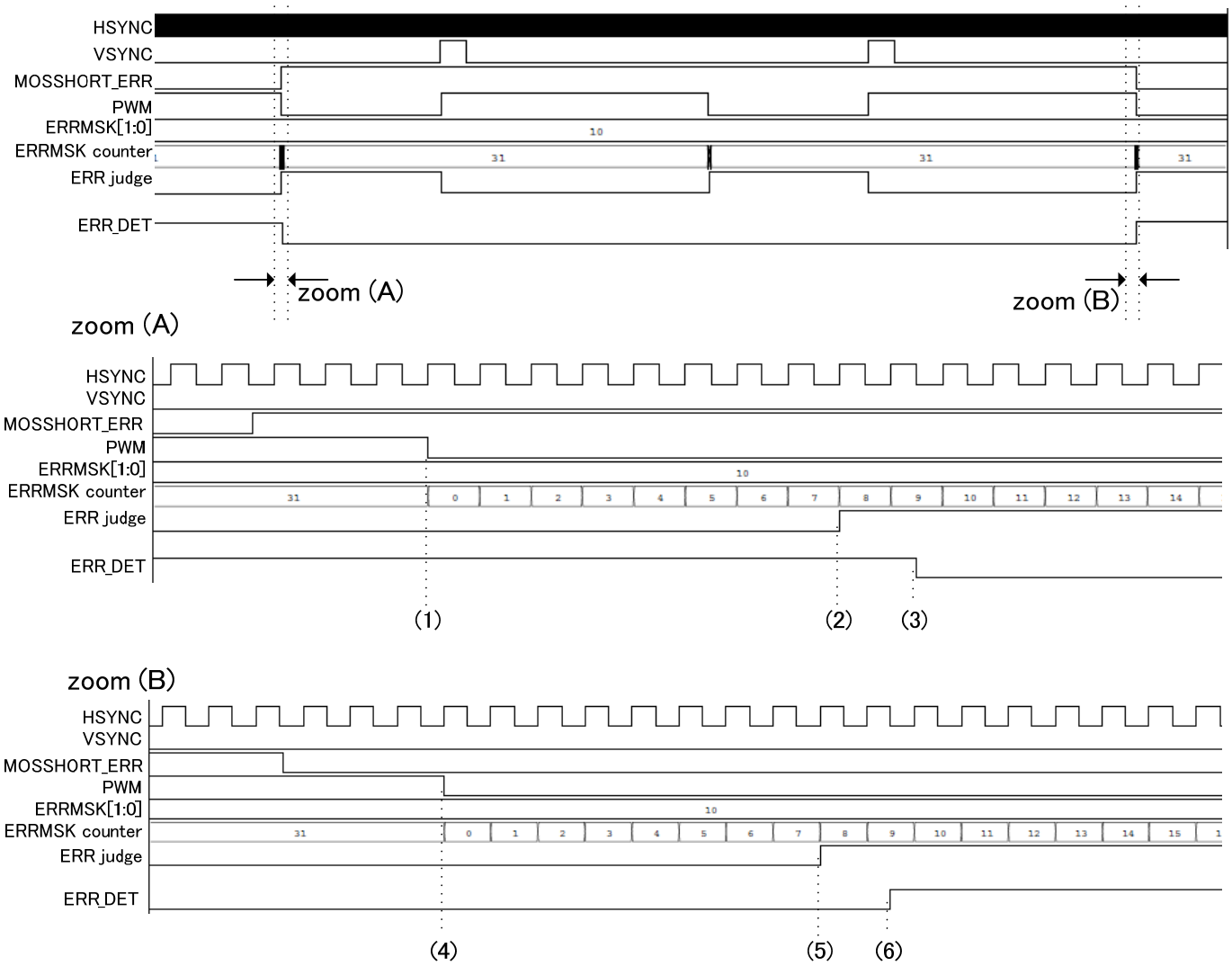


Figure 19-2. Timing Chart for Error detection 2

Zoom (A) is the operation of ERROR detection.
(1)…When the abnormal signal MOSSHORT_ERR(internal signal) is detected, and PWM=L, the abnormal condition is detected, ERRMSK counter starts.
(2)…When ERRMSK counter reaches to the register ERRMSK[1:0]=10b, the condition is judged to the abnormal. The internal signal ERR_judge=H.
(3)…The external pin ERR_DET turns to ERR_DET=L within 4 clks of HSYNC.

Zoom (B) is the operation of ERROR release.
(4)…When the abnormal signal is released (MOSSHORT_ERR=L) and PWM=L, ERRMSK counter starts.
(5)…When ERRMSK counter reaches to the register ERRMSK[1:0] =10b, the condition is judged to the normal. The internal signal ERR_judge=H.
(6)…The external pin ERR_DET turns to ERR_DET=HiZ (High as pulled up) within 4 clks of HSYNC.

◆Normal operating mode, start sequence

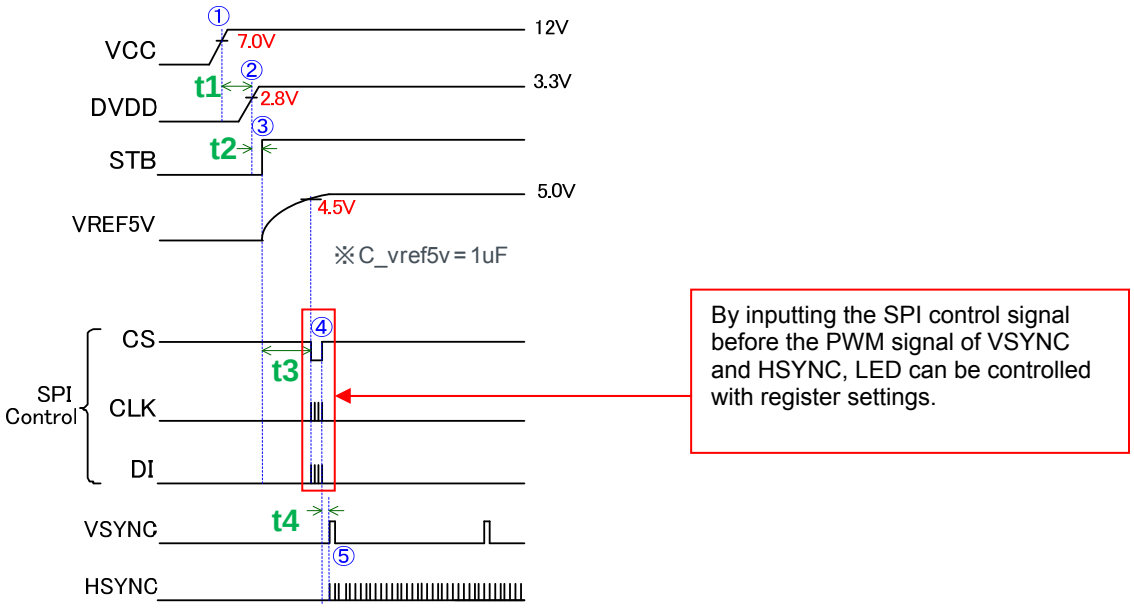


Figure 20. Starting Sequence for normal operation

When you light the LED by general SPI control, please follow the sequence below.

① Input the power supply of VCC.
(If the voltage of VCC pin becomes higher than 7.0V, the analog block starts operating.)

② Input the power supply of DVDD.
(If the voltage of DVDD pin becomes higher than 2.8V, reset of the logic block is released.)

③ Launch the STB from L to H.
(The voltage of VREF5V pin charged by STB=H. If the voltage of VREF5V pin becomes higher than 4.5V, the LED driver starts operating.)

④ Write the data to the register by SPI control, then set the LED driver.
(Set of the LED driver operation.)

⑤ Input the VSYNC, HSYNC signal which is for PWM dimming.
(Set of the PWM dimming operation.)

start sequence characteristics:

timing	Symbol	Need time min	unit
① - ②	t1	5.0	us
② - ③	t2	1.0	us
③ - ④	t3	85.0	us
④ - ⑤	t4	tHSYNCCYC (HSYNC 1cycle)	-

◆PWM dimming mode, Boot sequence

In BD9271KUT, as process mode, there is a test mode for running the LED driver, even there is no environment for SPI control. After inputting the power supply of VCC and DVDD, by setting the STB to H, it can be changed to PWM dimming operation mode achieved by duty control immediately. And the operating conditions are as below

Power supply：VCC and DVDD are in normal operating range.
・VCC=9.0V～35V, DVDD=3.0V～3.6V

Settings of LED driver（Default settings of register）
・Set all CHs to ON state （LED 1 CH～16CH）
・Setting voltage for LED current（Voltage of S1～S16 pin）：0.30V
・Reference voltage of error amplifier：0.60V
・Soft start setting：16 count of VSYNC

PWM dimmingoperation mode

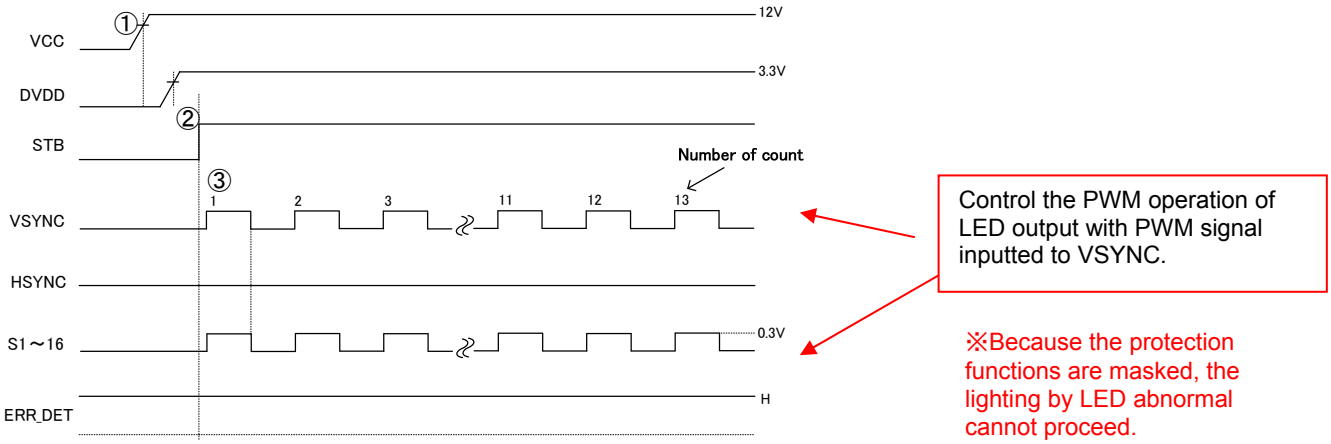


Figure 21. Starting Sequence for PWM dimming1

Settings of PWM dimming operation mode
- ・VSYNC=PWM dimming signal（Input the pulse signal for PWM dimming to VSYNC.）
- ・HSYNC=GND（Setting for abnormal detection）

When you use the PWM dimming mode, please follow the sequence below.

① Input the power supply of VCC and DVDD.
② Launch the STB from L to H.
③ Input the pulse signal to VSYNC.

PWM dimming operation mode (with abnormol detection function)

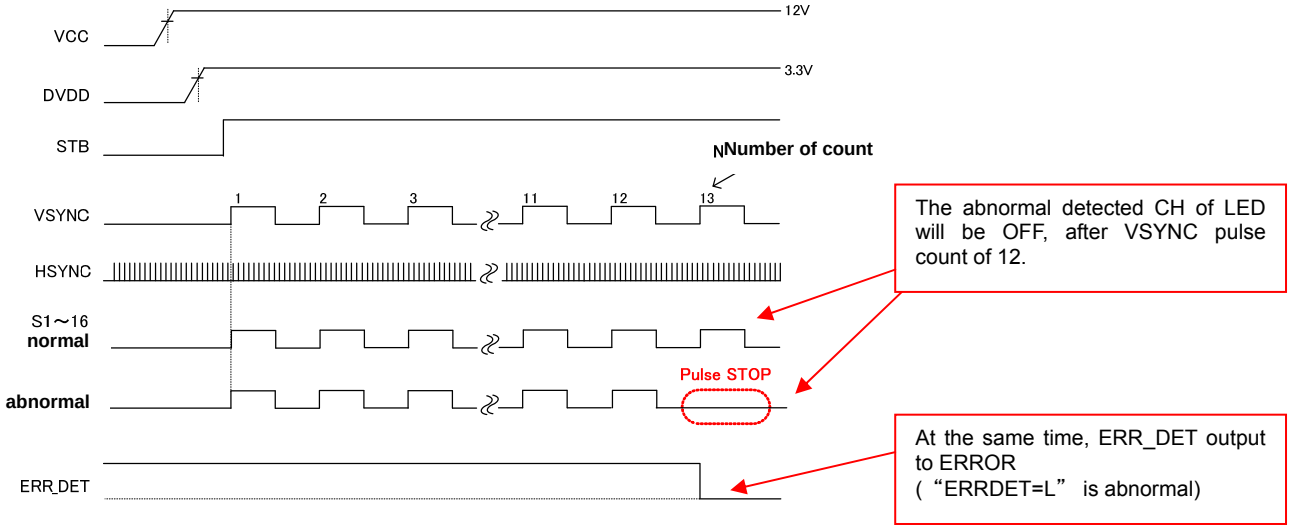


Figure 22. Starting Sequence for PWM dimming2

Setting of PWM dimming
- ・ VSYNC: PWM dimming signal (To input a pulse for PWM dimming to VSYNC pin)
- ・ HSYNC: 4096 counts during 1cycle of VSYNC signal

◆**Condition for protections**

Protection name	Protection pin	Detection Condition	Release Condition	Protection Type
LED OPEN	Dx	Dx < 0.1V CHx=EN,PWMx=High	Dx > 0.1V	Abnormal detection ERR_DET signal output
LEDSHORT	Dx	Dx > 5V (LSP=OPEN) CHx=EN,PWMx=High	Dx < 5V (LSP=OPEN)	Abnormal detection ERR_DET signal output
RES SHORT	Sx	Sx < 0.15V(*1) CHx=EN,PWMx=High	Sx > 0.15V(*1)	Abnormal detection ERR_DET signal output
MOSSHORT	Sx	Sx>0.15V(*1) CHx=EN,PWMx=Low	Sx < 0.15V(*1)	Abnormal detection ERR_DET signal output
VCC UVLO	VCC	VCC<6.7V	VCC>7.0V	Abnormal detection ERR_DET signal output

(*1)…The initial value of the detect threshold of RESSHORT and MOSSHORT are 0.15V. And those correspond to the register LEDREF.

- **LED_OPEN protection**

When PWMx=HIGH, If Drain pin becomes 0.1V(typ) or lower, ERR_DET = LOW is outputted and LED OPEN error will be detected.

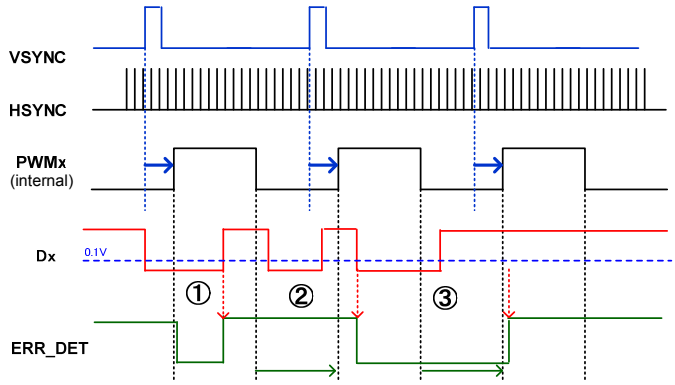


Figure 23. LED OPEN Protection

① When PWMx=HIGH, LED OPEN error is detected. ERR_DET=LOW is outputted.
If drain pin voltage is release condition, ERR_DET=HIGH is outputted.
② When PWMx=LOW, LED OPEN error is not detected.
③ When PWMx=HIGH, LED OPEN error is detected. When PWMx=LOW, If drain pin voltage is release condition, ERR_DET output keep-hold.

- **LED_SHORT protection**

When PWMx=HIGH, If Drain pin becomes 5V(typ) or more (LSP=OPEN), ERR_DET = LOW is outputted and LED SHORT error will be detected.

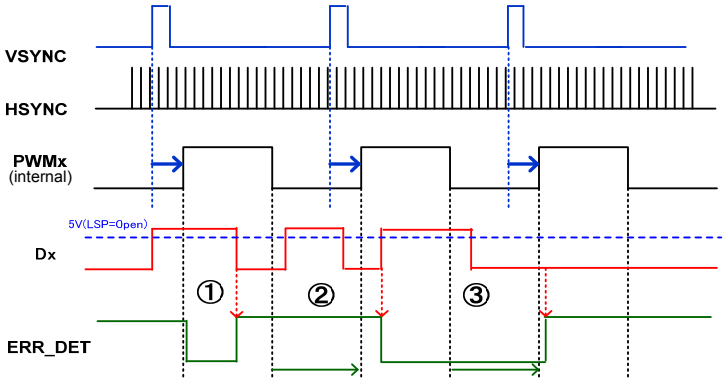


Figure 24. LED SHORT Protection

① When PWMx=HIGH, LED SHORT error is detected. ERR_DET=LOW is outputted.
If drain pin voltage is released, ERR_DET=HIGH is outputted.
② When PWMx=LOW, LED SHORT error is not detected.
③ When PWMx=HIGH, LED SHORT error is detected. When PWMx=LOW, even though the drain pin voltage is realeased, ERR_DET output is kept.

- **RESISTOR SHORT protection**
- **MOSFET SHORT protection**

When PWMx=HIGH, if the voltage of Source pin becomes lower than 0.15V(typ), ERR_DET = LOW is outputted and RES SHORT error will be detected, and this error state is realeased when the voltage of Sourse pin comes back to 0.15V(typ) or higher. The initial value of the detect threshold of RESSHORT and MOSSHORT are 0.15V. And those correspond to the register LEDREF.
When PWMx=LOW, if the voltage of Source pin becomes higher than 0.15V(typ), ERR_DET = LOW is outputted and RES SHORT error will be detected, and this error state is realeased when the voltage of Sourse pin comes back to 0.15V(typ) or lower.

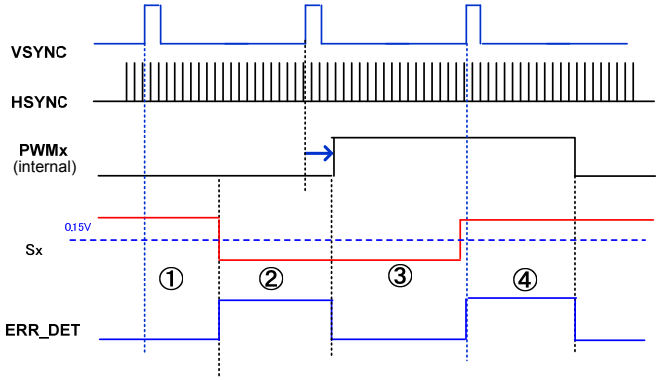


Figure 25. RESISTER SHORT Protection and MOSFET SHORT Protection

① When PWMx=LOW, If Source pin becomes 0.15V(typ) or more, MOS SHORT error is detected. ERR_DET=LOW is outputted.
② If source pin voltage is release condition, ERR_DET=HIGH is outputted.
③ When PWMx=HIGH, If Source pin becomes 0.15V(typ) or lower, RES SHORT error is detected. ERR_DET=LOW is outputted.
④ If source pin voltage is release condition, ERR_DET=HIGH is outputted.

Application of BD9271KUT

1. About the Feedback Between External LED Power Supply for DCDC Converter and COMP Pin

By connecting the COMP1,2 which are the error amplifier outputs of BD9271KUT to the feedback pins of DCDC converter (inv input), the state which the cathode voltages of LED bars are lower than the EAMP standard voltage (typ.0.6V) which is set by writing the registers is transmitted to DCDC side, and the DCDC voltage can be raised.

The error amplifier outputs of D1～D8, D9～D16 pins correspond the COMP1 pin and COMP2 pin respectively.

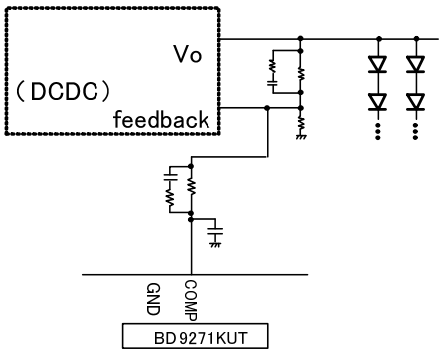


Figure 26. COMP Pin feedback

Due to the COMP1,2 pins of BD9271KUT are OPEN collector pins, basically the adjustment can be only allowed on the direction in which the DCDC output is raised. We suggest set the initial setting of the power supply of DCDC converter 10% lower than voltage at which the LEDs work normally.

In order to achieve a feedback which has good stability and efficiency to the LED power supply, we suggest insert the CR which practices the lead compensation to DCDC converter and the COMP output of BD9271KUT. The current-mode type DCDC converter is used more widely because it is easy to set the response speed and so on.

If it is hard to guarantee the stability of DCDC output, it may cause the heat of the external NMOS-FET. In this case, we suggest raise the initial value of the DCDC output, and increase the DCDC output capacity.

2. About the Clamp Circuit

In BD9271KUT, the absolute maximum voltage of D pin which is connected to the drain of external MOSFET is 40V. Due to it is necessary to raise the power supply voltage according to the VF of the used LED bar, the voltage of D pin maybe exceed the absolute maximum when PWM is LOW. In this case, in order to secure the absolute maximum voltage of the D pin, it is necessary to set up a clamp circuit at the drain side of the NMOSFET.

Zener Diode can be used as a solution for clamp circuit. We use the Diode of 36V (EDZ36B:ROHM) which has a lower Zener voltage than the absolute maximum voltage. About the LED, for example, in case of the LED which needs 3.5V for lighting, 2V cannot light it. For this, the method by using the Zener Diode is applicable when the LED supply voltage is under 80V.
When use this clamp circuit, please guarantee the absolute maximum voltage of NOMOS is lower than the absolute maximum voltage of the clamp circuit.

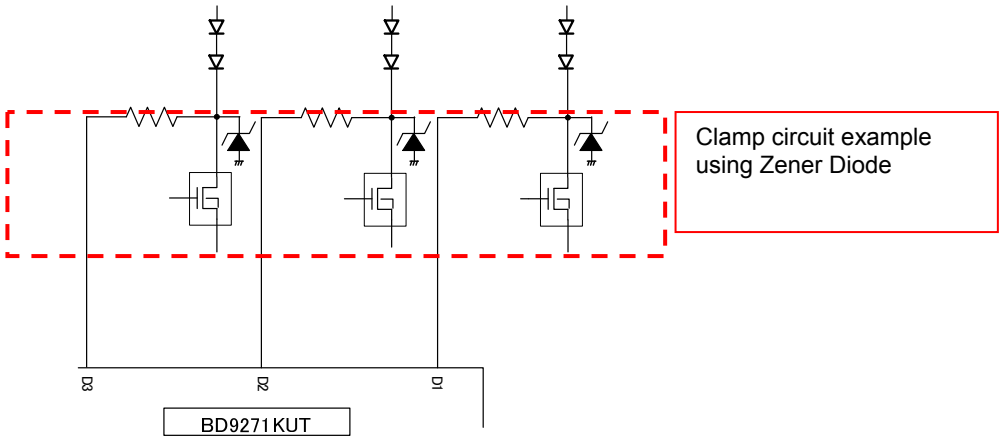


Figure 27. Clamp Circuit example using Zener Diode

When the LED supply voltage is over 80V, we can use the FET for clamp circuit. In this case, clamped power supply for FET gate voltage is necessary, for example, if VCC of BD9271KUT is 12V, it can be used.
In this case, the absolute maximum voltage is the clamp voltage.

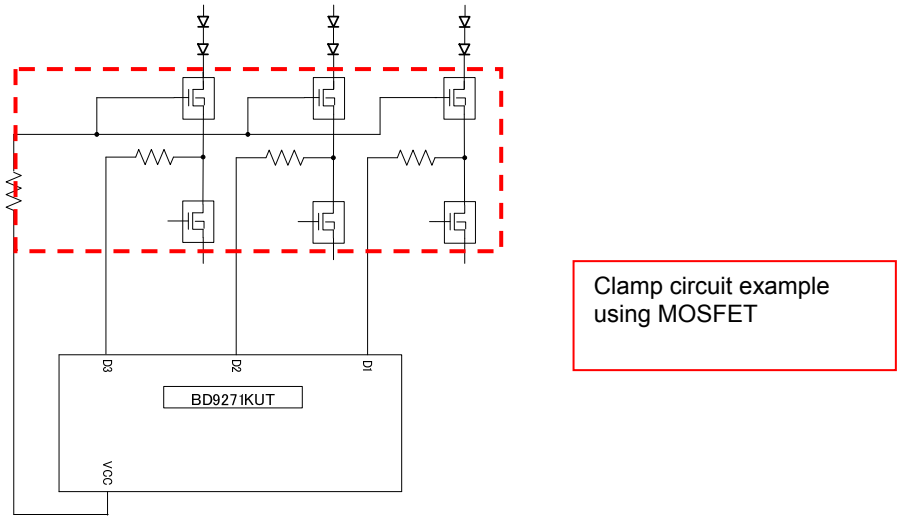


Figure 28. Clamp Circuit example using MOS FET

3. Example of Application Circuit (BD9271KUT + BD9286FV)

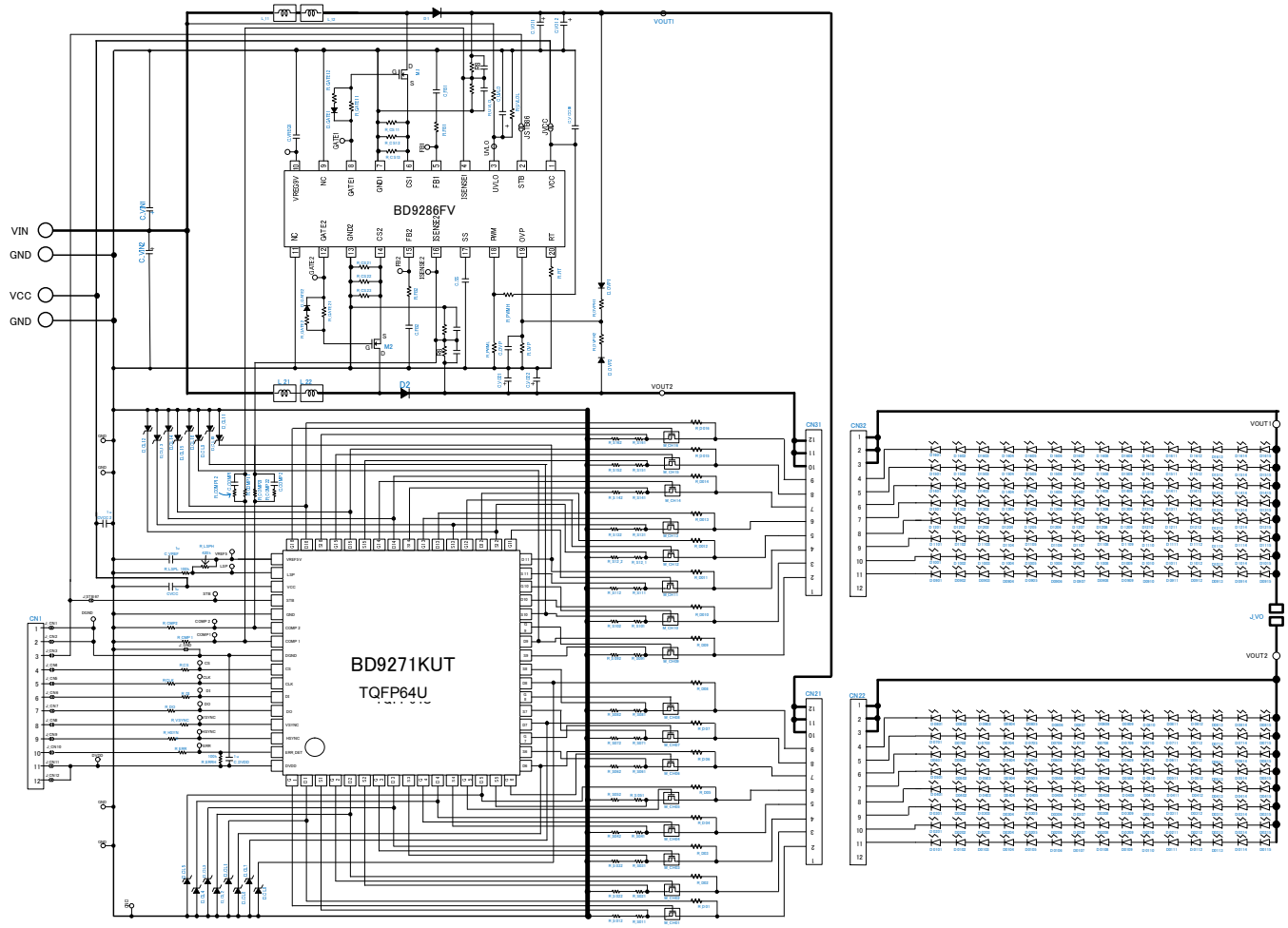


Figure 29. Application Circuit (BD9271KUT+BD9286FV)

4.Precautions in Application use

1.) This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings including the range of applied voltage or operation temperature. Failure status such as short-circuit mode or open mode can not be estimated. If a special mode beyond the absolute maximum ratings is estimated, physical safety countermeasures like fuse needs to be provided.

2.) The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.

3.) When this product is installed on a printed circuit board, attention needs to be paid to the orientation and position of IC. Wrong installation may cause damage to IC. Short circuit caused by problems like foreign particles entering between outputs or between an output and power GND also may cause damage.

4.) The pin connected a connector need to connect to the resistor for electrical surge destruction.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

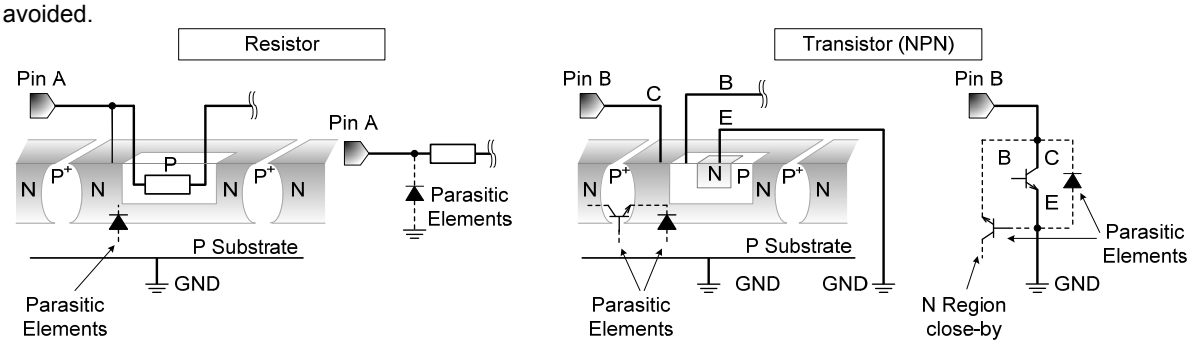


Figure 30. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

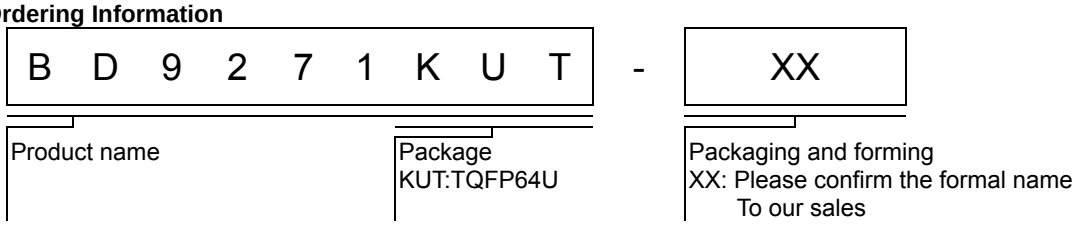
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

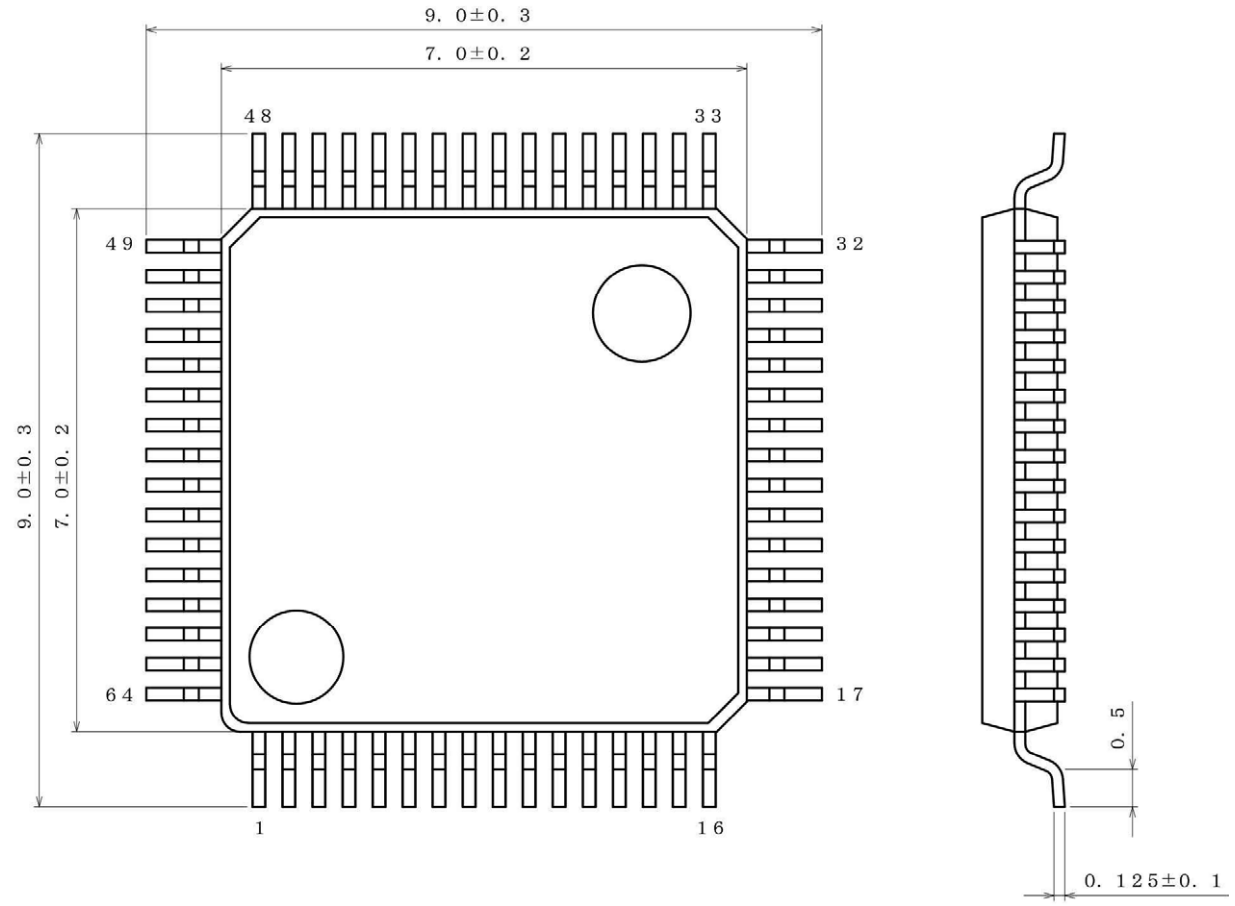
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

Ordering Information



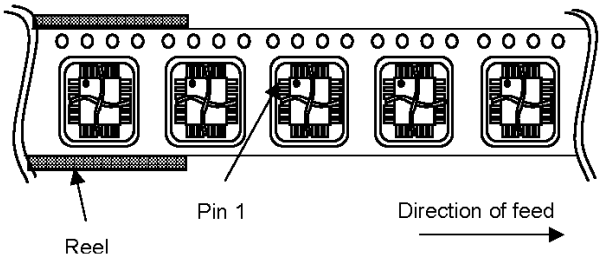
Physical Dimension Tape and Reel Information

Package Name	TQFP64U



< Tape and Reel Information >

Tape	Embossed carrier tape with dry pack
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
07.Jan.2013	001	New Release
22.Aug.2013	002	P13～19. Add comment about the update timing of the register
06.Mar.2014	003	P4. Comment correction about Pin54,55
		P9. Value correction about STB voltage
27.Feb.2015	004	P8, 25. Add comment that RESSHORT, MOSSHORT protection is corresponds to the register 02h, 03h.
		P12. Add about AC characteristics of HSYNC and VSYNC signals
		P13. The register updated timing is corrected.
		P18. Add comment about the mask interval SSMASKSET
		P20. Comment correction about the soft start register.
		P21. Update comment that ERROR control.
		P23. Add about Start-up sequence timing characteristics
21.Apr.2015	005	P12. As for HSYNC, VSYNC adding in Ver004, the comment for the HSYNC negative edge is deleted.
		P19. The state as DLY01[11:0]=000h is corrected.
22.Jul.2015	006	P1,P2,P29,P32 Change Package Name
		P33 Change Physical Dimension Tape and Reel Information
		P2 Add External Components Recommended Range

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.

BD9271KUT - Web Page

Distribution Inventory

Part Number	BD9271KUT
Package	TQFP64U
Unit Quantity	1500
Minimum Package Quantity	1500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes