

1 Channel High Side Switch IC

Current Limit High Side Switch IC

BD82048QVZ BD82049QVZ BD8205xQVZ Series

Description

BD820xxQVZ are Single Channel High Side Switch ICs employing N-channel power MOSFET with low On Resistance for the power supply line of universal serial bus (USB).

These ICs have a built-in over current detection circuit, thermal shutdown circuit, under voltage lockout and soft start circuit.

Features

- Over-Current Threshold
 - 1.15A(BD82048QVZ, BD82049QVZ)
 - > 1.65A(BD82050QVZ, BD82051QVZ)
 - 2.20A(BD82052QVZ, BD82053QVZ)
 - 2.80A(BD82054QVZ, BD82055QVZ)
- Control Input Logic
 - Active-High (BD82048QVZ, BD82050QVZ, BD82052QVZ, BD82054QVZ)
 - Active-Low (BD82049QVZ, BD82051QVZ, BD82053QVZ, BD82055QVZ)
- Output Discharge Function
- Reverse Current Protection when Power Switch Off
- Thermal Shutdown
- Open-Drain Fault Flag Output
- Under-Voltage Lockout
- OCD Fast Response
- Soft-Start Circuit

Applications

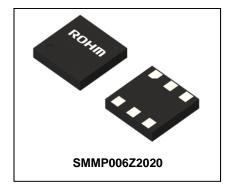
USB hub in consumer appliances, PC, PC peripheral equipment, etc.

Key Specifications

2.7V to 5.5V
63mΩ(Typ)
VZ: 1.15A(Typ)
VZ: 1.65A(Typ)
VZ: 2.20A(Typ)
VZ: 2.80A(Typ)
0.01µA(Typ)
ange: -40°C to +85°C
)

Package SMMP006Z2020

 $W(Typ) \times D(Typ) \times H(Max)$ 2.00mm \times 2.00mm \times 0.40mm



Typical Application Circuit

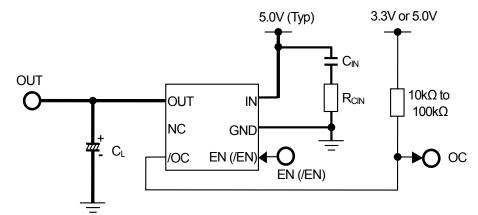


Figure 1. Typical Application Circuit

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Block Diagram

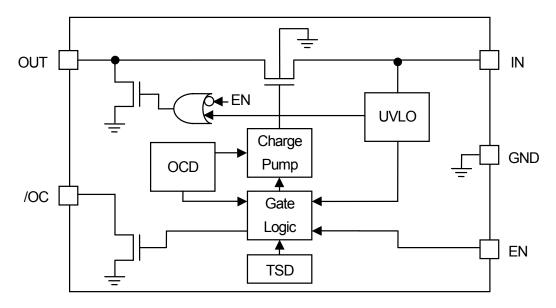


Figure 2. Block Diagram (BD82048QVZ, BD82050QVZ, BD82052QVZ, BD82054QVZ)

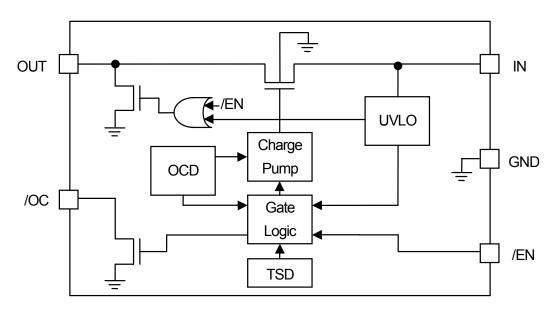
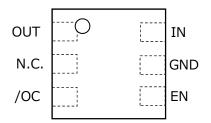


Figure 3. Block Diagram (BD82049QVZ, BD82051QVZ,BD82053QVZ, BD82055QVZ)

Pin Configuration



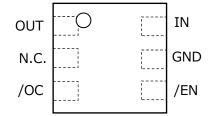


Figure 4. Pin Configuration (TOP VIEW) (BD82048QVZ, BD82050QVZ, BD82052QVZ, BD82054QVZ)

Figure 5. Pin Configuration (TOP VIEW) (BD82049QVZ, BD82051QVZ, BD82053QVZ, BD82055QVZ)

Pin Descriptions

Pin No.	Symbol	I/O	Function
1	OUT	0	Power switch output
2	N.C.	-	No Connection ^(Note 1)
3	/OC	0	Error flag output Low when over-current or thermal shutdown is activated Open drain output
4	EN, /EN	I	Enable input EN: High-level input turns on the switch /EN: Low-level input turns on the switch High level input > 2.0V, Low level input < 0.8V
5	GND	-	Ground
6	IN	I	Power supply input Input pin to the power switch and power supply input pin of the internal circuit

(Note 1) N.C. Pin is recommended to be shorted to GND. However, it can also be left open since it isn't internally connected to the IC.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
IN Supply Voltage	V _{IN}	-0.3 to +6.0	V
EN (/EN) Input Voltage	V _{EN} , V _{/EN}	-0.3 to +6.0	V
/OC Voltage	V _{/OC}	-0.3 to +6.0	V
/OC Sink Current	I _{/OC}	5	mA
OUT Voltage	V _{OUT}	-0.3 to +6.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

Deverator	Cumbal	Thermal Re	I Imit	
Parameter	Symbol	1s ^(Note 3)	2s2p ^(Note 4)	- Unit
SMMP006Z2020				
Junction to Ambient	θ_{JA}	380.2	196.0	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	126	93	°C/W

(Note 1) Based on JESD51-2A(Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt
Тор		
Copper Pattern	Thickness	
Footprints and Traces	70µm	

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Тор		2 Internal Laye	ers	Bottom		
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness	
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm	

Recommended Operating Conditions

Parameter	Symbol		Unit		
Farameter	Symbol	Min	Тур	Max	Offic
IN Operating Voltage	V _{IN}	2.7	5.0	5.5	V
Operating Temperature	Topr	-40	-	+85	°C

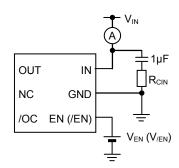
Electrical Characteristics (V_{IN} = 5V, Ta= 25°C, unless otherwise specified.) DC Characteristics

Dar	rameter	Symbol		Limit		Unit	Conditions
Parameter		Symbol	Min	Тур	Max	Offic	Conditions
Operating Curre	nt	I _{DD}	-	110	150	μΑ	V_{EN} =5V, V_{OUT} =Open (Active-High) $V_{/EN}$ =0V, V_{OUT} =Open (Active-Low)
Standby Current		I _{STB}	-	0.01	5	μА	V_{EN} =0V, V_{OUT} =Open (Active-High) V_{JEN} =5V, V_{OUT} =Open (Active-Low)
EN lancet Valtage		V _{ENH} , V _{/ENH}	2.0	-	ı	V	High input
EN Input Voltage	2	V _{ENL} , V _{/ENL}	-	-	0.8	V	Low input
EN Input Leakaç	је	I _{EN} , I _{/EN}	-1	+0.01	+1	μA	V _{EN} , V _{/EN} =0V or 5V
On Resistance		Ron	-	63	80	mΩ	I _{OUT} =0.5A
Reverse Leak C	urrent	I _{REV}	-	-	1	μA	V _{OUT} =5.5V, V _{IN} =0V
	BD82048QVZ BD82049QVZ	Ітн	0.86	1.15	1.44	Α	
Over-Current	BD82050QVZ BD82051QVZ		1.24	1.65	2.06	А	Current Load Slew rate
Threshold	BD82052QVZ BD82053QVZ		1.65	2.20	2.75	Α	100A/s
	BD82054QVZ BD82055QVZ		2.10	2.80	3.50	Α	
	BD82048QVZ BD82049QVZ		0.45	0.75	1.05	Α	
Short Circuit	BD82050QVZ BD82051QVZ		0.66	1.10	1.54	Α	V _{OUT} =0V, C _L =100μF
Output Current	BD82052QVZ BD82053QVZ	- I _{SC}	0.90	1.50	2.10	А	RMS
	BD82054QVZ BD82055QVZ		1.20	2.00	2.80	А	
Output Discharge Resistance		R _{DISC}	-	55	100	Ω	I _{OUT} =1mA, V _{EN} =0V (Active-High) I _{OUT} =1mA, V _{/EN} =5V (Active-Low)
/OC Output Low Voltage		V _{/OC}	-	-	0.4	V	I _{/OC} =1mA
/OC Output Leal	Current	IL _{/OC}	-	0.01	1	μA	V _{/OC} =5V
LN/LO The state of	1	V _{TUVH}	2.1	2.3	2.5	V	V _{IN} increasing
UVLO Threshold	1	V_{TUVL}	2.0	2.2	2.4	V	V _{IN} decreasing

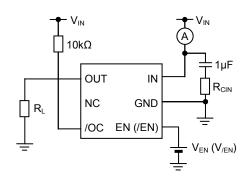
AC Characteristics

Demonstra	0	Limit			1.1:4	0 170
Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Output Rise Time	t _{ON1}	-	0.5	10	ms	
Output Turn-on Time	t _{ON2}	-	0.6	20	ms	D =100
Output Fall Time	t _{OFF1}	-	2	10	μs	$R_L=10\Omega$
Output Turn-off Time	t _{OFF2}	-	4	20	μs	
/OC Delay Time	t _{/OC}	4	7	15	ms	

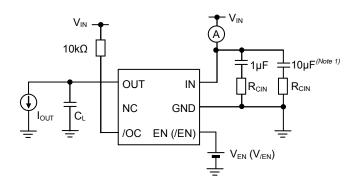
Measurement Circuit



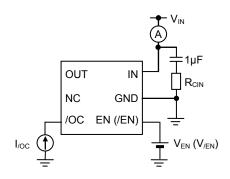
Operating Current, Standby Current



EN Input Voltage, Output Rise/Fall Time



On Resistance, Over-Current Protection (Note 1) Use capacitance of 10µF or more at output short test by using external supply.



/OC Output Low Voltage

Figure 6. Measurement Circuit

Timing Diagram

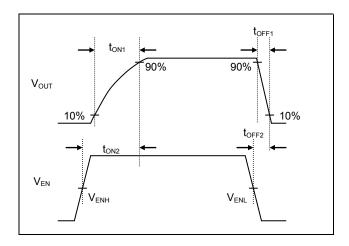


Figure 7. Output Rise/Fall Time (Active-High)

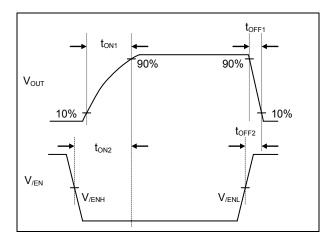


Figure 8. Output Rise/Fall Time (Active-Low)

Typical Performance Curves

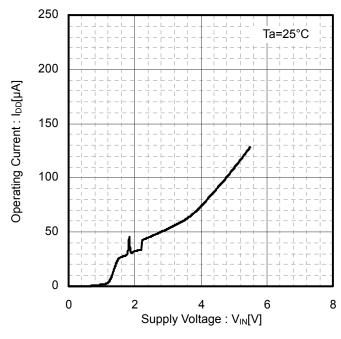


Figure 9. Operating Current vs Supply Voltage (EN Enable)

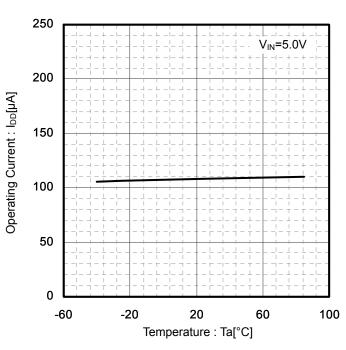


Figure 10. Operating Current vs Temperature (EN Enable)

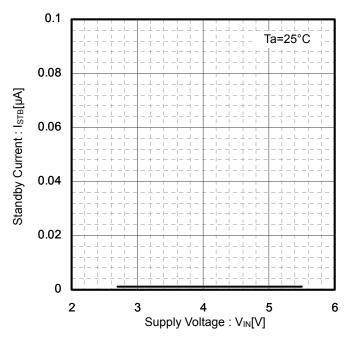


Figure 11. Standby Current vs Supply Voltage (EN Disable)

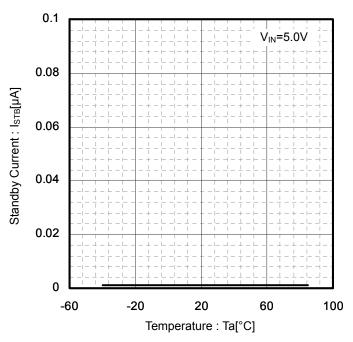


Figure 12. Standby Current vs Temperature (EN Disable)

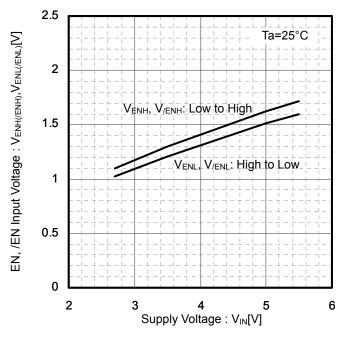


Figure 13. EN, /EN Input Voltage vs Supply Voltage

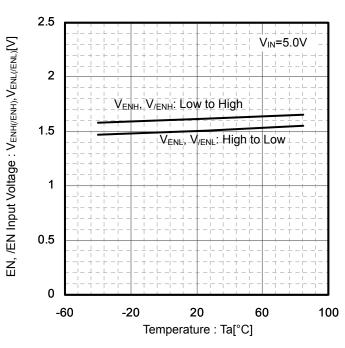


Figure 14. EN, /EN Input Voltage vs Temperature

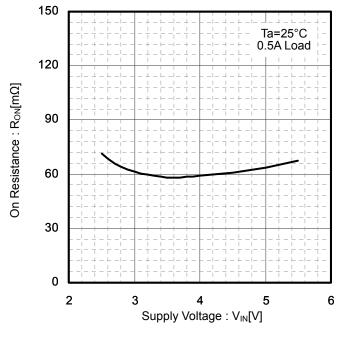


Figure 15. On Resistance vs Supply Voltage

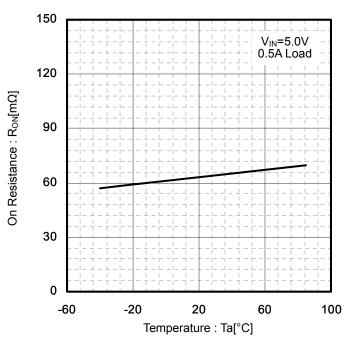


Figure 16. On Resistance vs Temperature

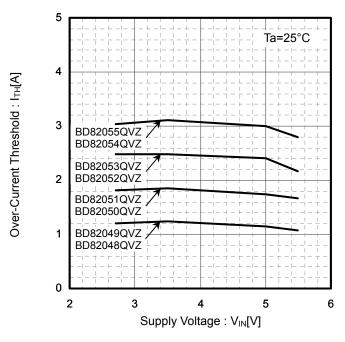


Figure 17. Over-Current Threshold vs Supply Voltage

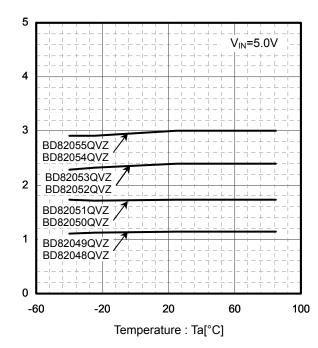


Figure 18. Over-Current Threshold vs Temperature

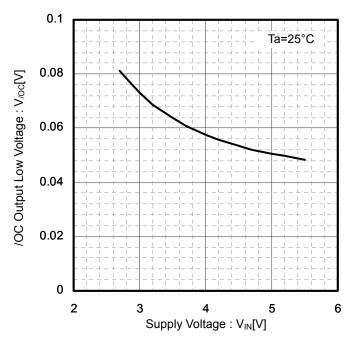


Figure 19. /OC Output Low Voltage vs Supply Voltage

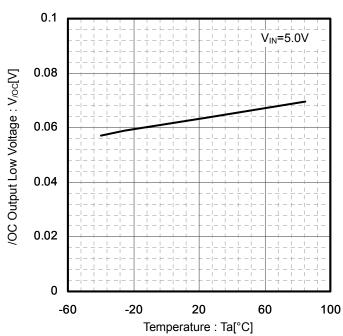


Figure 20. /OC Output Low Voltage vs Temperature

Over-Current Threshold: ITH[A]

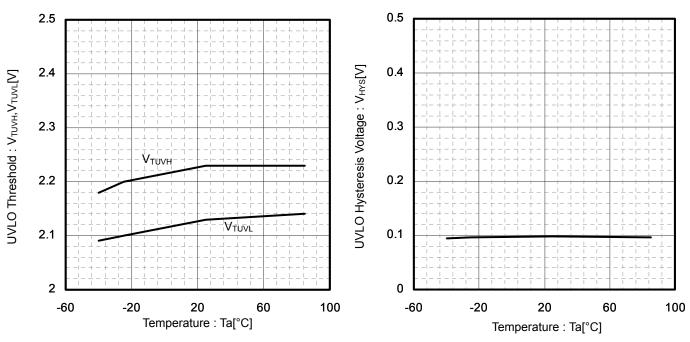


Figure 21. UVLO Threshold vs Temperature

Figure 22. UVLO Hysteresis Voltage vs Temperature

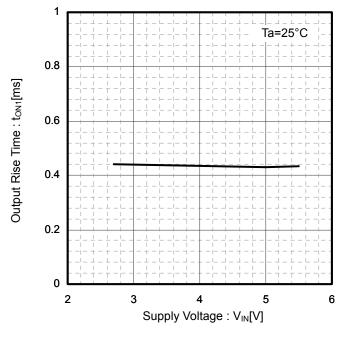


Figure 23. Output Rise Time vs Supply Voltage

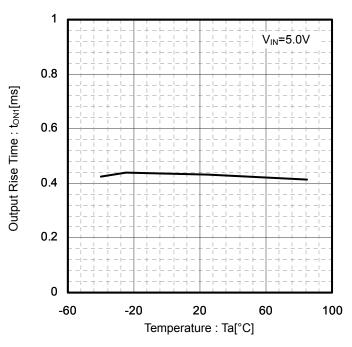


Figure 24. Output Rise Time vs Temperature

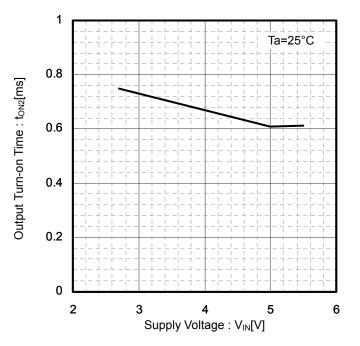


Figure 25. Output Turn-on Time vs Supply Voltage

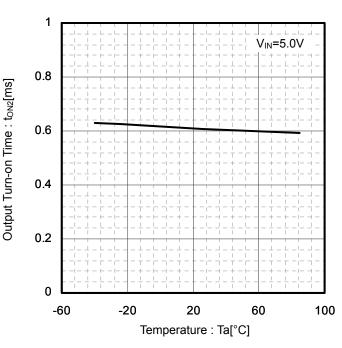


Figure 26. Output Turn-on Time vs Temperature

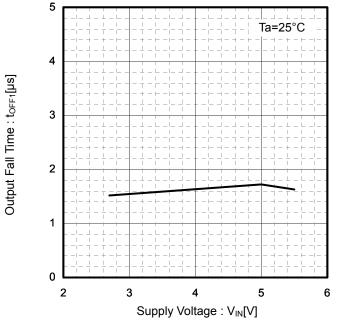


Figure 27. Output Fall Time vs Supply Voltage

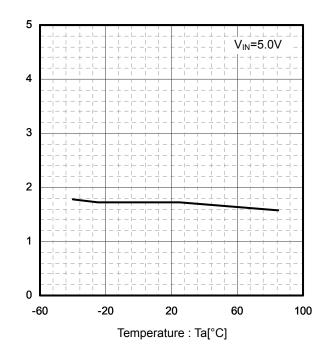


Figure 28. Output Fall Time vs Temperature

Output Fall Time : toff[µs]

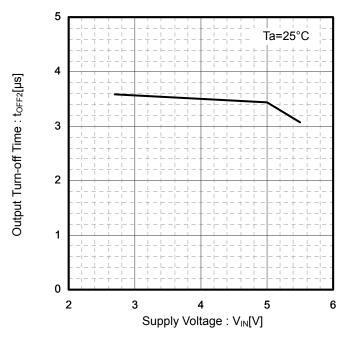


Figure 29. Output Turn-off Time vs Supply Voltage

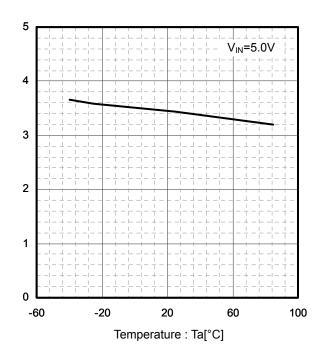


Figure 30. Output Turn-off Time vs Temperature

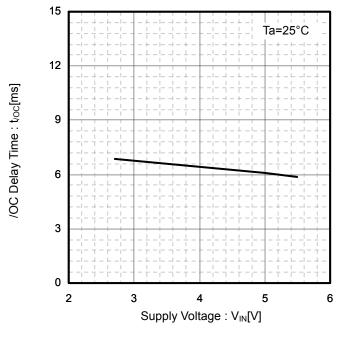


Figure 31. /OC Delay Time vs Supply Voltage

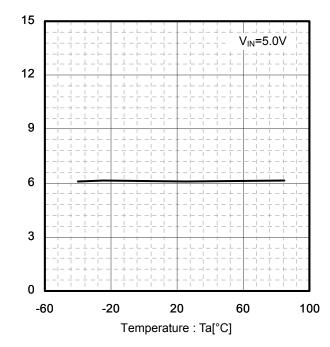


Figure 32. /OC Delay Time vs Temperature

Output Turn-off Time: toff[µs]

'OC Delay Time : t_{/oc}[ms]

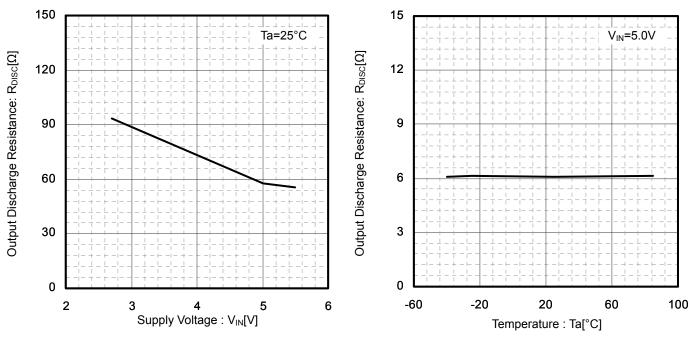
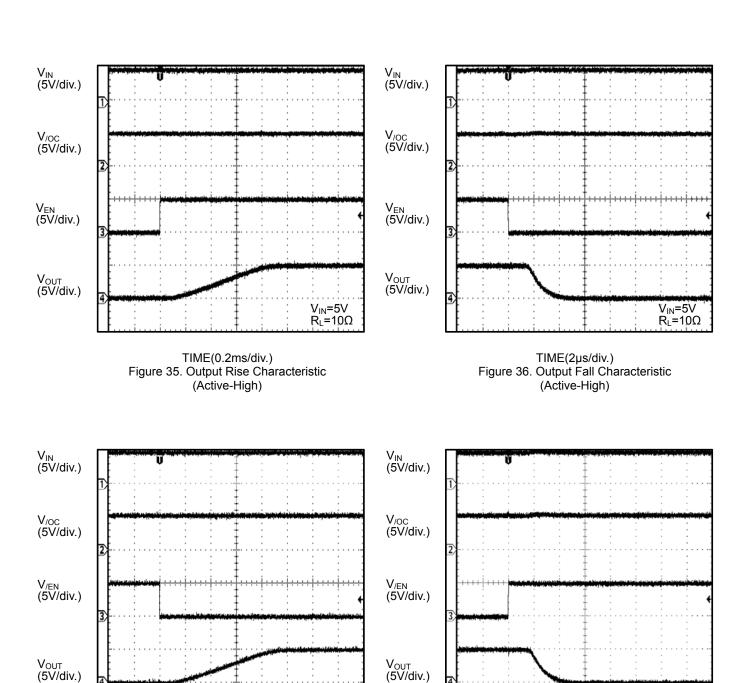


Figure 33. Output Discharge Resistance vs Supply Voltage

Figure 34. Output Discharge Resistance vs Temperature

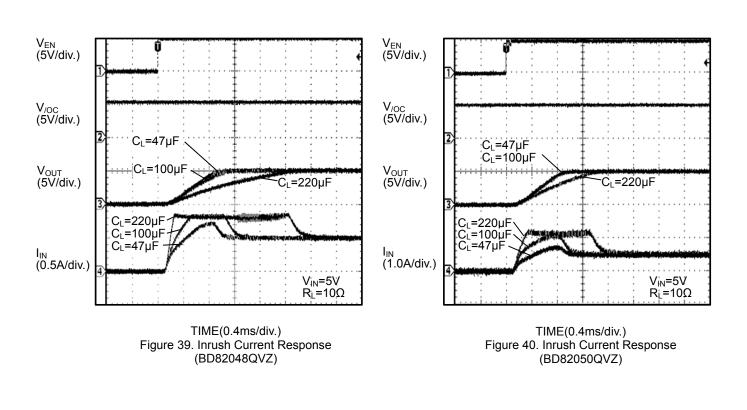


TIME(0.2ms/div.)
Figure 37. Output Rise Characteristic (Active-Low)

TIME(2µs/div.)
Figure 38. Output Fall Characteristic (Active-Low)

V_{IN}=5V R_L=10Ω

 V_{IN} =5V R_L =10 Ω



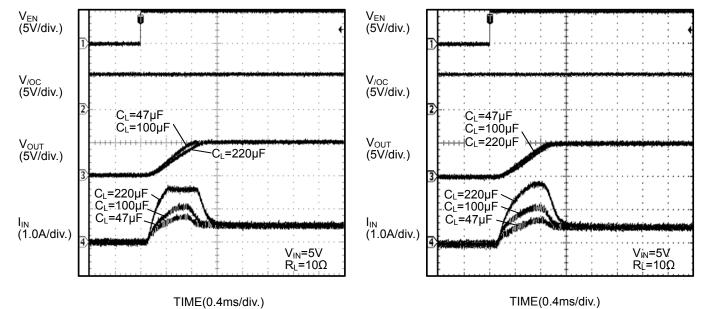
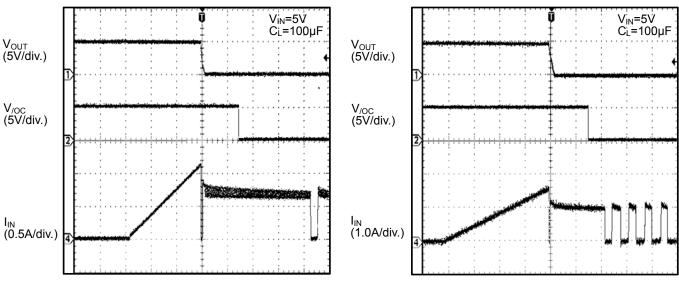


Figure 41. Inrush Current Response

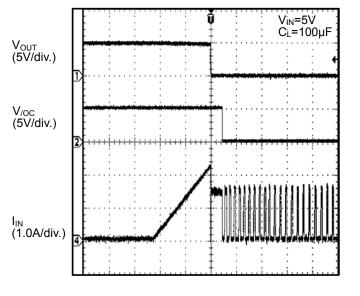
(BD82052QVZ)

Figure 42. Inrush Current Response (BD82054QVZ)

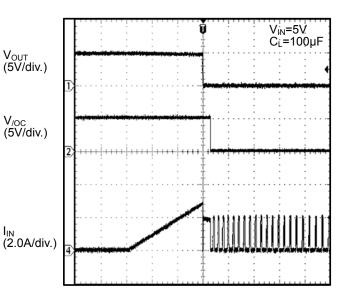


TIME(4ms/div.)
Figure 43. Over-Current Response Ramped Load
(BD82048QVZ)

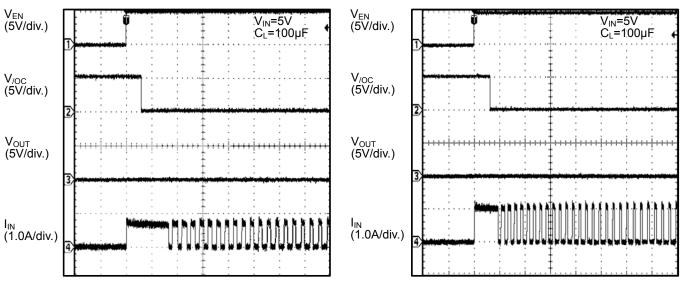
TIME(4ms/div.)
Figure 44. Over-Current Response Ramped Load
(BD82050QVZ)



TIME(10ms/div.)
Figure 45. Over-Current Response Ramped Load
(BD82052QVZ)

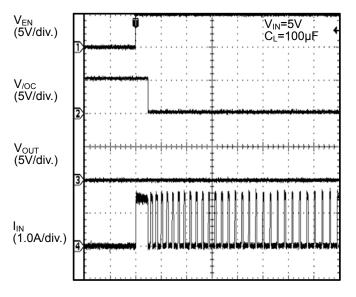


TIME(10ms/div.)
Figure 46. Over-Current Response Ramped Load
(BD82054QVZ)

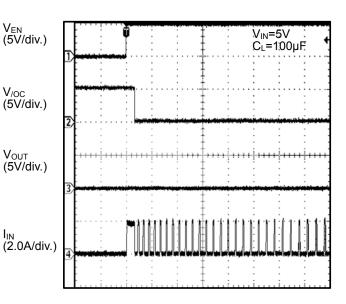


TIME(10ms/div.)
Figure 47. Over-Current Response
Enable during Short Circuit
(BD82048QVZ)

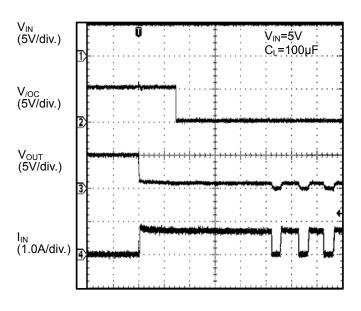
TIME(10ms/div.)
Figure 48. Over-Current Response
Enable during Short Circuit
(BD82050QVZ)



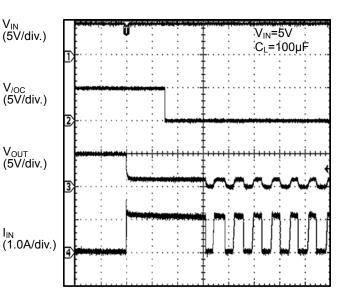
TIME(10ms/div.)
Figure 49. Over-Current Response
Enable during Short Circuit
(BD82052QVZ)



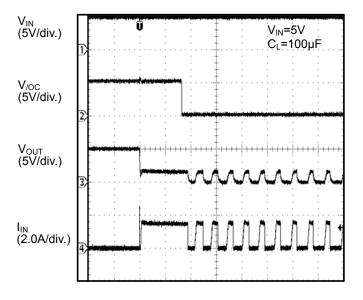
TIME(0.4ms/div.)
Figure 50. Over-Current Response
Enable during Short Circuit
(BD82054QVZ)



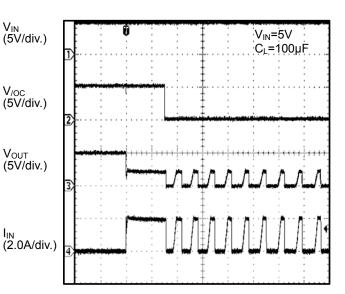
TIME(4ms/div.)
Figure 51. Over-Current Response
1Ω Load connected between VOUT and GND
(BD82048QVZ)



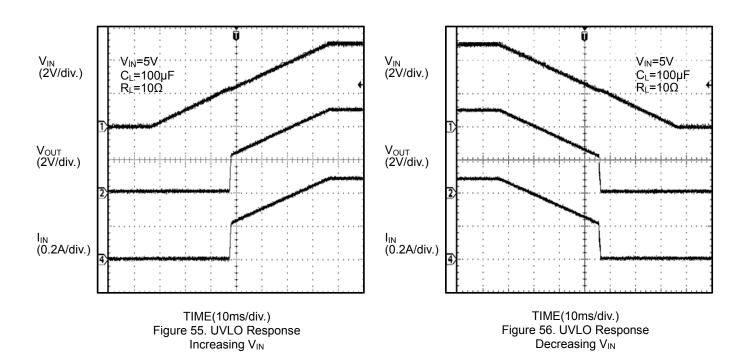
TIME(4ms/div.)
Figure 52. Over-Current Response
1Ω Load connected between VOUT and GND
(BD82050QVZ)



 $TIME (4ms/div.) \\ Figure 53. Over-Current Response \\ 1\Omega Load connected between VOUT and GND \\ (BD82052QVZ)$



TIME(4ms/div.)
Figure 54. Over-Current Response
1Ω Load connected between VOUT and GND
(BD82054QVZ)



Typical Application Circuit

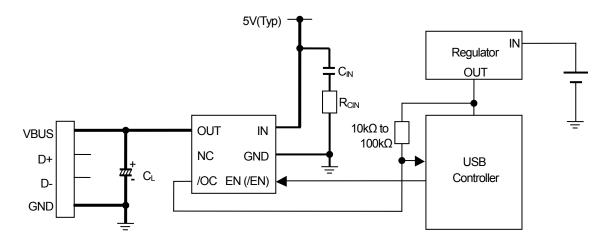


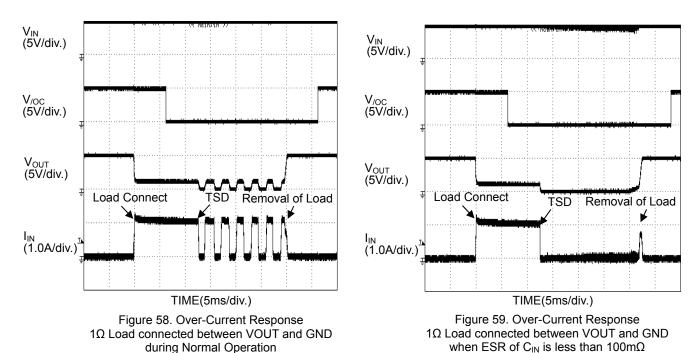
Figure 57. Typical Application Circuit

Application Information

The IN pin is used as the input of the switch and the power supply for the internal circuit of the IC. Therefore, there is a possibility that IC operation may be adversely affected by power line noise. This can be prevented by connecting a $1\mu F$ or higher bypass capacitor C_{IN} between the IN pin of the IC and the GND pin.

Additionally, when an excessive electric current flows during output short, the characteristic response of the IC could be influenced by noise due to inductance of power supply line. To decrease this effect, it is recommended to connect a $10\mu F$ to $100\mu F$ capacitor in parallel with CIN.

However, please use a capacitor connect to power line with ESR of at least $100m\Omega$ but less than 2Ω . If C_{IN} ESR is low, when overcurrent is detected, the current limit function may not be produced after TSD occurs as shown in Figure 59. To return from this state, the load should be disconnected or by resetting IN or EN.



Pull up /OC output via resistance value of $10k\Omega$ to $100k\Omega$.

Set up a value for C_L which satisfies the application, and should be connected near OUT pin.

When using the circuit with changes to the external circuit values, make sure to leave an adequate margin for external components including static and transitional characteristics as well as the design tolerances of the IC.

Functional Description

1. Switch Operation

IN pin and OUT pin are connected to the drain and the source of switch MOSFET respectively. The IN pin is also used as power source input to internal control circuit.

When the switch is turned on from EN control input, the IN pin and OUT pin are connected by a $63m\Omega(Typ)$ switch. In ON status, the switch is bidirectional. Therefore, when the potential of OUT pin is higher than that of the IN pin, current flows from OUT pin to IN pin.

Since the parasitic diode between the drain and the source of switch MOSFET is canceled, current flow from OUT to IN is prevented during off state (EN, /EN signal is disable). In addition, when the switch is off, an output electric discharge function is activated.

2. Thermal Shutdown Circuit (TSD)

If over current would continue, the temperature of the IC would increase drastically due to internal losses. If the junction temperature reaches beyond 135°C(Typ) during the condition of over-current detection, thermal shutdown circuit operates and turns power switch off and outputs error flag (/OC). Then, when the junction temperature decreases below 115°C(Typ), power switch is turned on and error flag (/OC) is cancelled. Unless the cause of the increase of the chip's temperature is removed or the output of power switch is turned off, this operation repeats.

The thermal shutdown circuit operates when the switch is on (EN, /EN signal is active).

3. Over Current Detection (OCD)

The over current detection circuit (OCD) limits current (I_{SC}) and outputs error flag (/OC) when current flowing in each switch MOSFET exceeds a specified value. There are three cases when the OCD circuit is activated. The OCD operates when the switch is on (EN, /EN signal is active).

- (1) When the switch is turned on while the output is in short-circuit status, the switch gets in current limit status immediately
- (2) When the output short-circuits or when high current load is connected while the switch is on, very large current will flow until the over-current limit circuit reacts. When this happens, the over-current limit circuit is activated and the current limitation is carried out.
- (3) When the output current increases gradually, current limitation does not work until the output current exceeds the over-current detection value. When it exceeds the detection value, current limitation is carried out.

4. Under-Voltage Lockout (UVLO)

UVLO circuit prevents the switch from turning on until V_{IN} exceeds 2.3V(Typ). If V_{IN} drops below 2.2V(Typ) while the switch is still on, then the UVLO will shut off the power switch. UVLO has a hysteresis of 100mV(Typ). Under-voltage lockout circuit works when EN, /EN signal is active. During UVLO operation and EN, /EN is active, output electric discharge function is activated.

5. Error Flag (/OC) Output

Error flag output is an N-channel MOSFET open drain output. Upon detection of over current or thermal overrun, the output level becomes low.

Over current detection has a delay filter. This delay filter prevents current detection flags from being sent during instantaneous events such as surge current due to switching or hot plug. If fault flag output is unused, /OC pin should be connected to open or ground line.

Functional Description - continued

6. Output Discharge Function

When the switch is turned off by disabling control input or when UVLO function is triggered, the $55\Omega(Typ)$ discharge circuit between OUT and GND turns on which quickly discharges the electric charge of the capacitive load. However, if the voltage of IN declines rapidly, then the OUT pin becomes Hi-Z without UVLO function.

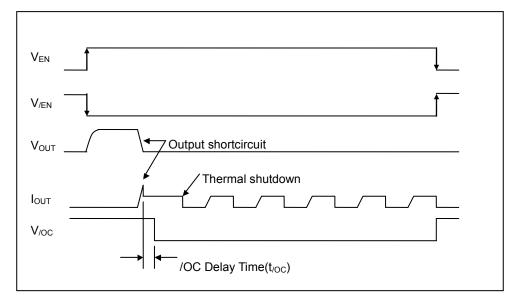


Figure 60. Over-Current Detection, Thermal Shutdown Timing.

I/O Equivalent Circuit

' !	<u>Equivalent Circ</u>	uit	
	Symbol	Pin No.	Equivalent Circuit
	OUT	1	IN OUT
	/OC	3	JOC JOC
•	EN, /EN	4	EN, /EN

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

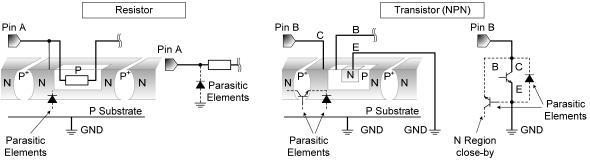


Figure 61. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit(TSD)

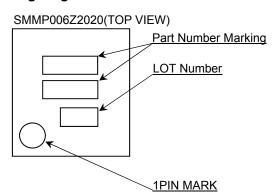
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

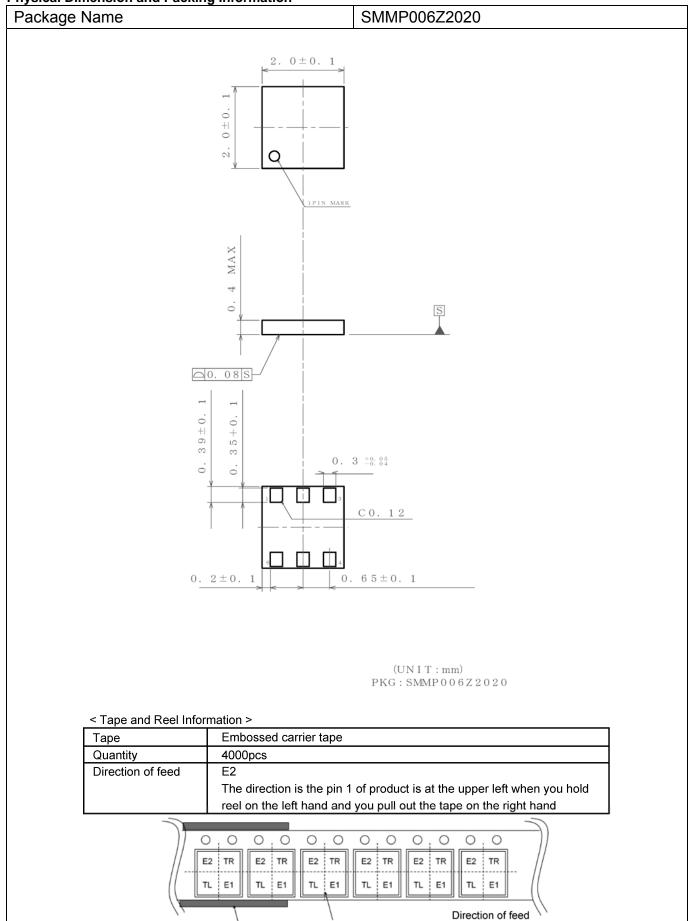


Marking Diagram



Over-Current Threshold(Typ)	Control Input Logic	Part Number Marking	Orderable Part Number
1.15A	Active-High	D82048	BD82048QVZ-E2
	Active-Low	D82049	BD82049QVZ-E2
1.65A	Active-High	D82050	BD82050QVZ-E2
	Active-Low	D82051	BD82051QVZ-E2
2.20A	Active-High	D82052	BD82052QVZ-E2
	Active-Low	D82053	BD82053QVZ-E2
2.80A	Active-High	D82054	BD82054QVZ-E2
	Active-Low	D82055	BD82055QVZ-E2

Physical Dimension and Packing Information



Pocket Quadrants

Reel

Revision History

Date	Revision	Changes
22.Sep.2017	001	New Release
25.Dec.2017	002	Addition of the series model information

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JÁPAN	USA	EU	CHINA
CLASSⅢ	CLASSIII	CLASS II b	CLASSIII
CLASSIV		CLASSⅢ	

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 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
 may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is
 exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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