

4ch White LED Driver with Buck-Boost and Built-in FET (32 LED Maximum)

BD81A04AMUV-M BD81A04AEFV-M

General Description

BD81A04AMUV-M/EFV-M is a white LED driver with the capability of withstanding high input voltage (40V Max). This driver has 4ch constant-current drivers integrated in 1-chip, where each channel can draw up to 120mA (Max), which is also suitable for high illumination LED drive. Furthermore, a buck-boost current mode DC/DC controller is also integrated to achieve stable operation during power voltage fluctuation. Light modulation (dimming function) is possible by PWM input. The Nch MOSFET for power surge is also integrated in the chip, thereby saving spaces of board sets.

Features

- Integrated Buck-Boost current mode DC/DC controller
- Integrated 4ch current driver for LED drive
- PWM light modulation (Dimming)-supported
- External switching frequency synchronization
- Built-In protection function (UVLO, OVP, OCP, SCP)
- LED abnormality detection function (Open/Short)
- Integrated V_{OUT} discharge function (Buck-Boost structure limitation)
- AEC-Q100 Qualified

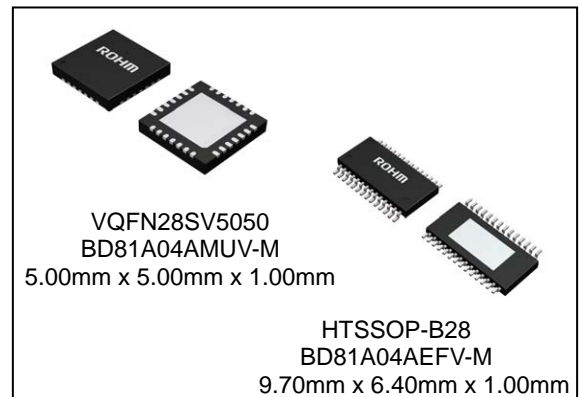
Application

Audio Display, Small and Medium type LCD Panels for Automotive use.

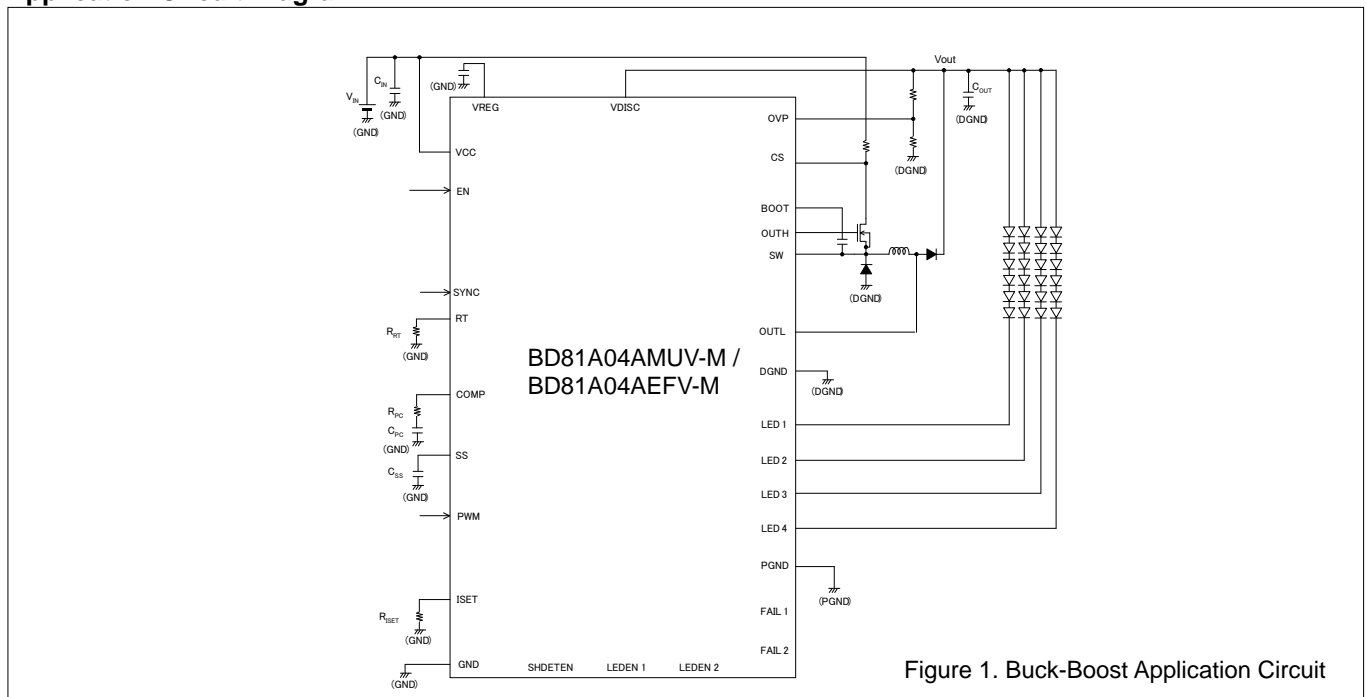
Key Specifications

Operating Input Voltage Range	4.5 to 35 V
Output LED Current Accuracy	$\pm 3.0\%$ @50mA
DC/DC Oscillation Frequency	200 to 2200kHz
Operating Temperature Range	-40 to +125°C
LED Maximum Output Current	120mA/ch

Package

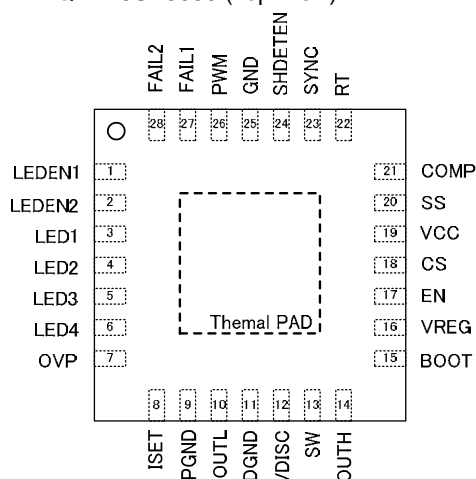
W(Typ) x D(Typ) x H(Max)


Application Circuit Diagram



Pin Configuration

VQFN28SV5050 (Top View)



HTSSOP-B28 (Top View)

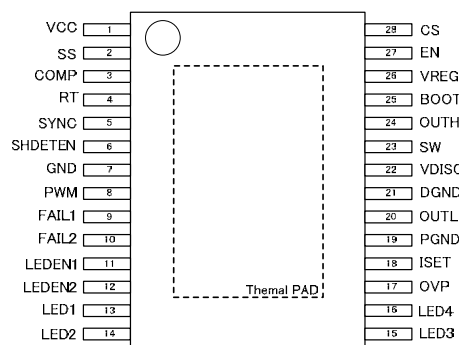


Figure 2. Pin Placement

Pin Description

VQFN28 SV5050	HTSSOP -B28	Terminal Pin Name	Function
1	11	LEDEN1	LED output pin enable terminal 1
2	12	LEDEN2	LED output pin enable terminal 2
3	13	LED1	LED output terminal 1
4	14	LED2	LED output terminal 2
5	15	LED3	LED output terminal 3
6	16	LED4	LED output terminal 4
7	17	OVP	Over-voltage detection terminal
8	18	ISET	LED output current setting terminal
9	19	PGND	LED output GND terminal
10	20	OUTL	Low side FET drain terminal
11	21	DGND	DC/DC output GND terminal
12	22	VDISC	Output voltage discharge terminal
13	23	SW	High side FET source terminal
14	24	OUTH	High side FET gate terminal
15	25	BOOT	High side FET driver power supply terminal
16	26	VREG	Internal constant voltage
17	27	EN	Enable terminal
18	28	CS	DC/DC current sense terminal
19	1	VCC	Input power supply terminal
20	2	SS	"Soft Start" Capacitor connection
21	3	COMP	ERR AMP output
22	4	RT	Oscillation Frequency-setting resistance input
23	5	SYNC	External synchronization signal input terminal
24	6	SHDETEN	Short detection enable signal
25	7	GND	Small signal GND terminal
26	8	PWM	PWM light modulation input terminal
27	9	FAIL1	"Failure" signal output terminal
28	10	FAIL2	LED open/short detection output signal
-	-	Thermal PAD	Back side thermal PAD (Please connect to GND)

Block Diagram

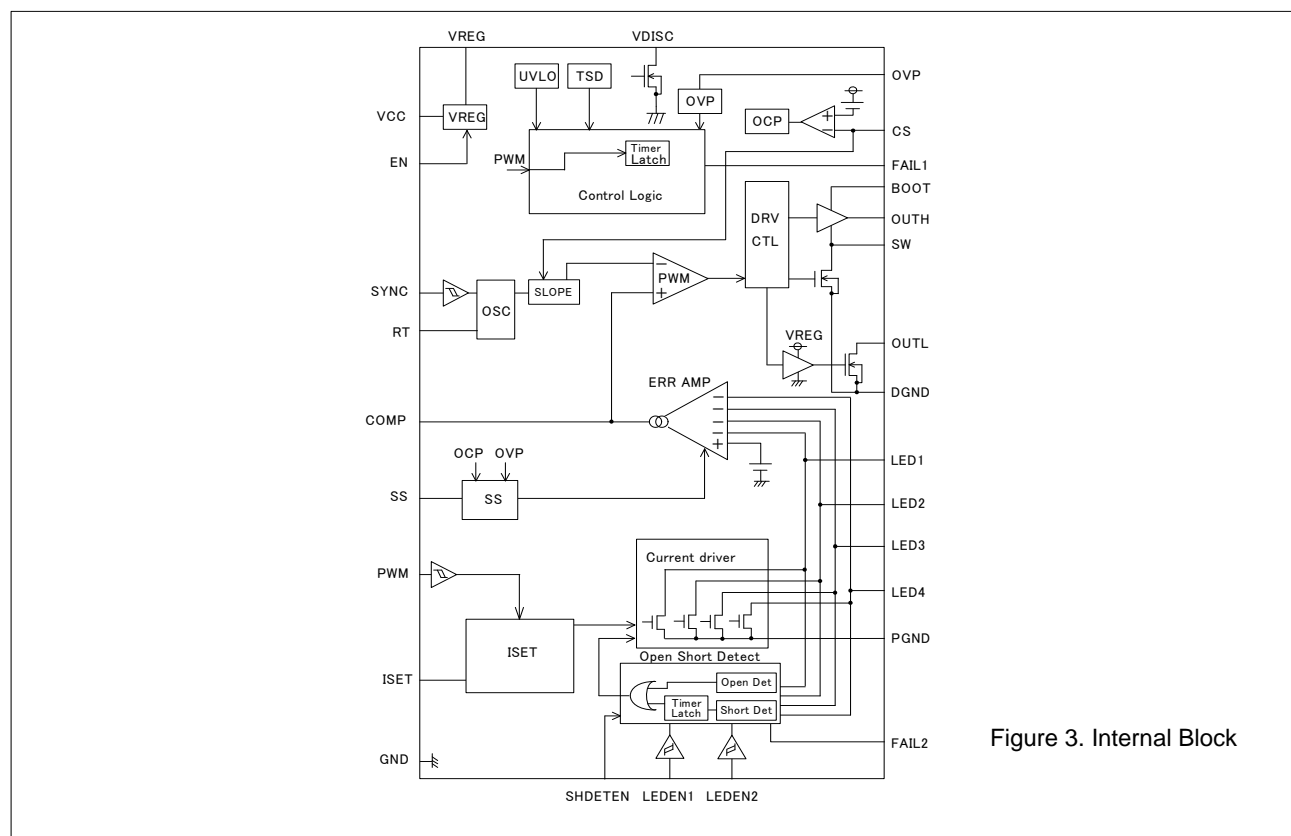


Figure 3. Internal Block

Absolute Maximum Ratings (Ta=25°C)

Item	Code	Rating	Unit
Power Supply Voltage	V _{CC}	40	V
BOOT, OUTH Pin Voltage	V _{BOOT} , V _{OUTH}	45	V
SW, CS, OUTL Pin Voltage	V _{SW} , V _{CS} , V _{OUTL}	40	V
BOOT-SW Pin Voltage	V _{BOOT-SW}	7	V
LED1 to 4, VDISC Pin Voltage	V _{LED1,2,3,4} , V _{VDISC}	40	V
VREG, OVP, FAIL1, FAIL2, LEDEN1, LEDEN2, ISET, PWM, SS, COMP, RT, SYNC, EN, SHDETEN Pin Voltage	V _{VREG} , V _{OVP} , V _{FAIL1} , V _{FAIL2} , V _{LEDEN1} , V _{LEDEN2} , V _{ISET} , V _{PWM} , V _{SS} , V _{COMP} , V _{RT} , V _{SYNC} , V _{EN} , V _{SHDETEN}	-0.3 to +7 < V _{CC}	V
Power Dissipation (VQFN28SV5050)	Pd(MUV)	4.56 (Note 1)	W
Power Dissipation (HTSSOP-B28)	Pd(EFV)	4.70 (Note 2)	W
Operating Temp Range	Topr	-40 to +125	°C
Storage Temp Range	Tstg	-55 to +150	°C
LED Maximum Output Current	I _{LED}	120 (Note 3)	mA
Junction Temperature	Tjmax	150	°C

Note 1 Mounted on a 4-layer 70mm×70mm×1.6mm glass epoxy PCB and gold foil area 70mm×70mm. Decrease by 36.5mW/°C for Ta above 25°C.

Note 2 Mounted on a 4-layer 70mm×70mm×1.6mm glass epoxy PCB and all layers heat radiation gold foil 5505mm². Decrease by 37.6mW/°C for Ta above 25°C.

Note 3 Current level/ch

Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings

Recommended Operating Conditions (Ta=25°C)

Item	Code	Rating	Unit
Power Supply Voltage	V _{CC}	4.5 to 35	V
DC/DC Oscillation Frequency Range	f _{osc}	200 to 2200	kHz
External Synchronization Frequency Range (Note 4) (Note 5)	f _{SYNC}	f _{osc} to 2200	kHz
External Synchronization Pulse Duty Range	F _{SDUTY}	40 to 60	%

Note 4 If not using an external synchronization frequency, please make the SYNC open and/or connect to GND.

Note 5 If using an external synchronization frequency, please do not conduct the operation such as switching to internal oscillation frequency in the middle of the process.

Electrical Characteristics ($V_{CC}=12V$, $T_a = T_j = -40^{\circ}C$ to $+125^{\circ}C$ *Unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Normal	Max		
Circuit Current	I _{CC}	-	-	10	mA	EN=High, SYNC=High, RT=OPEN PWM=Low, ISET=OPEN, C _{IN} =10μF
Standby Current	I _{ST}	-	-	10	μA	EN=Low, VDISC=OPEN
[VREG]						
Reference Voltage	V _{REG}	4.5	5.0	5.5	V	I _{REG} =-5mA, C _{REG} =2.2μF
[OUTH]						
OUTH High Side ON-Resistance	R _{ONHH}	1.9	3.5	6.2	Ω	I _{ON} =-10mA, Ta=25°C
		1.5	3.5	7.0	Ω	I _{ON} =-10mA, Ta=-40°C to +125°C
OUTH Low Side ON-Resistance	R _{ONHL}	1.0	2.5	5.0	Ω	I _{ON} =10mA, Ta=25°C
		0.8	2.5	5.5	Ω	I _{ON} =10mA, Ta=-40°C to +125°C
OCP Detection Voltage	V _{OLIMIT}	V _{CC} -0.66	V _{CC} -0.6	V _{CC} -0.54	V	
[OUTL]						
OUTL High Side ON-Resistance	R _{ONL}	0.44	0.8	1.15	Ω	I _{ON} =10mA, Ta=25°C
		0.20	0.8	2.10	Ω	I _{ON} =10mA, Ta=-40°C to +125°C
[SW]						
SW Low Side ON-Resistance	R _{ON_SW}	5.0	10.0	15.0	Ω	I _{ON} =10mA, Ta=25°C
		4.0	10.0	25.0	Ω	I _{ON} =10mA, Ta=-40°C to +125°C
[Error AMP]						
LED Control Voltage	V _{LED}	0.9	1.0	1.1	V	
COMP Sink Current	I _{COMPSINK}	20	80	160	μA	V _{LED} =2V, V _{COMP} =1V
COMP Source Current	I _{COMPSOURCE}	-160	-80	-20	μA	V _{LED} =0V, V _{COMP} =1V
[Oscillator]						
Oscillation Frequency 1	fosc1	285	300	315	kHz	R _T =27kΩ
Oscillation Frequency 2	fosc2	1800	2000	2200	kHz	R _T =3.9kΩ
[OVP]						
OVP Detection Voltage	V _{OVP1}	1.9	2.0	2.1	V	V _{OVP} =Sweep Up
OVP Hysteresis Width	V _{OVPHYS1}	0.45	0.55	0.65	V	V _{OVP} =Sweep Down
Pre-Boost Detection Voltage	V _{OVP2}	0.9	1.0	1.1	V	V _{OVP} =Sweep Up
Pre-Boost Hysteresis Width	V _{OVPHYS2}	0.33	0.43	0.53	V	V _{OVP} =Sweep Down

Electrical Characteristics ($V_{CC}=12V$, $T_a = T_j = -40^{\circ}C$ to $+125^{\circ}C$ *Unless otherwise specified.) - continued

Parameter	Symbol	Limits			Unit	Conditions
		Min	Normal	Max		
[UVLO]						
UVLO Detection Voltage	V _{UVLO}	3.2	3.5	3.8	V	V _{CC} : Sweep Down
UVLO Hysteresis Width	V _{UHYS}	250	500	750	mV	V _{CC} : Sweep Up, V _{REG} >3.5V
[LED Output]						
LED Current Relative Dispersion	I _{LED1}	-3	-	+3	%	I _{LED} =50mA, Ta=25°C ΔI _{LED1} =(I _{LED} /I _{LED_AVG} -1)×100
		-5	-	+5	%	I _{LED} =50mA, Ta=-40°C to +125°C ΔI _{LED1} =(I _{LED} /I _{LED_AVG} -1)×100
LED Current Absolute Dispersion	I _{LED2}	-3	-	+3	%	I _{LED} =50mA, Ta=25°C ΔI _{LED2} =(I _{LED} /50mA-1)×100
		-5	-	+5	%	I _{LED} =50mA, Ta=-40°C to +125°C ΔI _{LED2} =(I _{LED} /50mA-1)×100
ISET Voltage	V _{ISET}	0.9	1.0	1.1	V	R _{ISET} =100kΩ
PWM Minimum Pulse Width	T _{MIN}	20	-	-	μs	F _{PWM} =150Hz, I _{LED} =100mA
PWM Maximum Duty	D _{MAX}	-	-	100	%	F _{PWM} =150Hz, I _{LED} =50mA
PWM Frequency	f _{PWM}	-	-	20	kHz	Duty=2%, I _{LED} =50mA
[Protection Circuit]						
LED Open Detection Voltage	V _{OPEN}	0.2	0.3	0.4	V	V _{LED} = Sweep Down
LED Short Detection Voltage	V _{SHORT}	4.2	4.5	4.8	V	V _{LED} = Sweep Up
LED Short Detection Latch OFF Delay Time	t _{SHORT}	70	100	130	ms	R _{RT} =27kΩ
PWM Latch OFF Delay Time	t _{PWM}	70	100	130	ms	R _{RT} =27kΩ
SCP Latch OFF Delay Time	t _{SCP}	70	100	130	ms	R _{RT} =27kΩ
[Logic Input]						
Input High Voltage	V _{INH}	2.1	-	V _{REG}	V	
Input Low Voltage	V _{INL}	GND	-	0.8	V	
Input Current	I _{IN}	15	50	100	μA	V _{IN} =5V(EN,SYNC,PWM,LEDEN1,LEDEN2)
[FAIL Output (Open Drain)]						
FAIL Low Voltage	V _{OL}	-	0.1	0.2	V	I _{OL} =0.1mA

Typical Performance Curves

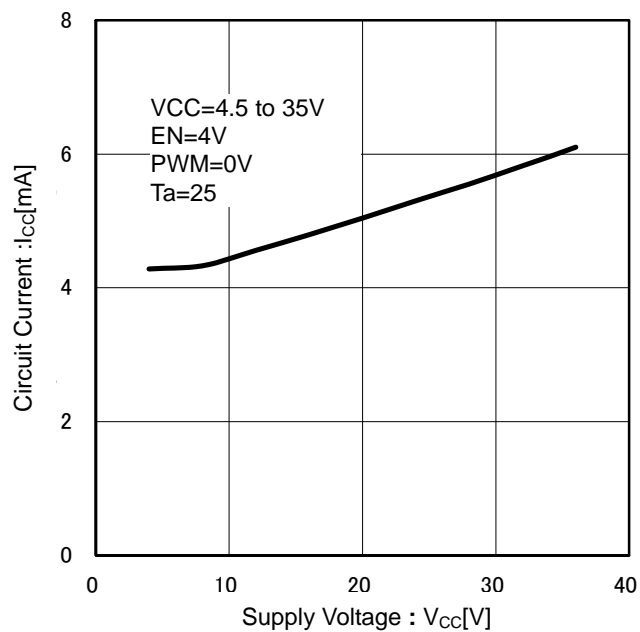


Figure 4. Circuit Current vs Supply Voltage

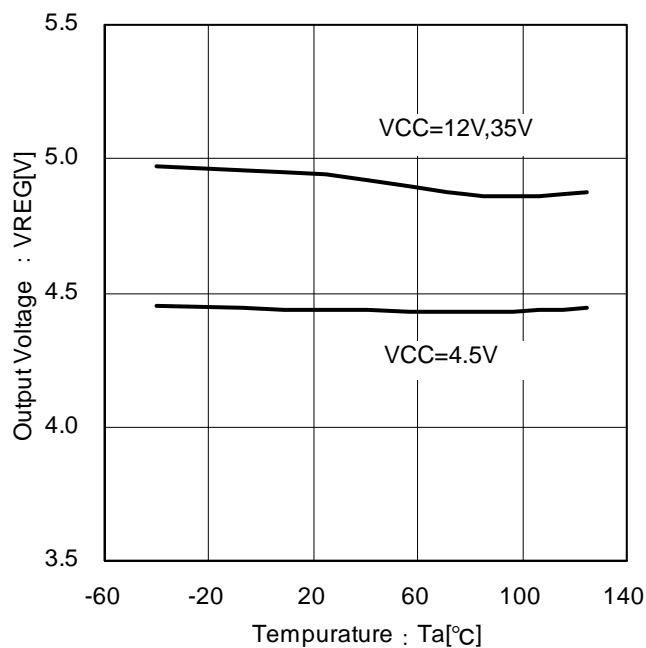
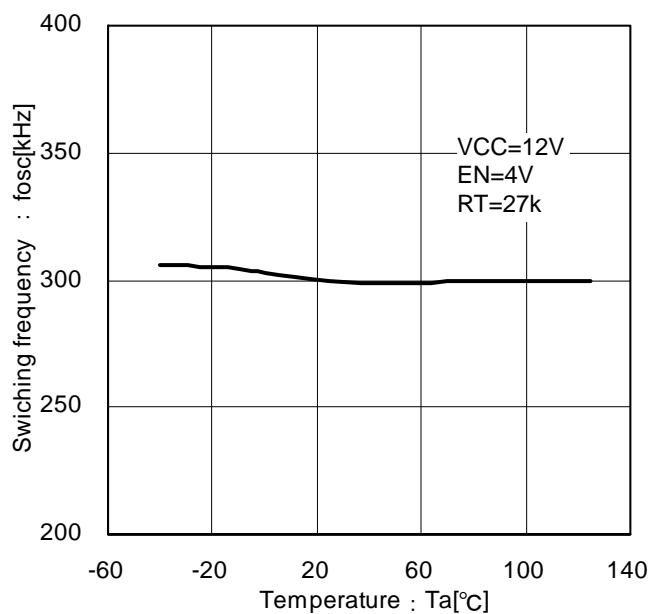
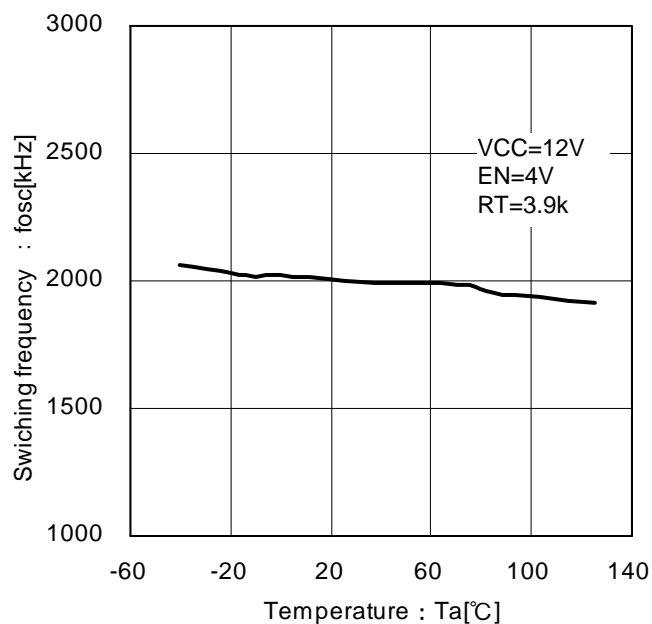


Figure 5. Output Voltage vs Temperature

Figure 6. Switching Frequency vs Temperature
(@300kHz)Figure 7. Switching Frequency vs Temperature
(@2000kHz)

Typical Performance Curves - continued

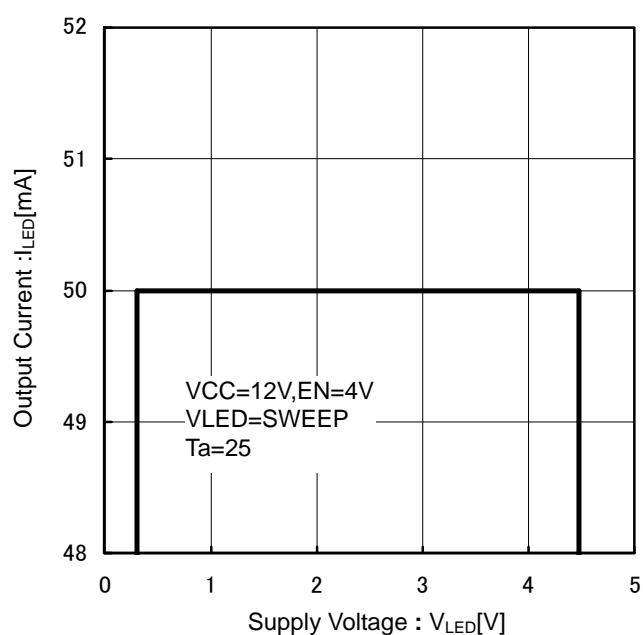


Figure 8. Output Current vs Supply Voltage

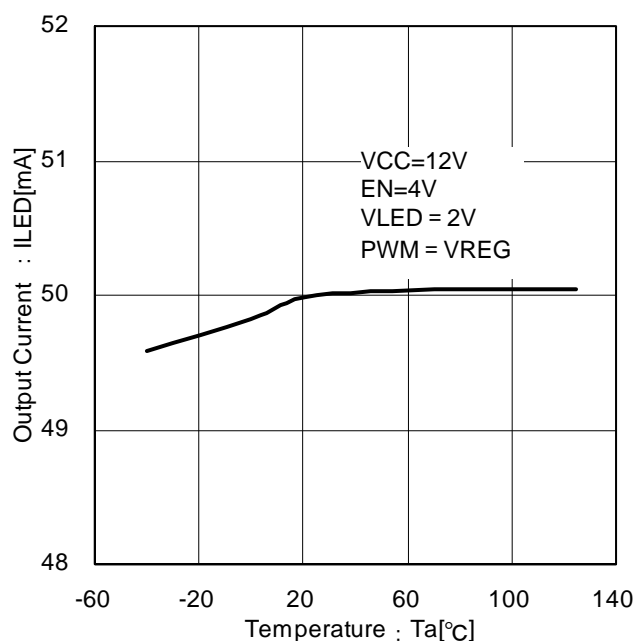


Figure 9. Output Current vs Temperature

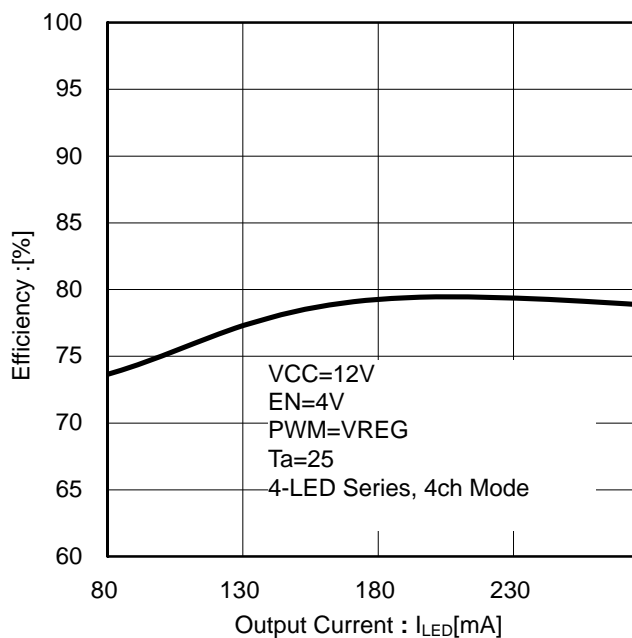


Figure 10. Efficiency vs Output Current (Buck-Boost Application)

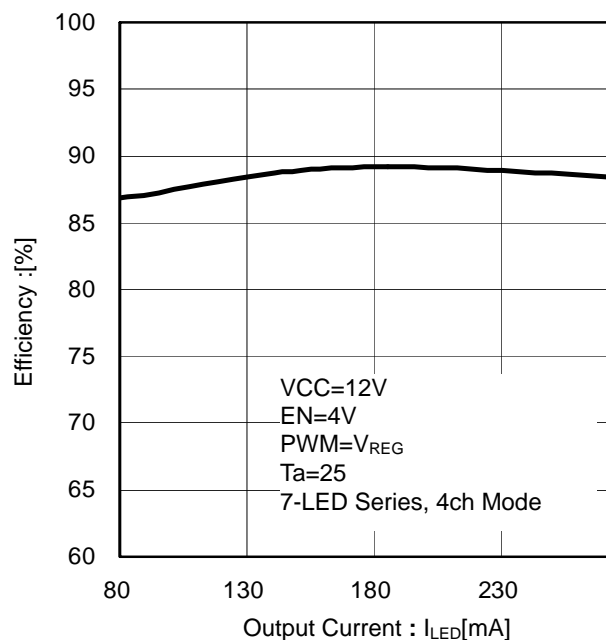


Figure 11. Efficiency vs Output Current (Boost Application)

Description of Blocks

1. Voltage Reference (V_{REG})

5V (Typ) is generated from the V_{CC} Input Voltage (when at EN=High). This voltage (V_{REG}) is used as power supply of internal circuit and when fixing the pins outside of the IC at a high voltage, as well. The UVLO protection is integrated in V_{REG}. The circuit starts to operate at V_{CC} 4.0V (Typ) and V_{REG}=3.5V (Typ) and stops when at V_{CC}≤3.5V (Typ) or V_{REG}≤2.0V (Typ). For release/cancellation condition and detection condition, please refer to Table 2 on page 11. Connect a capacitor (C_{REG}=2.2μF)(typ) to V_{REG} terminal for phase compensation. If the C_{REG} is not connected, the operation of circuit will be notably unstable.

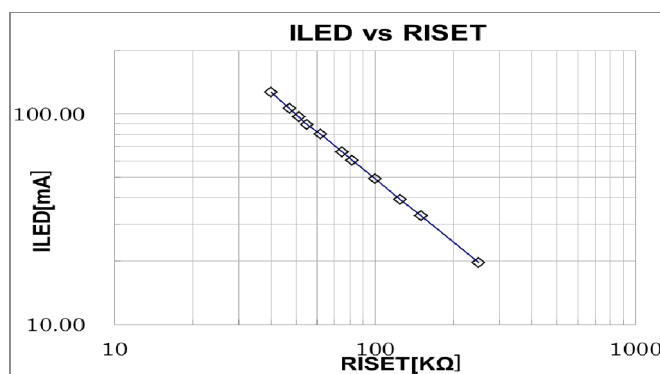
2. Constant Current Driver

Table1. LED Control Logic

LEDEN1	LEDEN2	LED1	LED2	LED3	LED4
L	L	ON	ON	ON	ON
H	L	ON	ON	ON	OFF
L	H	ON	ON	OFF	OFF
H	H	ON	OFF	OFF	OFF

If less than four constant-current drivers are used, please make the LED1~4 terminal 'open' while the output 'OFF' by LEDEN1 and LEDEN2 terminal. The truth table for these pins is shown above. If the unused constant-current driver output will be set open without the process of LEDEN1,2 terminals, the 'open detection' will be activated. The LEDEN1, 2 terminals is pulled down internally in the IC and it is low at 'open' condition. However, they should be connected to V_{REG} terminal or fixed to a logic HIGH when in use.

(1) Output Current Setting

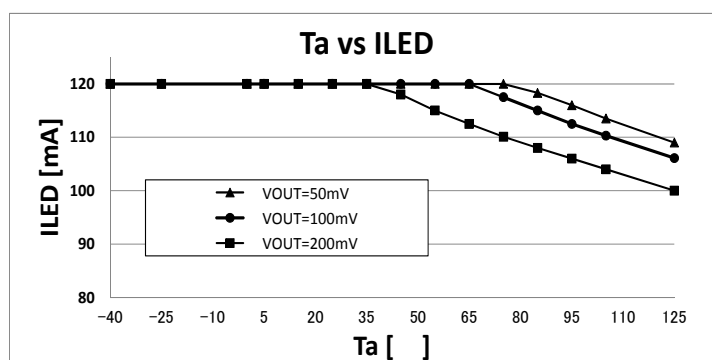
Figure 12. I_{LED} vs R_{ISET}

The Output Current I_{LED} can be obtained by the following equation:

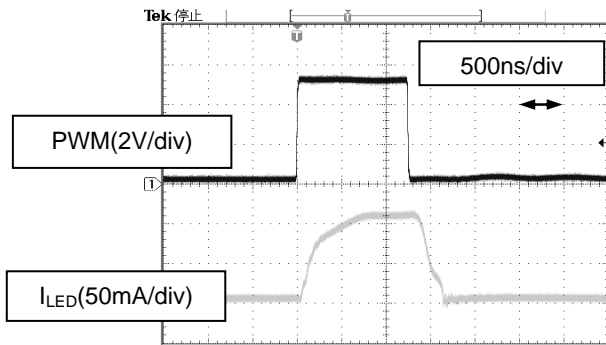
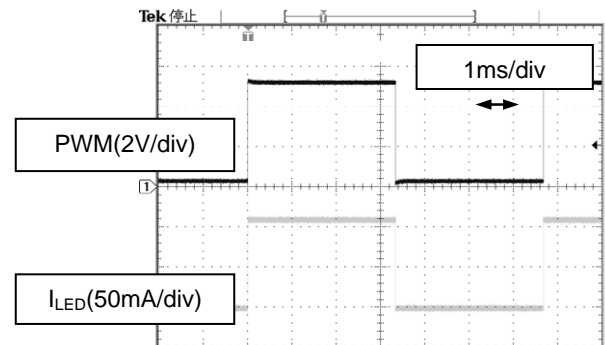
$$I_{LED} [mA] = (1.0V / R_{ISET} [k\Omega]) \times GAIN : GAIN = 5000 (Typ)$$

< Precaution During Current Setting >

If the output current I_{LED} is set to >100mA/ch, the stability of LED current within specified operating temperature range will decrease. LED current supply value will depend on the amount of ripple in output voltage (V_{OUT}). The figure below shows the temperature and the possible LED current maximum value setting, please adjust the ripple voltage in such a way that the LED current value setting will fall within the range as shown on the graph below. (ΔV_{OUT} : Output Ripple Voltage)

Figure 13. Temperature (Ta) vs Output LED Current (I_{LED})

(2) PWM Intensity Control

Figure 14. PWM=150Hz, Duty=0.02%, I_{LED} WaveformFigure 15. PWM=150Hz, Duty=50.0%, I_{LED} Waveform

The current driver ON/OFF of PWM dimmer is controlled in PWM terminal. The duty ratio of PWM terminal becomes duty ratio of I_{LED} . If PWM terminal is not conducted 100%, please set the PWM terminal fixed at HIGH. Output light intensity is greatest at 100% input.

3. Buck-Boost DC/DC Controller

(1) Number of LED in Series Connection

In this chip, the output voltage of the DC/DC converter is controlled in such a way that the forward voltage over each of the LED on the output is set 1.0V (Typ). The DC/DC operation is activated only when LED output is operating. When two or more LED are operating at the same time, the LED voltage output is held at 1.0V (Typ) per LED over the column of LED with the highest forward Voltage. Then the voltages of other LED output within same column will increased only in relation to the fluctuation of voltage. Enough consideration should be given to the change in power dissipation due to VF variations of LEDs. Please determine the allowable maximum VF variance of the total LEDs in series by using the description as shown below:

$$VF \text{ Variation Tolerance Voltage } 3.5V \text{ (Typ)} = \text{Short Detection Voltage } 4.5V \text{ (Typ)} - \text{LED Control Voltage } 1.0V \text{ (Typ)}$$

In addition, the 81.5% of OVP voltage setting is the 'trigger' of 'open detection (falling)'. The maximum value of OVP terminal output voltage is calculated as follows.

$$40V \text{ (DC/DC Output Maximum Rating Voltage)} \times 0.815 = 32.6V$$

Following this, the number of LED series is set in such a way the equation below can be met.

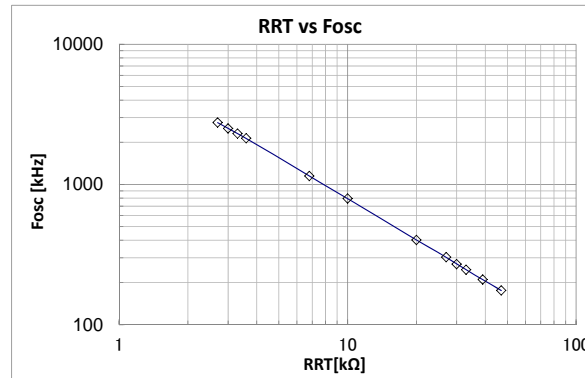
$$(32.6 - 1.1V) / V_F [V] > (\text{Max number of LED series})$$

(2) Over Voltage Protection Circuit (OVP)

The output of the DC/DC converter should be connected to the OVP pin via voltage divider. In determining an appropriate trigger voltage for OVP function, consider the total number of LEDs in series and the Maximum variation in VF. Also, bear in mind that LED Open Detection is triggered at $0.815 \times \text{OVP trigger voltage}$. When OVP terminal voltage drops to 1.45V (Typ) after OVP operation, the OVP will be released or cancelled. If R_{OVP1} (GND side), R_{OVP2} (Output Voltage side) and Output Voltage V_{OUT} , below is the equation:

$$V_{OUT}[V] \geq (R_{OVP1}[k\Omega] + R_{OVP2}[k\Omega]) / R_{OVP1}[k\Omega] \times 2.0V$$

OVP will engage when $V_{OUT} > 32V$ if $R_{OVP1}=22k\Omega$ and $R_{OVP2}=330k\Omega$.

(3) Buck-Boost DC/DC Converter Oscillation Frequency (f_{osc})Figure 16. f_{osc} vs R_{RT}

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 4). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillating frequency. Please set the resistance of R_{RT} using the data mentioned above and the logical equation mentioned below as reference.

$$f_{osc}[\text{kHz}] = (81 \times 10^5 / R_{RT}[\text{k}\Omega]) \times \alpha$$

Where:

81×10^5 is the constant value in IC (+5%)

α is the adjustment factor

(R_T : $\alpha =$ 41k Ω : 1.01, 27k Ω : 1.00, 18k Ω : 0.99, 10 k Ω : 0.98, 4.7k Ω : 0.97, 3.9k Ω : 0.96)

A resistor in the range of 3 k Ω to 41 k Ω is recommended. Settings that deviate from the frequency range shown above may cause switching to stop, and proper operation cannot be guaranteed.

(4) External Synchronization Oscillation Frequency (f_{sync})

The clock signal input to SYNC terminal can be performed from the outside therefore the internal oscillation frequency can be synchronized externally.

Do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin and the clock input to SYNC terminal is valid only in rising edge.

As for the external input frequency, the input of the internal oscillation frequency $\pm 20\%$ decided in RT terminal resistance is recommended.

(5) Soft Start Function (SS)

The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to prevention of the overshoot of the output voltage and the inrush current. If you don't use soft-start function, please set SS terminal open. For the computation of SS time, please refer to the formula on page 19.

4. Self-Check Function

Table 2. Detection Condition of Each Protection Function and the Operation during Detection

Protection Function	Detection Condition		Operation During Detection
	[Detection]	[Release/ Cancellation]	
UVLO	$V_{CC} < 3.5V$ or $V_{REG} < 2.0V$	$V_{CC} > 4.0V$ and $V_{REG} > 3.5V$	All Blocks Shuts down (Except for VREG)
TSD	$T_j > 175^{\circ}C$	$T_j < 150^{\circ}C$	All Blocks Shuts down (Except for VREG)
OVP	$V_{OVP} > 2.0V$	$V_{OVP} < 1.45V$	SS Pin Discharged
OCP	$V_{CS} \leq V_{CC} - 0.6V$	$V_{CS} > V_{CC} - 0.6V$	SS Pin Discharged
SCP	$V_{LED} < 0.3V$ or $V_{OVP} < 0.57V$ (100ms delay @300kHz)	EN or UVLO	Delay Counter starts and then Latches Off all blocks (Except for VREG)
LED Open Protection	$V_{LED} < 0.3V$ & $V_{OVP} > 1.8V$	EN or UVLO	Only the detected channel latches OFF
LED Short Protection	$V_{LED} > 4.5V$ (100ms delay @300kHz)	EN or UVLO	Only the detected channel latches OFF (After the counter starts)

Note1. The FAIL1 and FAIL2 output is reset when EN=Low \Rightarrow High or UVLO Detection \Rightarrow Release/ Cancel
(EN = Low or UVLO Detection are unfixed.)

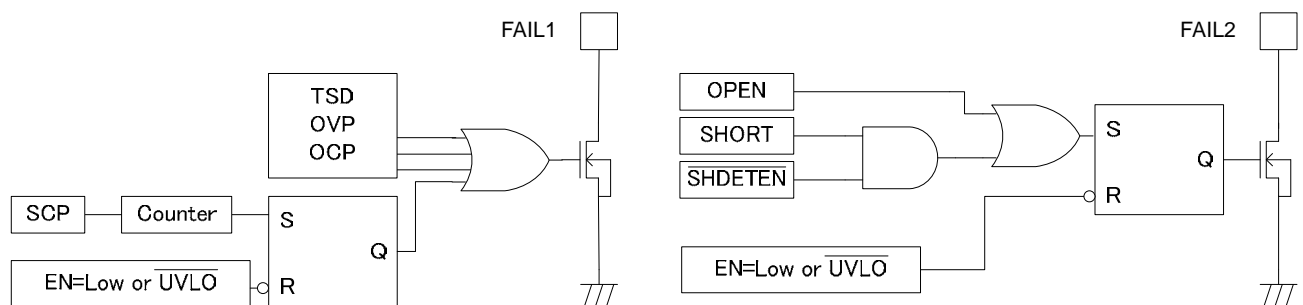


Figure 17. Protection Flag Output Block Diagram

The operating status of the built-in protection circuitry is propagated to FAIL1 and FAIL2 terminals (open-drain outputs). FAIL1 becomes low when TSD, OVP, OCP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected. If the FAIL terminal will not be used as flag output, please make the FAIL terminal open or connect it to GND. But if the FAIL terminal will be used as a flag output, it is recommended to pull-up the FAIL1, 2 terminals to VREG terminal.

(1) Under-Voltage Lock Out (UVLO)

The UVLO shuts down all the circuits other than V_{REG} when $V_{CC} < 3.5V$ (Typ) or $V_{REG} < 2.0V$ (Typ)

(2) Thermal Shut Down (TSD)

The TSD shuts down all the circuits other than V_{REG} when the T_j reaches $175^{\circ}C$ (Typ), and releases when the T_j becomes below $150^{\circ}C$ (Typ).

(3) Over-Current Protection (OCP)

The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor, and activates when the CS voltage becomes less than $V_{CC} - 0.6V$ (Typ).

When the OCP is activated, the external capacitor of the SS terminal becomes discharged and the switching operation of the DC/DC turns off.

(4) Over-Voltage Protection (OVP)

The output voltage of DC/DC is detected from the OVP terminal voltage, and the over-voltage protection will activate if the OVP terminal voltage becomes greater than $2.0V$ (Typ). When OVP is activated, the external capacitor of the SS terminal becomes discharged and the switching operation of the DC/DC turns off.

(5) Short Circuit Protection (SCP)

When the LED terminal voltage becomes less than 0.3V (Typ), the internal counter starts operating and latches off the circuit approximately after 100ms (when FOSC = 300kHz). If the LED terminal voltage becomes over 0.3V before 100ms, then the counter resets.

When the LED anode (i.e. DC/DC output voltage) is shorted to ground, then the LED current becomes off and the LED terminal voltage becomes low. Furthermore, the LED current also becomes off when the LED cathode is shorted to ground. Hence in summary, the SCP works with both cases of the LED anode and the cathode being shorted.

(6) LED Open Detection

When the LED terminal voltage is below 0.3V (Typ) as well as OVP terminal voltage >1.8V (Typ) simultaneously, the device detects as LED open and latches off that particular channel.

(7) PWM Low Interval Detection Circuit

After the EN loading, the low interval of PWM input is counted by built-in counter. The clock frequency of counter is the fosc Frequency, which is determined by R_{RT}, and stops the operation of circuits other than VREG at 32768 count. For fosc=300kHz, it becomes 'PWM low interval detection' after 100ms.

(8) Output Voltage Discharge Circuit (VDISC terminal)

Restarting DC/DC must be operated after discharging V_{OUT}. If using only pull-down resistance as setting OVP for discharging, it takes a lot time for discharging V_{OUT}. Therefore this product has functionality of circuit for discharge. When V_{DISC} terminal is connected to output of DC/DC, the output can be discharged when DCCD circuit become OFF (with EN changing high to low or detection of protect).

The discharge time t_{DISC} is expressed in the following equations.

$$t_{DISC}[s](Typ) = C_{OUT}[F] \times V_{OUT}[V] / 0.33$$

$$t_{DISC}[s](Max) = C_{OUT}[F] \times V_{OUT}[V] / 0.192$$

Where:

t_{DISC} : DC/DC Output Discharge Time

C_{OUT} : DC/DC Output Capacity

V_{OUT} : DC/DC Output Voltage

In the discharge of residual charge, it will take some t_{DISC} time. For EN re-loading, conduct after the time from OFF of DC/DC circuit to t_{DISC} (or higher) is opened.

(9) LED Short Detection Circuit

If the LED terminal voltage becomes >4.5V (Typ), the built-in counter operation will start and the latch will activate at oscillation frequency in 32770 count. In case of fosc=300kHz, it becomes 'Latch OFF' only with corresponding LED series after 100ms. During 'PWM light modulation', the LED Short Detection Operation is carried out only when PWM=High. If the LED Short Detection 'condition' is released/ cancelled while counter is running, the counter will reset and will return to normal operating condition. When LED Short Detection function will not be used, SHDETEN should be connected to VREG before starting therefore Turning OFF of Short Detection function. When LED Short Detection function is used, the SHDETEN should be connected to GND. In addition, the switching of SHDETEN=High/Low can be made during normal operation.

Timing Chart

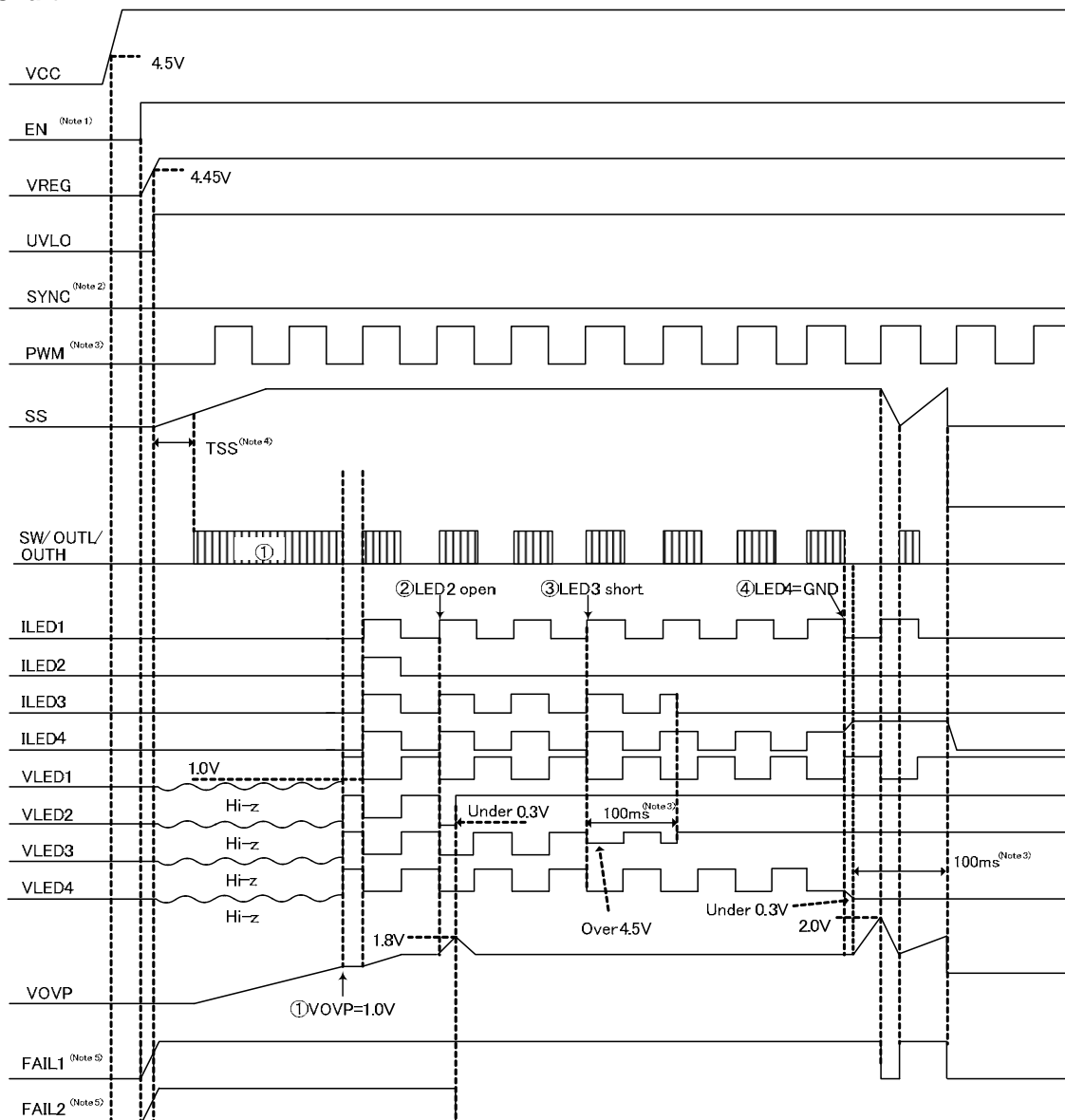


Figure 18. Protection Sequence Timing Chart

Note 1 Turn on EN after V_{CC} reaches the operating voltage range.

Note 2 The order of turning on PWM and SYNC is arbitrary.

Note 3 Approximately 100ms of delay when fosc=300kHz.

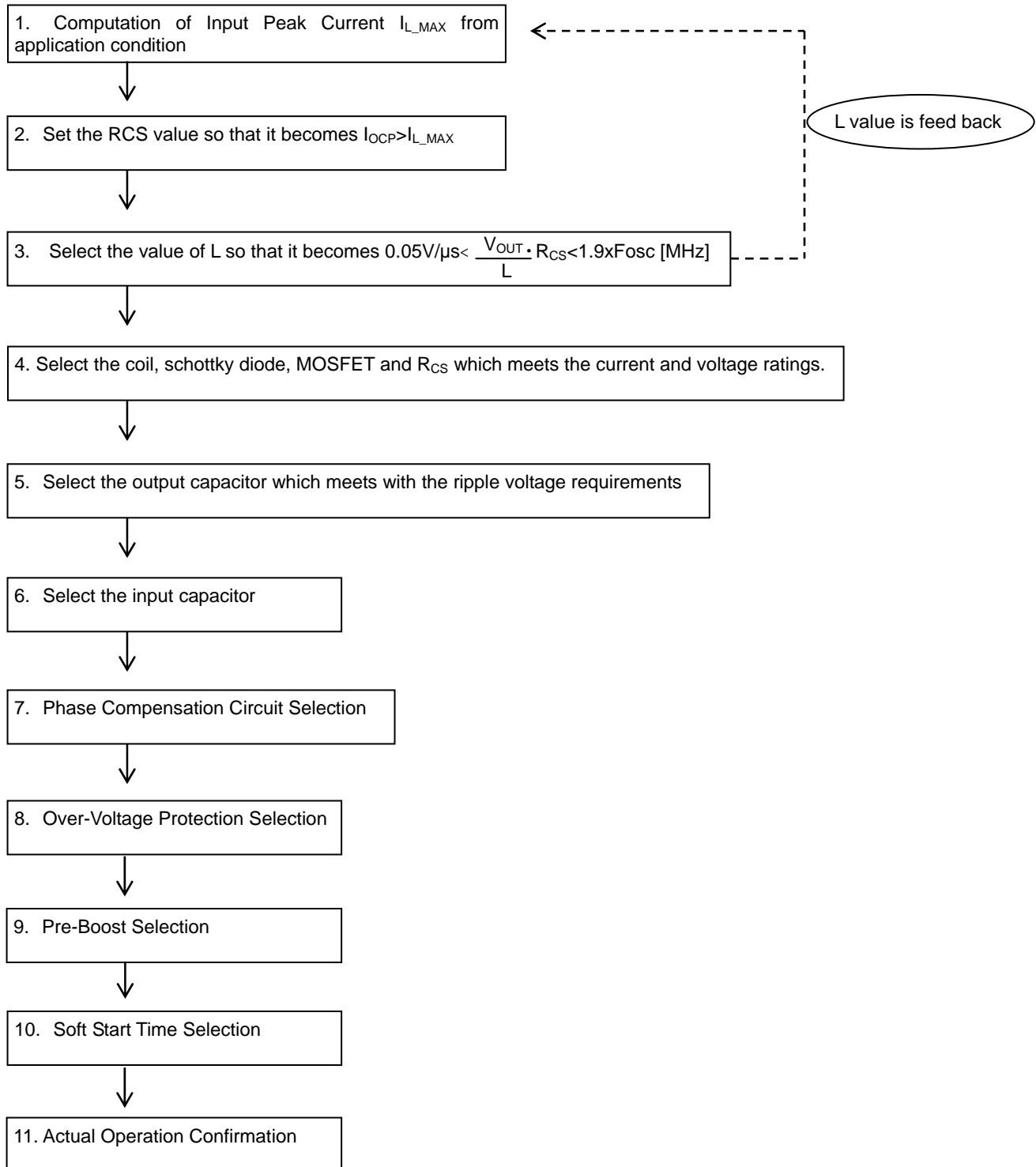
Note 4 The TSS expresses the time from UVLO release/cancel until the start of DC/DC switching. (Details on page 19)

Note 5 The timing chart is defined when pulling -up the FAIL Pin towards the VREG.

1. In between $V_{OVP} < 1.0V$, regardless it is PWM input, the DC/DC switching operation will be carried out (Pre-Voltage). By the $V_{OVP} \geq 1.0V$, the pre-voltage ends.
2. The LED2 is Open mode.
 $V_{LED2} < 0.3V$ and $V_{OVP} > 1.8V$ are detected and LED2 is Turned OFF. → FAIL2 becomes Low
3. LED3 is Short mode
 $V_{LED3} > 4.5V$ is detected and after 100ms, the (@fosc=300kHz) LED3 will Turn OFF.
4. VLED4 is shorted to GND.
 - (1) Output Voltage High, and OVP is detected with $V_{OVP} > 2.0V$.
→ SS discharged and FAIL1 becomes low.
 - (2) After detection of $V_{LED4} < 0.3V$, shutdown after about 100ms (@fosc=300kHz).

Procedure for external components selection

Follow the steps as shown below for selecting the external components.



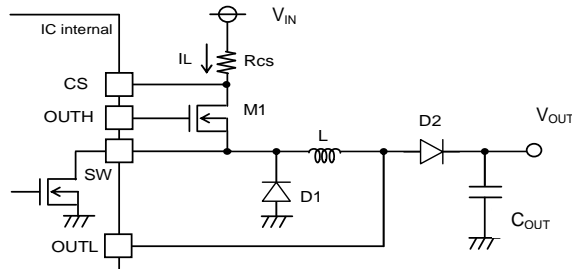
1. Input Peak Current I_{L_MAX} Computation (In case of Buck-Boost Application)

Figure 19. Output Application Circuit Diagram

(1) Max Output Voltage (V_{OUT_MAX}) Computation

Consider the V_F variation and number of LED connection in series for V_{OUT_MAX} derivation

$$V_{OUT_MAX} = (V_F + \Delta V_F) \times N + 1.1V$$

Where:

V_{OUT_MAX} [V] is the Max Output Voltage

V_F [V] is the LED V_F Voltage

ΔV_F is the LED V_F Voltage Variation

N is the No. of LED series

(2) Max Output Current I_{OUT_MAX} Computation

$$I_{OUT_MAX} = I_{LED} \times 1.03 \times M$$

Where:

I_{OUT_MAX} [A]: Max Input Peak Current

I_{LED} [A]: Output Current/Ch.

M : No. of LED parallel

(3) Max Input Peak Current I_{L_MAX} Computation

$$I_{L_MAX} = I_{L_AVG} + 1/2 \Delta I_L$$

Where:

I_{L_MAX} [A]: Max Input Peak Current

I_{L_AVG} [A]: Max Input Average Current

I_L [A] : Input Current Amplification

$$I_{L_AVG} = (V_{IN} + V_{OUT_MAX}) \times I_{OUT_MAX} / (n \times V_{IN})$$

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{1}{f_{osc}} \times \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

Where:

V_{IN} [V] : Input Voltage

N: Efficiency

f_{osc} : Switching Frequency

L [H]: Coil Value

(a) The worst case scenario for V_{IN} is when it is at the Minimum, and thus the Minimum value should be applied in the equation..

(b) The L value of 2.2 to 47 μ H is recommended. The current-mode Type of DC/DC conversion is adopted for BD81A04AMUV-M and BD81A04AEFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.

(c) n (efficiency) becomes almost 80%.

2. Setting of Over-Current Protection Value

Please select the R_{CS} value so that it becomes

$$V_{OCP_MIN}[V](=0.54V) \div R_{CS}[\Omega] > I_{L_MAX}[A]$$

3. Selection of the L inductor

In order to achieve stable operation of the 'current mode DC/DC converter', we recommend selecting the L value in the range indicated below.

$$0.05[V/\mu s] < \frac{V_{OUT}[V] \times R_{CS}[\Omega]}{L[\mu H]} < 1.9 \times f_{osc}[MHz]$$

Since there is almost $\pm 30\%$ variation in the value of coil L, keep enough margin and set.

The smaller $\frac{V_{OUT} \times R_{CS}}{L}$ allows stability improvement but slows down the response time.

4. Selection of Coil L, Diode D1, D2, MOSFET M1, R_{CS} and C_{OUT}

	Current Rating	Voltage Rating	Heat Loss
Coil L	$> I_{L_MAX}$	—	
Diode D1	$> I_{OCP}$	$> V_{IN_MAX}$	
Diode D2	$> I_{OCP}$	$> V_{OVP_MAX}$	
MOSFET M1	$> I_{OCP}$	$> V_{IN_MAX}$	
R_{CS}	—	—	$> I_{OCP}^2 \times R_{CS}$
C_{OUT}	—	$> V_{OVP_MAX}$	—

Please consider external parts deviation and make the setting with enough margin.

In order to achieve fast switching, choose the MOSFET's with the smaller gate-capacitance.

5. Selection of Output Capacitor

Select the output capacitor C_{OUT} based on the requirement of the ripple voltage V_{PP} .

$$V_{PP}[V] = \frac{I_{OUT}[A]}{C_{OUT}[F]} \times \frac{V_{OUT}[V]}{V_{OUT}[V] + V_{IN}[V]} \times \frac{1}{f_{osc}[Hz]} + I_{L_MAX}[A] \times RESR[\Omega]$$

Choose C_{OUT} that allows the V_{PP} to settle within the requirement. Allow some margin also, such as the tolerance of the external components.

6. Selection of Input Capacitor

A capacitor at the input is also required as the peak current flows between the input and the output in DC/DC conversion.

We recommend an input capacitor greater than $10\mu F$ with the ESR smaller than $100m\Omega$. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence lead to malfunction.

7. Phase Compensation Circuit Guidelines

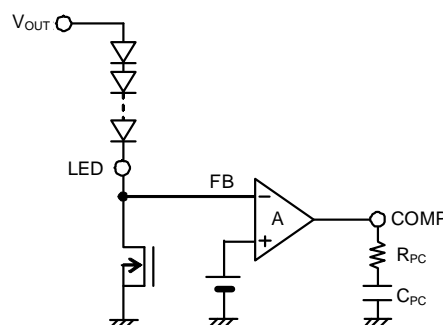


Figure 20. COMP Application Circuit Diagram

About Application Stability Condition

The stability in LED voltage feedback system is achieved when the following conditions are met.

- (1) The phase delay when gain is 1(0dB) is below $150^\circ C$ (or simply, phase margin $> 30^\circ C$).
- (2) The frequency (Unity Gain Frequency) when gain is 1(0dB) is $< 1/10$ of switching frequency.

One way to assure stability based on phase compensation is phase advancement close to Frequency and f_z insertion. In addition, the phase delay f_{p1} shall be decided based on C_{OUT} and Output impedance R_L . Respective formula shall be as follows.

$$\text{Phase-lead} \quad f_z[\text{Hz}] = \frac{1}{2\pi C_{pc}[F] R_{pc}[\Omega]}$$

$$\text{Phase-lag} \quad f_{p1}[\text{Hz}] = \frac{1}{2\pi R_L[\Omega] C_{OUT}[F]}$$

$$\text{The output impedance calculated from } R_L = \frac{V_{OUT}}{I_{OUT}}$$

Good stability would be obtained when the f_z is set between 1kHz ~ 10kHz.

In buck-boost applications, Right-Hand-Plane (RHP) Zero exists. This Zero has zero characteristic for gain and pole characteristic in terms of phase. As this Zero would cause instability when it is in the control loop, so it is necessary to keep RHP frequency more than GBW frequency.

$$f_{RHP}[\text{Hz}] = \frac{V_{OUT} \times [V_{IN} / (V_{OUT} + V_{IN})]^2}{2\pi I_{LOAD}[A] L[H]}$$

Where:

I_{LOAD} : Max Load Current

It is important to keep in Mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

8. Setting of Over-Voltage Protection(OVP)

Over-voltage protection (OVP) is set from the external resistance R_{OVP1} and R_{OVP2} .

The setting described below will be important in the either boost, buck, buck-boost applications.

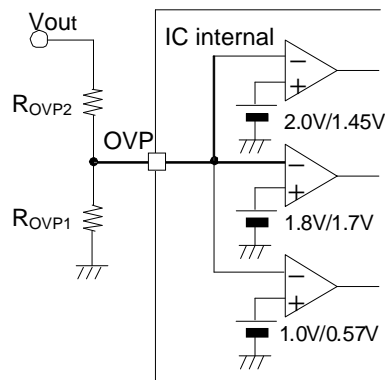


Figure 21. OVP Application Circuit

The OVP terminal detects the over-voltage when at >2.0V (Typ) and stops the DC/DC operation. In addition, it detects the open condition when OVP terminal is at >1.8V (Typ) and LED1 to 4 pin voltage is at <0.3V (Typ), and the circuit is latched to OFF (Please refer to page 11, Self-Check Function). In preventing error in detection of OPEN, it is necessary that the resistor partial pressure voltage of the maximum value of output voltage shall be less than the MIN value of OPEN detection voltage. Please set the R_{OVP1} and R_{OVP2} is such a way the formula shown below can be met.

$$V_{OUT}(\text{Max}) \times (R_{OVP1} / (R_{OVP1} + R_{OVP2})) < V_{OPEN}(\text{Min}) \dots (1)$$

Where:

V_{OUT} is the : DC/DC Output Voltage

V_{OPEN} is the OVP Pin Open Detection Voltage

Sample 1: When $V_F=3.2V \pm 0.3V$ LED is used in 8series

$$V_{OUT}(\text{Max}) = 1.1V(\text{LED Control Voltage Max}) + (3.2V + 0.3V) \times 8 = 29.1V$$

$$\text{Open Detection OVP Pin Voltage } V_{OPEN}(\text{Min}) = 1.7V$$

$$\text{If } R_{OVP1}=20k\Omega, \text{ please set by } R_{OVP2} > 322.3k\Omega \text{ from (1)}$$

Sample 2: $V_F=3.2V\pm0.3V$ LED is used in 3series

$$V_{OUT} (Max) = 1.1V (LED \text{ Control Voltage Max}) + (3.2V + 0.3V) \times 3 = 11.6V$$

$$\text{Open Detection OVP Pin Voltage } V_{OPEN} (Min) = 1.7V$$

If $R_{OVP1}=20k\Omega$, please set by $R_{OVP2} > 116.5k\Omega$ from (1).

9. Setting of Pre-Boost Voltage (OVP)

OVP circuit detects abnormality in DC/DC output start-up when OVP pin voltage is below 1.0V (Typ).

To shorten the starting time at Low PWM duty condition, as far as pre-boost condition (DC/DC not starting at 1.0V (Typ)) is concerned, the OVP pin will carry out a 100% switching without relying on PWM duty. For this, to be able to carry-out the normal PWM modulation, it would be important that the output voltage minimum value of OVP resistance voltage shall exceed the pre-boost setting OVP voltage maximum value. Please conduct the setting for R_{OVP1} and R_{OVP2} in such a way it meets the formula below.

$$V_{OUT} (Min) \times (R_{OVP1} / (R_{OVP1} + R_{OVP2})) > V_{OVP} (Max) \dots (2)$$

Where:

V_{OUT} : DC/DC Output Voltage V_{OVP} : OVP Pre-Boost Voltage Setting

Sample 1: If the LED of $V_F=3.2V\pm0.3V$ is used in the 8series

$$V_{OUT} (Min) = 0.9V (LED \text{ Control Voltage Min}) + (3.2V - 0.3V) \times 8 = 24.1V$$

$$\text{Pre-Boost Voltage Setting } V_{OVP} (Max) = 1.1V$$

If $R_{OVP1}=20k\Omega$, it would be important to conduct setting by $R_{OVP2} < 418.2k\Omega$ from (2).

Sample 2: If the LED of $V_F=3.2V\pm0.3V$ is used in the 3series

$$V_{OUT} (Min) = 0.9V (LED \text{ Control Voltage Min}) + (3.2V - 0.3V) \times 3 = 9.6V$$

$$\text{Pre-Voltage Voltage Setting } V_{OVP} (Max) = 1.1V$$

If $R_{OVP1}=20k\Omega$, it would be important to conduct setting by $R_{OVP2} < 154.5k\Omega$ from (2).

< In case of $V_F=3.2V\pm0.5V$, 8series, $R_{OVP1}=20k\Omega$ and $R_{OVP2}=360k\Omega$ >

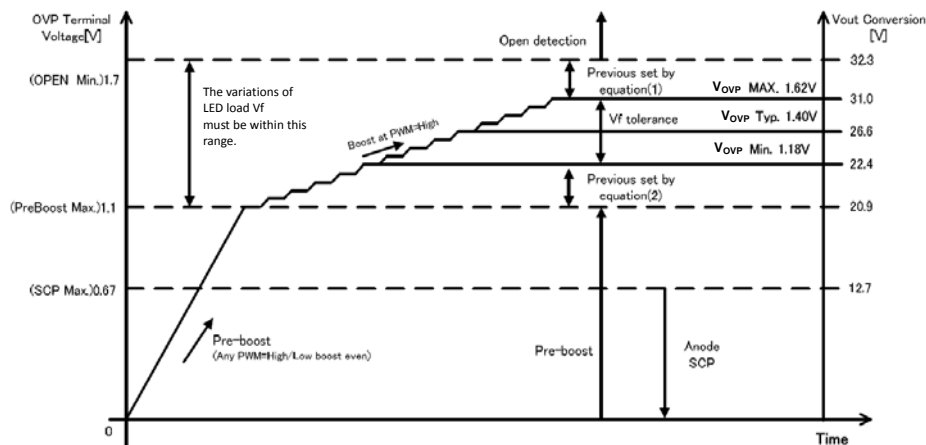


Figure 22. OVP Terminal Voltage Operation Model (8series)

< In case of $V_F=3.2V\pm0.5V$, 3series, $R_{OVP1}=20k\Omega$ and $R_{OVP2}=130k\Omega$ >

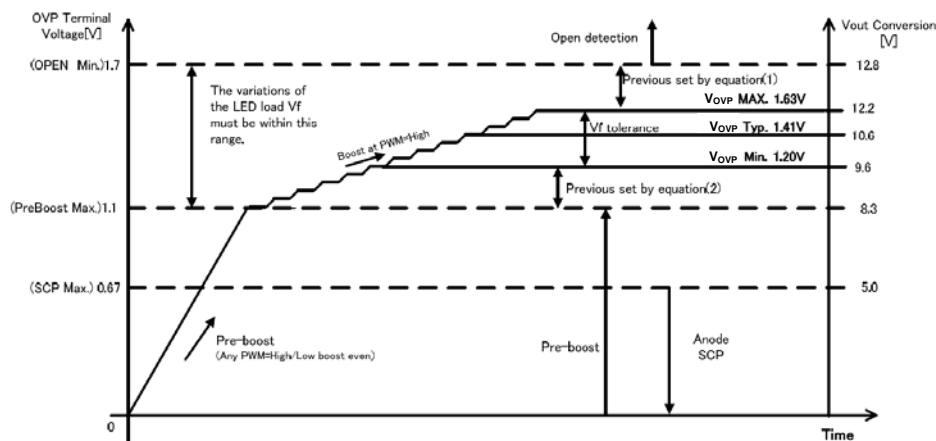


Figure 23. OVP Terminal Voltage Operation Model (3series)

There is a presence of pre-boost by initial voltage of V_{OUT} from the OVP terminal voltage setting and application construction. Shown below is the presence of pre-boost operation upon start.

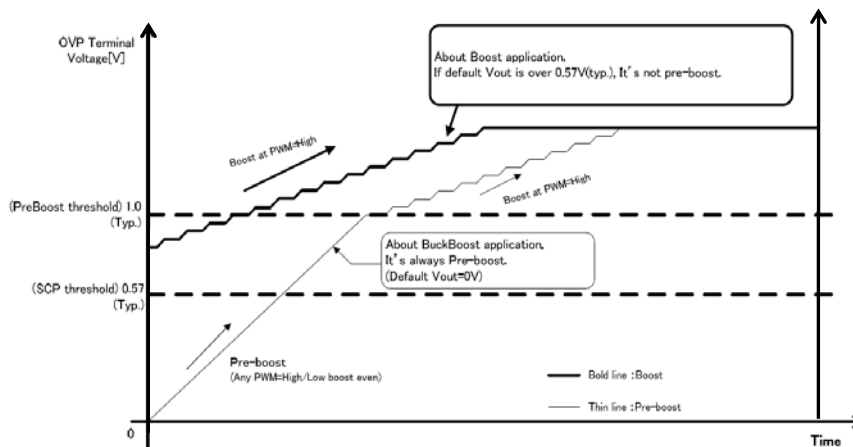


Figure 24. Not a Pre-boost model (V_{OUT} initial value is above 0.57V (Typ))

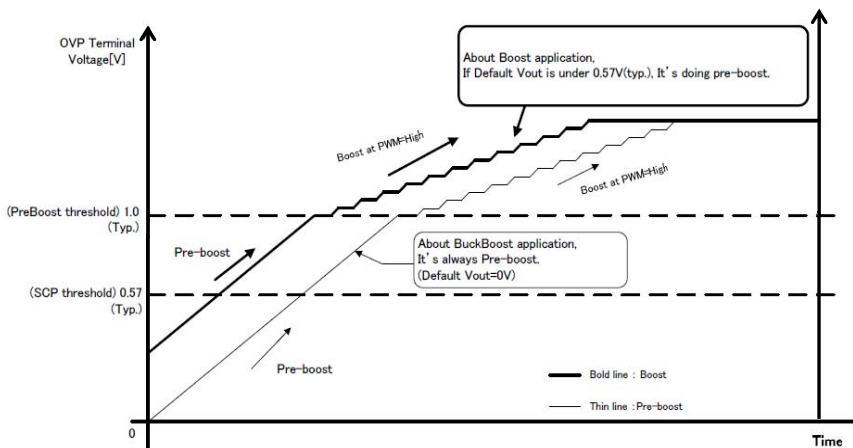


Figure 25. Pre-boost model (V_{OUT} initial value is below 0.57V (Typ))

10. Setting of Soft Start

The soft start circuit minimizes the coil current at the input and overshoot at the output voltage during the start-up condition. A capacitance in the range of 0.001 to 0.1 μ F is recommended. A capacitance of less than 0.001 μ F may cause overshoot at the output voltage. However, a capacitance greater than 0.1 μ F may cause massive reverse current through the parasitic elements when power supply is OFF and may damage the IC. In case, that it is necessary to use a capacitance greater than 0.1 μ F, ensure to have a reverse current protection diode at the V_{CC} or a bypass diode between the SS pin and V_{CC} pin

Soft start time (the time from E_N loading and PWM loading up to start of DC/DC switching) t_{SS} (Typ)

$$t_{SS}[S] = C_{SS}[\mu F] \times 0.7[V] / 5[\mu A]$$

Where;

C_{SS} : The capacitance at SS terminal

In C_{SS} setting and DC/DC oscillation frequency setting, there is a possibility that grounding protection will take time during start-up. This is occurring since grounding is detected before start-up when the start-time of DC/DC output due to C_{SS} setting becomes bigger than the time extension of grounding protection taking time. Please check the following setting of C_{SS} and Oscillating frequency.

$$trise[s] = C_{SS}[\mu F] \times V1[V] / I_{SS}[\mu A]$$

Where:

$trise$: DC/DC Output Start-Up Time

$V1$: IC Constant Voltage (Max 2.0V)

I_{SS} : SS Source Current (Min 2.0 μ A)

$$t_{SCP}[s] = 32770 \times (1/fosc[Hz])$$

Where:

t_{SCP} : SCP Latch OFF Delay Time

$fosc$: DC/DC Oscillating Frequency

SCP error detection avoidance condition: $trise < t_{SCP}$

11. Verification of the operation by taking measurements

The overall characteristics may change based on load current, input voltage, output voltage, inductance, load capacitance, switching frequency, and PCB layout. We strongly recommend verifying your design by taking the actual measurements.

I/O Recommended Operating Range

The I/O recommended operating range (V_{CC} vs V_{OUT}) of BD81A04AMUV-M/EFV-M is shown as follows.

The graphs below are the recommended operating range of output voltage (V_{OUT}) for the input voltage (V_{CC}). The data mentioned below is the reference data for ROHM evaluation board. So please always check the behavior of the evaluation board before using this IC.

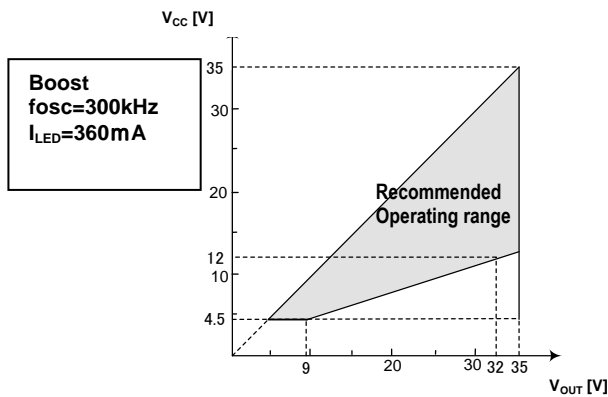


Figure 26. Boost, fosc=300kHz and I_{LED} =360mA Operating Range

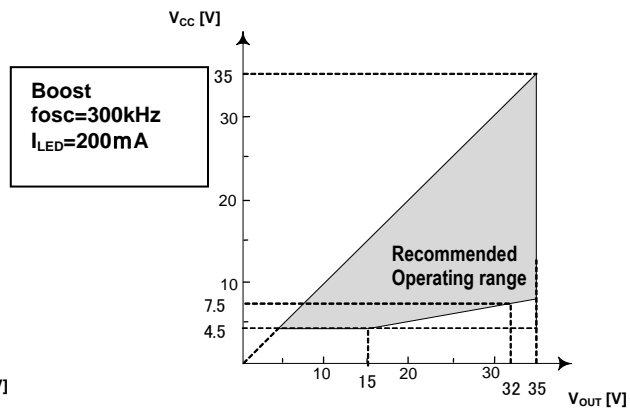


Figure 27. Boost, fosc=300kHz and I_{LED} =200mA Operating Range

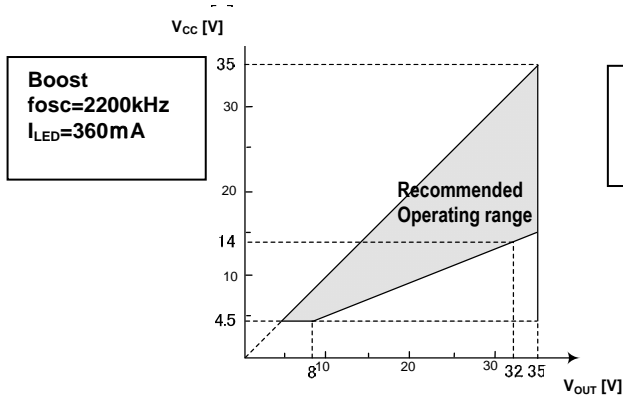


Figure 28. Boost, fosc=2200kHz and I_{LED} =360mA Operating Range

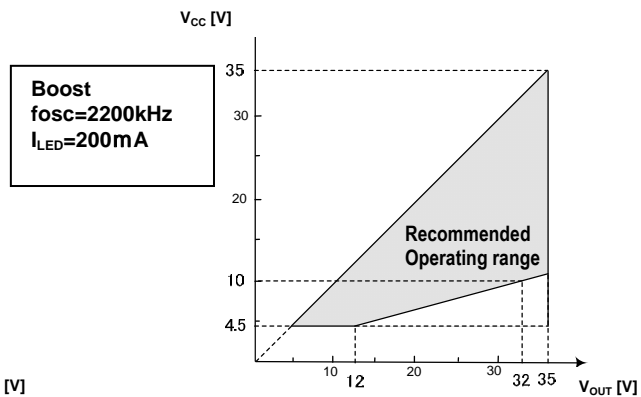


Figure 29. Boost, fosc=2200kHz and I_{LED} =200mA Operating Range

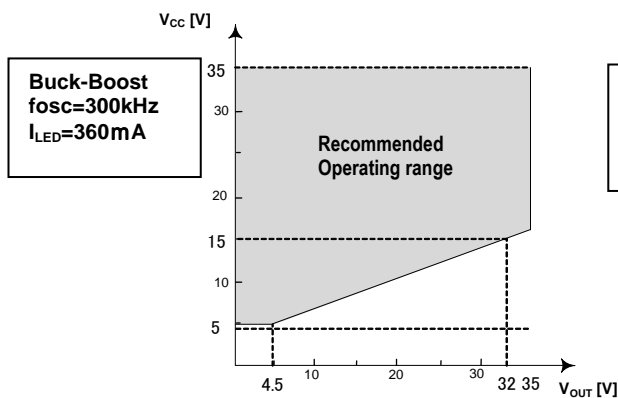


Figure 30. Buck-Boost, fosc=300kHz, I_{LED} =360mA Operating Range

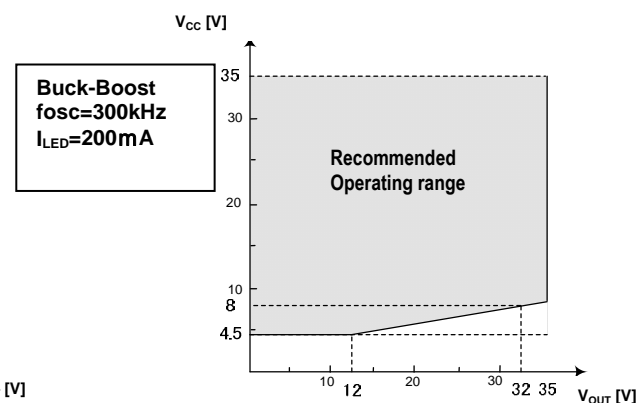


Figure 31. Buck-Boost, fosc=300kHz, I_{LED} =200mA Operating Range

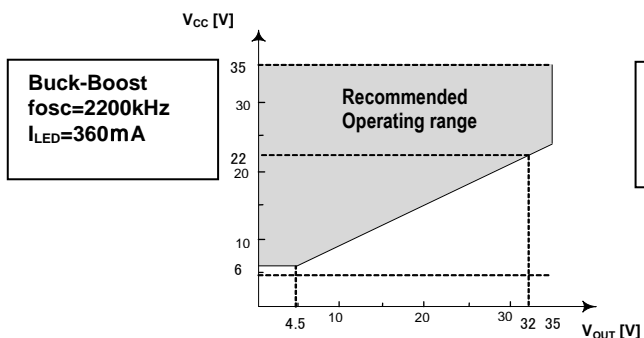


Figure 32. Buck-Boost, fosc=2200kHz, I_{LED} =360mA Operating Range

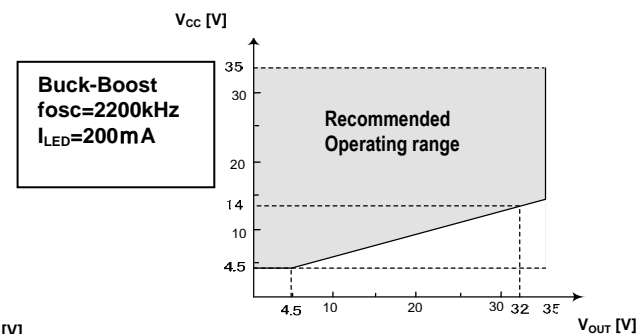


Figure 33. Buck-Boost, fosc=2200kHz, I_{LED} =200mA Operating Range

PCB Application Circuit

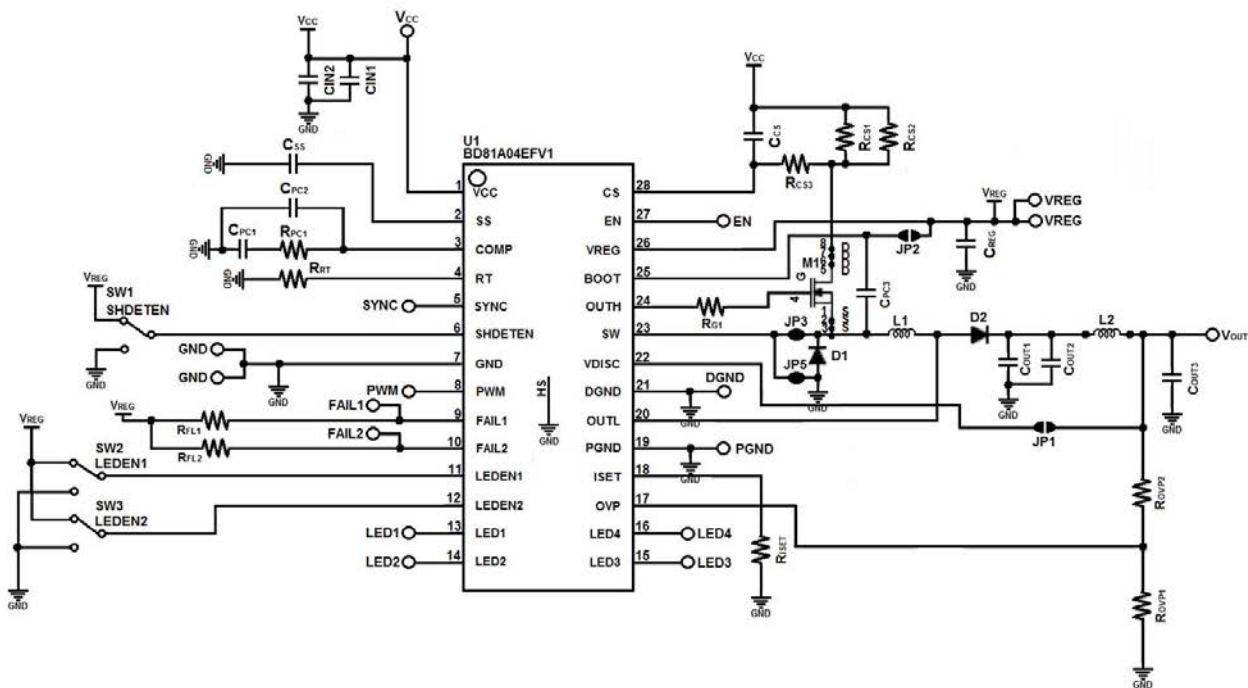


Figure 34. PCB Application Circuit

1. Set the R_{RT} resistance right near the RT terminal and do not put a capacitor.
2. Set the R_{ISET} resistance right near the ISET terminal pin and do not put a capacitor.
3. As much as possible, please put the coupling capacitors of C_{VCC} and C_{REG} as close as possible to the IC terminal pin.
4. Large current may pass through D_{GND} and P_{GND} , so routing low impedance to the system ground.
5. Noise should be minimized as much as possible on PWM, ISET, and COMP pins.
6. PWM, OUTH, SW, SYNC and LED1-4 carry switching signals, please be careful so that the surrounding pattern is not affected by crosstalk.
7. There is a heat radiation PAD at the back of the package. Please solder heat radiation PAD with the board.
8. Please make the buck FET (M1) gate resistance (R_{G1}) into 0Ω . When resistance is connected, the OFF timing is delayed at R_{G1} and M1 parasitic capacitance will have large current that will flow through internal transistor of M1 and SW. By this large current, detection of OCP will occur.
9. In relation to boost loop ($D2 \rightarrow COUT1 \rightarrow DGND \rightarrow M2 \rightarrow D2$) and buck loop ($VCC \rightarrow RCS \rightarrow M1 \rightarrow D1 \rightarrow DGND \rightarrow GND \rightarrow CIN1 \rightarrow VCC$) for the reduction of noise, please study and consider board layout at shortest minimum impedance.

PCB Board External Components List

Serial No.	Component Name	Component Value	Product Name	Manufacturer
1	CIN1	10 μ F	GRM31CB31E106KA75B	Murata
2	CIN2	(open)	-	-
3	CPC1	0.1 μ F	GRM188B31H104KA92	Murata
4	CPC2	(open)	-	-
5	RPC1	510 Ω	MCR03 Series	Rohm
6	CSS	0.01 μ F	GRM188B31H104KA92	Murata
7	RRT	27k Ω	MCR03 Series	Rohm
8	RFL1	100k Ω	MCR03 Series	Rohm
9	RFL2	100k Ω	MCR03 Series	Rohm
10	CCS	(open)	-	-
11	RCS1	620m Ω	MCR100 Series	Rohm
12	RCS2	620m Ω	MCR100 Series	Rohm
13	RCS3	0 Ω	-	-
14	CREG	2.2 μ F	GRM188B31A225KE33	Murata
15	CPC3	0.1 μ F	GRM188B31H104KA92	Murata
16	M1	-	RSH070N05	Rohm
17	M2	(open)	-	-
18	D1	-	RB050L-40	Rohm
19	D2	-	RB050L-40	Rohm
20	L1	33 μ H	SLF10145T-330M1R6-H	TDK
21	L2	(open)	-	-
22	COUT1	10 μ F	GRM31CB31E106KA75B	Murata
23	COUT2	10 μ F	GRM31CB31E106KA75B	Murata
24	COUT3	(open)	-	-
25	ROVP1	30k Ω	MCR03 Series	Rohm
26	ROVP2	360k Ω	MCR03 Series	Rohm
27	RISET	100k Ω	MCR03 Series	Rohm
28	RG1	0 Ω	-	-
29	RG2	(open)	-	-
30	JP1	0 Ω	-	-
31	JP2	(open)	-	-
32	JP3	0 Ω	-	-
33	JP4	0 Ω	-	-
34	JP5	(open)	-	-

Application Board Circuit

When using it as Boost DC/DC converter

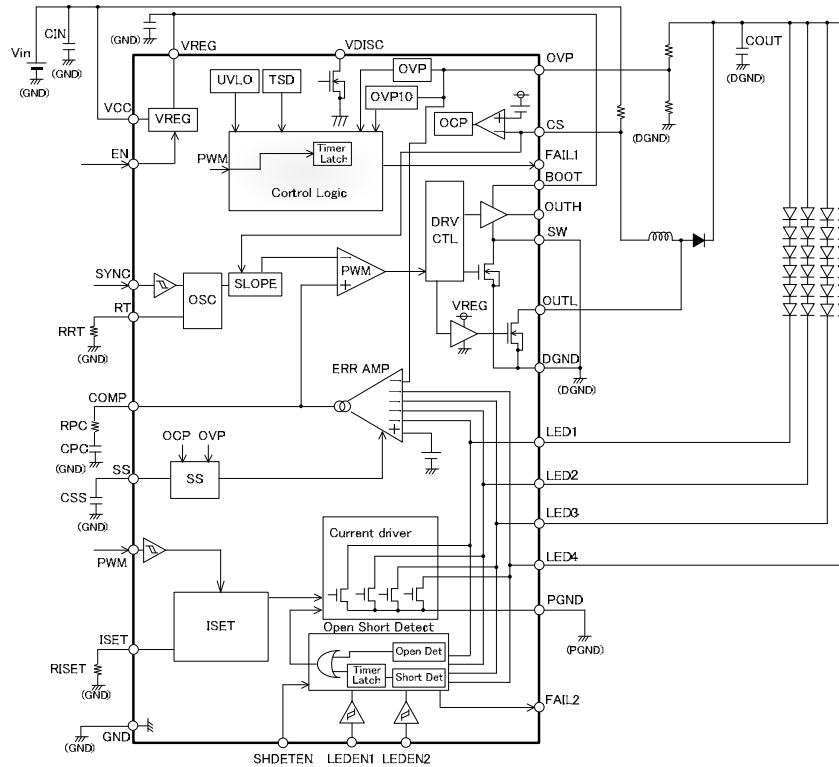


Figure 35. Boost application circuit

Note: When using as boost DC/DC converter, if the V_{OUT} and LED terminal are shorted, the over-current from V_{IN} cannot be prevented. To prevent overcurrent, carry out measure such as inserting fuse in between V_{CC} and R_{CS} . In case there is a current capacity towards each input terminal of EN, PWM, LEDEN1, LEDEN2, SYNC, please insert a limit resistance in between each terminals.

When using it as Buck DC/DC Converter

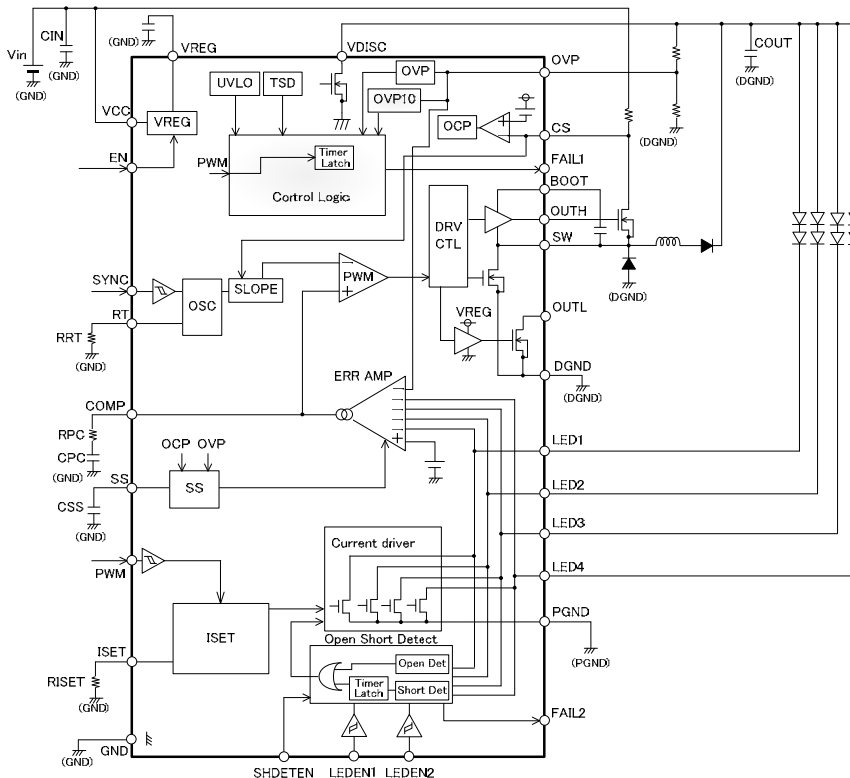


Figure 36. Buck application circuit

Additional parts for EMC

1. This part adjusts "Slew Rate" of high side FET. (Parts ex. R=MCR03 series 4.7 Ω)
2. This part decreases noise of current loop of high side FET. (Parts ex. C=0.01uF//1000pF)
3. This part decreases spectrum of high frequency on power line. (Parts ex. C=0.01uF//1000pF)
4. This low Pass Filter decreases noise of power line. (Parts ex. L=6.8uF, C=10uF)
5. This common mode filter decreases noise of power line. (Parts ex. CMF=ACM70V, C=0.1uF//0.01uF)
6. This chip beas decreases ringing of switching for low side FET. (Parts ex. MPZ2012S101A)
7. This snubber circuit decreases spectrum of high frequency of low side FET. (Parts ex. R=MCR10 series 10 Ω , C=100pF)
8. This snubber circuit decreases ringing of switching for low side FET. (Parts ex. R=MCR10 series 10 Ω , C=100pF)

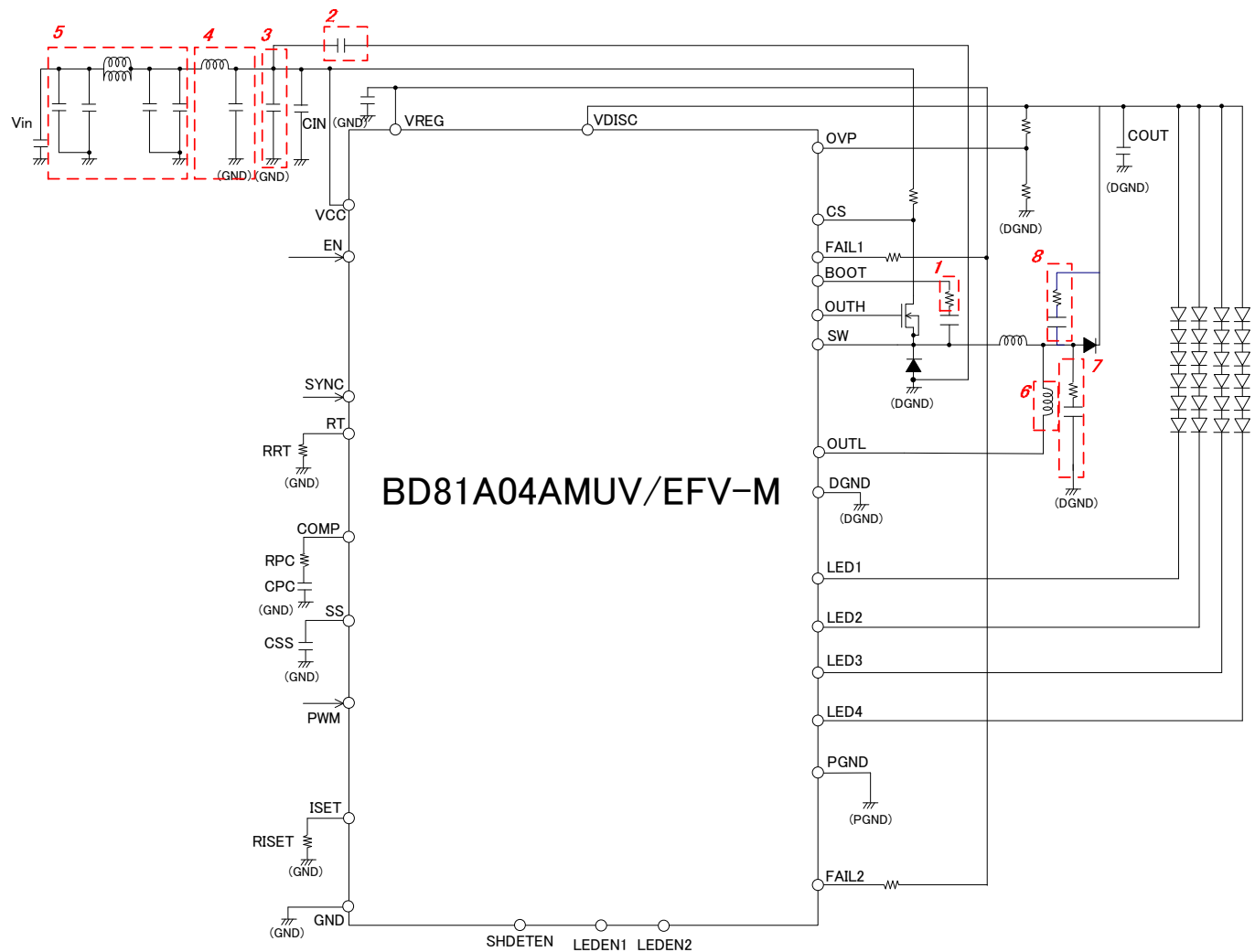


Figure 37. Application parts for EMC

Attention Point for PCB Layout

The layout pattern influences characteristic, such as efficiency and a ripple greatly. So, it is necessary to examine carefully about it.

Boost DC/DC has "Loop1" (in Figure 38). Placement of these parts should be compact. And wiring should be low-impedance (e.g. Cout's GND and DGND should be very near).

Also, Back-Boost DC/DC has "Loop2". Placement of these parts and wiring should be compact and low-impedance (e.g. Cin's GND and D1's GND should be very near).

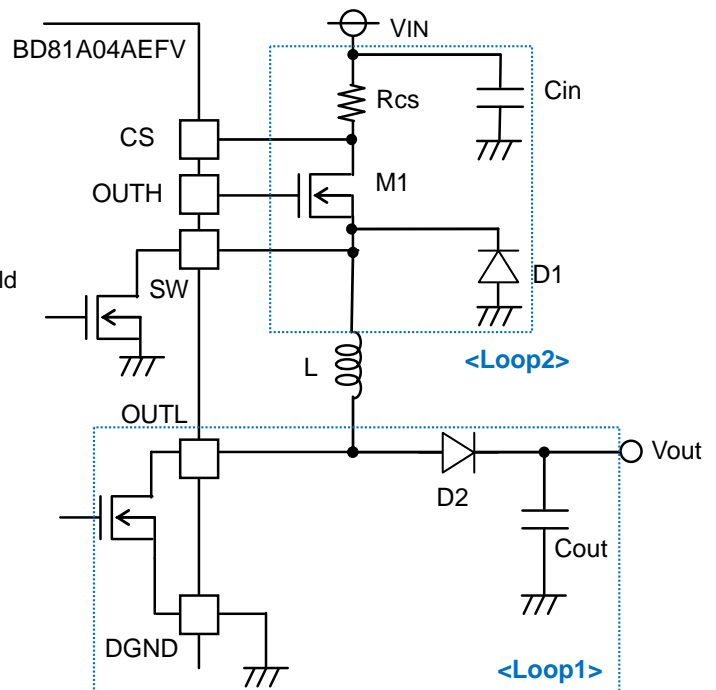


Figure 38. circuit of DC/DC block

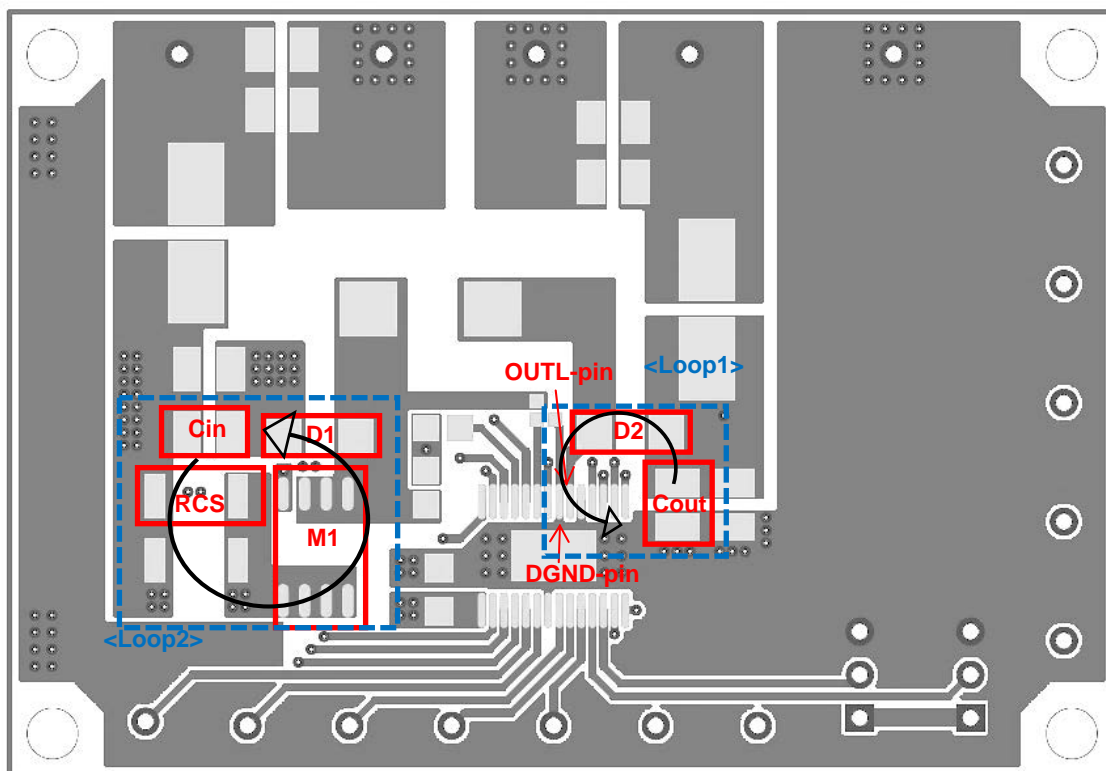


Figure 39. BD81A04AEFV PCB TOP-layer

Calculation of Power Consumption

$$\begin{aligned}
 P_c &= I_{CC} \times V_{CC} \\
 &+ C_{ISS1} \times V_{REG} \times F_{SW} \times V_{REG} \\
 &+ C_{ISS2} \times V_{REG} \times F_{SW} \times V_{REG} \\
 &+ \{ V_{LED} \times M + \Delta V_F \times (M-1) \} \times I_{LED} \\
 &+ R_{ONFET} \times I_{FET} \times I_{FET}
 \end{aligned}$$

- • • ① Circuit Power
- • • ② Boost FET(Built-In) Drive Step Power
- • • ③ Buck FET(Externally installed) Drive Step Power
- • • ④ Current Driver Power
- • • ⑤ Built-In FET Power

$$I_{L_AVG} = (V_{CC} + V_{OUT}) / V_{CC} \times I_{OUT} / n$$

$$I_{FET} = I_{L_AVG} \times V_{OUT} / (V_{CC} + V_{OUT})$$

$$I_{OUT} = I_{LED} \times 1.03 \times M$$

$$V_{OUT} = (V_F + \Delta V_F) \times N + V_{LED}$$

- • • ⑥ Inductance Average Current
- • • ⑦ Current Flowing Through Boost FET(Built-In)
- • • ⑧ LED Output Current
- • • ⑨ DC/DC Output Voltage

P _c [W]	: IC Power Consumption	I _{CC} [A]	: Max Circuit Current	V _{CC} [V]	: Power Supply Voltage
C _{ISS1} [F]	: Boost FET Gate Capacitance	C _{ISS2} [F]	: Buck FET Gate Capacity	V _{REG} [V]	: V _{REG} Voltage
F _{SW} [Hz]	: Switching Frequency	V _{LED} [V]	: LED Control Voltage	I _{LED} [A]	: LED Output Current
N	: Number of LED in series	M	: Number of LED series in Parallel	V _F [V]	: LED Forward Voltage
ΔV _F [V]	: LED V _F difference	R _{ONFET} [Ω]	: Boost FET ON- Resistance	η	: Efficiency

< Sample Calculation > I_{CC}=10mA, V_{CC}=12V, C_{ISS1}=65pF, C_{ISS2}=2000pF, V_{REG}=5V, F_{SW}=2200kHz, V_{LED}=1V, I_{LED}=50mA, N=7series, M=4channel,

If V_F=3.5V, ΔV_F=0.5V, R_{ONFET}=1.15Ω, η=80%

$$V_{OUT} = (3.5V + 0.5V) \times 7series + 1V = 29V$$

$$I_{OUT} = 50mA \times 1.03 \times 4channel = 0.206A$$

$$I_{L_AVG} = (12 + 29V) / 12V \times 0.206A / 0.8 = 0.88A$$

$$I_{FET} = 0.88A \times 29V / (12V + 29V) = 0.622A$$

$$\begin{aligned}
 P_c(4) = & 10mA \times 12V + 65pF \times 5V \times 2200kHz \times 5V + 2000pF \times 5V \times 2200kHz \times 5V + \\
 & \{ 1.0V \times 4 + 0.5V \times (4-1) \} \times 50mA + 1.15\Omega \times 0.622A \times 0.622A = 0.953[W] \text{ will be the result.}
 \end{aligned}$$

The above mentioned is a simple calculation and sometimes the value may differ from the actual value.

I/O Equivalent Circuit

2.SS 	3.COMP 	4.RT
5.SYNC,6.SHDETEN,8.PWM,11.LEDEN1,12.LEDEN2 		9.FAIL1,10.FAIL2
13~16. LED1~4 	17.OVP 	18.ISET
20.OUTL 	22.VDISC 	23.SW
24.OUTH 	25.BOOT 	26.VREG
27.EN 	28.CS 	

All values will become Typ value.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. GND Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding Input Pins of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

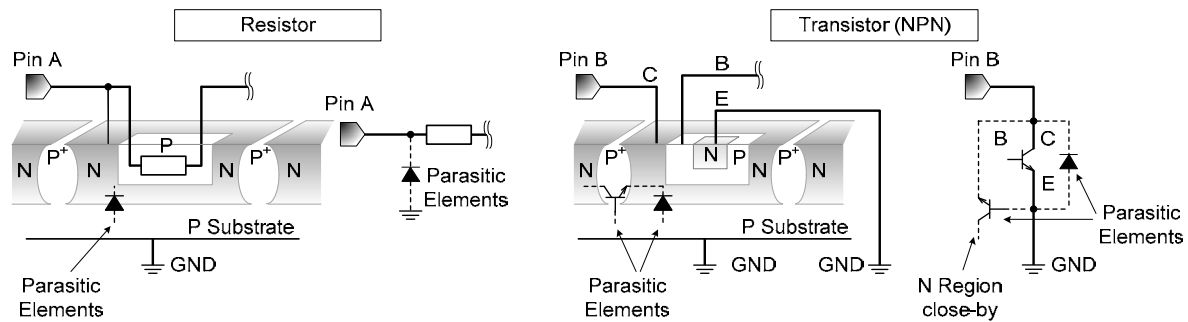


Figure 40. Parasitic Element

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

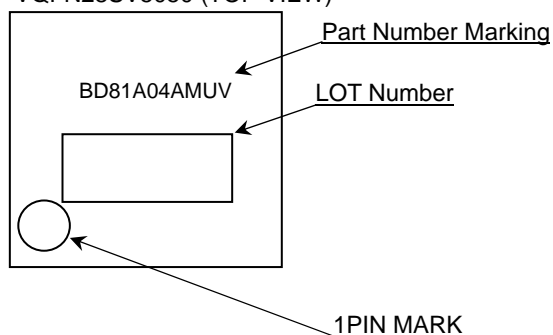
Ordering Information

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Package MUV:VQFN28SV5050		Packaging M: High Reliability Design E2: Reeled, embossed taping (VQFN28SV5050)

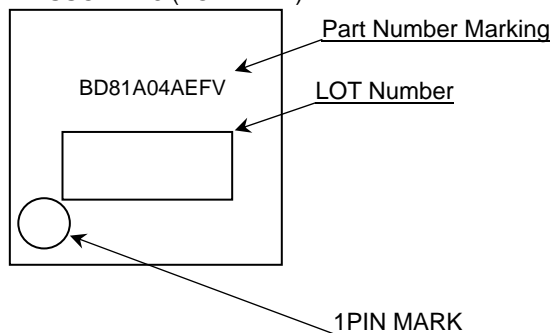
B D 8 1 A 0 4 A E F V	-	ME2
Package EFV:HTSSOP-B28		Packaging M: High Reliability Design E2: Reeled, embossed taping (HTSSOP-B28)

Marking Diagram

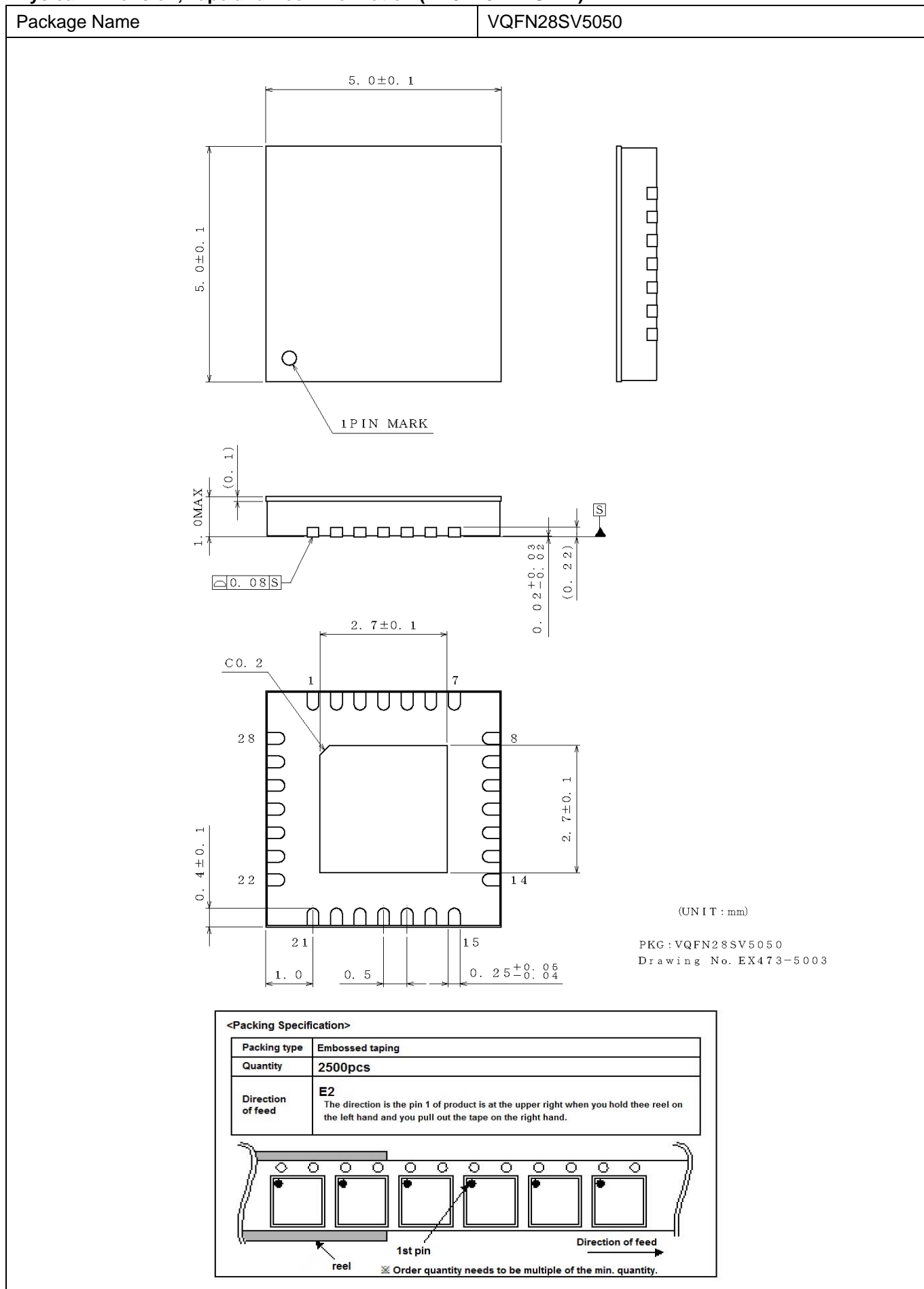
VQFN28SV5050 (TOP VIEW)



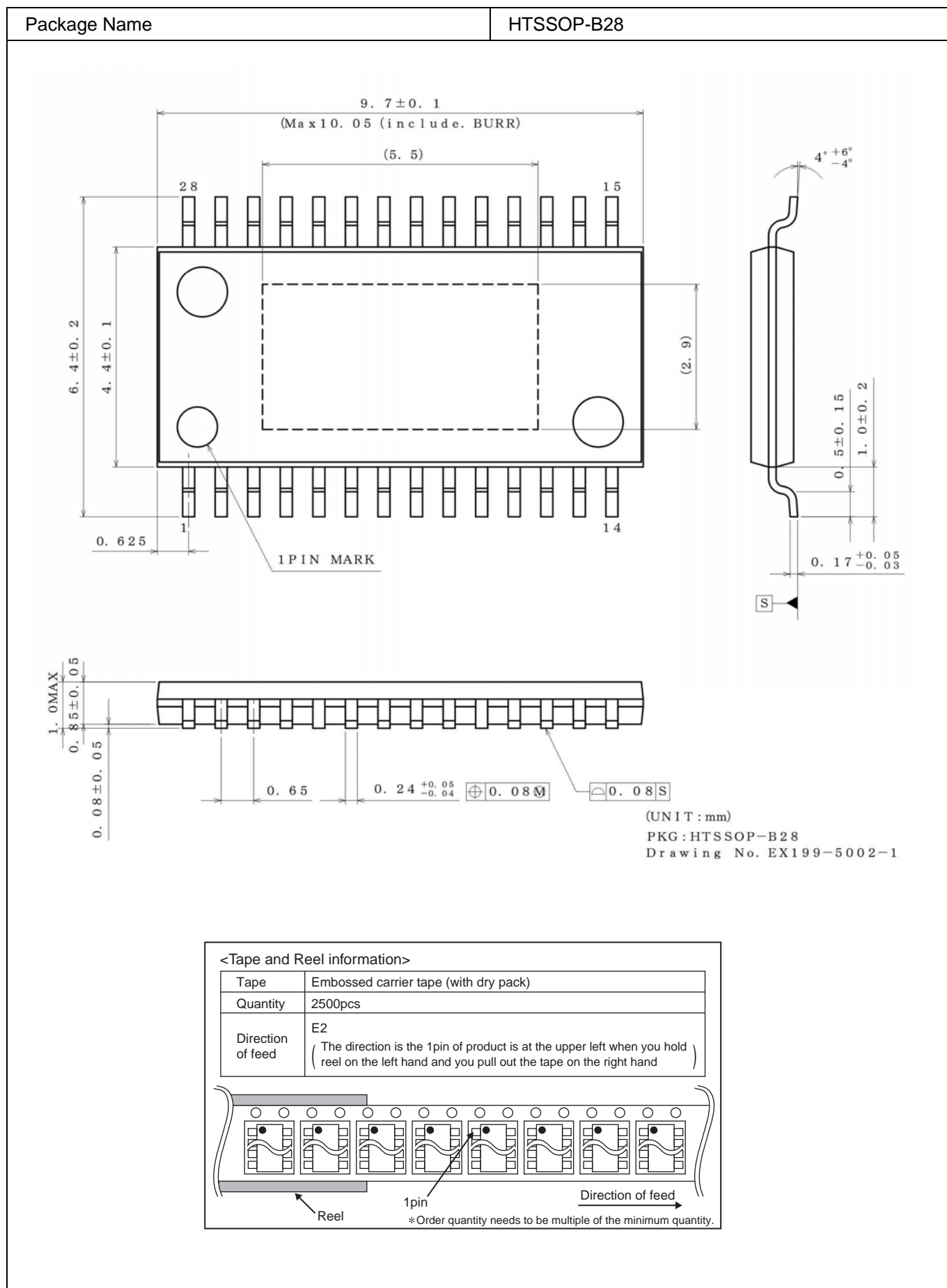
HTSSOP-B28 (TOP VIEW)



Physical Dimension, Tape and Reel Information (BD81A04AMUV-M)



Physical Dimension, Tape and Reel Information (BD81A04AEFV-M)



Revision History

Date	Revision	Changes
22.Oct.2013	002	New Release.
4.Dec.2013	003	P.1 Add "AEC-Q100 Qualified".

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 - [f] Sealing or coating our Products with resin or other coating materials
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 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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