Datasheet

Power Supply IC Series for TFT-LCD Panels

Gamma voltage generated IC with built-in DAC

BD81010MUV

General Description

The feature of gamma voltage generated IC BD81010MUV provides a single-chip solution with a high-precision 10-bit DAC setting controlled by I^2C serial communications interface, a buffer amp (14ch), and a operational amplifier for HVDD (1ch).

Features

- Single-chip Design means Fewer Components
- Built in 10bit DAC (14ch)
- Built in DAC Output Buffer Amplifier (14ch)
- Built in Operation Amplifier (1ch) for HVDD
- I^2C Interface (SDA, SCL)
- Thermal Shutdown Circuit
- Under-voltage Lockout Protection Circuit
- Power ON Reset Circuit
- Input Tolerant (SDA, SCL, EN)

Applications

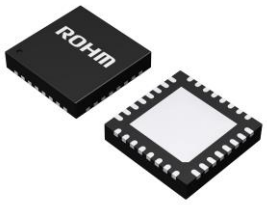
It may be used with TFT-LCD panels, such as big screen and high resolution LCD televisions.

Key Specifications

- Power Supply Voltage Range(VDD): 2.1V to 3.6V
- Power Supply Voltage Range(VCC): 8.0V to 18.0V
- Operating Temperature Range: -40°C to +85°C

Package

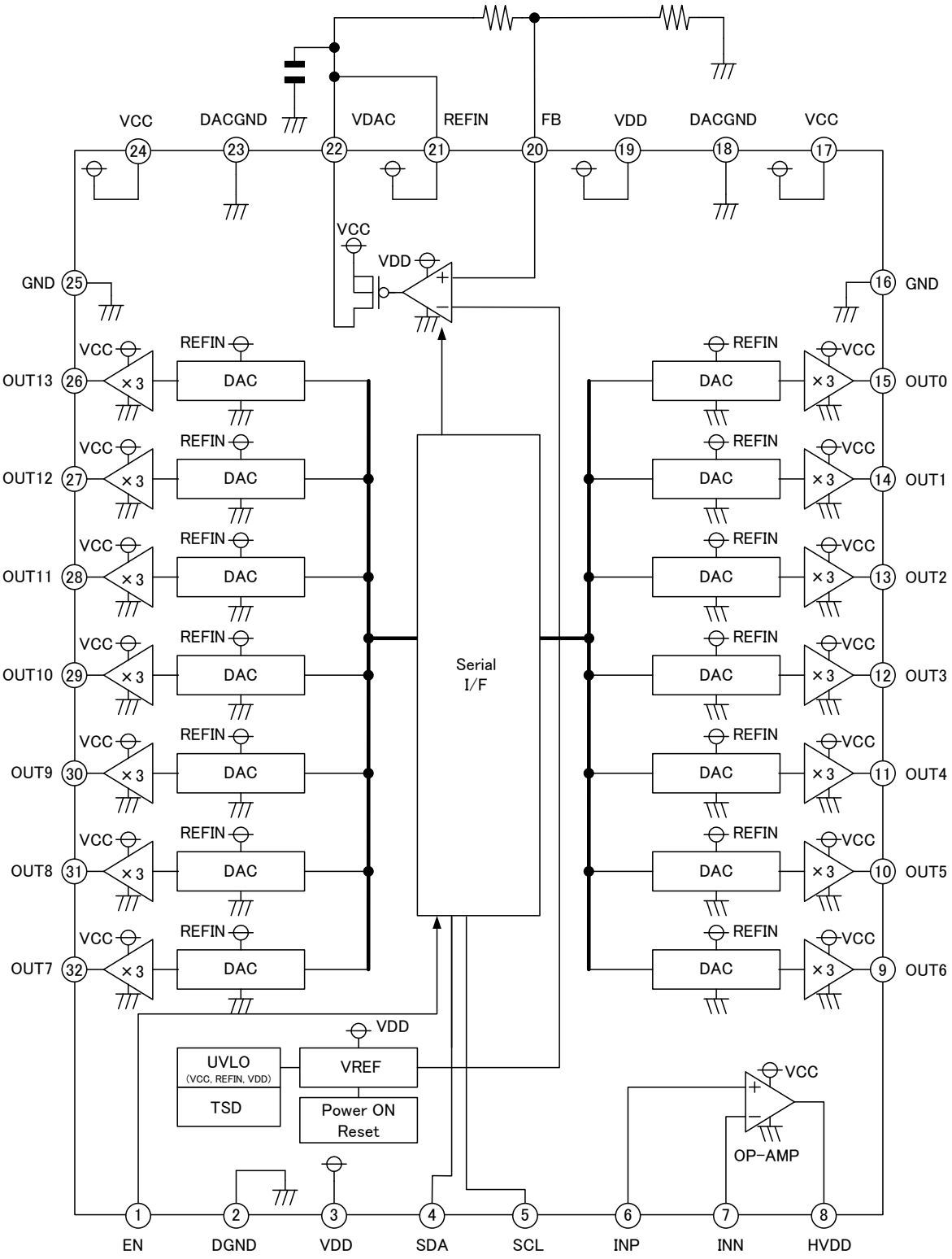
W(Typ) x D(Typ) x H(Max)



VQFN032V5050
5.00mm x 5.00mm x 1.00mm

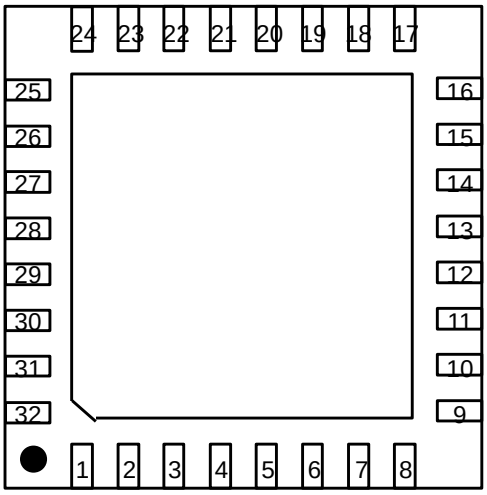
○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Block Diagram



Pin Configuration

TOP VIEW



Pin Description

PIN No.	Pin name	Function	PIN No.	Pin name	Function
1	EN	VDAC enable pin	17	VCC	Power supply input
2	DGND	Logic , Protection circuit GND input	18	DACGND	GND input for DAC
3	VDD	Logic power supply input	19	VDD	Logic power supply input
4	SDA	Serial data input pin	20	FB	Feedback pin
5	SCL	Serial clock input pin	21	REFIN	DAC reference voltage input pin
6	INP	Amplifier + input pin	22	VDAC	DAC voltage output
7	INN	Amplifier – input pin	23	DACGND	GND input for DAC
8	HVDD	HVDD amplifier output pin	24	VCC	Power supply input
9	OUT6	Gamma output pin	25	GND	Buffer amplifier GND input
10	OUT5	Gamma output pin	26	OUT13	Gamma output pin
11	OUT4	Gamma output pin	27	OUT12	Gamma output pin
12	OUT3	Gamma output pin	28	OUT11	Gamma output pin
13	OUT2	Gamma output pin	29	OUT10	Gamma output pin
14	OUT1	Gamma output pin	30	OUT9	Gamma output pin
15	OUT0	Gamma output pin	31	OUT8	Gamma output pin
16	GND	Buffer amplifier GND input	32	OUT7	Gamma output pin

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage 1	V_{DD}	4.5	V
Power Supply Voltage 2	V_{CC}	19.0	V
REFIN Voltage	V_{REFIN}	7.0	V
DAC Reference Voltage	V_{DAC}	7.0	V
OP. Amplifier Input Pin Voltage	V_{INP}, V_{INN}	15.0	V
Functional Pin Voltage	V_{EN}	4.5	V
2 Lines Serial Terminal Voltage	V_{SDA}, V_{SCL}	4.5	V
Junction Temperature	Tjmax	150	°C
Power Dissipation	Pd	4.56 (Note 1)	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) To use the IC at temperatures over Ta=25°C, derate power rating by 27.4mW/°C.
When mounted on a four-layer glass epoxy board measuring 74.2mm x 74.2mm x 1.6mm.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +85°C)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage 1	V_{DD}	2.1	3.6	V
Power Supply Voltage 2	V_{CC}	8.0	18.0	V
REFIN Voltage	V_{REFIN}	2.1	5.5	V
DAC Reference Voltage	V_{DAC}	2.1	5.5	V
OP. Amplifier Input Pin Voltage	V_{INP}, V_{INN} (< VCCH - 2.5[V])	0.0	14.0	V
Function Terminal Voltage	V_{EN}	-0.1	+3.6	V
2 Lines Serial Terminal Voltage	V_{SDA}, V_{SCL}	-0.1	+3.6	V
2 Lines Serial Frequency	f_{CLK}	-	400	kHz
VDAC Output Capacity	C_{VDAC}	1.0	-	µF

Electrical Characteristics (Unless otherwise noted, Ta=25°C, V_{DD}=3.3V, V_{CC}=15.0V, V_{REFIN}=5.0V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【 Regulator (VDAC) 】						
FB Voltage	V_{FB}	0.492	0.500	0.508	V	
Input Bias Current	I_{FB}	-1.2	0.0	1.2	µA	V_{FB}=0.60V
Current Capability	I_O	10	50	-	mA	
【 Gamma Amplifier 】						
Sink Current Capability Nch Side (AMP0)	IooA	-	-10.0	-6.6	mA	during REG0=3BBh (14.0V) setting, OUT0=15V input
Sink Current Capability Nch Side (AMP1 to AMP12)	IooB	-	-30	-20	mA	during REG1 to REG12=199h (6.0V) setting, OUT1to OUT12=7V input
Sink Current Capability Nch Side (AMP13)	IooC	-	-60	-40	mA	during REG13=043h (1.0V) setting, OUT13=2V input
Source Current Capability Pch Side (AMP0)	IoiA	40	60	-	mA	during REG0=3BBh (14.0V) setting, OUT0=13V input
Source Current Capability Pch Side (AMP1 to AMP12)	IoiB	20	30	-	mA	during REG1 to REG12=199h (6.0V) setting, OUT1to OUT12=5V
Source Current Capability Pch Side (AMP13)	IoiC	6.6	10.0	-	mA	during REG13=043h (1.0V) setting, OUT13=0V input
Load Stability (OUT0)	⊿VO-A	-	10	70	mV	I_O=0mA to -30mA REG0=199h (6.0V) setting
Load Stability (OUT1 to OUT12)	⊿VO-B	-	10	70	mV	I_O=-15mA to 15mA REG1 to REG12=199h (6.0V) setting
Load Stability (OUT13)	⊿VO-C	-	10	70	mV	I_O=0mA to 30mA REG13=199h (6.0V) setting
MAX Output Voltage (OUT0)	VOH-A	V_{CC}-0.20	V_{CC}-0.10	-	V	I_O=-30mA
MAX Output Voltage (OUT1 to OUT12)	VOH-B	V_{CC}-1.00	V_{CC}-0.50	-	V	I_O=-15mA
MAX Output Voltage (OUT13)	VOH-C	V_{CC}-0.60	V_{CC}-0.30	-	V	I_O=-5mA
MIN Output Voltage (OUT0)	VOL-A	-	0.30	0.60	V	I_O=5mA
MIN Output Voltage (OUT1 to OUT12)	VOL-B	-	0.60	1.20	V	I_O=15mA
MIN Output Voltage (OUT13)	VOL-C	-	0.10	0.20	V	I_O=30mA
Slew Rate (AMP0)	SR-A	1	4	-	V/µsec	OUT0=No-load
Slew Rate (AMP1 to OUT12)	SR-B	1	4	-	V/µsec	OUT1 to OUT12= No-load
Slew Rate (AMP13)	SR-C	1	4	-	V/µsec	OUT13= No-load
【 10 Bit DAC 】						
Resolution	RES	-	10	-	Bit	
Integral Non-linearity Error (INL)	LE	-2	-	+2	LSB	00Ah to 3F5h is the allowable margin of error against the ideal linear.
Differential Non-linearity Error (DNL)	DLE	-2	-	+2	LSB	00Ah to 3F5h is the allowable margin of error against the ideal increase of 1LSB.

Electrical Characteristics – continued (Unless otherwise noted, Ta=25°C, V_{DD}=3.3V, V_{CC}=15.0V, V_{REFIN}=5.0V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【 Control Signal 1 (EN) 】						
Threshold Voltage 1	V_{ENth1}	0.8	-	1.7	V	
Threshold Voltage 2	V_{ENth2}	0.6	-	1.7	V	V_{DD}=2.5V
Input Sinking Current	I_{EN}	10.0	16.5	23.1	µA	V_{EN}=3.3V
【 Control Signal 2 (SDA, SCL) 】						
Threshold Voltage 1	V_{th1}	0.8	-	1.7	V	
Threshold Voltage 2	V_{th2}	0.6	-	1.7	V	V_{DD}=2.5V
MIN Output Voltage	V_{OCL}	-	-	0.4	V	I_{SDA}=3mA
【 Operation Amplifier 】						
Input Offset Voltage	V_{OFF-HV}	-15	-	+15	mV	
Input Bias Current	I_{B-HV}	-1.2	0.0	+1.2	µA	
Sink Current Capability (Nch side)	I_{ooHV}	-	-100	-66	mA	during V_{INP} = 7V, INN = HVDD setting, V_{HVDD}=8V input
Source Current Capability (Pch side)	I_{oiHV}	66	100	-	mA	during V_{INP} = 7V, INN = HVDD setting, V_{HVDD}=6V input
Load Stability	⊿VO-HV	-	10	70	mV	V_{INP} = 7V, INN = HVDD setting I_O=-50mA to +50mA
MAX Output Voltage	V_{OH-HV}	V_{CC}-0.20	V_{CC}-0.10	-	V	I_O=-30mA
MIN Output Voltage	V_{OL-HV}	-	0.10	0.20	V	I_O=30mA
Slew Rate	SRHV	1	4	-	V/µsec	HVDD=No-load
【 Whole Device 】						
VDD under-voltage Protection Voltage	V_{DDUV}	1.7	1.9	2.1	V	VDD falling voltage
VDD under-voltage Protection Hysteresis Voltage	V_{DDHY}	-	100	-	mV	
VCC under-voltage Protection Voltage	V_{CCUV}	2.3	2.6	2.9	V	VCC falling voltage
VCC under-voltage Protection Hysteresis Voltage	V_{CCHY}	-	400	-	mV	
REFIN under-voltage Protection Voltage	V_{REFUV}	1.7	1.9	2.1	V	REFIN falling voltage
REFIN under-voltage Protection Hysteresis Voltage	V_{REFHY}	-	100	-	mV	
VDD Circuit Current	I_{CCL}	0.31	0.51	0.71	mA	No-load output, DAC initial value setting
VCC Circuit Current	I_{CCH}	4.4	8.6	13.2	mA	No-load output, DAC initial value setting

Operation of each block

(1) Regulator (VDAC)

This is a regulator block for setting a reference voltage of DAC.

VDAC has enable function so that if EN=Low, shut down is performed, or EN=High, settable VDAC voltage by FB voltage and external resistor. At this time, VDAC voltage < 5.5[V] (MAX operating voltage) should be configured.

VDAC output capacity (C11) is set over 1[µF].

Phase compensation (C12) is able to use as OPEN, but it is recommended to set the PCB pattern.

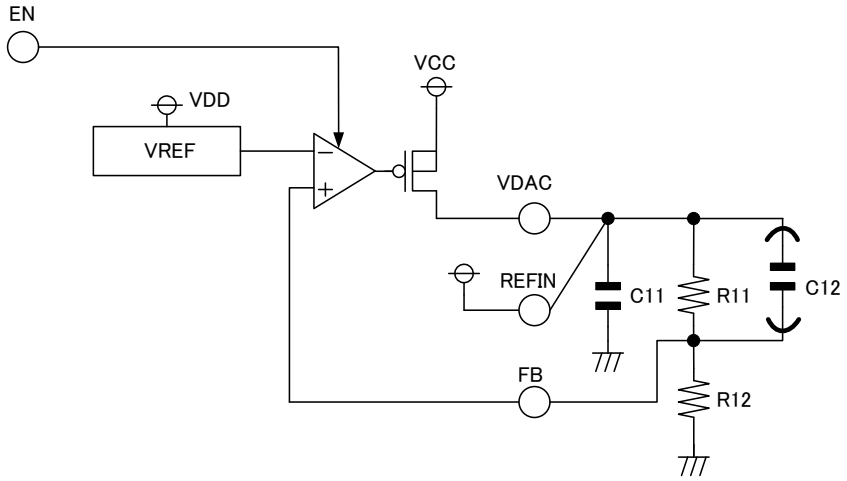


Figure 1. Regulator block

$$VDAC = 0.50 \times \frac{R11 + R12}{R12} \quad [V]$$

Example) In case R11=18[kΩ], R12=2 [kΩ], VDAC equals to 5.0[V].

10[kΩ] to 100[kΩ] is a recommended range for the sum of setting value of R11,R12. If the setting is below 10[kΩ], consumption current may increase, thus resulting in degraded power efficiency. If the setting exceeds 100[kΩ], offset voltage is likely increase due to the input bias current.

(2) 10 Bit DAC Block

・Serial data control block

The serial interface uses a 2-line serial data format (SCL, SDA).

The serial data control block consists of a register that stores data from the SDA and SCL pins, and a DAC circuit that receives the output from this register and provides adjusted voltages to other IC blocks.

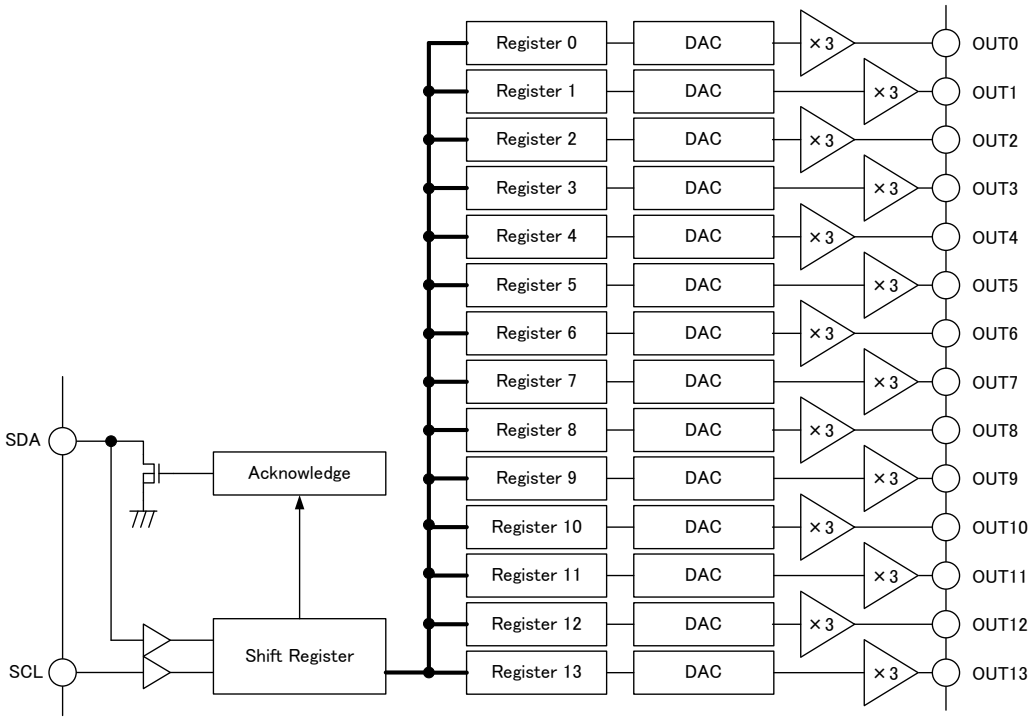


Figure 2. Serial Block Diagram

・Register (Ch0 to Ch13)

A serial signal (consisting of 10-bit gamma correction voltage values) input using the serial interface or I^2C bus interface is held for each register address.

Data is initialized by the reset signal generated during a power-on reset.

・DAC

The DAC LOGIC converts the 10-bit digital signal read to the register to a voltage.

・Amp (Ch0 to Ch13)

The Amp amplifies the voltage output from the DAC LOGIC by 3 times.

While Under Voltage Lock-Out (UVLO) circuit or Thermal Shut Down (TSD) circuit is operating, output goes into Hi-z.

In case connecting high capacity capacitor with low ESR, damping is needed with a resistor to keep phase margin.

・Output Voltage setting mode

Writes to a register address specified by I^{2}C BUS.

Mode for writing from I^{2}C BUS to register are (i)Single mode and (ii)Multi mode.

On single mode, write data to one designated register.

On multi mode, multi data write can be performed continuously from a start address register specified with the second byte of data.

Single mode or multi mode can be configured by having or not having “stop bit”.

(i) Single mode timing chart

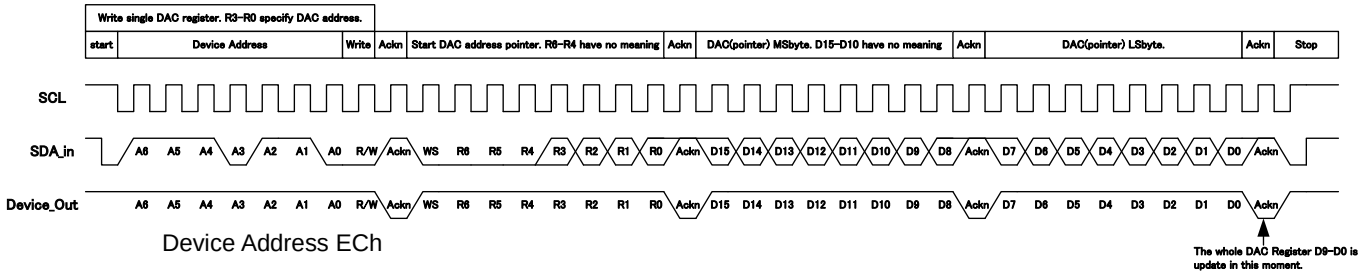


Figure 3. Output Voltage Setting (Single mode)

(ii) Multi mode timing chart

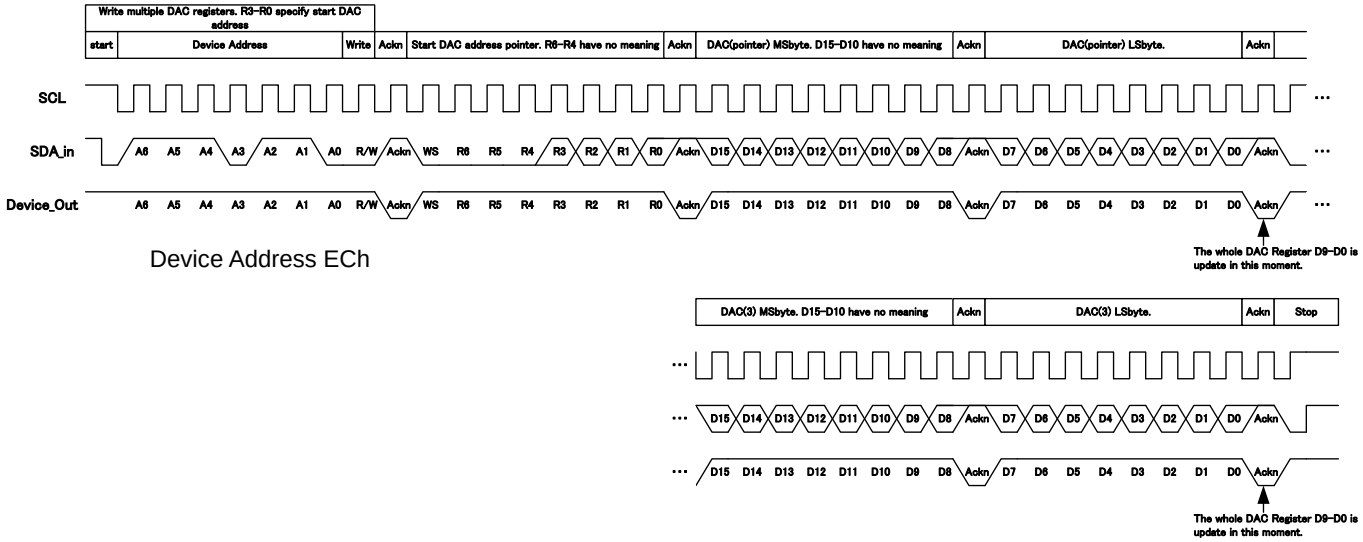


Figure 4. Output Voltage Setting (Multi mode)

・Device address

Device addresses A6 to A0 are specific to the IC and should be set as follows: (A6 to A0) = 1110110.

The lower 4 bits (R3 to R0) of the second byte are used to store the register address.

R6 to R4 should be set to 0 as usual.

・Command interface

Use I²C BUS for command interface with host. Writing or reading by specifying 1 byte select address, along with slave address. I²C BUS Slave mode format is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	DATA	A	P

S : Start condition

Slave Address : After slave mode(7bit), with read mode (H) or light mode (L), send 8 bit data in all. (MSB first)）

A : Acknowledge

Added acknowledge bit per byte in sending and receiving data.

If the data is sent/ received properly, “L” is send/ received.

Sending/ Receiving ”H” means lack of acknowledge.

Select Address : Use 1 byte select address.

DATA : Data byte. Sending/ Receiving data. （MSB first）.

P : Stop condition

The case where writing 3FCh to DAC1（Single mode）

S	Slave Address	A	Select Address	A	Register1 DATA0	A	Register1 DATA1	A	P
(Ex.)	ECh		01h		03h		FCh		

: Slave from master : Master from slave

The case where writing 3FCh from DAC0 to DAC3 (Multi mode)

S	Slave Address	A	Select Address	A	Register0 DATA0	A	Register0 DATA1	A	Register1 DATA0	A	Register1 to 3 DATA0,DATA1	A	P
(Ex.)	ECh		00h		03h		FCh		03h				

: Slave from master : Master from slave

・DAC register address diagram

Register Address				Register name		BIT								Initial value	Output pin
R3	R2	R1	R0			7	6	5	4	3	2	1	0		
0	0	0	0	Register 0	DATA0	X	X	X	X	X	X	D9	D8	03BBh	OUT0
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	1	Register 1	DATA0	X	X	X	X	X	X	D9	D8	0376h	OUT1
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	1	0	Register 2	DATA0	X	X	X	X	X	X	D9	D8	0332h	OUT2
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	1	1	Register 3	DATA0	X	X	X	X	X	X	D9	D8	02EEh	OUT3
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	0	0	Register 4	DATA0	X	X	X	X	X	X	D9	D8	02AAh	OUT4
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	0	1	Register 5	DATA0	X	X	X	X	X	X	D9	D8	0265h	OUT5
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	1	0	Register 6	DATA0	X	X	X	X	X	X	D9	D8	0221h	OUT6
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	1	1	Register 7	DATA0	X	X	X	X	X	X	D9	D8	01DDh	OUT7
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	0	0	0	Register 8	DATA0	X	X	X	X	X	X	D9	D8	0199h	OUT8
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	0	0	1	Register 9	DATA0	X	X	X	X	X	X	D9	D8	0154h	OUT9
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	0	1	0	Register 10	DATA0	X	X	X	X	X	X	D9	D8	0110h	OUT10
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	0	1	1	Register 11	DATA0	X	X	X	X	X	X	D9	D8	00CCh	OUT11
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	Register 12	DATA0	X	X	X	X	X	X	D9	D8	0088h	OUT12
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	1	Register 13	DATA0	X	X	X	X	X	X	D9	D8	0043h	OUT13
					DATA1	D7	D6	D5	D4	D3	D2	D1	D0		

DATA0：Upper 8 bits, DATA1：Lower 8 bit, X：don’t care, D9 to D0：Data bit

・I²C Timing

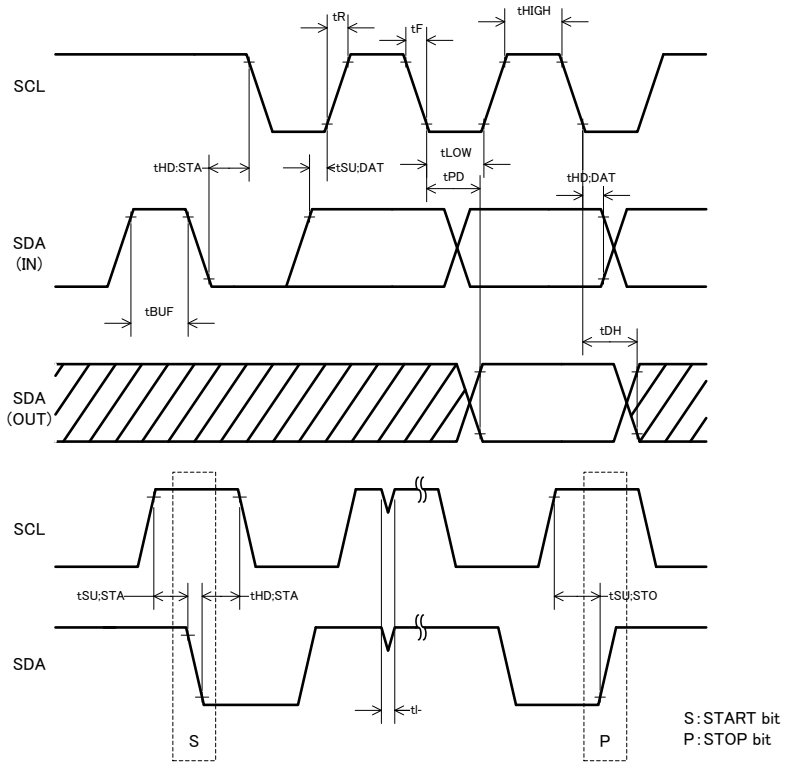


Figure 5. Timing

・Timing regulation

Parameter	Symbol	FAST mode			Unit
		MIN	TYP	MAX	
SCL Frequency	f_{SCL}	-	-	400	kHz
SCL"H" time	t_{HIGH}	0.6	-	-	µs
SCL"L" time	t_{LOW}	1.2	-	-	µs
Rise time	t_R	-	-	0.3	µs
Fall time	t_F	-	-	0.3	µs
Start condition holding time	$t_{HD;STA}$	0.6	-	-	µs
Start condition setup time	$t_{SU;STA}$	0.6	-	-	µs
SDA Holding time	$t_{HD;DAT}$	100	-	-	ns
SDA Setup time	$t_{SU;DAT}$	100	-	-	ns
Acknowledge delay time	t_{PD}	-	-	0.9	µs
Acknowledge holding time	t_{DH}	-	0.1	-	µs
Stop condition setup time	$t_{SU;STO}$	0.6	-	-	µs
BUS open time	t_{BUF}	1.2	-	-	µs
Noise spike width	t_I	-	0.1	-	µs

・Buffer output setting

The relation between buffer output voltage (OUT0 to OUT13) and DAC setting value is shown below.

$$Output\ voltage\ (OUT0\ to\ OUT13) = \frac{DAC\ setting\ value + 1}{1024} \times 3 \times REFIN$$

Buffer output terminals OUT0 to OUT13 output after UVLO release of VCC. While UVLO detection, the output is HiZ.

(3) Operation amplifier for HVDD

If output current ability over ±20mA is needed for DAC output, shown below.

Only using an amplifier, voltage is able to set by resistor, shown below Figure 7.

- For the reference side, use the regulator output type of power supply.
- It is recommended to set the RCOM1,RCOM2 in the range of 10kΩ to 100kΩ.
  Setting them to not more than 10kΩ may increase current consumption, thus resulting in degraded power efficiency.
  Setting them to not less than 100kΩ may result in higher offset voltage due to the input bias current of 0.1μA(TYP).
- In case connecting HVDD with low ESR capacitor, damping is needed with a resistor (R32) to keep phase margin.

Use the buffer type if HVDD is not used, and ground the INP pin.

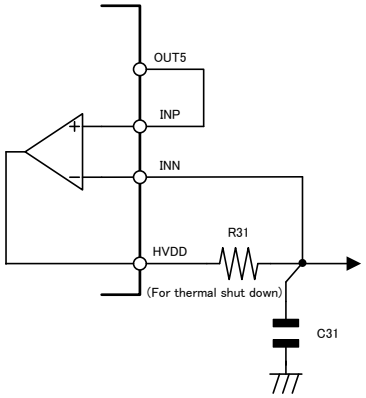


Figure 6. Use as output for DAC

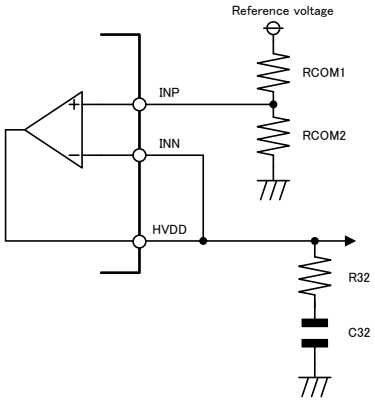


Figure 7. Use amplifier only by having resistor divider

(4) Power On Reset

When the digital power supply VDD is activated, each IC generates a reset digital to initialize the serial I/F and each registers.

(5) UVLO(Under Voltage Lock Out)

Turns output OFF when the voltage of digital power supply VDD, amplifier power supply VCC and DAC reference voltage REFIN goes below the limit value.

(6) TSD(Thermal Shut Down)

The TSD circuit turns output off when the chip temperature reaches or exceeds approximately 175°C in order to prevent thermal destruction or thermal runaway. When the chip returns to a specified temperature, the circuit resets.

The TSD circuit is designed only to protect the IC itself. Application thermal design should ensure operation of the IC below the junction temperature of approximately 150°C.

Sequence image

1. EN=High before VCC power supply turns ON

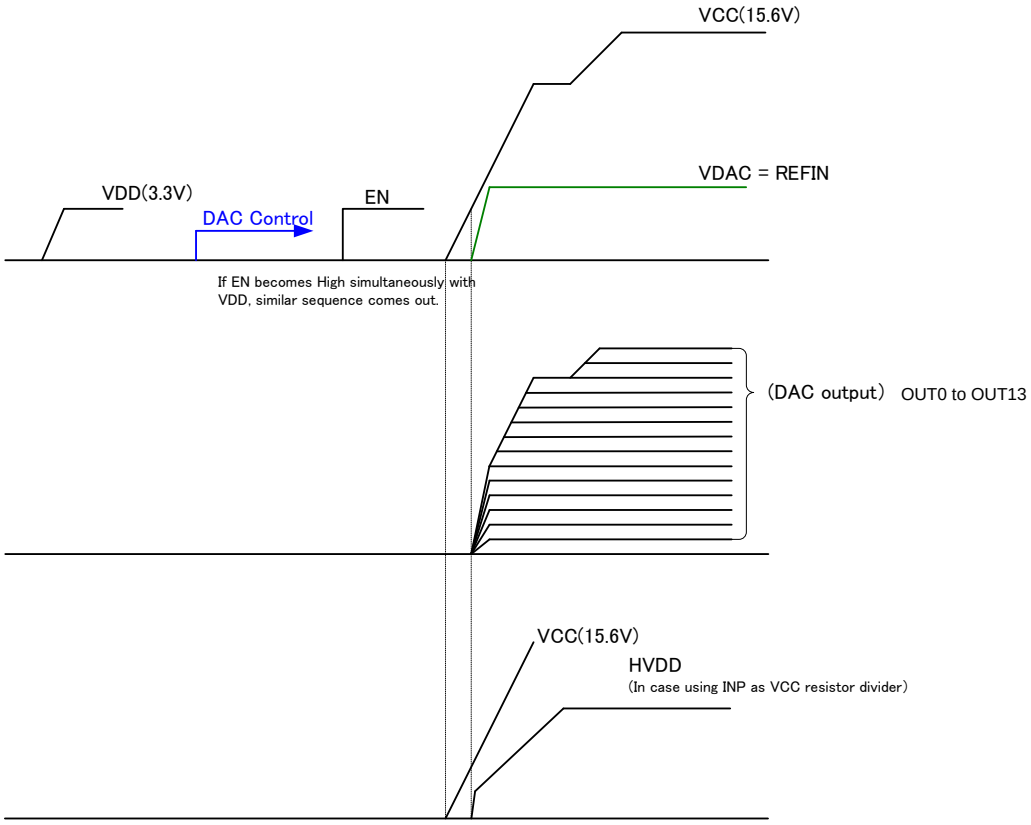


Figure 8. Sequence image 1

2. EN=High after VCC power supply turns ON

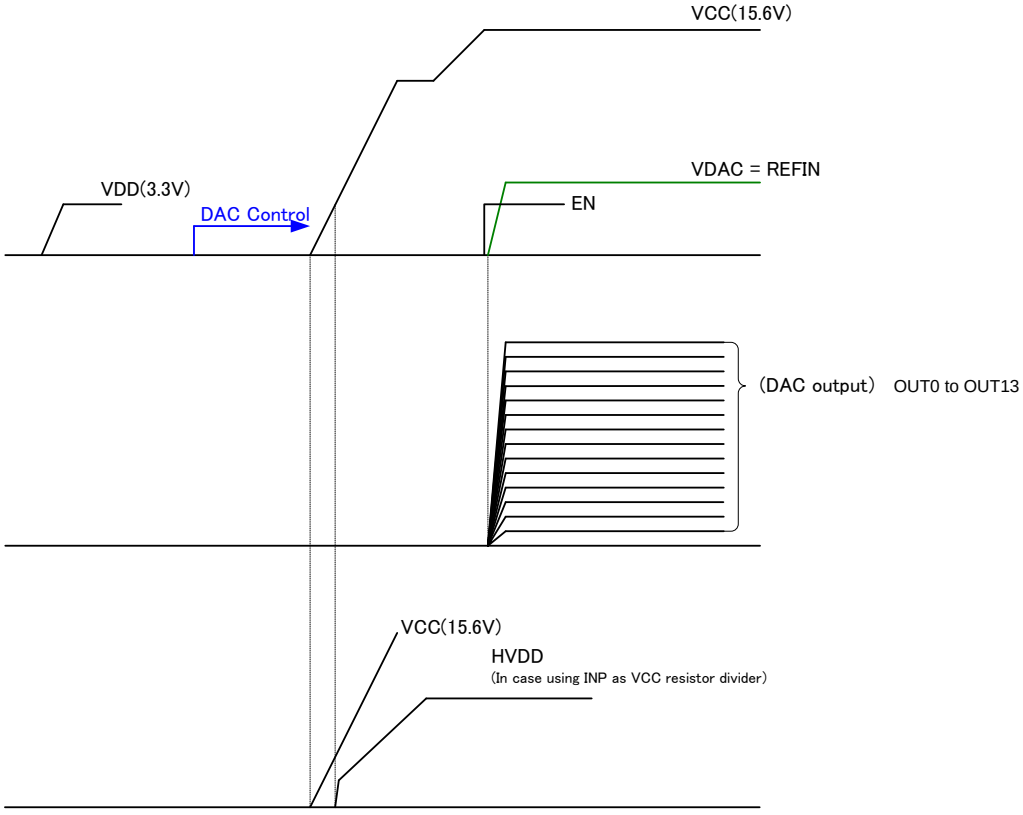


Figure 9. Sequence image 2

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

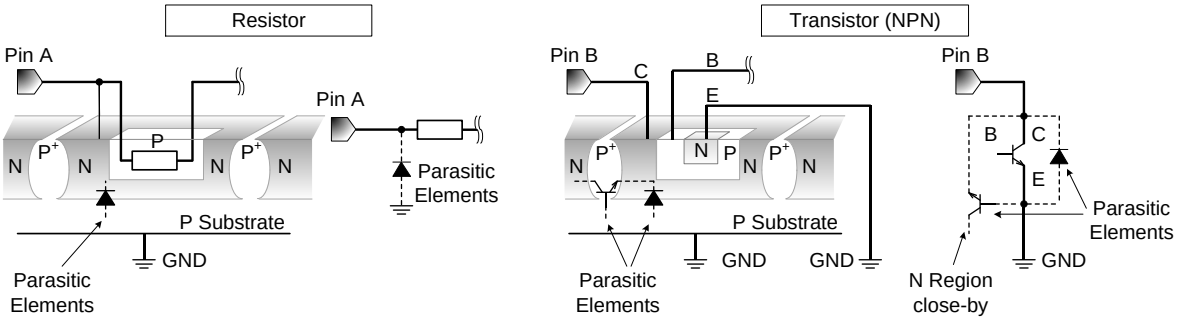


Figure 10. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

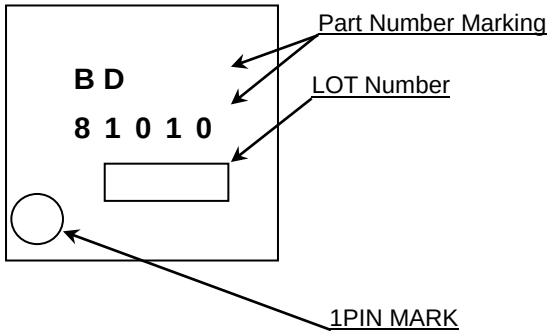
Ordering Information

B D 8 1 0 1 0 M U V	-	E 2

- Part number
- Package
  MUV: VQFN032V5050
- Packaging and forming specification
  E2: Embossed tape and reel

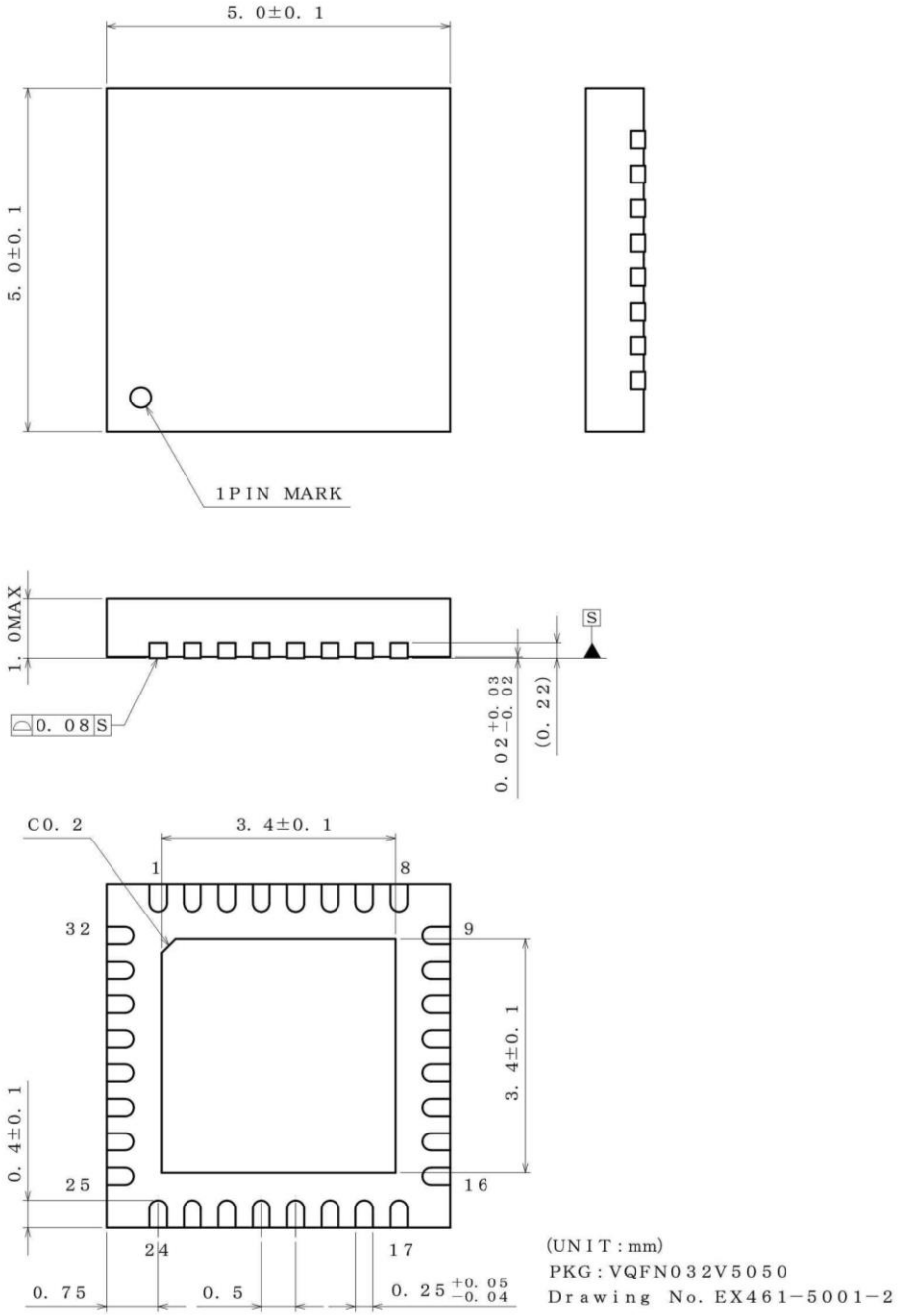
Marking Diagram

VQFN032V5050 (TOP VIEW)



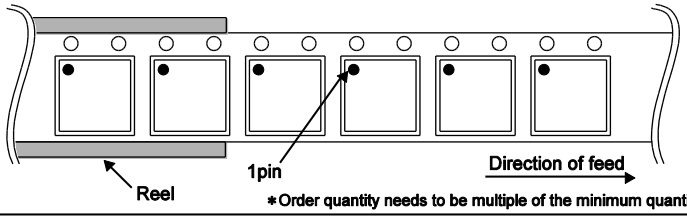
Physical Dimension, Tape and Reel Information

Package Name	VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
19.Feb.2016	001	New Release

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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BD81010MUV - Web Page

Distribution Inventory

Part Number	BD81010MUV
Package	VQFN032V5050
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes