High-performance Regulator IC Series for PCs

Ultra Low Dropout Linear Regulators(4A) for Desktop PC

BD3522EFV, BD35221EFV, BD35222EFV

● Description

BD3522EFV / BD35221EFV / BD35222EFV ultra low-dropout linear chipset regulator operates from a very low input supply, and offers ideal performance in low input voltage to low output voltage applications. It incorporates a built-in N-MOSFET power transistor to minimize the input-to-output voltage differential to the ON resistance (R_{ON}=50mΩ) level. By lowering the dropout voltage in this way, the regulator realizes high current output (Io_{max}=4.0A) with reduced conversion loss, and thereby obviates the switching regulator and its power transistor, choke coil, and rectifier diode. Thus, BD3522EFV / BD35221EFV / BD35222EFV designed to enable significant package profile downsizing and cost reduction. In BD3522EFV, an external resistor allows the entire range of output voltage configurations between 0.65 and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to whatever power supply sequence is required.

● Features

1) Internal high-precision reference voltage circuit(0.65V±1%)
2) Internal high-precision output voltage circuit <BD35221EFV/BD35222EFV>
3) Built-in VCC undervoltage lockout circuit (VCC=3.80V)
4) NRCS (soft start) function reduces the magnitude of in-rush current
5) Internal Nch MOSFET driver offers low ON resistance (28mΩ typ)
6) Built-in short circuit protection (SCP)
7) Built-in current limit circuit (4.0A min)
8) Built-in thermal shutdown (TSD) circuit
9) Variable output (0.65~2.7V) <BD3522EFV>
10) High-power package HTSSOP-B20 : 6.5mm x 6.4mm x 1.0mm
11) Tracking function

● Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

● Line-up

Maximum Output Voltage	Package	Product name
Adjustable (0.65~2.7V)		BD3522EFV
1.2V (fixed)	HTSSOP-B20	BD35221EFV
1.5V (fixed)		BD35222EFV

Oct. 2008

●Absolute maximum ratings

Parameter	Symbol	Limit			Unit
		BD3522EFV	BD35221EFV	BD35222EFV	
Input Voltage 1	VCC	6.0 *1			V
Input Voltage 2	VIN	6.0 *1			V
Maximum Output Current	IO	4*1			A
Enable Input Voltage	Ven	6.0			V
Power Dissipation 1	Pd1	1.00 *2			W
Power Dissipation 2	Pd2	1.45 *3			W
Power Dissipation 3	Pd3	2.31 *4			W
Power Dissipation 4	Pd4	3.20 *5			W
Operating Temperature Range	Topr	-10～+100			℃
Storage Temperature Range	Tstg	-55～+125			℃
Maximum Junction Temperature	Tjmax	+150			℃

*1 Should not exceed Pd.
*2 Reduced by 8mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, no copper foil area)
*3 Reduced by 11.6mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 2-layer,
        copper foil area : 15mm×15mm)
*4 Reduced by 18.5mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 2-layer,
        copper foil area : 70mm×70mm)
*5 Reduced by 25.6mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 4-layer,
        copper foil area : 70mm×70mm)

●Operating Voltage(Ta=25℃)

Parameter	Symbol	BD3522EFV		BD35221EFV		BD35222EFV		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Voltage 1	VCC	4.3	5.5	4.3	5.5	4.3	5.5	V
Input Voltage 2	VIN	0.7	VCC-1 *6	1.25	VCC-1 *6	1.55	VCC-1 *6	V
Output Voltage Setting Range	Vo	VFB	2.7	1.2 (fixed)		1.5 (fixed)		V
Enable Input Voltage	Ven	-0.3	5.5	-0.3	5.5	-0.3	5.5	V
NRCS Capacity	CNRCS	0.001	1	0.001	1	0.001	1	μF

*6 VCC and VIN do not have to be implemented in the order listed.

★This product is not designed for use in radioactive environments.

●Electrical Characteristics (Unless otherwise specified, Ta=25℃, VCC=5V, VEN=3V, VIN=1.7V, R1=3.9kΩ, R2=3.3kΩ)
BD3522EFV

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	I_{CC}	-	1.4	2.2	mA	
VCC Shutdown Mode Current	I_{ST}	-	0	10	μA	V_{EN}=0V
Output Voltage	I_O	4.0	-	-	A	
Feedback Voltage 1	$V_{FB}1$	0.643	0.650	0.657	V	
Feedback Voltage 2	$V_{FB}2$	0.637	0.650	0.663	V	Tj=-10 to 100℃
Line Regulation 1	REG.l1	-	0.1	0.5	%/V	V_{CC}=4.3V to 5.5V
Line Regulation 2	REG.l2	-	0.1	0.5	%/V	V_{IN}=1.2V to 3.3V
Load Regulation	REG.L	-	0.5	10	mV	I_O=0 to 4A
Output ON Resistance	Ron	-	28	50	mΩ	I_O=4A,V_{IN}=1.2V Tj=-10 to 100℃
Standby Discharge Current	I_{DEN}	1	-	-	mA	V_{EN}=0V, V_O=1V
[ENABLE]						
Enable Pin Input Voltage High	EN_{HIGH}	2	-	-	V	
Enable Pin Input Voltage Low	EN_{LOW}	-0.2	-	0.8	V	
Enable Input Bias Current	I_{EN}	-	6	10	μA	V_{EN}=3V
[FEEDBACK]						
Feedback Pin Bias Current	I_{FB}	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	I_{NRCS}	12	20	28	μA	
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	$V_{CC}UVLO$	3.5	3.8	4.1	V	V_{CC}:Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	$V_{CC}HYS$	100	160	220	mV	V_{CC}:Sweep-down
VD Undervoltage Lockout Threshold Voltage	$V_D UVLO$	$V_{REF}\times 0.6$	$V_{REF}\times 0.7$	$V_{REF}\times 0.8$	V	V_D:Sweep-up
[SCP]						
SCP Start up Voltage	V_{OSCP}	$V_O\times 0.3$	$V_O\times 0.4$	$V_O\times 0.5$	V	V_{FB}=0, V_{GATE}=2.5V
SCP Threshold Voltage	V_{SCPTH}	1.05	1.15	1.25	V	V_{FB}=VCC, V_{GATE}=2.5V
Charge Current	I_{SCP}	2	4	6	μA	
Standby Voltage	$V_{SCPSTBY}$	-	-	50	mV	

●Electrical Characteristics (Unless otherwise specified, Ta=25℃, V_{CC}=5V, V_{EN}=3V, V_{IN}=1.7V)
BD35221EFV

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	I_{CC}	-	1.4	2.2	mA	
VCC Shutdown Mode Current	I_{ST}	-	0	10	μA	V_{EN}=0V
Output Voltage	I_O	4.0	-	-	A	
Feedback Voltage 1	$V_{OS}1$	1.188	1.200	1.212	V	
Feedback Voltage 2	$V_{OS}2$	1.176	1.200	1.224	V	Tj=-10 to 100℃
Line Regulation 1	REG.l1	-	0.1	0.5	%/V	V_{CC}=4.3V to 5.5V
Line Regulation 2	REG.l2	-	0.1	0.5	%/V	V_{IN}=1.25V to 3.3V
Load Regulation	REG.L	-	0.5	10	mV	I_O=0 to 4A
Output ON Resistance	Ron	-	28	50	mΩ	I_O=4A,V_{IN}=1.2V Tj=-10 to 100℃
Standby Discharge Current	I_{DEN}	1	-	-	mA	V_{EN}=0V, V_O=1V
[ENABLE]						
Enable Pin Input Voltage High	EN_{HIGH}	2	-	-	V	
Enable Pin Input Voltage Low	EN_{LOW}	-0.2	-	0.8	V	
Enable Input Bias Current	I_{EN}	-	6	10	μA	V_{EN}=3V
[NRCS]						
NRCS Charge Current	I_{NRCS}	12	20	28	μA	
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	V_{CC}UVLO	3.5	3.8	4.1	V	V_{CC}:Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	V_{CC}HYS	100	160	220	mV	V_{CC}:Sweep-down
VD Undervoltage Lockout Threshold Voltage	V_DUVLO	$V_O \times 0.6$	$V_O \times 0.7$	$V_O \times 0.8$	V	V_D:Sweep-up
[SCP]						
SCP Start up Voltage	V_{OSCP}	$V_O \times 0.3$	$V_O \times 0.4$	$V_O \times 0.5$	V	V_{FB}=0, V_{GATE}=2.5V
SCP Threshold Voltage	V_{SCPTH}	1.05	1.15	1.25	V	V_{FB}=VCC, V_{GATE}=2.5V
Charge Current	I_{SCP}	2	4	6	μA	
Standby Voltage	$V_{SCPSTBY}$	-	-	50	mV	

●Electrical Characteristics (Unless otherwise specified, Ta=25℃, V$_{CC}$=5V, V$_{EN}$=3V, V$_{IN}$=1.7V)
BD35222EFV

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	I$_{CC}$	-	1.4	2.2	mA	
VCC Shutdown Mode Current	I$_{ST}$	-	0	10	μA	V$_{EN}$=0V
Output Voltage	I$_O$	4.0	-	-	A	
Feedback Voltage 1	V$_{OS}$1	1.485	1.500	1.515	V	
Feedback Voltage 2	V$_{OS}$2	1.470	1.500	1.530	V	Tj=-10 to 100℃
Line Regulation 1	REG.I1	-	0.1	0.5	%/V	V$_{CC}$=4.3V to 5.5V
Line Regulation 2	REG.I2	-	0.1	0.5	%/V	V$_{IN}$=1.55V to 3.3V
Load Regulation	REG.L	-	0.5	10	mV	I$_O$=0 to 4A
Output ON Resistance	Ron	-	28	50	mΩ	I$_O$=4A,V$_{IN}$=1.5V Tj=-10 to 100℃
Standby Discharge Current	I$_{DEN}$	1	-	-	mA	V$_{EN}$=0V, V$_O$=1V
[ENABLE]						
Enable Pin Input Voltage High	EN$_{HIGH}$	2	-	-	V	
Enable Pin Input Voltage Low	EN$_{LOW}$	-0.2	-	0.8	V	
Enable Input Bias Current	I$_{EN}$	-	6	10	μA	V$_{EN}$=3V
[NRCS]						
NRCS Charge Current	I$_{NRCS}$	12	20	28	μA	
NRCS Standby Voltage	V$_{STB}$	-	0	50	mV	V$_{EN}$=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	V$_{CC}$UVLO	3.5	3.8	4.1	V	V$_{CC}$:Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	V$_{CC}$HYS	100	160	220	mV	V$_{CC}$:Sweep-down
VD Undervoltage Lockout Threshold Voltage	V$_D$UVLO	V$_O$×0.6	V$_O$×0.7	V$_O$×0.8	V	V$_D$:Sweep-up
[SCP]						
SCP Start up Voltage	V$_{OSCP}$	V$_O$×0.3	V$_O$×0.4	V$_O$×0.5	V	V$_{FB}$=0, V$_{GATE}$=2.5V
SCP Threshold Voltage	V$_{SCPTH}$	1.05	1.15	1.25	V	V$_{FB}$=VCC, V$_{GATE}$=2.5V
Charge Current	I$_{SCP}$	2	4	6	μA	
Standby Voltage	V$_{SCPSTBY}$	-	-	50	mV	

Vo
50mV/div

49mV

Io
2A/div

4.0A

Io=0A→4A/4μsec   T(10μsec/div)

Fig.1 Transient Response
(0→4A)
Co=22μF, Cfb=1000pF

Vo
50mV/div

59mV

Io
2A/div

4.0A

Io=0A→4A/4μsec   T(10μsec/div)

Fig.2 Transient Response
(0→4A)
Co=100μF

Vo
50mV/div

46mV

Io
2A/div

4.0A

Io=0A→4A/4μsec   T(10μsec/div)
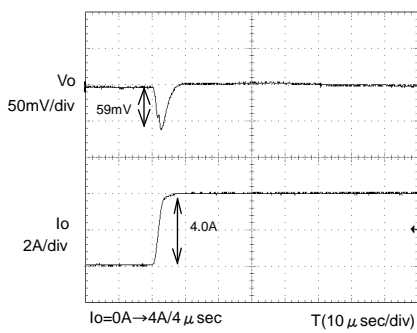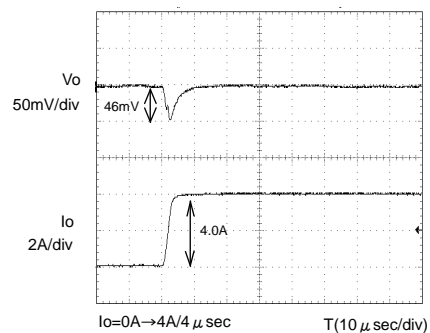
Fig.3 Transient Response
(0→4A)
Co=100μF, Cfb=1000pF

Vo
50mV/div

42mV

Io
2A/div

4.0A

Io=4A→0A/4μsec   T(100μsec/div)
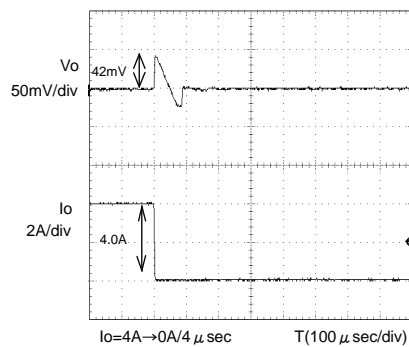
Fig.4 Transient Response
(4→0A)
Co=22μF, Cfb=1000pF

Vo
50mV/div

41mV

Io
2A/div

4.0A

Io=4A→0A/4μsec   T(100μsec/div)

Fig.5 Transient Response
(4→0A)
Co=100μF

Vo
50mV/div

41mV

Io
2A/div

4.0A

Io=4A→0A/4μsec   T(100μsec/div)
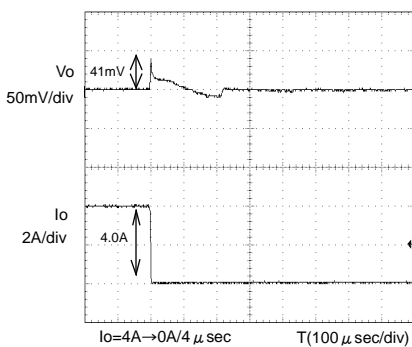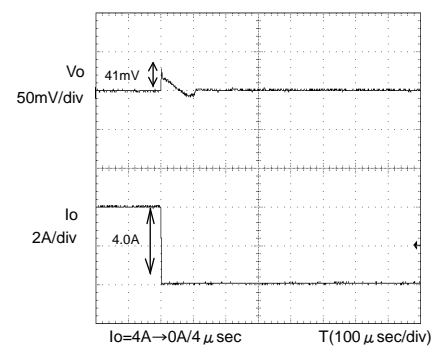
Fig.6 Transient Response
(4→0A)
Co=100μF, Cfb=1000pF

Ven
2V/div

VNRCS
2V/div

Vo
1V/div

T(20μsec/div)
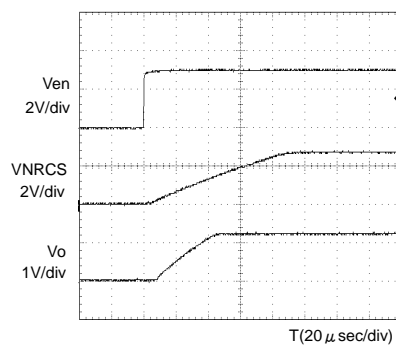
Fig.7 Waveform at output start

Ven
2V/div

VNRCS
2V/div

Vo
1V/div

T(2msec/div)
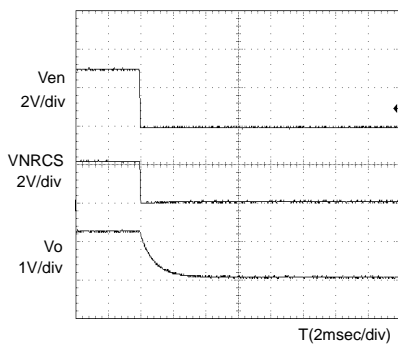
Fig.8 Waveform at output OFF

VCC
5V/div

Ven
2V/div

VIN
2V/div

Vo
1V/div

VCC→VIN→Ven

Fig.9 Input sequence

VCC
5V/div

Ven
2V/div

VIN
2V/div

Vo
1V/div

VIN→VCC→Ven

Fig.10 Input sequence

VCC
5V/div

Ven
2V/div

VIN
2V/div

Vo
1V/div

Ven→VCC→VIN

Fig.11 Input sequence

VCC
5V/div

Ven
2V/div

VIN
2V/div

Vo
1V/div

VCC→Ven→VIN
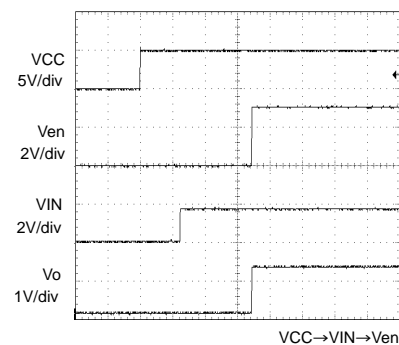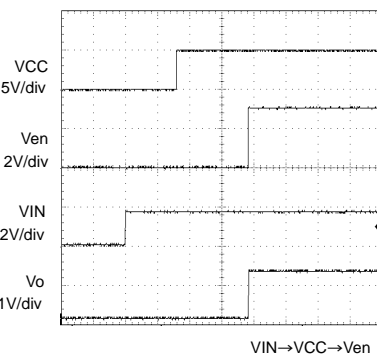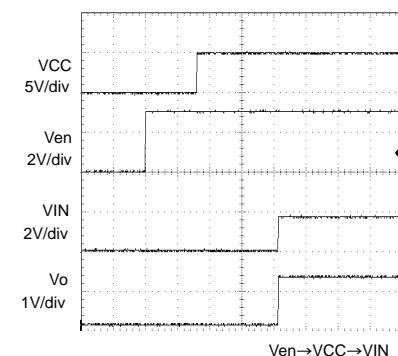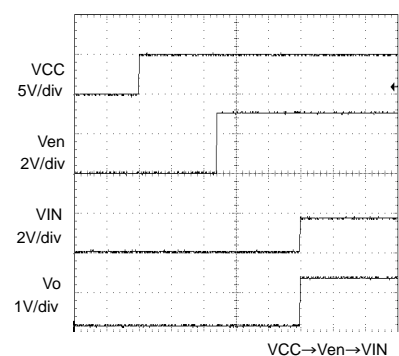
Fig.12 Input sequence

●Reference Data
BD3522EFV
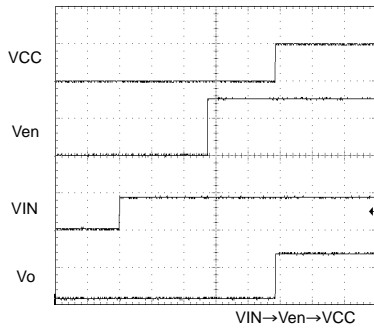
Fig.13 Input sequence
VIN→Ven→VCC
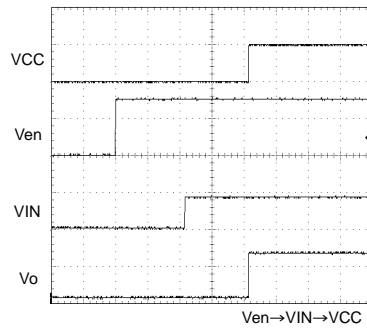
Fig.14 Input sequence
Ven→VIN→VCC
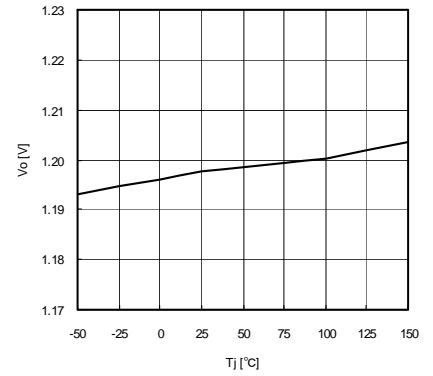
Fig.15 Tj-Vo
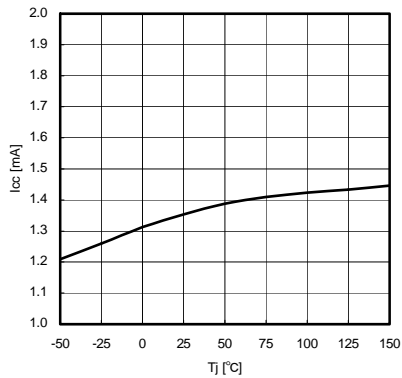
Fig.16 Tj-ICC
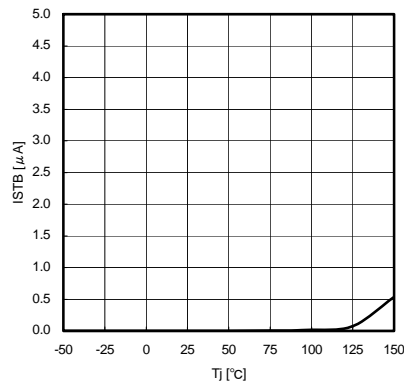
Fig.17 Tj-ISTB
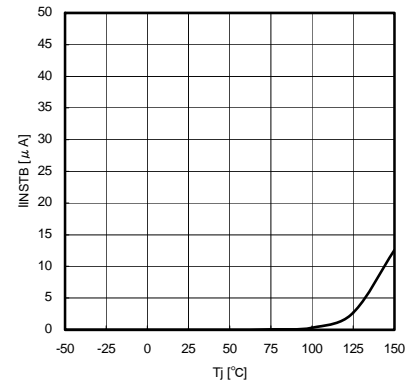
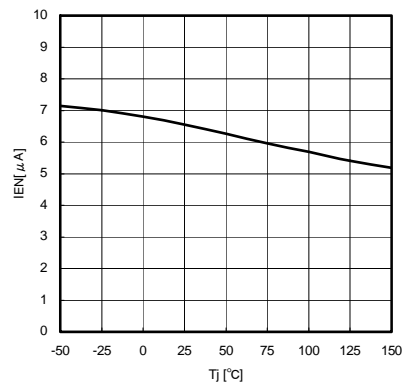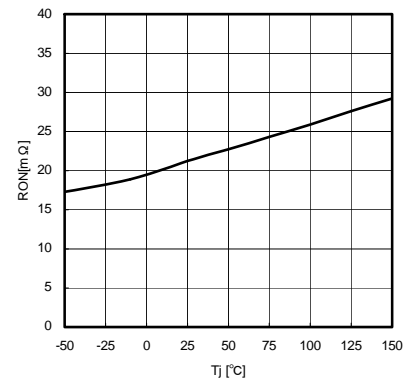Fig.18 Tj-IINSTB
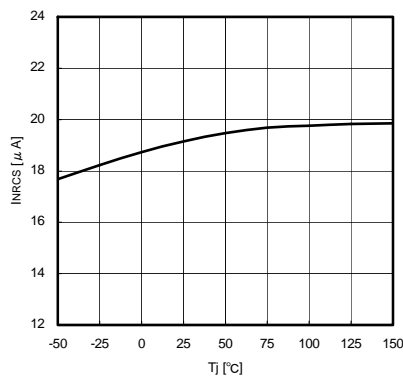
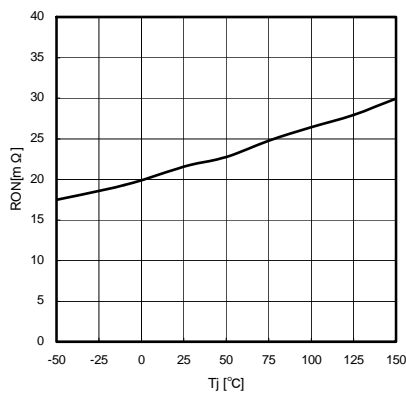Fig.19 Tj-INRCS

Fig.20 Tj-IEN

Fig.21 Tj-RON
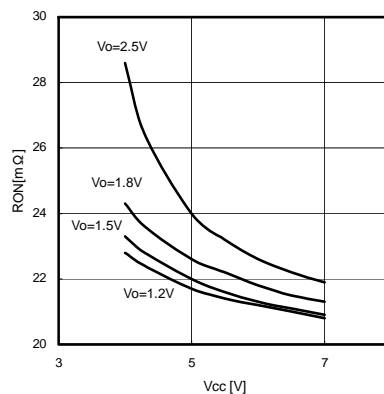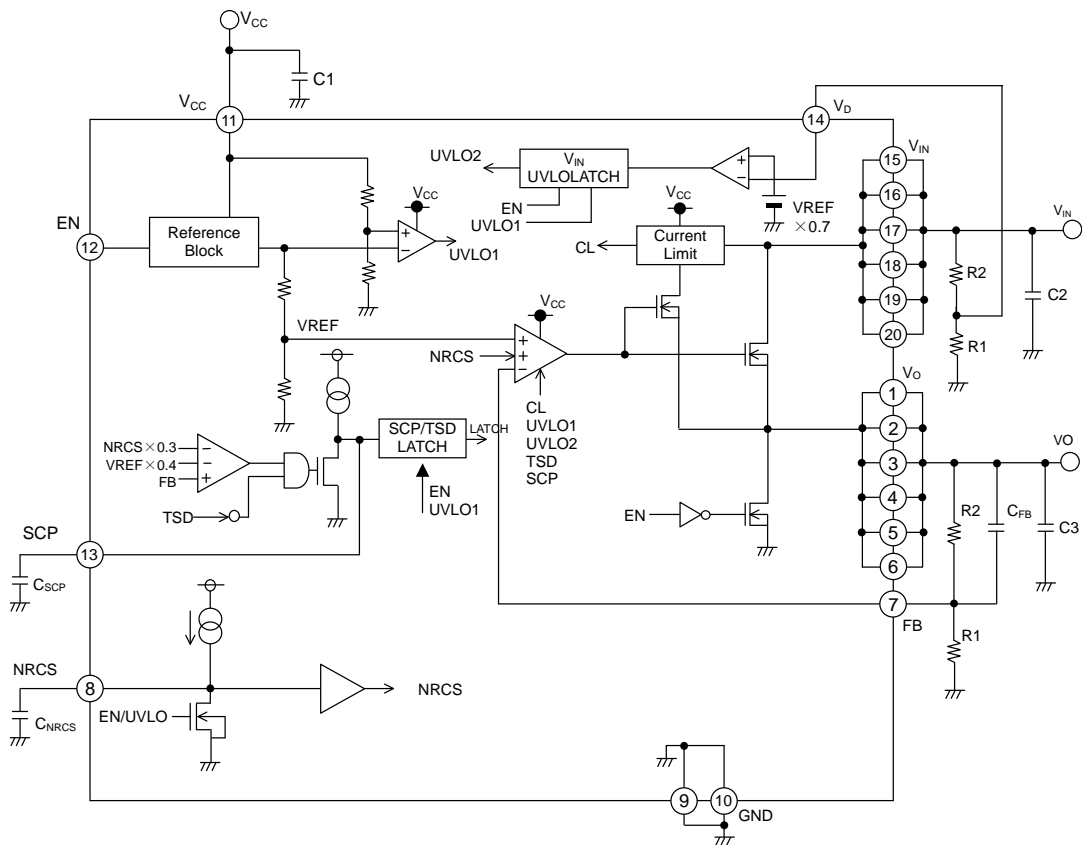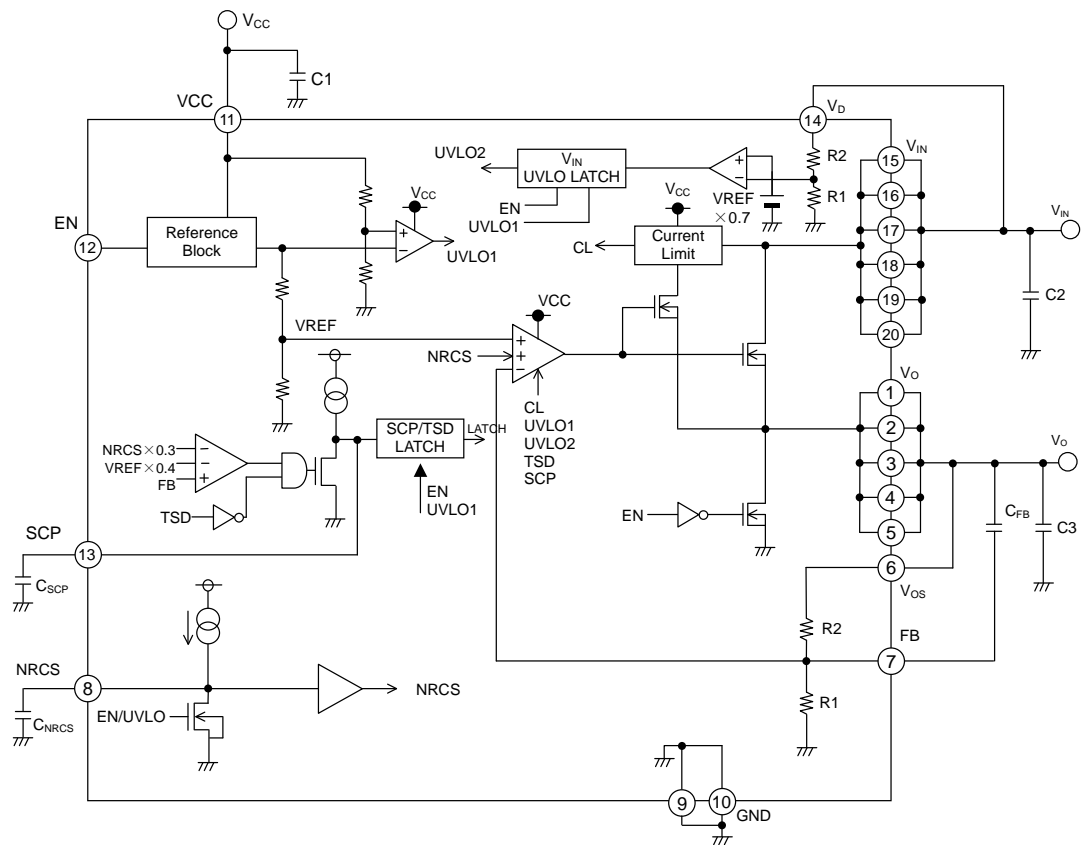(VCC=5V/VO=1.2V)

Fig.22 Tj-RON
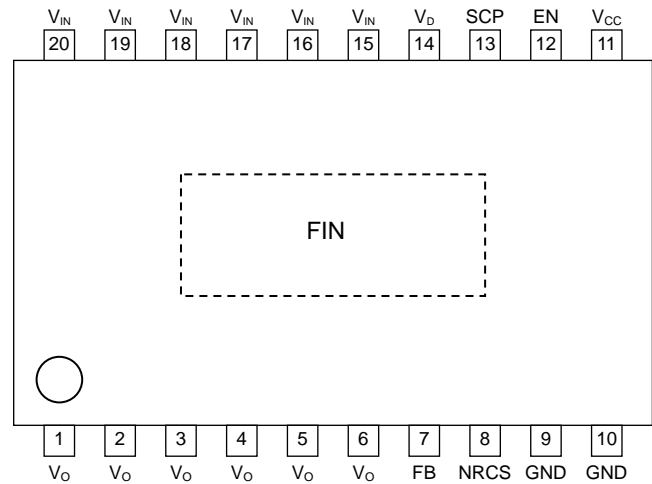(VCC=5V/VO=1.5V)

Fig.23 VCC-RON

●Block Diagram

BD3522EFV

BD35221EFV/BD35222EFV

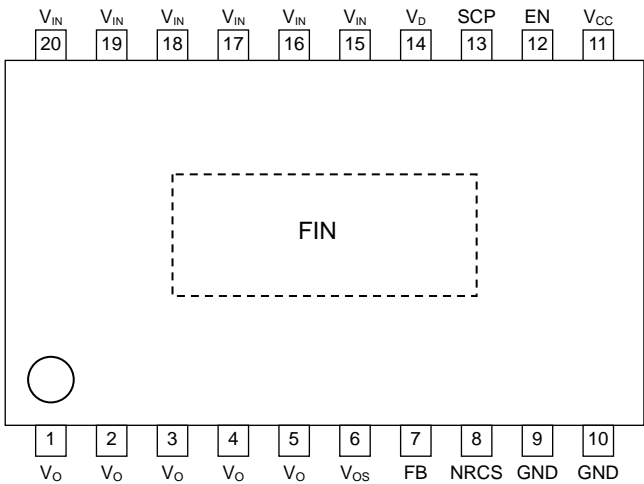● Pin Layout

BD3522EFV

V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_D	SCP	EN	V_{CC}
20	19	18	17	16	15	14	13	12	11

FIN

1	2	3	4	5	6	7	8	9	10
V_O	V_O	V_O	V_O	V_O	V_O	FB	NRCS	GND	GND

BD35221EFV/BD35222EFV

V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_{IN}	V_D	SCP	EN	V_{CC}
20	19	18	17	16	15	14	13	12	11

FIN

1	2	3	4	5	6	7	8	9	10
V_O	V_O	V_O	V_O	V_O	V_{OS}	FB	NRCS	GND	GND

● Pin Function Table

BD3522EFV

PIN No.	PIN name	PIN Function
1	V_O	Output Voltage Pin
2	V_O	Output Voltage Pin
3	V_O	Output Voltage Pin
4	V_O	Output Voltage Pin
5	V_O	Output Voltage Pin
6	V_O	Output Voltage Pin
7	FB	Reference Voltage Feedback Pin
8	NRCS	In-rush Current Protection (NRCS) Capacitor Connection Pin
9	GND	Ground Pin
10	GND	Ground Pin
11	V_{CC}	Power supply pin
12	EN	Enable input pin
13	SCP	SCP Delay Time Setting Capacitor Connection Pin
14	VD	VIN Input Voltage Detect Pin
15	V_{IN}	Input Voltage Pin
16	V_{IN}	Input Voltage Pin
17	V_{IN}	Input Voltage Pin
18	V_{IN}	Input Voltage Pin
19	V_{IN}	Input Voltage Pin
20	V_{IN}	Input Voltage Pin
-	FIN	Connected to heatsink and GND

BD35221EFV/BD35222EFV

PIN No.	PIN name	PIN Function
1	V_O	Output Voltage Pin
2	V_O	Output Voltage Pin
3	V_O	Output Voltage Pin
4	V_O	Output Voltage Pin
5	V_O	Output Voltage Pin
6	V_{OS}	Output Voltage Control Pin
7	FB	Reference Voltage Feedback Pin
8	NRCS	In-rush Current Protection (NRCS) Capacitor Connection Pin
9	GND	Ground Pin
10	GND	Ground Pin
11	V_{CC}	Power supply pin
12	EN	Enable input pin
13	SCP	SCP Delay Time Setting Capacitor Connection Pin
14	VD	VIN Input Voltage Detect Pin
15	V_{IN}	Input Voltage Pin
16	V_{IN}	Input Voltage Pin
17	V_{IN}	Input Voltage Pin
18	V_{IN}	Input Voltage Pin
19	V_{IN}	Input Voltage Pin
20	V_{IN}	Input Voltage Pin
-	FIN	Connected to heatsink and GND

●Operation of Each Block

・AMP

This is an error amp compares the reference voltage (0.65V) with V_O to drive the output Nch FET (Ron=50mΩ). Frequency optimization helps to realize rapid transient response, and to support the use of ceramic capacitors on the output. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to VCC. When EN is OFF, or when UVLO is active, output goes LOW and the output of the NchFET switches OFF.

・EN

The EN block controls the regulator's ON/OFF state via the EN logic input pin. In the OFF position, circuit voltage is maintained at 0μA, thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin V_O, thereby draining the excess charge and preventing the IC on the load side from malfunctioning. Since no electrical connection is required (e.g. between the VCC pin and the ESD prevention diode), module operation is independent of the input sequence.

・V_{CC}UVLO

To prevent malfunctions that can occur during a momentary decrease in V_{CC}, the UVLO circuit switches the output OFF, and (like the EN block) discharges NRCS and V_O. Once the UVLO threshold voltage (TYP3.80V) is reached, the power-on reset is triggered and output continues.

・V_DUVLO

V_D pin is the V_{IN} voltage detect pin. When V_D voltage exceeds the threshold voltage, V_DUVLO becomes active. Once active, the status of output voltage remains ON even if V_D voltage drops. (When V_{IN} voltage drops, SCP engages and output switches OFF.) Unlike EN and V_{CC}, it is effective at output startup. V_DUVLO can be restored either by reconnecting the EN pin or V_{CC} pin.

・CURRENT LIMIT

When output is ON, the current limit function monitors the internal IC output current against the parameter value. When current exceeds this level, the current limit module lowers the output current to protect the load IC. When the overcurrent state is eliminated, output voltage is restored to the parameter value. However when output voltage falls to or below the SCP startup voltage, the SCP function becomes active and the output switches OFF.

・NRCS (Non Rush Current on Start-up)

The soft start function enabled by connecting an external capacitor between the NRCS pin and ground. Output ramp-up can be set for any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a 20μA (TYP) constant current source to charge the external capacitor. Output start time is calculated via the formula below.

$$T_{NRCS} \text{ (typ.)} = \frac{C_{NRCS} \times V_{FB}}{I_{NRCS}}$$

・TSD (Thermal Shut down)

The shutdown (TSD) circuit automatically is latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus serving to protect the IC against "thermal runaway" and heat damage. Because the TSD circuit is intended to shut down the IC only in the presence of extreme heat, it is crucial that the Tj (max) parameter not be exceeded in the thermal design, in order to avoid potential problems with the TSD.

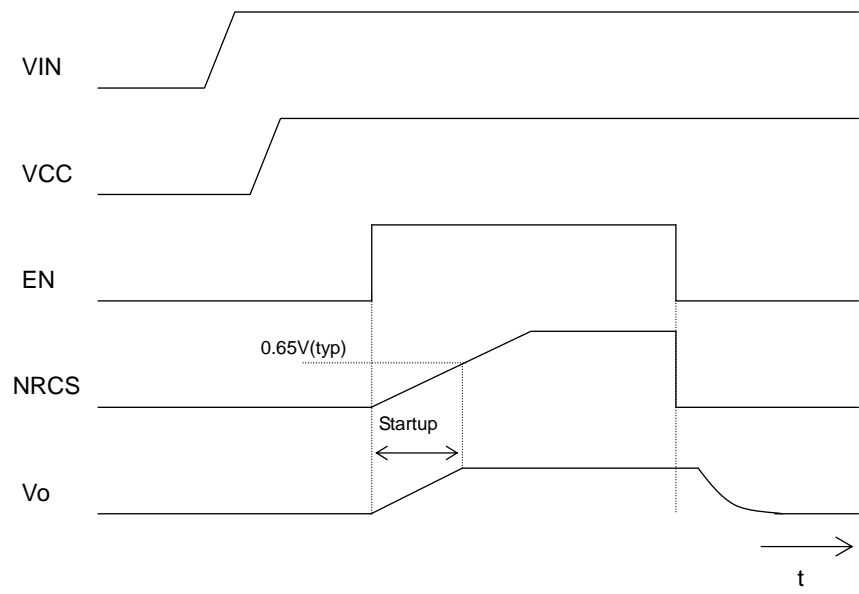$$T_{TSD} \text{ (typ.)} = \frac{C_{SCP} \times V_{SCPTH}}{20uA}$$

・V_{IN}

The V_{IN} line acts as the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the V_{CC} pin and the ESD protection diode) is necessary, V_{IN} operates independent of the input sequence. However, since an output NchFET body diode exists between V_{IN} and V_O, a V_{IN}-V_O electric (diode) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to V_{IN} from V_O.

・SCP

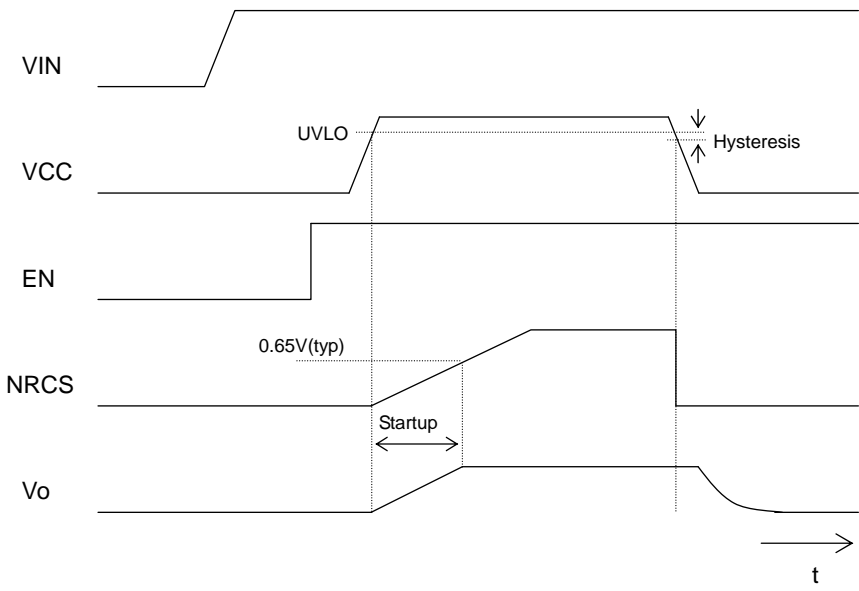When output voltage (Vo) drops, the IC assumes that V_O pin is shorted to GND and switched the output voltage OFF. After the GND short has been detected and the programmed delay time has elapsed, output is latched OFF. It is also effective during output startup. SCP can be cleared either by reconnecting the EN pin or V_{CC} pin. Delay time is calculated via the formula below.

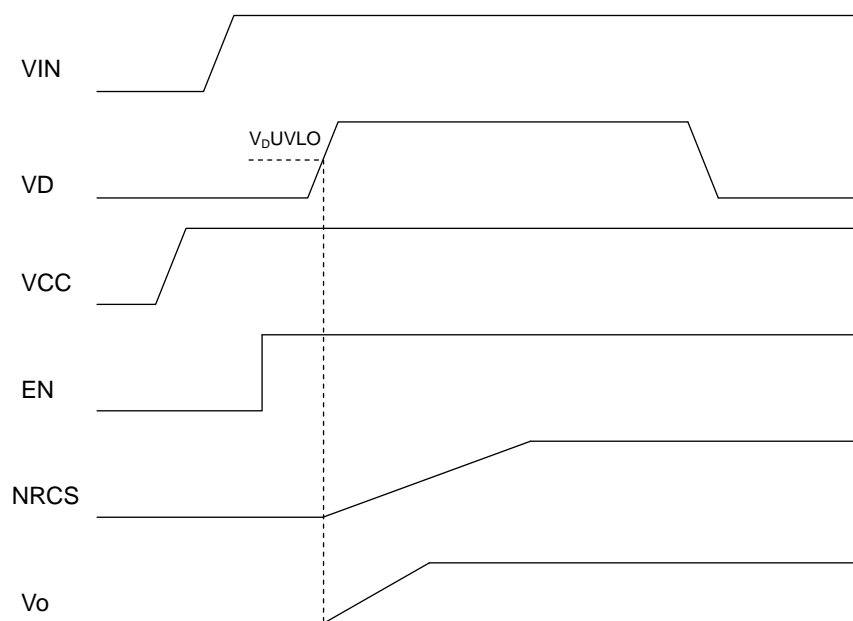$$T_{SCP} \text{ (typ.)} = \frac{C_{SCP} \times V_{SCPTH}}{I_{SCP}}$$
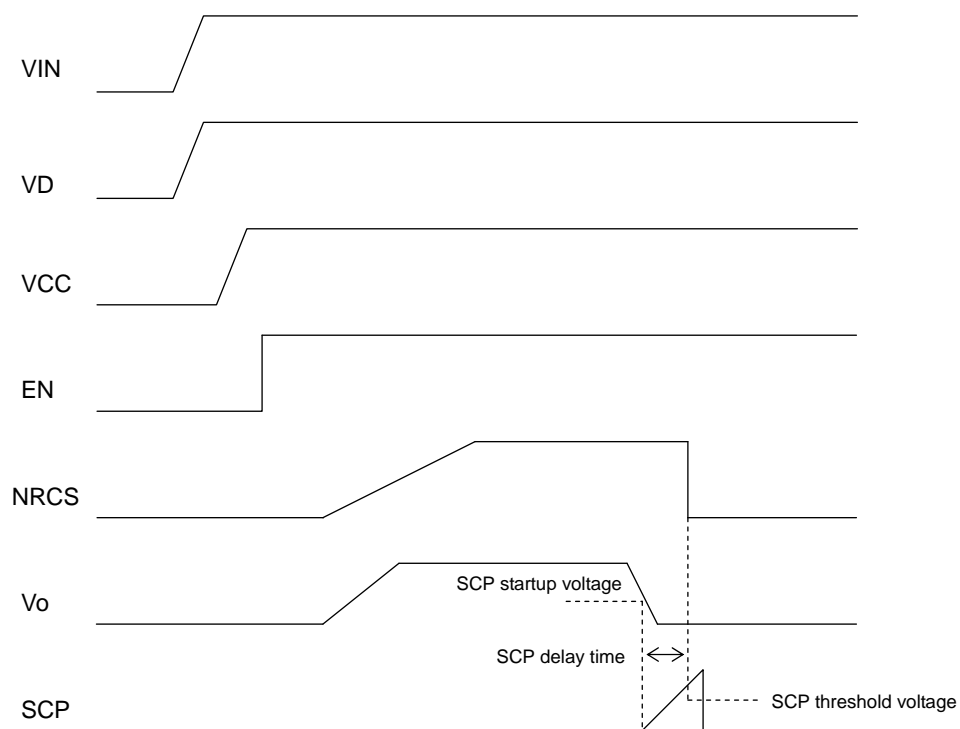
●Timing Chart
EN ON/OFF

VIN

VCC

EN

NRCS

0.65V(typ)

Startup

Vo

t

VCC ON/OFF

VIN

VCC

UVLO

Hysteresis

EN

NRCS

0.65V(typ)

Startup

Vo

t

● Timing Chart
VD ON

VIN

VD

V_DUVLO

VCC

EN

NRCS

Vo

SCP OFF

VIN

VD

VCC

EN

NRCS

Vo

SCP startup voltage
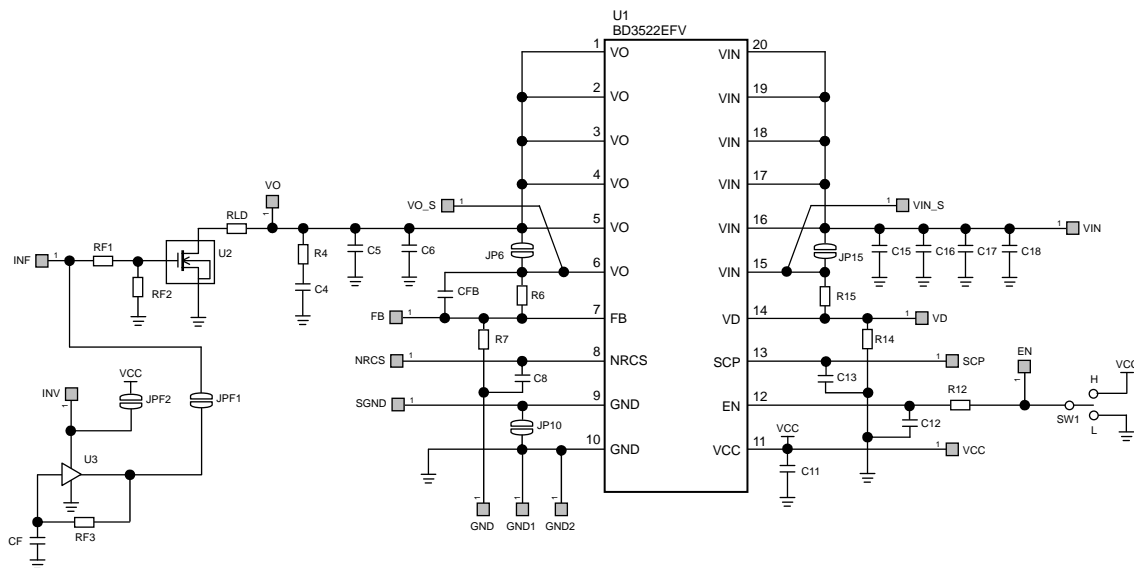
SCP delay time

SCP

SCP threshold voltage

●Evaluation Board

■ BD3522EFV Evaluation Board Schematic

■ BD3522EFV Evaluation Board List

Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD3522EFV
C6	22uF	KYOCERA	CM316B226M06A
C8	0.01uF	MURATA	GRM188B11H103KD
C11	1uF	MURATA	GRM188B11A105KD
C13	330pF	MURATA	GRM188B11H331KD
C15	10uF	KYOCERA	CM21B106M06A
C18(*1)	150uF	SANYO	6TPB150M

Component	Rating	Manufacturer	Product Name
CFB	1000pF	MURATA	GRM188B11H102KD
R6 (@V_{OUT}=1.2V)	3.3kΩ	ROHM	MCR03EZPF3301
R7	3.9Ω	ROHM	MCR03EZPF3901
R121	0kΩ	-	jumper
R14	3.9kΩ	ROHM	MCR03EZPF3901
R15(@V_{OUT}=1.2V)	3.3kΩ	ROHM	MCR03EZPF3301

*1 provision for supply impedance of instruments

■ BD3522EFV Evaluation Board Layout

Silk Screen (Top)

Silk Screen (Bottom)

TOP Layer

Middle Layer_1

Middle Layer_2

Bottom Layer

●Recommended Circuit Example (BD3522EFV)

R15 R14

VIN C20

C13

C12 EN

C11 Vcc

| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |
| V_IN | V_IN | V_IN | V_IN | V_IN | V_IN | VD | SCP | EN | Vcc |

| Vo | Vo | Vo | Vo | Vo | Vo | FB | NRCS | GND | GND |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

C8

R6 R7

C1 C6

Component	Recommended Value	Programming Notes and Precautions
R6/R7	3.3k /3.9k	IC output voltage can be set with a configuration formula $V_{FB} \times (R6+R7)/R7$ using the values for the internal reference output voltage (V_{FB}) and the output voltage resistors (R6, R7). Select resistance values that will avoid the impact of the FB bias current ($\pm 100nA$). The recommended total resistance value is 10KΩ.
C1	22μF	To assure output voltage stability, please be certain the output capacitors are connected between Vo pin and GND. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22μF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.
C11/C20	1μF/10μF	Input capacitors reduce the output impedance of the voltage supply source connected to the (V_{CC}, V_{IN}) input pins. If the impedance of this power supply were to increase, input voltage (V_{CC}, V_{IN}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 1μF/10μF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C8	0.01μF	The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (VIN to VO) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.
C6	1000pF	This component is employed when the C16 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.
C13	330pF	The Short Circuit Protection (SCP) function and the Thermal Shut Down (TSD) function are built into the IC. Constant current comes from the SCP pin when SCP function or TSD function is operated. (SCP:4μA, TSD:20μA TYP.) The voltage occurred in SCP pin by this current overstep the threshold voltage, the status of voltage becomes OFF. Capacitors with low susceptibility to temperature (330pF or more) are recommended, in order to assure a stable TSD delay setting time. In light of this information, please confirm the capacitor value to prevent startup defective.

● Recommended Circuit Example (BD35221EFV/BD35222EFV)

Component	Recommended Value	Programming Notes and Precautions
C1	22 μF	To assure output voltage stability, please be certain the output capacitors are connected between Vo pin and GND. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22 μF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.
C11/C20	1 μF/10 μF	Input capacitors reduce the output impedance of the voltage supply source connected to the (V_{CC}, V_{IN}) input pins. If the impedance of this power supply were to increase, input voltage (V_{CC}, V_{IN}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 1 μF/10 μF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C8	0.01 μF	The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (V_{IN} to V_O) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.
C6	1000pF	This component is employed when the C16 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.
C13	330pF	The Short Circuit Protection (SCP) function and the Thermal Shut Down (TSD) function are built into the IC. Constant current comes from the SCP pin when SCP function or TSD function is operated. (SCP:4 μA, TSD:20 μA TYP.) The voltage occurred in SCP pin by this current overstep the threshold voltage, the status of voltage becomes OFF. Capacitors with low susceptibility to temperature (330pF or more) are recommended, in order to assure a stable TSD delay setting time. In light of this information, please confirm the capacitor value to prevent startup defective.

●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 100℃.
2. Chip junction temperature (Tj) can be no higher than 150℃.

Chip junction temperature can be determined as follows:

① Calculation based on ambient temperature (Ta)
$Tj = Ta + \theta j\text{-}a \times W$

<Reference values>

θ j-a: HTSSOP-B20   125℃/W   1-layer substrate (no copper foil area)
86.2℃/W   1-layer substrate (copper foil area : 15mm×15mm)
54.1℃/W   2-layer substrate (copper foil area : 70mm×70mm)
39.1℃/W   2-layer substrate (copper foil area : 70mm×70mm)
Substrate size: $70 \times 70 \times 1.6mm^3$ (substrate with thermal via)

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 6.5mm×6.4mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below enable to get the superior heat radiation characteristic. (This figure is the image. It is recommended that the VIA size and the number is designed suitable for the actual situation.).
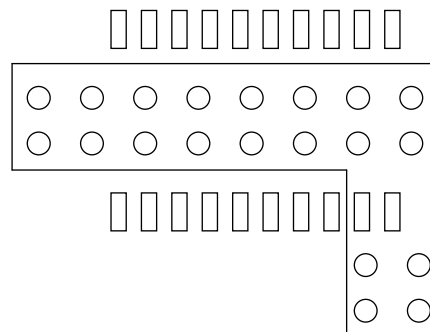
Most of the heat loss that occurs in the BD3522EFV is generated from the output Nch FET. Power loss is determined by the total VIN-Vo voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the VIN and Vo in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3522EFV) make certain to factor conditions such as substrate size into the thermal design.

Power consumption (W) = { Input voltage (VIN)- Output voltage (Vo) } × Io(Ave)

Example) Where VIN=1.7V, VO=1.2V, Io(Ave) = 4A,
Power consumption (W) = { 1.7(V)-1.2(V) } × 4.0(A)

= 2.0(W)

●Input-Output Equivalent Circuit Diagram (BD3522EFV)
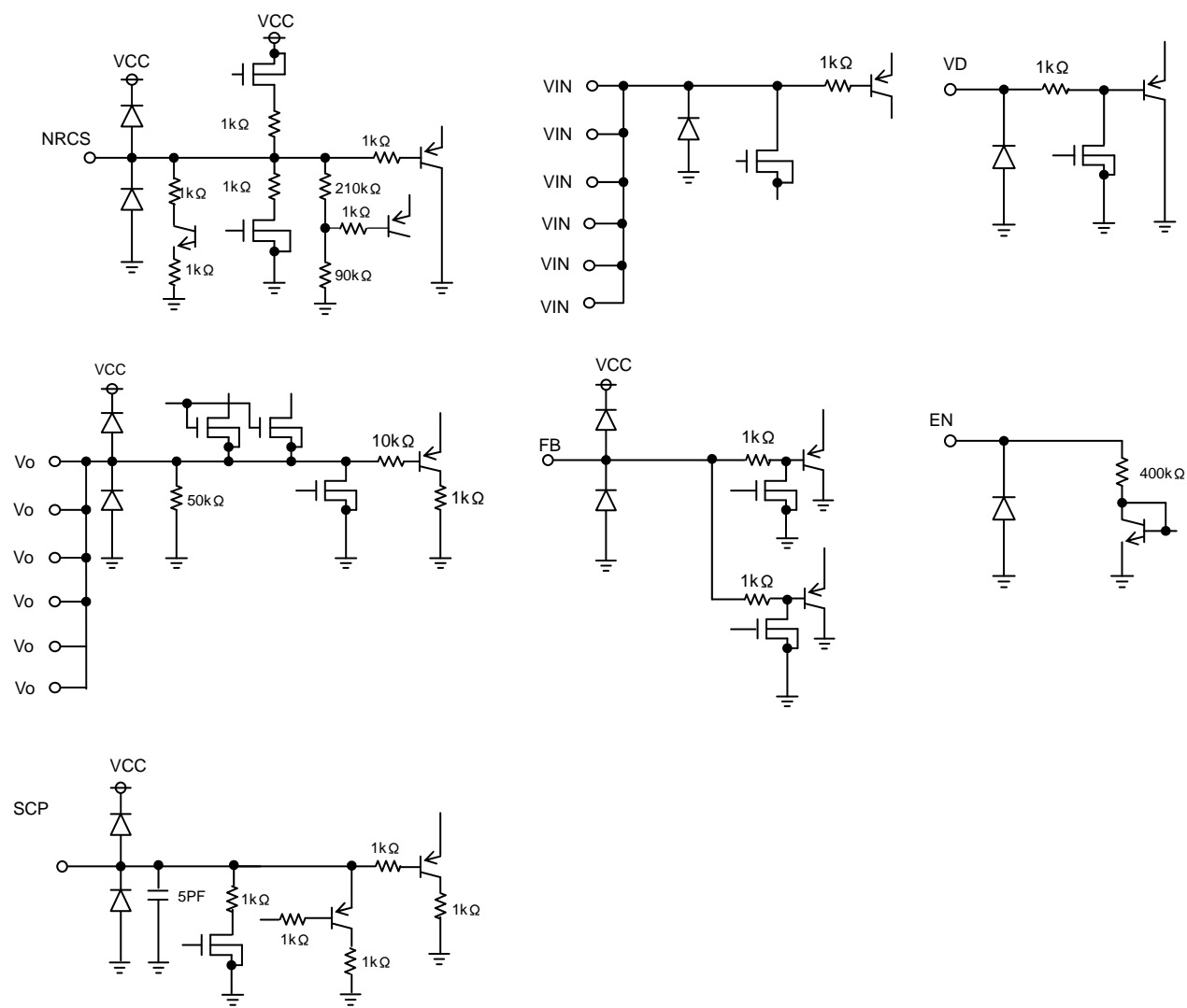
●Operation Notes

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward
   Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines
   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO
   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit
   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)
BD3522EFV/BD35221EFV/BD35222EFV	175

10. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.
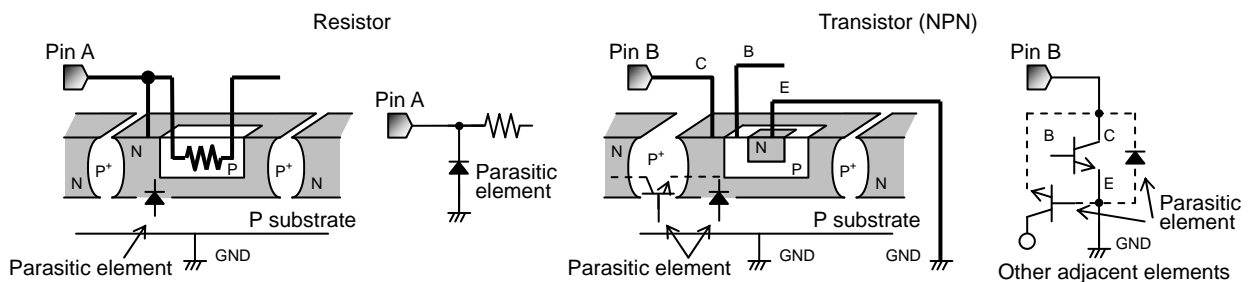
Example of IC structure

12. Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Heat Dissipation Characteristics

◎**HTSSOP-B20**

70mm×70mm×1.6mm (PCB with Thermal Via)
① 1 layer substrate (substrate surface copper foil area:0mm×0mm)
  θ j-a=125℃/W
② 2 layer substrate (substrate surface copper foil area:15mm×15mm)
  θ j-a=86.2℃/W
③ 2 layer substrate (substrate surface copper foil area:15mm×15mm)
  θ j-a=54.1℃/W
④ 4 layer substrate (substrate surface copper foil area:70mm×70mm)
  θ j-a=39.1℃/W
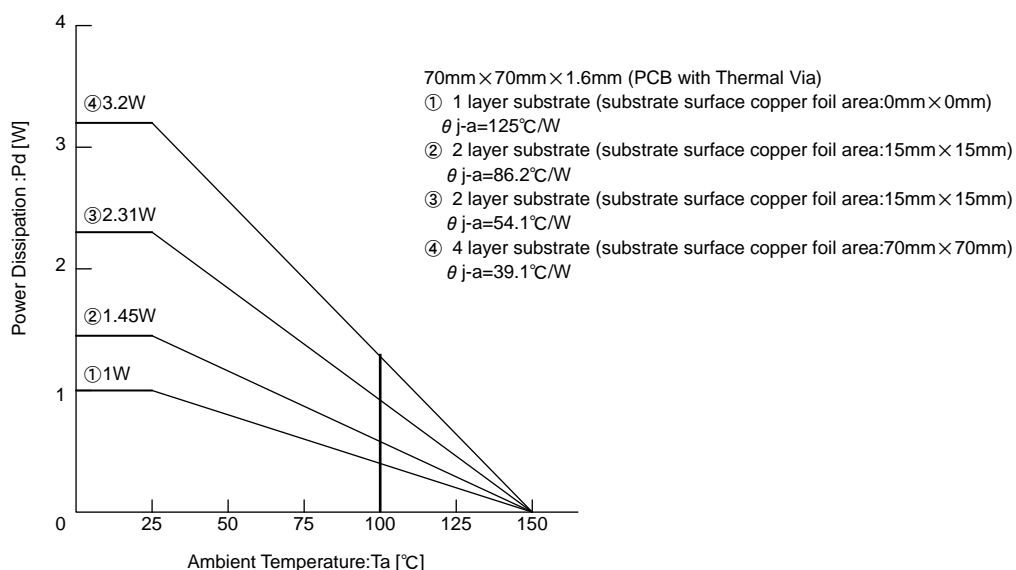
(HTSSOP-B20)

● Type Designations (Ordering Information)

| B | D | 3 | 5 | 2 | 2 | E | F | V | – | E | 2 |

Product Name
・ BD3522
・ BD35221
・ BD35222

Package Type
・ EFV: HTSSOP-B20

E2:Emboss tape reel opposite draw-out side: 1 pin

HTSSOP-B20

<Dimension>

6.5 ± 0.1
6.4 ± 0.2
4.4 ± 0.1
0.5 ± 0.15
1.0 ± 0.2
0.325
0.17 ⁺⁰·⁰⁵₋₀.₀₃
1.0Max.
0.85 ± 0.05
0.08 ± 0.05
0.65
0.2 ⁺⁰·⁰⁵₋₀.₀₄
0.08 S

(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel   1pin   Direction of feed

※When you order , please order in times the amount of package quantity.

The products listed in this catalog are designed to be used with ordinary electronic equipment or devices (such as audio visual equipment, office-automation equipment, communications devices, electrical appliances and electronic toys).
Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

Appendix