BCT3024
24 CHANNELS LED DRIVER

GENERAL DESCRIPTION

The BCT3024 is a LED driver with independent 24 output channels, and the output current of each channel can be programmed to achieve 256 levels by I2C interface. The output current of each channel can be set at up to 38mA (Max.) by an external resistor and independently scaled by a factor of 1, 1/2, 1/3 and 1/4.

The chip can be turned off by pulling the SDB pin lowor by using the software shutdown feature to reduce power consumption.

BCT3024 is available in QFN4x4-32L (4mm × 4mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Internal reset register
- Modulate LED brightness with 256 levels
- Each channel can be controlled independently
- Each channel can be scaled independently by 1,1/2, 1/3 and 1/4
- -40°C to +85°C temperature range
- QFN4x4-32L (4mm × 4mm)

APPLICATIONS

Mobile phones and other hand-held devices for LED display
LED in home appliances.

ORDERING INFORMATION

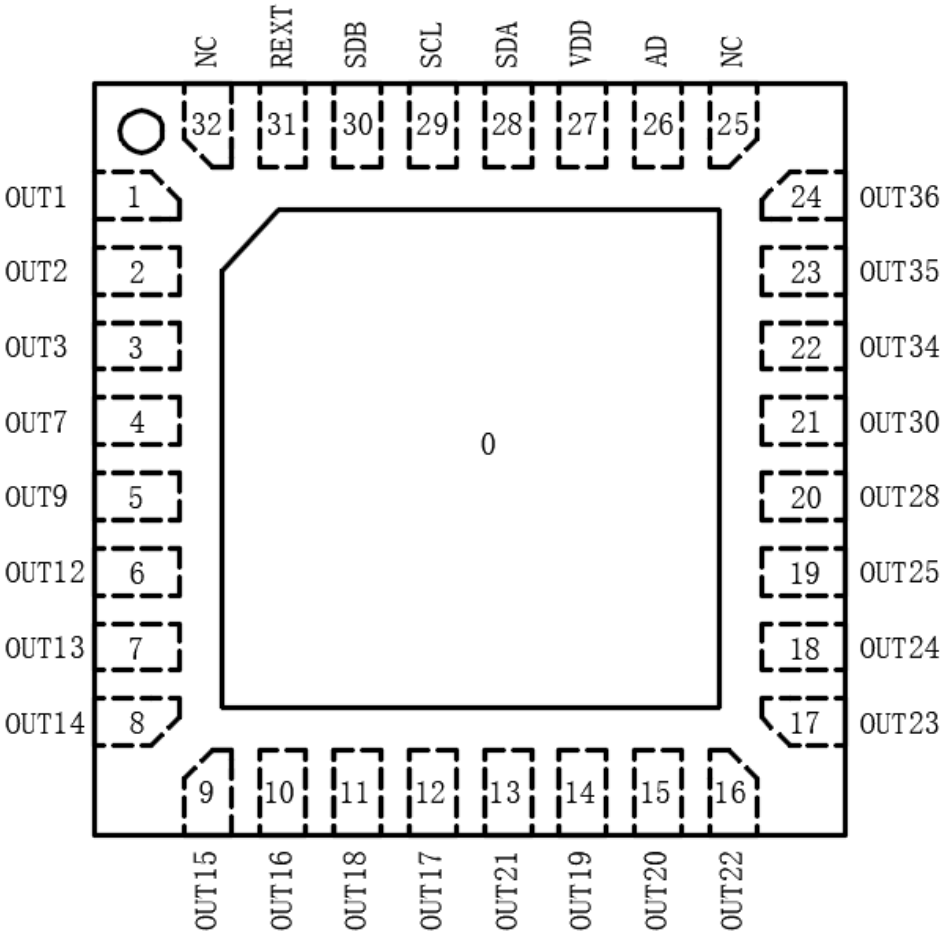
Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT3024EGJ-TR	QFN4x4-32L	-40°C to +85°C	3024 XXXXX	4000

Note:

"XXXXX" in marking will be appeared as the batch code.

PIN CONFIGURATION

QFN4x4-32L



PIN DESCRIPTION

No.	Pin	Description
0	GND	Ground.
1~3	OUT1 ~ OUT3	Output channel 1~3 for LEDs.
4	OUT7	Output channel 7 for LEDs.
5	OUT9	Output channel 9 for LEDs.
6~10	OUT12 ~ OUT16	Output channel 12~16 for LEDs.
11	OUT18	Output channel 18 for LEDs.
12	OUT17	Output channel 17 for LEDs.
13	OUT21	Output channel 21 for LEDs.
14~15	OUT19~ OUT20	Output channel 19~20 for LEDs.
16~19	OUT22~ OUT25	Output channel 22~25 for LEDs.
20	OUT28	Output channel 28 for LEDs.
21	OUT30	Output channel 30 for LEDs.
22~24	OUT34 ~ OUT36	Output channel 34~36 for LEDs.
25,32	NC	No Connect
26	AD	I2C address setting.
27	VDD	Power supply.
28	SDA	I2C serial data.
29	SCL	I2C serial clock.
30	SDB	Shutdown the chip when pulled low.
31	R_EXT	Input terminal used to connect an external resistor. This regulates the global output current.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.3V to 6V
Voltage at SCL, SDA, SDB, OUT1 to OUT36.....-0.3V to V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}..... 150°C
Storage temperature range,T_{STG}..... －65°C ~ +150°C
Operating temperature range, T_A…… −40°C ~ +85°C
Package thermal resistance (Mounted on JEDEC standard 4,layer(2s2p) PCB test board), $R_{\theta JA}$..... 36.4°C/W (QFN)
ESD (HBM).....±4kV

NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

Typical values are TA = 25°C, VCC = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{MAX}	Maximum global output current	V_{CC} = 4.2V, V_{OUT} = 0.8V R_{EXT} = 2kΩ, SL = "00" (Note 1)		38		mA
I_{OUT}	Output current	V_{OUT} = 0.6V R_{EXT} = 3.3kΩ, SL = "00"		23		mA
I_{CC}	Quiescent power supply current	R_{EXT} = 3.3kΩ		9		mA
I_{SD}	Shutdown current	V_{SDB} = 0V or software shutdown T_A = 25°C, V_{CC} = 3.6V	2	3	5	μA
I_{OZ}	Output leakage current	V_{SDB} = 0V or software shutdown, V_{OUT} = 5.5V			0.2	μA
V_{EXT}	Output voltage of R-EXT pin			0.58		V
Logic Electrical Characteristics (SDA, SCL, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V		5 (Note2)		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC}		5 (Note2)		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μ s
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs

ELECTRICAL CHARACTERISTICS（Continued）

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_R	Rise time of both SDA and SCL signals, receiving	(Note 3)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 3)		20+0.1C_b	300	ns

Note 1: The recommended minimum value of REXT is 2kΩ, or it may cause a large current.

Note 2: Guaranteed by design.

Note 3: Cb = total capacitance of one bus line in pF. ISINK ≤ 6mA. tR and tF measured between 0.3 h VCC and 0.7 h VCC

DETAILED DESCRIPTION

I2C INTERFACE

The BCT3024 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The BCT3024 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Since BCT3024 only supports write operations, A0 must always be "0". The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write only):

Bit	A7:A3	A2:A1	A0
Value	01111	AD	0

AD connected to GND, AD = 00;

AD connected to VCC, AD = 11;

AD connected to SCL, AD = 01;

AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the BCT3024。

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.
The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

DETAILED DESCRIPTION（Continued）

After the last bit of the chip address is sent, the master checks for the BCT3024's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the BCT3024 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of BCT3024, the register address byte is sent, most significant bit first.
BCT3024 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the BCT3024 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into BCT3024, load the address of the data register that the first data byte is intended for. During the BCT3024 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to BCT3024 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to BCT3024 (Figure 5)

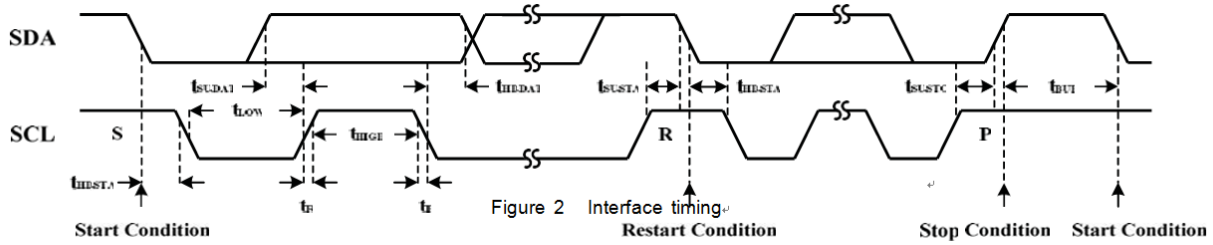


Figure 2 Interface timing

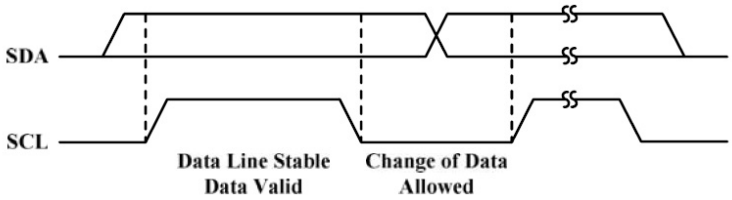


Figure 3 Bit transfer

DETAILED DESCRIPTION（Continued）

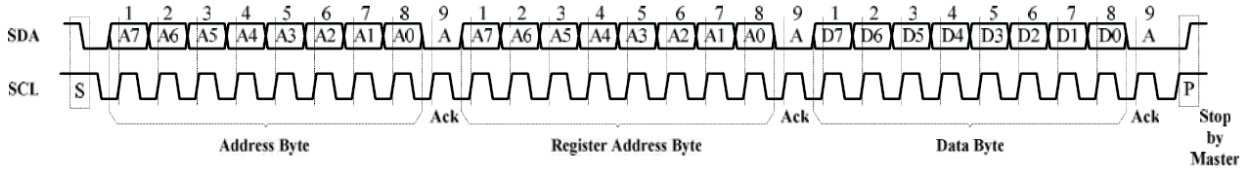


Figure 4 Writing to BCT3024(Typical)

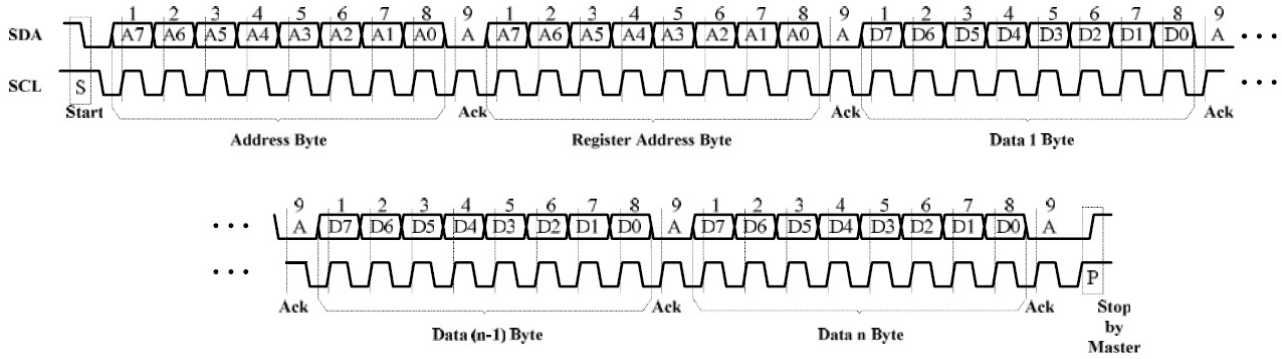


Figure 5 Writing to BCT3024(Automatic address increment)

Registers Definition

Table 2 Register Function

Address	Name	Function	Table	Default
00h	Shutdown Register	Set software shutdown mode	3	0000 0000
01h~24h	Brightness Register	36 channels brightness register (OUT1 to OUT36)	4	
25h	Update Register	Load brightness register and LED Control Register's data	-	xxxx xxxx
26h~49h	LED Control Register	Channel 1 to 36 enable bit and current (OUT1 to OUT36)	5	0000 0000
4Ah	Global Control	setting Set all channels enable	6	
4Fh	Reset Register	Reset all registers into default value	-	xxxx xxxx

Registers Definition（Continued）

Note：A description of the terminal not shown in Pin Configuration，for example OUT4

1）In a typical Writing way（see Figure 4）, the address and data of OUT4 are neglect.

2）In a Automatic address increment Writing way（see Figure 5）, OUT4 address and data cann't be neglect, We recommend writing data 0x00.

Table 3 00h Shutdown Register

Bit	D7:D1	D0
Name	-	SSD
Default	0000000	0

The Shutdown Register sets software shutdown mode of BCT3024

SSD Software Shutdown Enable

0 Software shutdown mode

1 Normal operation

Table 4 01h~24h Brightness Register(OUT1~OUT36)

Bit	D7:D0
Name	Brightness
Default	0000 0000

Brightness[7:0]

In normal mode, the eight bits setting the brightness of the output channel.

00000000 0/256 Light down

00000001 2/256

00000010 3/256

..... …… ……

11111111 256/256 the brightest

25H Brightness Update Register

The data sent to the Brightness Registers and the LED Control Registers will be stored in temporary registers. A write operation of "0000 0000" value to the Update Register is required to update the registers (01h~24h, 26h~49h).

Table 5 26h~49h LED Control Register (OUT1~OUT36)

Bit	D7:D3	D2:D1	D0
Name	-	SL	OUT
Default	00000	00	0

The LED Control Registers store the on or off state of each LED and set the output current.

Registers Definition（Continued）

SL Output Current Setting (IOUT)
00 IMAX
01 IMAX/2
10 IMAX/3
11 IMAX/4

OUT LED State
0 LED off
1 LED on

Table 6 4Ah Global Control Register

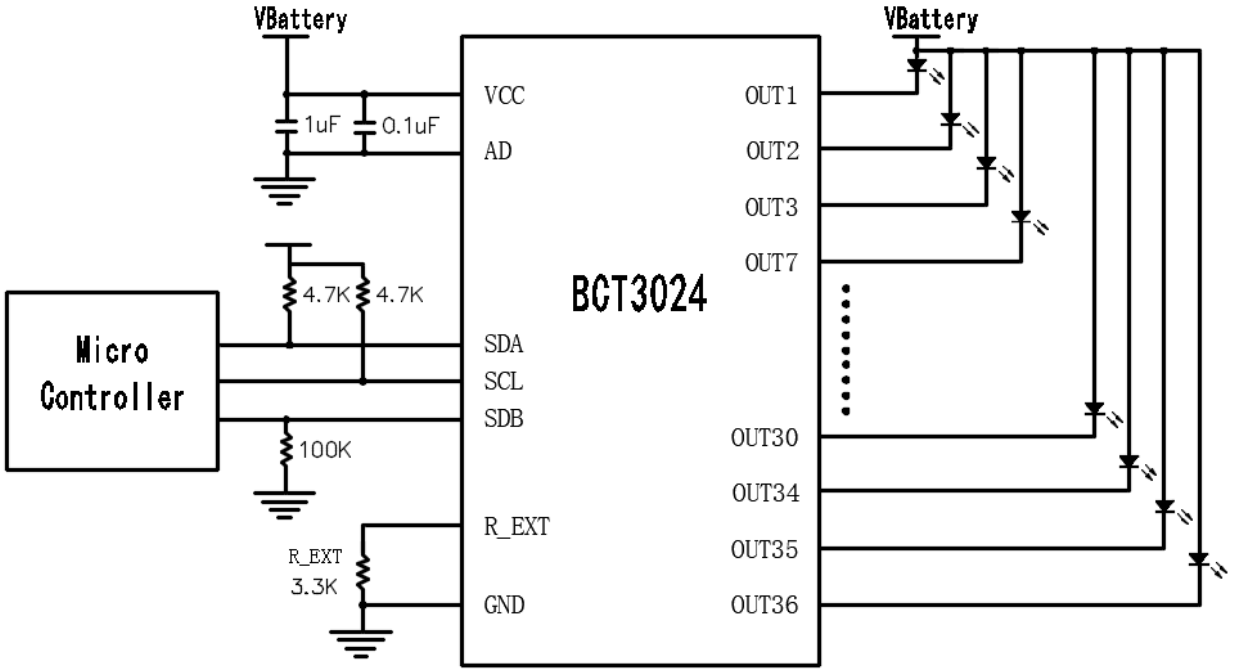
Bit	D7:D1	D0
Name	-	G_EN
Default	0000 000	0

The Global Control Register set all channels enable.

G_EN Global LED Enable
0 Normal operation
1 Shutdown all LEDs

4Fh Reset Register
Once user writes “0000 0000” data to the Reset Register, BCT3024 will reset all registers to default value.
On initial power-up, the BCT3024 registers are reset to their default values for a blank display.

TYPICAL APPLICATION CIRCUIT

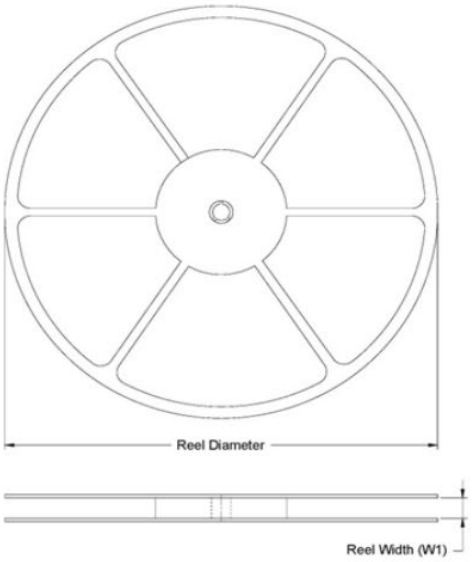


Note 1: The maximum global output current is set up to 23mA when REXT = 3.3kΩ. The maximum global output current can be set by external resistor REXT, IMAX=76/REXT

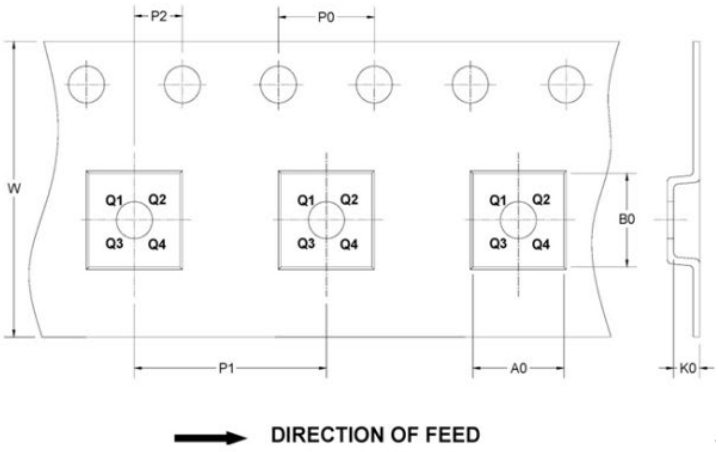
Note 2: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

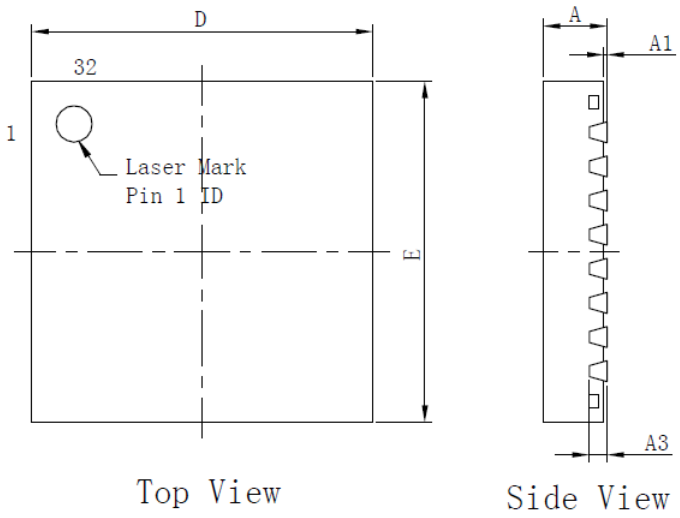


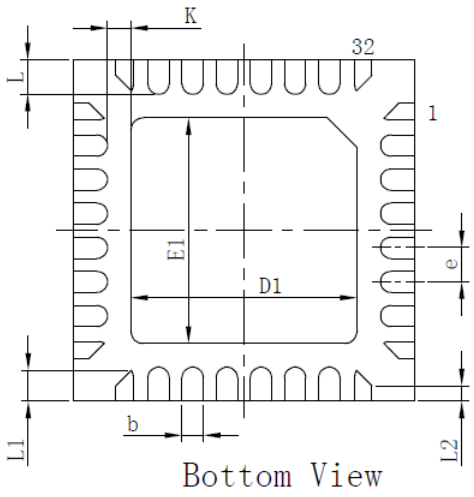
KEY PARAMETER LIST OF TAPE AND REEL

Device Name	Package Type	Reel Diameter	Unit: mm								Pin 1 Quadrant	Reel Q'ty
			Reel Width W1	A0	B0	K0	P0	P1	P2	W		
BCT3024EGJ-TR	QFN4x4-32L	13"	13.5	4.25	4.25	1.05	4.00	8.00	2.00	12.00	Q1	4000

PACKAGE INFORMATION

QFN4x4-32L





尺寸 / 标注	最小	标准	最大	尺寸 / 标注	最小	标准	最大
A	0.70	0.75	0.80	E1	2.55	2.65	2.75
A1	0.00	—	0.05	e		0.40TYP	
A3		0.203REF		K	0.20	–	–
b	0.15	0.20	0.25	L	0.30	0.40	0.50
D	3.90	4.00	4.10	L1	0.31	0.36	0.41
E	3.90	4.00	4.10	L2	0.13	0.18	0.23
D1	2.55	2.65	2.75				

Note:

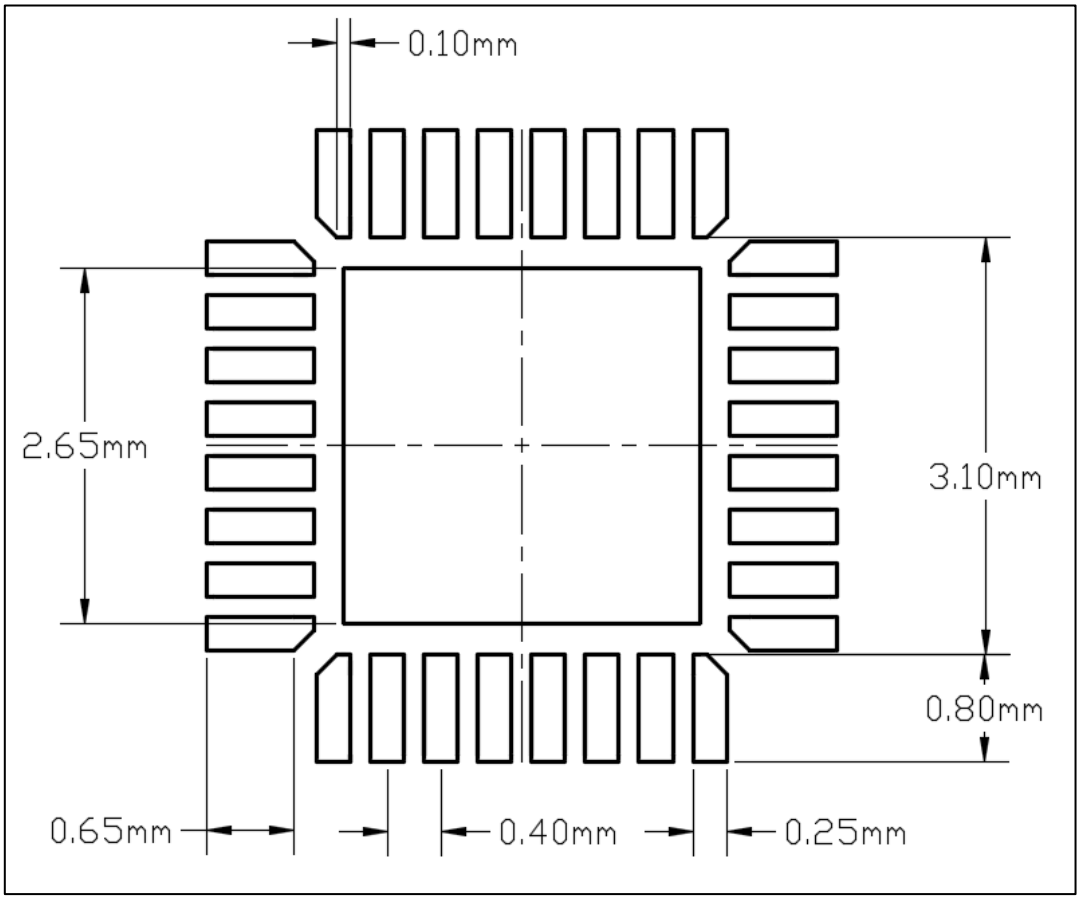
1.Controlling dimension: MM

2.Reference document: na close tool

3.The pin's sharp and thermal pad shows different sharp among different factories.

RECOMMENDED LAND PATTERN

QFN4x4-32L



Note:

1.Land pattern complies to IPC-7351.

2.This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.