BCM56990

25.6-Tb/s Multilayer Switch

Overview

The Broadcom® BCM56990 device is a class of high-radix, high-bandwidth network switching devices supporting up to 64 × 400GbE, 128 × 200GbE, 256 × 100GbE, 256 × 40GbE, 256 × 25GbE, or 256 × 10GbE ports. The device features a maximum of 64 integrated Blackhawk7 SerDes cores, each with eight integrated 56-Gb/s PAM4 SerDes transceivers and associated PCS for native support of numerous physical connectivity options, enabling a broad range of media, speed, and reach. The BCM56990 delivers high-bandwidth, glueless network connectivity up to 25.6 Tb/s on a single chip.

The BCM56990 is a high-performance and high-capacity device designed to meet the requirements for next-generation data center and cloud computing environments. The BCM56990 architecture delivers complete L2 and L3 switching, routing, and tunneling capabilities at line rate and maximum port density, with low power and latency. Software compatibility is maintained across the StrataXGS® product portfolio to simplify customer designs and reduce customer time-to-market.

As server interfaces transition to higher Ethernet speeds and virtualization continues to increase link utilization, data center networks demand switches with dense 10GbE to 400GbE connectivity at the edge and aggregation layers. With up to 512 50G PAM4 SerDes and flexibility in configuring 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE ports, a single BCM56990 switching chip can be used to build scalable, cost-effective leaf, spine, Top of Rack (ToR), blade, and aggregation switches across the entire data center.

The BCM56990 has extensive features to address the rapidly increasing scale of data center network deployments and distributed computing applications. The following list highlights some of the BCM56990 features:

- Large forwarding databases
- Powerful load balancing
- Extensive support for streaming and inband telemetry
- Advanced congestion management
- Robust buffer performance including many-to-one burst absorption capabilities that assist in TCP incast scenarios

With the BCM56990 device, customers can build data centers with much higher server node counts while simultaneously improving per-port power efficiency. The BCM56990 is built using state-of-the-art silicon process technology and incorporates advanced power-management features to minimize power based on the features in use.

Applications

- Data center spine, leaf, ToR, blade, and aggregation switching
- Mobile core switches
- Cloud computing
- Large-scale enterprise campus backbone
- Service provider core switching

Features

General features

- 512 × 50G PAM4 SerDes configuration.
- Flexible port configurations: 10GbE to 400GbE support with run-time reconfigurability (Flexport™).
- Oversubscription to maximize I/O throughput.
- Low pin-to-pin latency in cut-through and store-and-forward modes.
- Supports IEEE 802.3bj Clause 91 forward error correction (FEC), IEEE 802.3bj Clause 93 100GbE-KR4 transmit training, and IEEE 802.3ap Clause 72 10G-KR transmit training.

Data center features:

- Hardware-based encapsulation.
- Data center bridging capability exchange protocol (DCBX) congestion management: priority-based flow Control (PFC) and Enhanced Transmission Selection (ETS).
- IEEE 802.1Qbg Edge Virtual Bridging and IEEE 802.1Qbh Bridge Port Extension support.
- Support for VxLAN.
- Per virtual machine traffic shaping.

L2 and L3 packet processing:

- Full IPv4 and IPv6 routing support.
- Hardware-based encapsulations, including Multiprotocol Label Switching (MPLS), generic routing encapsulation (GRE), and Intra-Site Automatic Tunnel Addressing Protocol (ISATAP).
- Three-stage field processing with ingress field processor (IFP) stage support for the exact-match feature.
- Unified forwarding table for flexible allocation of L3 host, longest prefix match (LPM) entry, IFP key compression entry, and IFP Exact Match entry.
- Flexible ingress and egress counter pools.

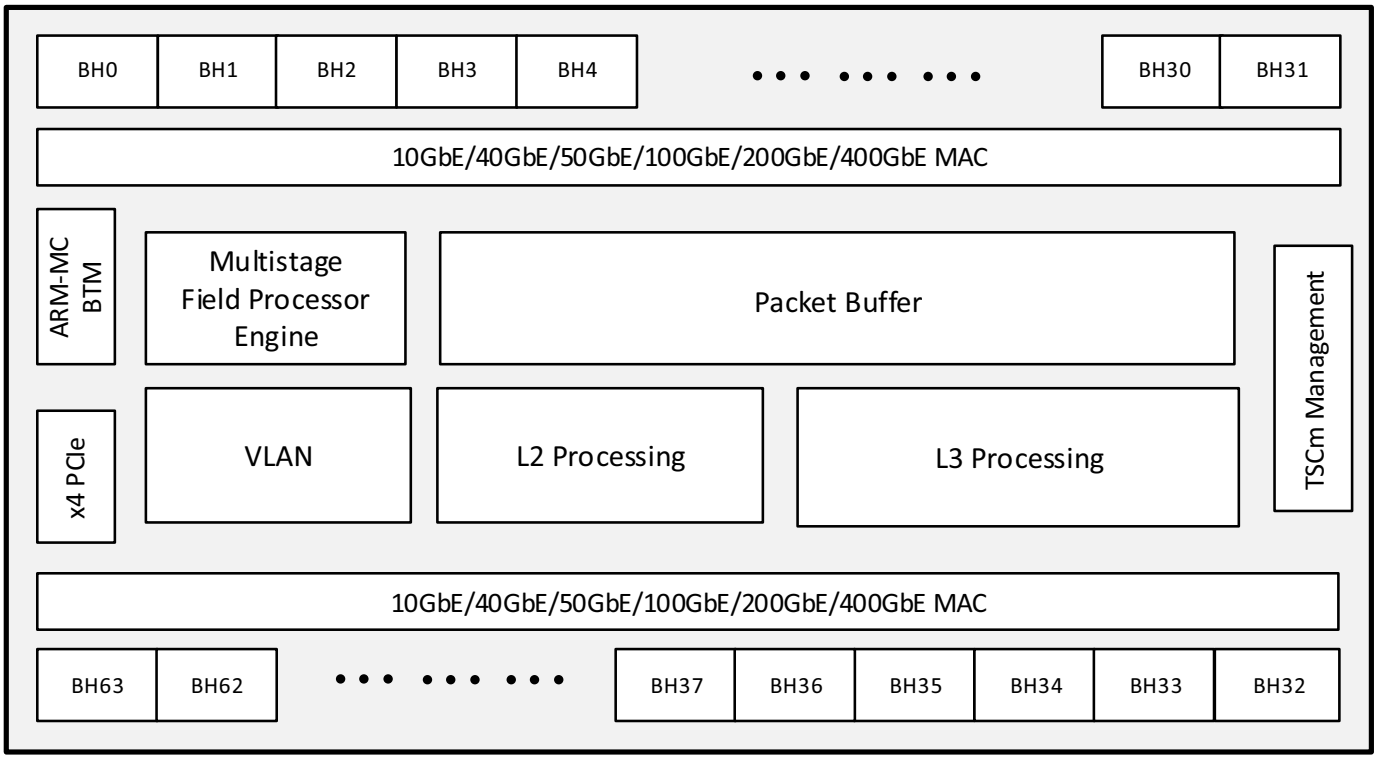
Buffering and traffic management:

- Integrated high-performance SmartBuffer memory for maximum burst absorption and service guarantees.
- Full Quality of Service (QoS) support:
  - Priority flow control (PFC).
  - Weighted random early discard (WRED).
  - Single-rate Three Color Marking (srTCM) and Two-rate Three Color Marking (trTCM) for color marking and metering.
- Congestion management capabilities including destination module flow control and ECN.
- Dynamic load balancing for equal cost multipath (ECMP) groups in Hierarchical ECMP load balancing.
- Packetized memory management unit (MMU) statistic.
- Network monitoring.
- Network congestion detection.
- sFlow redirect.
- Visibility and packet tracing.
- Transient capture buffer.
- Enhanced load balancing.
- Enhanced trunk hashing capabilities: RTAG7, symmetric hash, flex hash, and resilient hash.
- Support for jumbo frames up to 9416 bytes.
- Support for 12 queues per port and the following scheduling algorithms: strict priority (SP), round-robin (RR), weighted round-robin (WRR), and weighted deficit round robin (WDRR).

Additional features:

- Comprehensive time synchronization support:
  - Integrated IEEE 1588v2 processor.
  - IEEE 802.1AS support.
  - Synchronous Ethernet (SyncE).
  - Ingress and egress per packet times stamping.
- sFlow support including ingress, egress, and flex sampler, with an option to forward truncated sFlow packets to a remote agent.
- Two dedicated 10G auxiliary Ethernet ports can be used for management.
- x4 PCI Express (PCIe) Gen3 interface to support a local CPU.
- Adjustable voltage scaling (AVS) for reduced average and peak power.
- Scalable StrataXGS architecture supports high-performance fixed and modular switch designs.

Figure 1: 25.6-Tb/s Multilayer Switch



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Chapter 1: Introduction

The Broadcom BCM56990 device has the I/O bandwidth and throughput shown in the following tables.

NOTE: The BCM56990 supports SerDes controller cores Blackhawk7 (BH7), which is PAM4-based, and Merlin (TSCm).

Table 1: BCM56990 I/O Bandwidth and Throughput

Device	I/O Bandwidth (Tb/s)	Number of Blackhawk7 Cores	Number of Dedicated Management Ports	Typical Configuration
BCM56990	25.6	64	2	64 × 400G, 256 × 100G

The BCM56990 includes the configurations described in the following table.

Table 2: BCM56990 Device Port Configurations

Device	400 Gb/s	200 Gb/s	100 Gb/s	50 Gb/s	10 Gb/s
BCM56990	64 maximum	128 maximum	256 maximum	256 maximum	256 maximum

The BCM56990 supports a maximum of 256 front-panel ports by using 64 Blackhawk7 SerDes cores in the data path's sixteen pipelines. The front-panel ports can be configured as Ethernet ports or HiGig3™ (HG3) ports. Additionally, the device contains one Merlin SerDes core that can support a maximum of two auxiliary ports. The Merlin core consists of four SerDes lanes. If an auxiliary port is configured in single SerDes lane mode, lane 0 or lane 2 should be used. If the port is configured in Reduced Pin Extended Attachment Unit Interface (RXAUI) mode, either lanes 0 and 1, or lanes 2 and 3 should be used. If a single auxiliary port is used, the four-lane 10 Gigabit Attachment Unit Interface (XAUI) port mode should be used. The device also supports a four-lane PCIe interface that can be operated at Gen1, Gen2, and Gen3 speeds. The PCIe interface is typically connected to the root complex of the host CPU as an x1, x2, or x4 PCIe Gen1, Gen2, or Gen3 interface.

Chapter 2: Device Overview

The BCM56990 has a modular, high-performance packet-switching architecture and provides the following benefits:

- Flexible port configurations
- Scalable throughput
- Scalable packet processing features
- Low pin-to-pin latency

2.1 Feature List

The following table lists the BCM56990 features.

Table 3: BCM56990 Features

Feature	Description
Configuration	■ 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE multilayer Ethernet or HiGig3 switch. ■ All ports operate in oversubscription mode. ■ Flexible SerDes contains eight SerDes lanes per Blackhawk7, configured to operate in any of the following configurations: – 10GbE (1-lane) – 25GbE (1-lane) – 40GbE (4-lane) – 50GbE (1-lane) – 50GbE (2-lane) – 100GbE (2-lane) – 100GbE (4-lane) – 200GbE (4-lane) – 400GbE (8-lane)
L2 Switching	■ L2 learn cache for software-based learning. ■ Software-based MAC address aging. ■ Ethernet/IEEE 802.3 frame-size support (64 bytes to 1522 bytes) and jumbo frame support of up to 9416 bytes. ■ Reserved MAC address table for CPU control packets, bridge protocol data units (BPDUs), and the ability to perform shared VLAN switching.
L2 Multicast	Three port-filtering modes (PFM) to control multicast packet behavior.
VLAN	■ Supports 4K VLANs. ■ Supports up to 128 VLAN profiles on a per-VLAN basis. ■ Assigns VLAN for untagged and priority tagged packets based on ports (port-based VLANs). ■ Ingress filtering for IEEE 802.1Q VLAN security.
Spanning Tree Group Table	Indicates spanning tree state of each port for each spanning tree group.

Table 3: BCM56990 Features (Continued)

Feature	Description
Mirroring	■ Ingress and egress mirroring support. ■ Four mirror-to-port (MTP) ports are supported. They are shared by ingress and egress mirroring logic. The device can support any combination of four mirroring port types. ■ A separate packet is created for each MTP port. ■ MTP receives unmodified packet for ingress mirroring. ■ MTP receives modified packet for egress mirroring. ■ Remote switched port analyzer (RSPAN) mirroring, VLAN mirroring, flow mirroring. ■ Encapsulated remote switched port analyzer (ERSPAN) mirroring into a GRE tunnel. ■ Multiple packets can be generated in the StrataXGS architecture: one packet for the switched copy, and four mirror copies that can be of any type. ■ Payload zeroing and truncation for mirrored copies.
DSCP	■ Per-port differentiated services code point (DSCP) remarking. ■ DSCP remarking based on a filter processor (FP) filter match. ■ DSCP-to-IEEE 802.1p mapping. ■ Remap incoming DSCP to new outgoing DSCP.
Layer 3 Routing (IPv4 and IPv6)	■ Native support for IPv4 and IPv6 unicast and multicast routing. ■ Direct-attached hosts in the L3 table. ■ LPM-based routing. ■ ECMP and weighted-cost multipath (WCMP) routing: ECMP path resolution based on source IP address, protocol, IPv6 flow label, and TCP/UDP port. ■ Software-based aging support. ■ Routing of IPv6 packets. ■ True 128-bit IPv6 support as well as /64 support for LPM.
Virtual Routing and Forwarding (VRF)	■ Segmentation of L3 routing tables. ■ Virtual private network (VPN) ID assigned based on ingress port, VLAN, or flow.
IP Multicast	■ Simultaneous L2 bridging and L3 routing. ■ Flexible multicast packet replication. ■ Optional source port checks. ■ Dual lookup: {S, G, V} and {*, G, V}. ■ Ability to fall back to L2 multicast lookup on IP multicast (IPMC) miss. ■ Port filter mode (PFM) per VLAN for L2 multicast, IPv4 multicast, and IPv6 multicast packets. ■ Control trapping of unknown IPMC packets to CPU on a per VLAN, per IP-type basis. ■ IP multicast address consistency check with destination MAC address.
IPv6 Tunneling	■ IPv6-in-IPv6: The outer header is IPv6, and the payload is IPv6. ■ IP-in-IPv6 tunnel: The outer header is IPv6, and the payload is IPv4.
GRE Tunneling	■ Supports IPv4 as payload. ■ Supports IPv6 as payload.
Preclassification VLAN Field Processor (VFP)	■ 512 entries. ■ Rules for assignment of VLAN based on flexible criteria, block packets, bind MAC address with IP address, and assign VRF ID. ■ Supports single-wide and double-wide modes. ■ Field selectors on per port, per slice, and per packet type basis. ■ Ability to add or replace VLAN tag, change priority, assign classification ID, and drop.
Protection Switching	Dedicated hardware support for the following: ■ MPLS fast reroute (FRR). ■ Per next hop (Layer 3).

Table 3: BCM56990 Features (Continued)

Feature	Description
Ingress Field Processor (IFP)	IFP supports the following rules for L2 through L7 packet classification on ingress access control lists (ACLs), ingress metering, and ingress statistics: ■ 3K entries per pipe: 160-bits per entry. ■ Nine logical slices allowing nine parallel lookups and matches. ■ Supports 16 logical tables. ■ Parses 190-bytes deep into packet. ■ ACL-based policing. ■ Ingress port-based filtering with a maximum of 18 IFP ports per pipeline. ■ Multiple lookups, matches, and actions per packet. ■ MAC destination address remarking. ■ Class-based marking for service-level agreements (SLAs). ■ Traffic class definition based on the filter. ■ Classification of different packet formats (IPv6, IPv4, HTLS, IEEE 802.1Q, Ether II, and IEEE 802.3). ■ Supports single-wide and double-wide mode for IPv6 filtering. ■ TCP and UDP source and destination port number range checking. ■ Filtering IP packets with options. ■ Metering support on ingress ports and CPU queues. ■ Programmable meters allow policing of flows. ■ Dual leaky bucket meters support srTCM, trTCM, and modified trTCM (RFC2697, RFC2698, and RFC4115). ■ Metering granularity from 8 Kb/s to 1 Mb/s. ■ Per-port, per-slice, and per-packet type field selection. ■ Filter on multistage classifier classification ID, source MAC classification ID, or VRF ID.
Egress Field Processor (EFP)	EFP supports the following rules for packet classification on egress ACLs and egress statistics: ■ 512 entries. ■ Parses 128-bytes deep into packet. ■ Filter on fully modified packets allowing egress ACLs. ■ Filter on modified L3 routed and IPMC replicated packets. ■ Keys based on L2 through L4 fields for IPv4 and IPv6 packets: ■ Actions: drop, change DSCP, change inner or outer priority, change inner or outer VLAN ID, change outer, and tag protocol identifier (TPID). ■ Byte-based and packet-based statistics.
Port Security	■ Supports IEEE 802.1X. ■ Blocking of egress ports on per-MAC address basis. ■ Blocking of egress ports, on a per-VLAN basis, for broadcast, unknown unicast, and multicast packets.
BroadShield™: Denial-of-Service (DoS) Attack Prevention	■ Built-in illegal address check (IPv4 and IPv6). ■ Land packets (source IP = destination IP). ■ Null scan (TCP sequence number = 0, control bits = 0). ■ Ping flood (flood of ICMP packets). ■ SYN/SYN-ACK flooding. ■ SYN with sPort < 1024. ■ Smurf attack. ■ Individual control over handling of DoS packet.
BroadShield HPAE	■ Limits access based on source or destination MAC address, and source or destination IP address. ■ Detection Dynamic Host Configuration Protocol (DHCP) snooping and IP address snooping. ■ Classification of groups based on L2 through L4 field.

Table 3: BCM56990 Features (Continued)

Feature	Description
CPU Protocol Packet Processing	■ Ability to control CPU protocol packet handling individually, including BPDU, Address Resolution Protocol (ARP), Internet Group Management Protocol (IGMP), Multicast Listener Discovery (MLD), and DHCP. ■ Individual control of trapping protocol packets and setting internal priority. ■ Extensive control of handling of IGMP and MLD packet types.
QoS	■ Shared unicast (UC) and multicast (MC) queues (12 per port). ■ VLAN shaping support. ■ 48 CoS queues for CPU. ■ Three drop precedence colors. ■ Per-port, per-CoS drop profiles. ■ Minimum and maximum bandwidth guarantee (shaping) per CoS, per port. ■ Traffic shaping available on CPU queues: bandwidth based and packet-per-second based. ■ Programmable priority to CoS queue mapping. ■ Provides two levels of drop precedence per queue. ■ Explicit Congestion Notification (ECN) support. ■ SP, WRR, and WDRR mechanism for shaped queue selection. ■ PFC. ■ Linear programming of bucket size of egress port shaping and CoS shaping. ■ Supports ingress port rate-based policing and pause flow control. ■ Mapping of incoming priority, CFI to outgoing priority and drop precedence.
Memory Management Unit	■ Integrated SmartBuffer. ■ Transition cut-through switching for low latency. ■ Static and dynamic memory allocation. ■ Programmable transmit queue thresholds. ■ Ingress cell triggers for back pressure. ■ Cell and packet thresholds for triggering head-of-line (HOL) blocking prevention. ■ WRED congestion control.
Port Table	Per-port configuration settings and attributes (for example, L2 learning, port discards, VLAN handling, and priority assignment).
IEEE 802.1bb PFC	Enables per-priority flow control, so that a low-priority application that is causing congestion can be throttled without impacting higher priority or loss-sensitive applications.
IEEE 802.1az Enhanced Transmission Selection (ETS)	Enables per-priority group minimum bandwidth guarantees.
Flexible Counters	■ Programmable packet and byte RX and TX counters for forwarding addresses (such as MAC, IP, and MPLS). ■ Programmable packet and byte RX and TX counters for service instances (VLAN, VRF, and so on).
Management Information Base (MIB)	■ sFlow support, RFC 3176. ■ Remote Network Monitoring (RMON) MIB Extensions for Switched Networks (SMON), IETF RFC 2613. ■ RMON statistics group, IETF RFC 2819. ■ SNMP interface group, IETF RFC 1213, 2836. ■ Ethernet-like MIB, IETF RFC 1643. ■ Ethernet MIB, IEEE 802.3u. ■ Bridge MIB, IETF RFC 1493.
Oversubscription	■ Clock frequency is set to match the aggregated port bandwidth assumed under application-worst-case loading conditions. ■ Reduces peak power based on system traffic loading and packet length mix assumptions.
Low-Latency Mode	This is the default mode of operation and uses the maximum allowable internal clock rates, resulting in the highest power. It is possible to reduce the internal clock rates, trading off higher latency versus lower power.

Table 3: BCM56990 Features (Continued)

Feature	Description
IP Multicast	■ Simultaneous L2 bridging and L3 routing. ■ Flexible multicast packet replication. ■ Optional source port checks. ■ Dual lookup: {S, G, V} and {*,G, V}. ■ Protocol-Independent Multicast (PIM): PIM Sparse Mode (PIM-SM), PIM Dense Mode (PIM-DM), and PIM Source Specific Multicast (PIM-SSM) for encapsulation. ■ DVMRP on a per-VLAN basis. ■ Reverse path forwarding checks. ■ Ability to fall back to L2 multicast lookup on IPMC miss. ■ Port filtering mode (PFM) per VLAN for L2 multicast, IPv4 multicast, and IPv6 multicast packets. ■ Controls trapping of unknown IPMC packets to CPU on a per VLAN, per IP-type basis. ■ IP multicast address consistency check with destination MAC address.
Tunnel Encapsulation and Deencapsulation	■ IPv6 to IPv4. ■ ISATAP. ■ Configured tunnels. ■ IP-IP (mobile-IP) tunnels. ■ MPLS.
Network Time Sync	Packet-based time synchronization (IEEE 1588 and IEEE 802.1AS): ■ Integrated IEEE 1588 v2 processor for running Precision Time Protocol (PTP) stack and clock recovery servo. ■ One-step and two-step time stamping. ■ High-precision frequency synthesizer. ■ Synchronous Ethernet layer-one clock recovery. PTP: ■ Transparent clock. ■ Boundary clock.
Resilient and Versatile Hashing	■ Provides the same resource isolation attributes of consistent hashing. ■ Minimizes the imbalance among resources within the same resource group when adding or deleting load-balancing resources.
Overtemperature Protection	Supports real-time temperature monitoring and the ability to set temperature for interrupt.
In-band Network Telemetry	Supports insertion of metadata in packets for identifying network faults and isolating their location, transient failures, congestion information, and latency.
PSAMP	Samples the packets from a network device, and the transmission of samples to a collector device, with the appropriate meta-data.
ECMP Group Dynamic Load Balancing with Flow Monitoring	■ Randomly samples packets undergoing dynamic load balancing (DLB) and copy-to-CPU. ■ Samples the packet to mirror or the CPU when macroflow assignment or re-assignment occurs.
Stacking and Chassis	Supports HiGig3 in transit mode only.

The following table lists BCM56990 device scalability.

Table 4: BCM56990 Device Scalability

Feature	BCM56990
I/O Bandwidth	25,600G
Number of SerDes	512 × 50G
Integrated Packet Buffer Memory	113.66 MB
MAC Entries	8K for exact match 128K without exact match.
L2MC	512 **NOTE:** Can be increased to 1K if L3MC is not used and IFP rules are added.
Blackhawk7 Cores	64
VLAN	4K
Source Virtual Ports	8192
Virtual Forwarding Instances (VFI)	8192
VRF	8192
L3 Hosts/LPM – Merged with Unified Forwarding Table (UFT) and Algorithmic Longest Prefix Match (ALPM)	Without Exact Match: ■ Algorithmic LPM (v4): 850K ■ Algorithmic LPM (v6_64): 360K ■ Algorithmic LPM (v6_128): 240K With Exact Match: 64K ■ Algorithmic LPM (v4): 5K ■ Algorithmic LPM (v6_64): 2K ■ Algorithmic LPM (v6_128): 1K
L3 Multicast groups	512
Field Processor Total Rules/Slices	
Preingress	512/4 (512 per pipe)
Ingress	3K/9 (3K per pipe)
Egress	512/4 (512 per pipe)
ECMP groups	4096 maximum
ECMP Members per Group	4K maximum
Total ECMP Group Members	64K
Ports per Modules	256 front panel ports

Table 5: Device Table Lookup Size

Table	Depth	Description
DSCP_TABLE	4096	DSCP table.
EFP_POLICY_TABLE	512	Policy table for determining actions in the EFP.
EGR_DSCP_TABLE	4096	Egress DSCP table to select the new DSCP for outer tunnel header packets (64 entries for each of the 128 profiles).
EGR_GPP_ATTRIBUTE	136	Egress global physical port (GPP) attribute table, feature-specific Ethernet.
EGR_IP_TUNNEL	8192	Egress IP tunnel table. Makes new tunnel headers.
EGR_IPMC	512	Per-IPMC group attributes needed in EP.
EGR_L3_INTF	8192	L3 interface table.

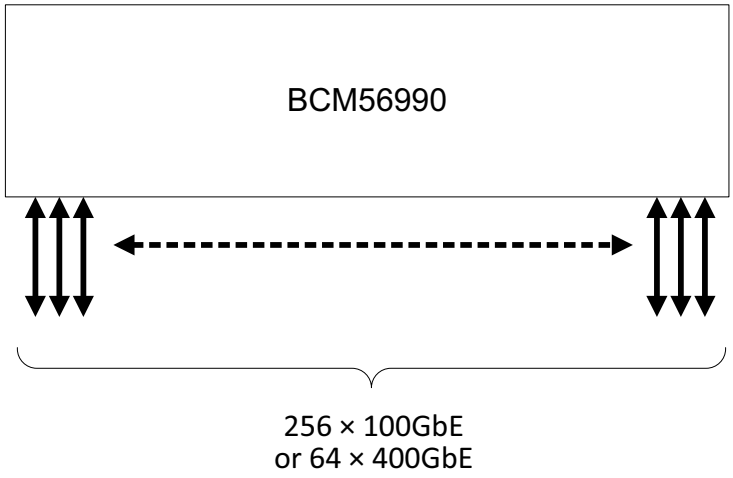
Table 5: Device Table Lookup Size (Continued)

Table	Depth	Description
EGR_L3_NEXT_HOP	32768	Egress L3 next-hop table.
EGR_VLAN_STG	64	Egress spanning tree state table.
IFP_METER_TABLE	512	Per-pipe meter table structures for the IFP.
IFP_POLICY_TABLE	3072	Per-pipe policy table for determining actions in the IFP.
ING_L3_NEXT_HOP	32768	L3_NEXT_HOP table.
L2_ENTRY	8192	L2_ENTRY_SINGLE table combined mac_address and VID/VFI or VNTAG or ETAG or TREE_ID (TRILL) or VSAN_ID (FCoE).
	131072	New mode where all UFT banks are dedicated for L2_ENTRY to get higher scale. Either classic 8K table or the 128K table can be used. Mixed mode is not supported.
L2_ENTRY_UFT_SINGLE	131072	Combinations of mac_address and VID/VFI or VNTAG or ETAG or TREE_ID (TRILL) or VSAN_ID (FCoE).
L2_USER_ENTRY	256	Combined L2_ENTRY TCAM and data RAM for guaranteed L2 entries and BPDUs.
L2MC	512	L2 multicast table.
L3_ECMP	16384	L3 equal cost multipath table.
L3_IIF	8192	L3 input interface properties.
L3_IPMC	512	L3 IPMC table.
L3_TUNNEL_SINGLE	16384	Single L3 tunnel table Ternary Content Addressable Memory (TCAM).
L3_TUNNEL_DOUBLE	8192	Double L3 tunnel table TCAM.
L3_TUNNEL_QUAD	4096	Quad L3 tunnel table TCAM.
MPLS_ENTRY_SINGLE	16384	MPLS label single lookup. Dual-hash table with keys and data.
PROT_NHI_TABLE	256	Protection switching next hop table.
SOURCE_TRUNK_MAP_TABLE	272	Source trunk map table.
VFP_POLICY_TABLE	1024	Policy table for determining actions in the VLAN Filter Processor (VFP).

2.2 Target Applications: 100GbE, 200GbE, or 400GbE Aggregation Switch

Data center switching represents a fast-growing segment of the Ethernet switching market and is the primary driver behind 100GbE, 200GbE, and 400GbE port growth. Data centers are where computer resources (servers or blade chassis) are centralized and managed in a structured way utilizing high-efficiency Ethernet or HiGig3 connectivity. A single 64 × 400GbE, 128 × 200GbE, or 256 × 100GbE aggregation switch (as shown in the following figure) can be built using a single BCM56990 device.

Figure 2: 64 × 400GbE Aggregation Switch



Chapter 3: System Interfaces

This section provides a brief functional description of BCM56990 interfaces. The signal descriptions and AC and DC timing sections provide the electrical description of each interface in more detail.

NOTE: For more information about the interfaces that support Broadcom-proprietary logical protocols, refer to the *BCM56990 Theory of Operation* (56990-PG1xx).

The BCM56990 external interfaces are described in the following table.

Table 6: BCM56990 External Interfaces

Interface	Description
50G Blackhawk7 Octal SerDes	■ Integrated octal 50G PAM4 or NRZ SerDes core for front-panel ports. ■ 400GbE ■ 200GbE ■ 100GbE ■ 50GbE ■ 40GbE ■ 25GbE ■ 10GbE **NOTE:** Does not support 1G. ■ Supports full-duplex operation (half-duplex is not supported at any speed).
10G Merlin Quad SerDes	■ Integrated SerDes core for management ports. Supports up to two ports, lanes 0 and 2 only. ■ 40GbE: XAUI, RXAUI, CR4, and KR4. ■ 10GbE: XFI, SFI, KR, CR, XAUI, and RXAUI. ■ 2.5GbE: 2500BASE-X. ■ 1GbE: 10 Mb/s, 100 Mb/s, and 1000 Mb/s SGMII, and 1000BASE-X ■ Supports full-duplex operation (half-duplex is not supported at any speed).
CPU (PCIe)	■ x4 PCIe v3.0-compliant interface. ■ Scatter-gather direct memory access (DMA) for packet transfer to CPU. ■ Table DMA for copying any switch table into system memory. ■ Statistics DMA for gathering on-chip statistics counters. ■ Packet DMA for transferring packets from and to the CPU.
LED	■ Integrated on-chip controller for up to 512 system LEDs at a 30-Hz refresh rate. ■ Simple micro-controller implementation with instructions optimized for LED control. ■ Low-cost two-wire interface to system LEDs. ■ 512 bytes of program RAM. ■ 512 bytes of data RAM. ■ LED micro controller has direct hardware access to per-port speed, duplex state, flow control state, link state, and transmit and receive activity.
Media Independent Interface Management (MIIM)	■ IEEE 802.3u-compliant MIIM interface for communication with external PHY devices. ■ 2.5 MHz operation. ■ Compliant to CL22 and CL45.
BSC	■ CPU-controlled master mode to communicate with other NXP I^2C-compatible devices.
JTAG	■ JTAG-compliant interface supports boundary scan operations. ■ 12.5 MHz operation.

Table 6: BCM56990 External Interfaces (Continued)

Interface	Description
BroadSync®	■ Packet-based time synchronization support: IEEE 802.1AS and IEEE 1588. ■ Provides time-of-day synchronization to grand master clock source. ■ Master mode to accept time-of-day information from a grand master clock source. ■ Slave mode to externalize the time-of-day information to an external device.
AVS or recommended operating voltage (ROV)	■ AVS or ROV pins. This interface connects to system power supply control pins to scale core input voltage to the device at the appropriate level to optimize device's power consumption.

3.1 Blackhawk7 SerDes

The Blackhawk7 SerDes is the versatile physical layer interface for the BCM56990, and it is specifically designed to support up to 400 Gb/s. This serial interface supports the following features:

- Octal SerDes block supporting eight serial links.
- Support for data rates of 10.3125 Gb/s up to 56.25 Gb/s per serial link.

The BCM56990 device incorporates PAM4-based SerDes cores that allow the device to support low-latency throughput, oversubscription capability, and Flexport configuration. The BH7 macro consists of the digital control logic and a Blackhawk7 analog block. The terms BH, BH7, TSC, and Blackhawk7 are used interchangeably in this document.

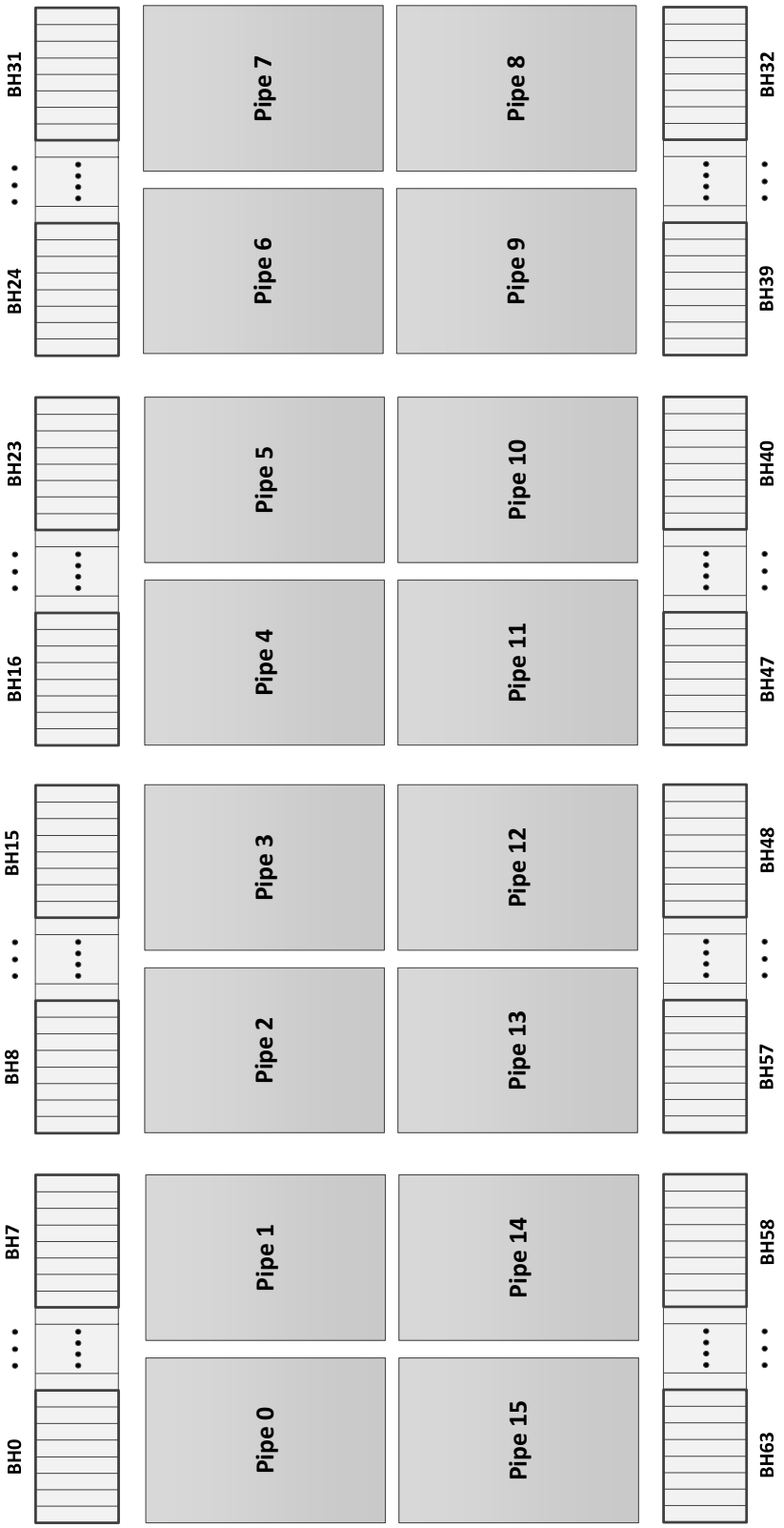
The BCM56990 device has 64 Blackhawk7 cores. Each Blackhawk7 contains eight SerDes lanes. Each Blackhawk7 lane can be configured as a single individual port, or multiple lanes can be aggregated into an single port.

The 64 Blackhawk7 cores in the device are separated into the following sixteen pipes:

- Pipe-0: Blackhawk7 [31:0]
- Pipe-1: Blackhawk7 [63:32]
- Pipe-2: Blackhawk7 [95:64]
- Pipe-3: Blackhawk7 [127:96]
- Pipe-4: Blackhawk7 [159:128]
- Pipe-5: Blackhawk7 [191:160]
- Pipe-6: Blackhawk7 [223:192]
- Pipe-7: Blackhawk7 [255:224]
- Pipe-8: Blackhawk7 [287:256]
- Pipe-9: Blackhawk7 [319:288]
- Pipe-10: Blackhawk7 [351:320]
- Pipe-11: Blackhawk7 [383:352]
- Pipe-12: Blackhawk7 [415:384]
- Pipe-13: Blackhawk7 [447:416]
- Pipe-14: Blackhawk7 [479:448]
- Pipe-15: Blackhawk7 [511:480]

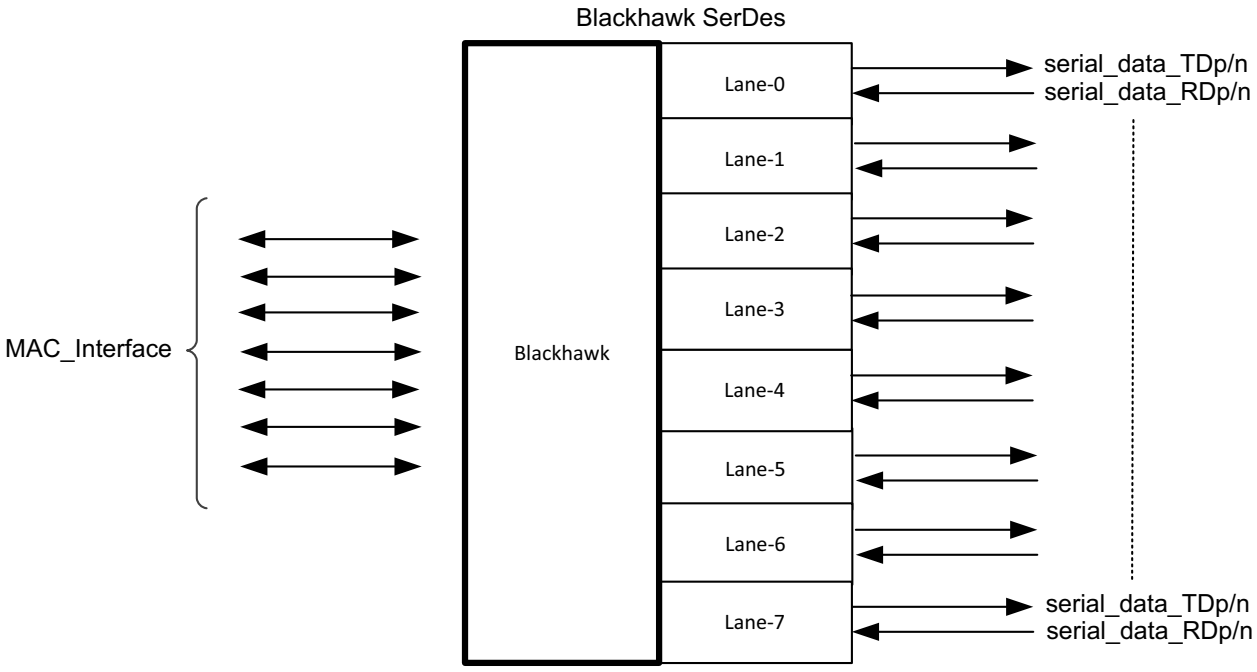
The device contains 64 Blackhawk7 cores divided into 16 pipes of four Blackhawk7 cores, which enables up to 25,600G of I/O bandwidth. See the following figure for the Blackhawk7 configuration within each pipe.

Figure 3: Blackhawk7 (BH) Configuration



The following figure is a conceptual view of the relation of the Blackhawk7 block within the device. The number of Blackhawk7 cores supported depends on the device part number.

Figure 4: Conceptual View for Blackhawk7, Eight SerDes Lanes



The following table shows the different Blackhawk7 configurations.

Table 7: Blackhawk7 Configurations

Port Speed	Interface Type	Logical Lane Type	Physical Lanes	FEC	Signaling Mode
400G	400GAUI-8 (C2C, C2M) 400GBASE-KR8 400GBASE-CR8	FEC	8	RS544	26.5625G PAM4
		FEC	8	RS272	26.5625G PAM4
200G	200GAUI-4 (C2C, C2M) 200GBASE-KR4 200GBASE-CR4	FEC	4	RS544	26.5625G PAM4
		FEC	4	RS272	26.5625G PAM4
		PCS/VIRTUAL	4	None	25.78125G PAM4
100G	100GAUI-2 (C2C, C2M) 100GBASE-KR2 100GBASE-CR2	FEC	2	RS544	26.5625G PAM4
		FEC	2	RS272	26.5625G PAM4
		PCS/VIRTUAL	2	None	25.78125G PAM4
		FEC	2	RS528	25.78125G PAM4
	100GAUI-4 (C2C, C2M) 100GBASE-KR4 100GBASE-CR4	FEC	4	RS544	26.5625G NRZ
		FEC	4	RS528	25.78125G NRZ
		PCS/VIRTUAL	4	None	25.78125G NRZ

Table 7: Blackhawk7 Configurations (Continued)

Port Speed	Interface Type	Logical Lane Type	Physical Lanes	FEC	Signaling Mode
50G	LAUI-2 (C2C, C2M) 50GAUI-2 (C2C, C2M) 50GBASE-KR2 50GBASE-CR2	FEC	2	RS544	26.5625G NRZ
		FEC	2	RS528	25.78125G NRZ
		PCS/VIRTUAL	2	None	25.78125G NRZ
	50GAUI-1 (C2C, C2M) 50GBASE-KR 50GBASE-CR	FEC	1	RS544	26.5625G PAM4
		FEC	1	RS272	26.5625G PAM4
		FEC	1	RS528	25.78125G PAM4
		PCS/VIRTUAL	1	None	25.78125G NRZ
40G	XLAUI XLPPI 40GBASE-CR4 40GBASE-KR4	PCS/VIRTUAL	4	BASE-R	10.3125G NRZ
		PCS/VIRTUAL	4	None	10.3125G NRZ
	XLAUI2	PCS/VIRTUAL	2	None	20.625G NRZ
25G	25GAUI (C2C, C2M) 25GBASE-C 25GBASE-CR-S 25GBASE-CR 25GBASE-KR	FEC	1	RS528	25.78125G NRZ
		PCS/VIRTUAL	1	BASE-R	25.78125G NRZ
		PCS/VIRTUAL	1	None	25.78125G NRZ
10G	10G-KR SFI XFI	PCS/VIRTUAL	1	BASE-R	10.3125G NRZ
		PCS/VIRTUAL	1	None	10.3125G NRZ

NOTE: The lane-swapping mode is configurable.
For PAM4 modes without FEC (single-lane 50G and dual-lane 100G and 200G) or using RS528 FEC (single-lane 50G and dual-lane 100G), the lane speed is 51.5625G.
The BCM56990 supports simultaneous operation of all seven port speeds (also called speed modes) listed in this table across various ports of the chip. However, within a single Blackhawk7 core, there are restrictions on which port modes can coexist. For more information, see Section 3.2.1, Flexport Configuration, and refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).

NOTE: A minimum of 1325-MHz core clock frequency is required to support 400G ports, and the core clock frequency cannot be changed dynamically.

3.2 Blackhawk7 Octal SerDes Configuration Guidelines

Each device has up to 64 Blackhawk7 cores, depending on the device part number. The Blackhawk7 cores are organized into 16 pipes. None of the 16 pipes can exceed one-sixteenth of the total switching throughput. In configurations where not all ports are active, bandwidth should be balanced across all 16 data pipelines.

A physical port consists of one or more SerDes lane in the device. There are up to 64 Blackhawk7 cores, each with eight physical SerDes lanes. A logical port is defined as a front-panel, CPU, or loopback port. Each Blackhawk7 Port Macro (PM) can have up to four logical ports, and the total number of logical ports per device is 256 + 11 = 267 ports. Out of 267, up to 256 ports, excluding the management port, can be assigned as front-panel ports. The rest are used as follows:

- Two management ports
- One CPU port
- Eight internal loopback ports

Physical-port to logical-port numbering limitations exist across pipes that are integrated into the SDK software.

3.2.1 Flexport Configuration

Blackhawk7 supports the ability to change a port configuration (speed and number of lanes per port) at runtime without affecting the operation of the other ports or requiring the device to be reset. If the SerDes continue to be associated with the same logical ports, then the Flexport configuration amounts to a speed change and can be handled automatically by the Blackhawk7 driver. Logical ports can be added, removed, or associated with a different number of SerDes through user API calls. The configuration of the SerDes within a Blackhawk7 core can be changed without affecting the ports using the remaining SerDes.

The Blackhwak7 port macro deploys a single PLL that can generate one of the following three basic VCO frequencies:

- 10.3125 GHz or 20.625 GHz: 40G and 10G (NRZ).
- 25.78125 GHz: 200G, 100G, and 50G (PAM-4/NRZ).
- 26.5625 GHz: 400G (PAM-4).

10G NRZ speeds and 25G NRZ speeds can be simultaneously supported in the same port macro.

The SDK software sets the initial PLL frequency after collecting all available port speeds allocated within a Blackhawk7 core. Changing the initial VCO to a different frequency requires a Blackhawk7 reset. The following table shows which port speeds can be flexed for a particular VCO frequency. In the table, an X indicates a port speed with the associated VCO frequency cannot be flexed.

Table 8: BCM56990 Flexport Restrictions

VCO Frequency (GHz)[a]	PAM-4: 400G	PAM4/NRZ: 200G, 100G, and 50G	NRZ: 25G	NRZ: 40G and 10G
26.5625	Flexport capable	Flexport capable	X	X
25.78125	X	Flexport capable	Flexport capable	Flexport capable
20.625	X	X	X	Flexport capable

a. The VCO frequency also depends on the FEC mode. For example, 100G-PAM4 operating in FEC-528 has a different VCO than FEC-544 even though the port speed is 100GbE. This implies that Flexport will not operate when ports within the same port macro have different FEC settings while operating at the same port speed.

3.3 HiGig3 Support

HiGig3 is a generic system header (GSH) that allows multiple devices to exchange metadata and function as one logical system. It is an upgraded HiGig™ packet format using standard Ethernet encapsulation. For more information, refer to the *BCM56990 Theory of Operation* (56990-PG1xx).

NOTE: The device supports HiGig3 only as a transit node. It does not initiate or terminate HiGig3 headers.

3.4 10G Merlin SerDes Core

The Merlin SerDes core is the management-port physical-layer interface for the BCM56990 specifically designed to support up to one 40GbE or two 10GbE management ports on a single Merlin. This interface supports the following features:

- The Merlin SerDes has four serial links and can support the following configurations:
  - One port in XAUI mode.
  - Two ports in single-lane mode.
  - Two ports in RXAUI mode.
- Single-lane mode supports 1000BASE-X, SGMII, 2500BASE-X, SFI, XFI, or 10GBASE-KR.
- Two-lane mode supports RXAUI.
- Four-lane mode supports 40GbE and XAUI.
- There is no support for mixing a two-lane and a four-lane port with any other port type.
- All single-lane port types can be mixed.

NOTE: When a 2500BASE-X port is mixed with an SFI, XFI, or 10GBASE-KR port, the transmit jitter on the 2500BASE-X port violates the IEEE specification.

3.5 PCIe

The PCIe interface provided by the BCM56990 switch conforms to the PCIe Gen3 specification and supports Gen1 and Gen2. The BCM56990 PCIe interface supports x1, x2, or x4 wide connections (8.0G link speed or 7.88 Gb/s data rate in each direction). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

The device provides strap signals to limit the maximum link speed and link width of the PCIe interface. The internal pulls on the strap signals cause the device to default to allowing a maximum link width of x4 and PCIe Gen3 link speeds.

For all PCIe speeds, the design requires quad serial peripheral interface (QSPI) flash memory programmed with Broadcom-provided firmware to be connected to the IP_QSPI interface on the device, and the device must be strapped to perform a download from this memory. This is required because the firmware configures the PCIe interface into a mode that is functional and compliant to the Gen3 specification. The exact strap settings and design requirements are as follows:

- BOOT_DEV[2:0] = 3’b000
- MHOST0_BOOT_DEV = 1’b1
- PCIE_FORCE_GENTYPE[1:0] = 2’b00
- QSPI flash memory is programmed with Broadcom-provided firmware
- QSPI flash memory is connected to IP_QSPI interface

NOTE: Design requirements include a QSPI flash memory that contains the Broadcom-provided PCIe firmware for all PCIe operating modes.The device must also be strapped to download and execute the code from this flash memory for the PCIe interface to be functional.

3.6 LED

There are three LED processors in the BCM56990 device that support up to 256 physical ports plus two management ports. Each LED processor includes a two-wire (clock and data) LED interface to control system LEDs. Both LED_CLK and LED_DATA are outputs. When active, LED_CLK is a 5-MHz clock. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED_DATA bits. The LED_DATA signal is pulsed high at the start of each LED refresh cycle. The LED refresh cycle is repeated approximately every 30 ms to refresh the LEDs. The LED timing diagrams are shown in the following figures.

Figure 5: Single LED Refresh Cycle

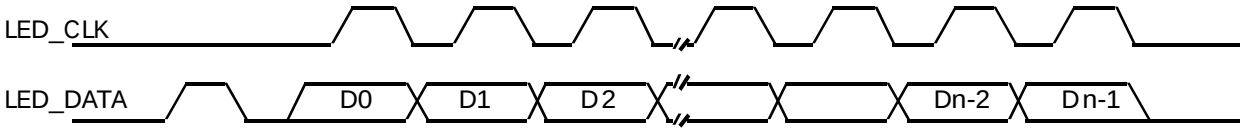
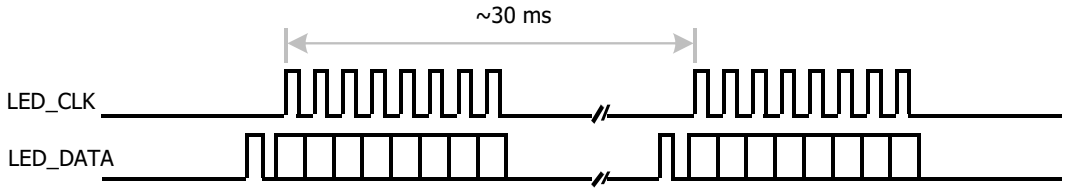


Figure 6: LED Refresh Timing



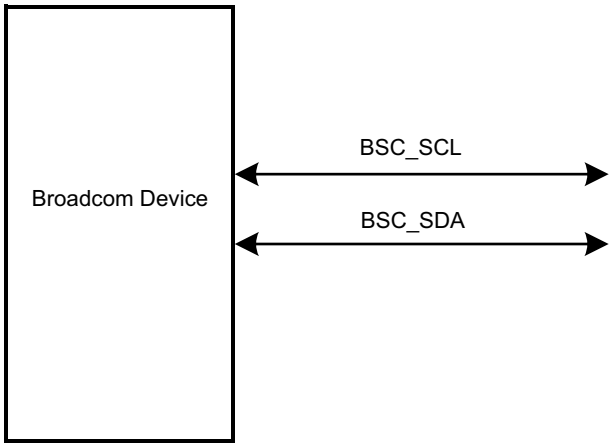
3.7 MIIM

The CPU Management Interface Controller (CMIC) supports the IEEE 802.3u standard MIIM interface: a two-wire serial bus controlled by the CMIC that allows register access to all the PHYs in the system. This interface can read data from the PHY or write data to the PHY. The two signals for MIIM are MDC (clock) and MDIO (bidirectional data). The CPU uses this interface to program the internal and external PHY registers. The MIIM interface can be configured to support Clause 45.

3.8 Broadcom Serial Control

The BCM56990 switch provides a Broadcom Serial Control (BSC) interface to communicate with other devices that support a similar interface. This interface is a NXP I^2C-compatible interface. The supported signals are shown in the following figure.

Figure 7: BSC Interface



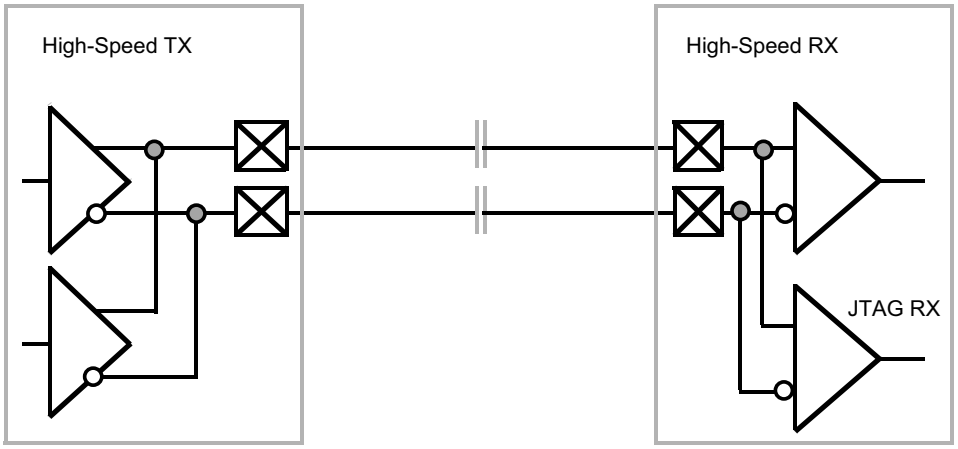
The BSC interface is supported in master mode only. The supported BSC data protocol format is big endian, which is consistent with the NXP I^2C protocol supported by other vendors.

3.9 JTAG

A standard JTAG interface is provided for boundary scan operations. This interface uses a standard five-pin interface and supports operational speeds up to 12.5 MHz.

Traditional JTAG provides the capability to test for opens and shorts when the device is mounted on the PCB. Because current technology requires that most high-speed differential signals must be AC-coupled, the traditional DC test for opens and shorts can produce false results. To provide a means of testing high-speed differential signals, the BCM56990 supports the latest JTAG specification, IEEE 1149.6 (also known as AC-JTAG). AC-JTAG can enable the detection of manufacturing faults on high-speed differential lines on the PCB. The device incorporates independent transceivers with low-load capacitance to avoid any adverse effect on the high-speed differential signals. The following figure shows the supported JTAG signals.

Figure 8: AC-JTAG Test Block



3.10 BroadSync

The BroadSync interface provides a way to externalize the timing information and clock signals generated by the global timing module, which is an internal clock adjustment block. The BroadSync interface can also be used as an input to receive timing from an external source or synchronize timing information in a multichip system. The BroadSync interface is used by ordinary clocks (OCs) in either a master or slave role. When the OC is a master, the BroadSync interface is configured as an input, accepting timing information from external hardware. When the OC is a slave, BroadSync is configured as an output, providing timing information to external hardware.

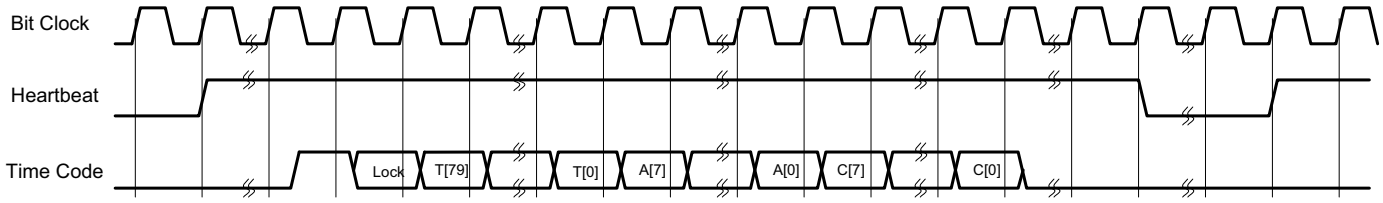
The BroadSync interface consists of the following three bidirectional signals that can be configured as outputs (master mode) or inputs (slave mode):

- TS_SYNC – Heartbeat clock. Signals the start of the transmission of the synchronized time value.
- TS_BIT_CLK – Bit clock. Used for the data transfer of the synchronized time value.
- TS_TIME_VAL – Time code or synchronized time value.

3.10.1 Slave Mode: BroadSync Signals as Inputs

In slave mode, the external hardware provides the bit clock and heartbeat clock signals as shown in the following figure. During each heartbeat period, the external hardware also shifts in the time code values. The shifted time value corresponds to the time of the most recent rising edge of the heartbeat signal. The heartbeat and time code signals are sampled off the negative edge of the bit clock.

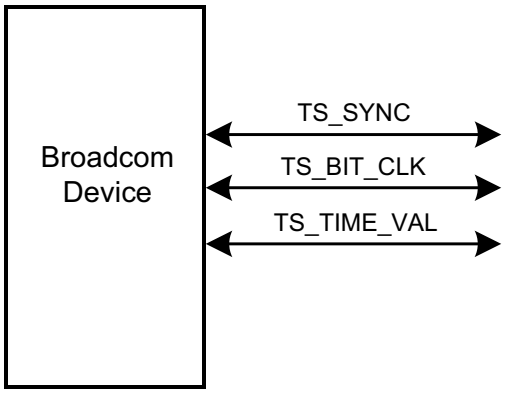
Figure 9: BroadSync Interface Timing Diagram



3.10.2 Master Mode: BroadSync Signals as Outputs

In master mode, the device provides the bit clock, heartbeat, and time code signals and enables the external devices to synchronize their behavior with that of the master. The signals supported are shown in the following figure.

Figure 10: BroadSync Interface



Chapter 4: Signal Descriptions

This section describes the device hardware signals. Table 9 lists signal type conventions, and Table 10 provides the signal name descriptions.

Table 9: Signal Types

Abbreviation	Description
I	Input
O	Output
B	Bidirectional signal
B_{OD}	Open drain bidirectional signal
B_{PD}	Bidirectional signal with internal pull-down
B_{PU}	Bidirectional signal with internal pull-up
I_{PD}	Input with internal pull-down
I_{PU}	Input with internal pull-up
O_{OD}	Output with open drain
PWR/GND	Power/ground plane
NC	No connect
P	Positive leg
N	Negative leg

4.1 Pin Description

The signal descriptions in this section apply the BCM56990 device.

Table 10: Device Signal Descriptions

Names	Quantity	I/O	Voltage	Description
System Signals				
SYS_RST_L	1	I_{PU}	1.8V	Device reset (active low).
AVS[7:0]	8	O	1.8V	AVS output. These outputs are to be connected to a VRM 11.1 compliant module to configure the appropriate core supply voltage for this device (See Table 11, Operating Conditions, for default voltage settings).
RESCAL[4:0]_REXT	5	I	0.75V	For each RESCAL pin and a nearest GND pin, connect a 4.53-kΩ resistor through a low-impedance path to ground. Each resistor calibrates the impedance of the SerDes cores in the device. A total of nine separate resistors are required.
PCIE_INTR_L	1	O	1.8	Active low-interrupt signal that asserts whenever the PCIe core sends an interrupt using an in-band mechanism like INT-X or MSI.
Subtotal	15	—	—	—
Required Clocks				
CORE_PLL_FREFp/n	2	I	1.8V Diff CML	50-MHz differential core logic reference clock. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
IPROC_PLL_FREFp/n	2	I	1.8V Diff CML	50-MHz differential iProc/CMIC reference clock. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
PCIe_REFCLKp/n	2	I	0.75V Diff CML	100-MHz PCIe differential PCIe clock. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
TSC_MGMT_REFCLKp/n	2	I	0.75V Diff CML	156.25-MHz differential Merlin SerDes core reference clock. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
TSC3_I_REFCLKp/n TSC28_I_REFCLKp/n TSC35_I_REFCLKp/n TSC60_I_REFCLKp/n	8	I	0.75V Diff CML	156.25-MHz differential Blackhawk7 SerDes core reference clock. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
Subtotal	16	—	—	—

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
Optional Clocks				
BS_PLL0_FREFp/n BS_PLL1_FREFp/n	4	I	1.8V	12.8-MHz, 20-MHz, 25-MHz, 32-MHz, or 50-MHz differential reference clock used for the BroadSync0 and BroadSync1 logic. When this clock is not supplied, the device can be configured to use a buffered version of the 50-MHz reference clock supplied through the CORE_PLL_FREFp/n inputs. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
TS_PLL_FREFp/n	2	I	1.8V	50-MHz differential reference clock used for the TimeSync logic. When this clock is not supplied, the device can be configured to use a buffered version of the 50-MHz reference clock supplied via the CORE_PLL_FREFp/n inputs. For external AC-coupling capacitor and termination resistor requirements, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).
Subtotal	6	—	—	—
Strap Signals				
PCIe_FORCE_GEN[1:0]	2	I_{PD}	1.8V	Selects the maximum operating rate of the PCIe interface: ■ 2'b00: Interface can operate at PCI Express Gen1, Gen2, or Gen3 speeds. ■ 2'b01: Interface can operate at PCI Express Gen1 speed. ■ 2'b10: Interface can operate at PCI Express Gen1 or Gen2 speeds. ■ (Others): Reserved. **NOTE:** When the PCIe interface is configured to support Gen3 speeds, the MHOST0_BOOT_DEV strap signal must be pulled high, and the BOOT_DEV[2:0] signals must be pulled low. A QSPI flash memory must be connected to the IPROC_QSPI interface and contain the PCIe Gen3 microcode.
PCIe_FORCE_LANE[1:0]	2	I_{PD}	1.8V	Selects the maximum link width of the PCIe interface: ■ 2'b00: Interface can operate at x1, x2, or x4 link widths. ■ 2'b01: Interface can operate at x1 link width only. ■ 2'b10: Interface can operate at x1 or x2 link widths. ■ (Others): Reserved.
MHOST0_BOOT_DEV	1	I_{PD}	1.8V	Selects the way mHost0 (the first internal Arm R5) is brought out of reset: ■ 1'b0: mHost0 is held in reset. ■ 1'b1: mHost0 comes out of reset and begins executing code based on the setting of the BOOT_DEV[2:0] strap signals. **NOTE:** This signal must be pulled high for normal operation.

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
MHOST1_BOOT_DEV	1	I_{PD}	1.8V	Selects the way mHost1 is brought out of reset: ■ 0: Tightly coupled memory (TCM) in iProc (default). ■ 1: Boot ROM inside iProc (reserved).
BOOT_DEV[2:0]	3	I_{PD}	1.8V	Selects the boot flow for mHost0 (the first internal Arm R5): ■ 3'b000: Load all necessary code from QSPI flash attached to IPROC_QSPI interface and begin execution. ■ (Others): Reserved. **NOTE:** These signals must be set to 3'b000.
QSPI_4BYTE_ADDR	1	I_{PD}	1.8V	Selects the operating mode of the QSPI flash device connected to the IPROC_QSPI interface: ■ 1'b0: QSPI flash is operating in 3-byte address mode. ■ 1'b1: QSPI flash is operating in 4-byte address mode.
QSPI_ADDR_BPC_MODE	1	I_{PD}	1.8V	Selects the mode that is used for sending commands and addresses to the QSPI flash device connected to the IPROC_QSPI interface: ■ 1'b0: Commands and addresses are sent serially, and data is sent in parallel. ■ 1'b1: Commands, addresses, and data are sent in parallel.
QSPI_DUAL_LANE	1	I_{PD}	1.8V	Selects the operating mode of the IPROC_QSPI interface: ■ 1'b0: IPROC_QSPI interface operates using a serial interface. ■ 1'b1: IPROC_QSPI interface operates using a two-bit parallel interface. **NOTE:** If this signal is pulled high, the IPROC_QSPI_QUAD_LANE signal must be pulled low.
QSPI_QUAD_LANE	1	I_{PD}	1.8V	Selects the operating mode of the IPROC_QSPI interface: ■ 1'b0: IPROC_QSPI interface operates using a serial interface. ■ 1'b1: IPROC_QSPI interface operates using a four bit parallel interface. **NOTE:** If this signal is pulled high, the IPROC_QSPI_DUAL_LANE signal must be pulled low.
Subtotal	13	—	—	—

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
PCIe Interface				
PCIe_RDp/n[3:0]	8	I	0.75V	PCIe receive differential serial data. Four lanes of 2.5 Gb/s or 5 Gb/s differential signal for lanes 3, 2, 1, and 0.
PCIe_TDp/n[3:0]	8	O	0.75V	PCIe transmit differential serial data. Four lanes 2.5 Gb/s or 5 Gb/s differential signals for lanes 3, 2, 1, and 0.
PCIe_PERST_L	1	I_{PU}	1.8V	PCIe reset signal. Connect this pin to PCIe_PERST_L from the root complex.
PCIe_WAKE_L	1	O_{OD}	1.8V	Bidirectional open drain, active-low PCIe interface wake signal. Requires an external pull-up.
Subtotal	18	—	—	—
JTAG Signals				
JTRST_L	1	I_{PU}	1.8V	JTAG test controller reset (active low). When asserted, the test controller is held in reset. This signal should be made accessible for JTAG debugging. For normal operation, this signal should be pulled low.
JTCE[1:0]	2	I_{PD}	1.8V	JTAG test controller enable: ■ 2'b0x: Functional mode or Arm R5 debug mode. ■ 2'b10: Non-functional mode or Logicvision TAP mode. ■ (Others): Reserved. These signals should be brought to pads with the ability to stuff a pull-up resistor. These resistors should not be stuffed for normal operation.
JTCK	1	I_{PD}	1.8V	JTAG test clock.
JTDI	1	I_{PU}	1.8V	JTAG test data in.
JTDO	1	O	1.8V	JTAG test data out.
JTMS	1	I_{PU}	1.8V	JTAG test mode select.
Subtotal	7	—	—	—

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
BSC Signals				
IPROC_BSC[1:0]_SCL	2	B_{OD}	1.8V	BSC interface clocks (100 kHz and 400 kHz). These interfaces can function only as master interfaces. These signals require an external pull-up to 1.8V, even if the interface is unused.
IPROC_BSC[1:0]_SDA	2	B_{OD}	1.8V	BSC interface data. These interfaces function only as master interfaces. These signals require an external pull-up to 1.8V, even if the interface is unused.
IPROC_BSC2_SCL	1	B_{OD}	1.8V	BSC interface clock. This interface functions only as a slave interface. This signal requires an external pull-up to 1.8V, and the BSC2 interface should be connected for debugging purposes.
IPROC_BSC2_SDA	1	B_{OD}	1.8V	BSC interface data. This interface functions only as a slave interface. This signal requires an external pull-up to 1.8V, and the BSC2 interface should be connected for debugging purposes.
BSC_SA[1:0]	2	B_{OD}	1.8V	BSC interface slave address selects the lower two bits of the BSC slave address used on the BSC2 interface.
Subtotal	8	—	—	—
LED Interface				
IPROC_LED[4:0]_CLK	5	O_{PD}	1.8V	Clocks for serial bit streams for port status LEDs. Each clock corresponds to the associated IPROC_LED[4:0]_DATA data signal. Port status information is all brought to a common micro-controller that can choose which IPROC_LED[4:0] interfaces to drive for full flexibility.
IPROC_LED[4:0]_DATA	5	O_{PD}	1.8V	Data signals for serial bit streams for port status LEDs. Each data signal corresponds to the associated IPROC_LED[4:0]_CLK clock. Port status information is all brought to a common micro-controller that can choose which IPROC_LED[4:0] interfaces to drive for full flexibility.
Subtotal	10	—	—	—

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
Network Timing Signals				
IPROC_BS[1:0]_CLK	2	B_{PD}	1.8V	BroadSync clocks. Synchronizes time code data transfer with the associated IPROC_BS[1:0]_HB and IPROC_BS[1:0]_TC signals. When configured as outputs, the BroadSync heartbeat and time code signals are driven off the rising edge of the bit clock. When configured as inputs, the heartbeat and time code signals are sampled off the negative edge of the bit clock.
IPROC_BS[1:0]_HB	2	B_{PD}	1.8V	BroadSync heartbeat clock that signals the start of the synchronized time value transmission. Each signal is configurable as an output or an input by using a register. When configured as output, this signal is driven off the rising edge of the bit clock. When configured as input, this signal is sampled off the negative edge of the bit clock.
IPROC_BS[1:0]_TC	2	B_{PD}	1.8V	BroadSync synchronized time code. Serially shifts time value, one bit per rising edge of the bit clock. Each signal is configurable as an output or an input by using a register. When configured as output, this signal is driven off the rising edge of the bit clock. When configured as input, this signal is sampled off the negative edge of the bit clock.
IPROC_TS_GPIO[5:0]	6	B_{PU}	1.8V	General purpose I/O signals with the ability to trigger internal timestamp capture in input mode or be automatically controlled by the TimeSync logic in output mode. These signals can also be configured as general purpose outputs or inputs (with interrupt generation capability). When configured as an input, a weak internal pull-up or pull-down resistor can be enabled. By default, these signals are configured as inputs with an internal pull-up resistor enabled. These signals return to the default state when the SYS_RST_N signal is asserted.
L1_RCVRD_CLK	1	O	1.8V	Primary recovered clock from a user-selectable Ethernet SerDes receiver. This is primarily for enabling L1 clock synchronization. The output clock frequency is user configurable through a fractional divider and supports frequencies from 25 MHz to 156.25 MHz.
L1_RCVRD_CLK_VALID	1	O	1.8V	Status signal associated with the L1_RCVRD_CLK clock output. When this signal is high, it is an indication that the output clock is valid and is usable. When this signal is low, the output clock should not be used.
L1_RCVRD_CLK_BKUP	1	O	1.8V	Secondary recovered clock from a user-selectable Ethernet SerDes receiver. This is primarily for enabling L1 clock synchronization. The output clock frequency is user configurable through a fractional divider and supports frequencies from 25 MHz to 156.25 MHz.

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
L1_RCVRD_CLK_VALID_BKUP	1	O	1.8V	Status signal associated with the L1_RCVRD_CLK_BKUP clock output. When this signal is high, it is an indication that the output clock is valid and is usable. When this signal is low, the output clock should not be used.
Subtotal	16	—	—	—
General Purpose I/Os				
IPROC_G_GPIO[8:0]	9	B_{PU}	1.8V	General purpose I/O signals. These signals can be configured as outputs or inputs (with interrupt generation capability). When configured as an input, a weak internal pull-up or pull-down resistor can be enabled. By default, these signals are configured as inputs with an internal pull-up resistor enabled. These signals are reset back to inputs upon the assertion of the SYS_RST_L signal.
Subtotal	9	—	—	—
QSPI Signals				
IPROC_QSPI_CS_L	1	O	1.8V	QSPI slave select (active low).
IPROC_QSPI_HOLD_L	1	B_{PD}	1.8V	When the QSPI interface is operating in single- or dual-lane mode, this is the QSPI pause active low output signal. When operating in quad-lane mode, this is a bidirectional signal used as DQ[3].
IPROC_QSPI_MISO	1	B_{PD}	1.8V	When the QSPI interface is operating in single-lane mode, this is the serial input from the slave. When operating in dual- or quad-lane mode, this is a bidirectional signal used as DQ[1]. **NOTE:** The QSPI interface only supports operating as a master.
IPROC_QSPI_MOSI	1	B_{PD}	1.8V	When the QSPI interface is operating in single-lane mode, this is the serial output to the slave. When operating in dual- or quad-lane mode, this is a bidirectional signal used as DQ[0]. **NOTE:** The QSPI interface only supports operating as a master.
IPROC_QSPI_SCK	1	O	1.8V	QSPI clock.
IPROC_QSPI_WP_L	1	B_{PD}	1.8V	When the QSPI interface is operating in single- or dual-lane mode, this is the QSPI write protect active low output signal. When operating in quad-lane mode this is a bidirectional signal used as DQ[2].
Subtotal	6	—	—	—

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
SPI Signals				
IPROC_SPI0_SCK	1	B_{PU}	1.8V	SPI serial clock.
IPROC_SPI0_MISO	1	B_{PU}	1.8V	SPI serial input from the slave. **NOTE:** The SPI interface only supports operating as a master.
IPROC_SPI0_MOSI	1	B_{PU}	1.8V	SPI serial output to the slave. **NOTE:** The SPI interface only supports operating as a master.
IPROC_SPI0_SS_L	1	B_{PU}	1.8V	SPI slave select (active low).
Subtotal	4	—	—	—
UART Signals				
IPROC_UART0_CTS_L	1	I_{PU}	1.8V	Active low, Clear-to-Send signal used by first general-purpose UART.
IPROC_UART0_SIN	1	I_{PD}	1.8V	Serial input used by first general-purpose UART.
IPROC_UART0_RTS_L	1	O	1.8V	Active low, Request-to-Send signal used by first general-purpose UART.
IPROC_UART0_SOUT	1	O	1.8V	Serial output used by first general-purpose UART.
IPROC_UART1_SIN	1	I_{PD}	1.8V	Serial input used by second general-purpose UART.
IPROC_UART1_SOUT	1	O	1.8V	Serial output used by second general-purpose UART.
IPROC_UART2_CTS_L	1	I_{PU}	1.8V	Active low, Clear-to-Send signal used by the UART dedicated to mHost0 (the first internal Arm R5).
IPROC_UART2_SIN	1	I_{PD}	1.8V	Serial input used by the UART dedicated to mHost0 (the first internal Arm R5).
IPROC_UART2_RTS_L	1	O	1.8V	Active low, Request-to-Send signal used by the UART dedicated to mHost0 (the first internal Arm R5).
IPROC_UART2_SOUT	1	O	1.8V	Serial output used by the UART dedicated to mHost0 (the first internal Arm R5).
IPROC_UART3_CTS_L	1	I_{PU}	1.8V	Active low, Clear-to-Send signal used by the UART dedicated to mHost1 (the second internal Arm R5).
IPROC_UART3_SIN	1	I_{PD}	1.8V	Serial input used by the UART dedicated to mHost1 (the second internal Arm R5).
IPROC_UART3_RTS_L	1	O	1.8V	Active low, Request-to-Send signal used by the UART dedicated to mHost1 (the second internal Arm R5).
IPROC_UART3_SOUT	1	O	1.8V	Serial output used by the UART dedicated to mHost1 (the second internal Arm R5).
Subtotal	14	—	—	—
NOTE: All UART pins and features are for dedicated IEEE 1588 applications only. They do not support generic use.				

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
MIIM Signals				
IPROC_MDC[11:0]	12	O	1.2V	Serial management clocks for external PHY management. These signals conform to the Clause 45 electrical specification and protocol. Each clock corresponds to the associated IPROC_MDIO[11:0] signal. An external pull-up resistor on each signal to the IPROC_VDDO_[2:1] supply is recommended. The internal MDIO to Blackhawk7 core (TSC), MGMT (TSC_MGMT), and PCIe connection are in the following list. The external PHY mapping can be configured by SDK software. ■ MDIO[0]: TSC[0, 1, 2] ■ MDIO[1]: TSC[3, 4, 5] ■ MDIO[2]: TSC[6, 7, 8] ■ MDIO[3]: TSC[9, 10, 11] ■ MDIO[4]: TSC[12, 13, 14] ■ MDIO[5]: TSC[15, 16, 17] ■ MDIO[6]: TSC[18, 19, 20] ■ MDIO[7]: TSC[21, 22, 23] ■ MDIO[8]: TSC[24, 25, 26] ■ MDIO[9]: TSC[27, 28, 29] ■ MDIO[10]: TSC[30, 31] ■ MDIO[11]: TSC_MGMT and PCIe
IPROC_MDIO[11:0]	12	B_{OD}	1.2V	Serial management clocks for external PHY management. These signals conform to the Clause 45 electrical specification and protocol. An external pull-up resistor on each signal to the IPROC_VDDO_[2:1] supply is recommended.
Subtotal	24	—	—	—
Blackhawk7 Signals				
TSC[63:0]_RDp/n[7:0]	1024	I	0.75V	Blackhawk7 core[63:0] lane [7:0] receive differential pair.
TSC[63:0]_TDp/n[7:0]	1024	O	0.75V	Blackhawk7 core[63:0] lane [7:0] transmit differential pair.
Subtotal	2048	—	—	—
Management Merlin Signals				
TSC_MGMT_RDp/n[3:0]	8	I	0.75V	Merlin lane [3:0] receive differential pair.
TSC_MGMT_TDp/n[3:0]	8	O	0.75V	Merlin lane [3:0] transmit differential pair.
Subtotal	16	—	—	—

Table 10: Device Signal Descriptions (Continued)

Names	Quantity	I/O	Voltage	Description
Miscellaneous Signals				
TESTIO[58:0]	59	I	1.8V	Test I/O pins.
Subtotal	59	—	—	—
System Monitoring				
AVS_VTMON_ADC	1	I	Various	Input to analog-to-digital converter in adaptive voltage scaling monitor block. This input can be left unconnected; for factory use only.
AVS_VTMON_VDAC	1	O	Various	Output from digital-to-analog converter in adaptive voltage scaling monitor block. This output can be left unconnected; for factory use only.
TEMPDIODE[1:0]_FORCE_p/n	4	O	Various	Output from digital-to-analog converter in adaptive voltage scaling monitor block. This output can be left unconnected; for factory use only.
TRVDD0p75_[2:1]_SENSE	2	O	Various	TRVDD0p75 supply sense output used as a feedback voltage to the voltage regulator module for transmit and receive analog supplies.
TVDDH_[2:1]_SENSE	2	O	Various	TVDDH supply sense output used as a feedback voltage to the voltage regulator module for transmit and receive analog supplies.
VDD_SENSE[2:1]	2	O	Various	Core VDD supply sense output used as a feedback voltage to the voltage regulator module.
VSS_SENSE[2:1]	2	O	Various	Core VDD ground sense output used as a ground feedback to the voltage regulator module.
VTMON[14:0]_ADC_VDAC	15	B	Various	Input and outputs to analog-to-digital and digital-to-analog converters in process, temperature, and voltage monitoring blocks. These I/Os can be left unconnected; for factory use only.
Subtotal	29	—	—	—
Ground				
VSS	609	GND		Digital ground.
AGND	3775	GND		Analog ground.
Subtotal	4286	—	—	—
TOTAL	8371	—	—	—

4.2 BCM56990 Pin List by Ball Number

The pin list and ballout diagram for the BCM56990 device is provided in spreadsheet form on the Broadcom Customer Support Site (docSAFE). The spreadsheet serves as the official document containing the device's signal mapping.

Chapter 5: Electrical Specifications

5.1 Operating Conditions

The following table describes the recommended operation conditions for the BCM56990.

Table 11: Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
0.72V to 0.90V ± 3%, AVS core voltage[a]	—	–3%	AVS voltage	+3%	V
0.75V ± 3%, analog voltage	—	0.7275	0.75	0.7725	V
1.2V ± 3%, (analog and digital) voltage	—	1.164	1.2	1.236	V
1.80V ± 3%,(analog and digital) voltage	—	1.746	1.80	1.854	V
Ambient temperature	T_A	0	—	70	°C
Junction temperature	T_J	0	—	105	°C
NOTE:					

a. The VRM 11.1-compliant Voltage Regulator Module can be controlled through the BSC interface or AVS pins to provide the AVS core voltage. VRM must be set to the AVS voltage based on the AVS[7:0] I/O pin or AVS register to power up the device. For details, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).

5.2 Power-Up and Power-Down Specifications

The device requires a power-up and power-down sequence. Violating the power sequencing requirement can cause latch-up damage. See Section 5.5.1, Power-On Sequence, and the *BCM56990 Hardware Design Guidelines* (56990-DG1xx) for additional information.

5.3 Device Power Supply Requirements

The following table lists the maximum, per-rail power allowed for the power supplies in the BCM56990 device.

Table 12: BCM56990 Maximum Device Per-Rail Power for Power Supply Design

Rail	Supply Name	Voltage (V)	Maximum Power Supply Power (W)
AVS core digital	VDD	0.72 to 0.90	488.260
1.8V analog	*AVDD1p8	1.8	0.501
1.2V analog	TVDDH	1.2	8.096
0.75V analog PLLVDD	PLLVDD	0.75	3.520
0.75V analog TRVDD	TRVDD	0.75	86.17
1.2V digital	IP_VDDO*	1.2	0.400
1.8V digital	VDD18	1.8	2.601

NOTE: The maximum per-rail power in Table 12 is used to design the system power supply. Each supply-rail current may not track each other with process variations (that is, analog current goes up while digital current goes down). Table 13 power is used for thermal design and its value does not equal to the total maximum power from Table 12.

Table 13: System Thermal Design Maximum Power

Device	Maximum System Power
BCM56990	530.0W

NOTE: These maximum power values assume the use of the mandatory AVS feature. For AVS details, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).

Table 14: Per-SerDes (Eight Lanes), Per-Voltage Rail Maximum Power Numbers

Voltage Rail	Maximum Power (mW)
Blackhawk7 TVDD	191.4
Blackhawk7 TRVDD	1281.5
Blackhawk7 PLLVDD	55.0
Merlin (TSC_MGMT_RTVDD and TSC_MGMT_PVDD)	128.0
PCIe SerDes (PCIe_RTVDD and PCIe_PVDD)	138.0
NOTE: It is a design requirement that all SerDes cores must be connected to their specified supply rails. The Broadcom SDK ensures the digital portion of unused SerDes cores are held in reset and the analog portion of the core is placed into a power-down mode. This achieves the desired power savings automatically for unused SerDes cores.	

5.4 DC Characteristics

This section provides DC information about the BCM56990 device.

5.4.1 Standard 1.8V I/O Signals

The specifications shown in the following table apply to all CMOS 1.8V general I/O signals along with synchronous Ethernet interface, UART, GPIO, JTAG, SPI, QSPI, BSC, and LED signals except for MIIM interface signals, which are 1.2V.

Table 15: Standard 1.8V I/O Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	0.0	—	+1.98	V
Input low voltage	V_{IL}	0.0	—	0.35 × VDD1p8	V
Input high voltage	V_{IH}	0.65 × VDD1p8	—	—	V
Output low voltage	V_{OL}	—	—	0.45	V
Output high voltage	V_{OH}	VDD1p8 – 0.45	—	—	V
Output low current	IOL	8.0	—	—	mA
Output high current	IOH	8.0	—	—	mA
Pull-up or pull-down resistor	R_p	—	50	—	kΩ

NOTE: The overshoot and undershoot information is as follows

- Overshoot: The maximum limit is 500 mV above supply for no more than 10% of the duty cycle.
- Undershoot: The maximum limit is 500 mV below ground for no more than 10% of the duty cycle.

5.4.2 Management Interface

Table 16: MIIM, Clause 45 Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	—	0	—	1.5	V
Input low voltage	V_{IL}	—	—	—	0.36	V
Input high voltage	V_{IH}	—	0.84	—	—	V
Output low voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.20	V
Output low current	I_{OL}	V_{OL} = 0.2V	4.0	—	—	mA
Output high voltage	V_{OH}	I_{OH} = –100 µA	1.0	—	—	V
Output high current	I_{OH}	V_{OH} = 1.0V	—	—	–4.0	mA

NOTE: The overshoot and undershoot information is as follows

- Overshoot: The maximum limit is 500 mV above supply for no more than 10% of the duty cycle.
- Undershoot: The maximum limit is 500 mV below ground for no more than 10% of the duty cycle.

5.4.3 Reference Clocks

The following two figures apply to all reference clocks in this subsection.

Figure 11: Reference Clock Single-Ended DC Parameters

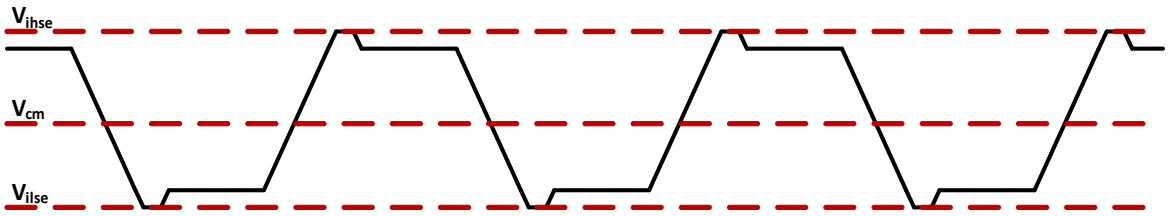
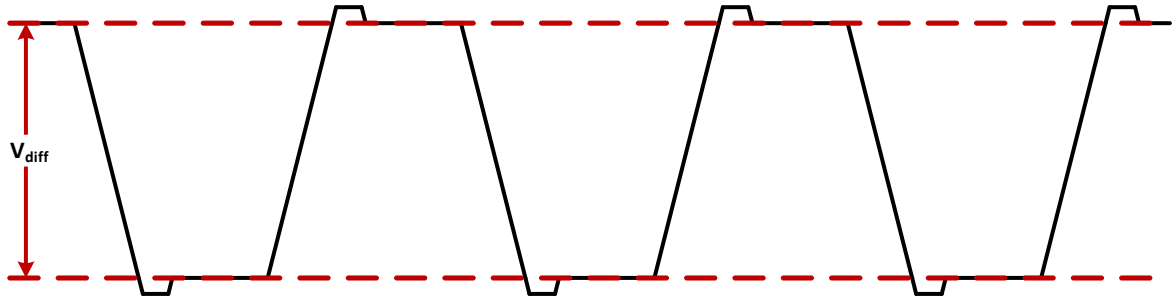


Figure 12: Reference Clock Differential DC Parameters



5.4.3.1 PCIe PLL Reference Clock (PCIe_REFCLK)

The PCI Express PLL clock handles clocking for the SerDes used for PCI Express connectivity and has the input structure shown in the following figure.

Figure 13: PCI Express PLL Input Structure

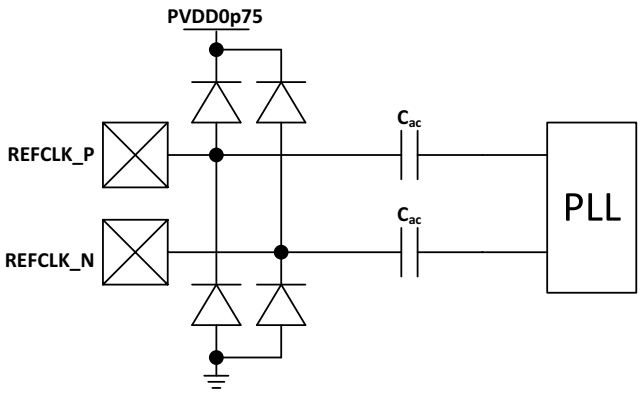


Table 17: PCI Express PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	375	—	mV_{se}
Single ended swing	V_{ilse} or V_{ihse}	0	—	800	mV_{se}
Differential swing	V_{diff}	600	—	1200	mV_{ppd}
Internal AC coupling	C_ac	—	6	—	pF
Internal differential termination	R_{term}	—	—	—	Ω

NOTE:
- External AC coupling is required. Recommended AC coupling capacitor value is 10 nF.
- External 100Ω termination resistor is required.

5.4.3.2 BroadSync PLL Reference Clocks (BS_PLL0_REFCLK and BS_PLL1_REFCLK)

The BroadSync PLLs clock the associated BroadSync block used to transmit or receive timing information from an external entity. They have the input structure shown in the following figure.

Figure 14: BroadSync PLL Input Structure

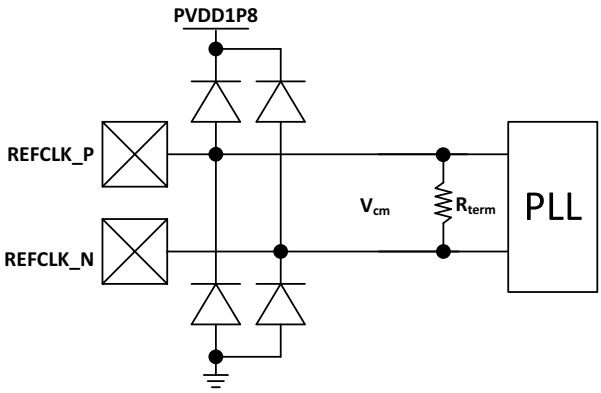


Table 18: BroadSync PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	650	—	mV_{se}
Differential swing	V_{diff}	500	—	2000	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω

a. External AC coupling is required. The recommended AC coupling capacitor value is 10 nF.

5.4.4 Blackhawk (TSC) Interface

Table 19: Blackhawk SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input voltage (differential peak-to-peak), AC-coupled	V_{ID}	85	—	1600	mVp-p
Input impedance (differential), integrated on-chip	R_{IN}	80	95	120	Ω
Transmitter					
Output voltage (differential peak-to-peak), programmable	V_{ODpp}	0	—	1050	mVp-p
Output impedance (differential)	R_{OUT}	—	85	—	Ω

5.4.5 Merlin (TSC_MGMT) Interface

Table 20: Merlin7 SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input voltage (differential peak-to-peak), AC-coupled	V_{ID}	85	—	1200	mVp-p
Input impedance (differential), integrated on-chip	R_{IN}	80	100	120	Ω
Transmitter					
Output voltage (differential peak-to-peak), programmable	V_{ODpp}	800	900	1200	mVp-p
Output impedance (differential)	R_{OUT}	—	100	—	Ω

5.4.6 PCIe Interface

Table 21: PCIe SerDes DC Characteristics

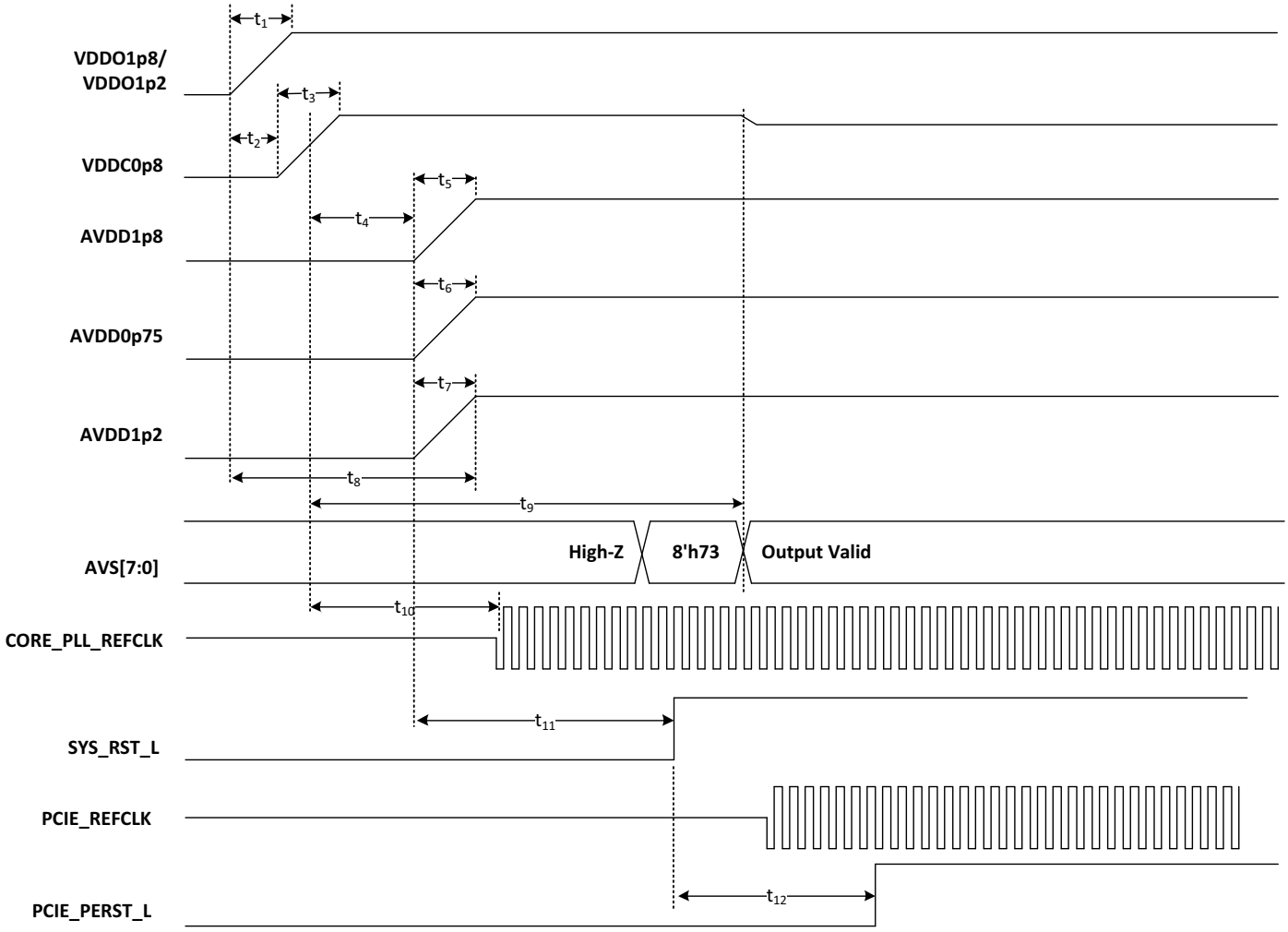
Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input voltage (differential peak-to-peak), AC-coupled	V_{ID}	85	—	1200	mVp-p
Input impedance (differential), integrated on-chip	R_{IN}	80	100	120	Ω
Transmitter					
Output voltage (differential peak-to-peak), programmable	V_{ODpp}	800	900	1200	mVp-p
Output impedance (differential)	R_{OUT}	—	100	—	Ω

5.5 AC Characteristics

5.5.1 Power-On Sequence

The following figure illustrates the sequence for power-on timing.

Figure 15: Power-On Timing



The following table describes the power-on timing requirements.

Table 22: Power-Up and Reset Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ramp time for 1.8V and 1.2V supplies	t_1	0.09	—	10	ms
Delay from start of 1.8V ramp to start of VDDC0P8 supply ramp	t_2	0.0	—	—	ms
Ramp time for VDDC0P8 Core supply	t_3	0.05	—	10	ms
Delay from VDDC0P8 ramped up to start of 0.72V, and 1.8 AVDD supplies ramp	t_4	VDD reaches 0.72V	—	—	ms
Ramp time for 1.8V analog supply	t_5	0.09	—	10	ms
Ramp time for 0.75V analog supply	t_6	0.04	—	10	ms
Ramp time for 1.2V analog supply	t_7	0.1	—	10	ms
Time from first supply starting to ramp to last supply finish ramping	$t_{8=}\ t_2+0.5*t_3+\ t_4+t_7$	—	—	10	ms
VDDC0P8 at 0.55V to valid output at AVS[3:0] output valid	t_9	14	—	90	ms
VDDC0P8 at 0.55V to CORE_PLL_REFCLK is stable	t_{10}	0	—	6.4	ms
Start of ramp of AVDD supplies to System Reset signal deassertion	t_{11}	120	—	—	ms
System Reset to PCIe Reset delay	t_{12}	100	—	—	ms

NOTE:

- All voltage supplies need to follow max ramp rate in table above and the rest of supplies use ramp rate 1V/50µs.
- After IO reset and before OTP is valid, AVS will drive 8’h73 (0.89375V per Intel VRM specification).

Table 23: Mapping of Device Power Signals to Supply Rails

Supply Name	Power Signal Names
VDDO1p8	VDD18, IPROC_VDDO_0, and SEQ18_VDDO
VDDO1p2	IPROC_VDDO_1
VDDC0p8	VDD
VDD0p75	TSC_MGMT_RTVDD, TSC_MGMT_PVDD, PCIe_RTVDD, PCIe_PVDD, TRVDD0p75_[2:1], and TSC[63:0]_PLLVDD0
VDD1p2	TVDDH_1 and TVDDH_2
VDD1p8	BS_PLL[1:0]_AVDD1p8, CORE_PLL_AVDD1p8, PP_PLL_AVDD1p8, IPROC_PLL_AVDD1p8, TS_PLL_AVDD1p8

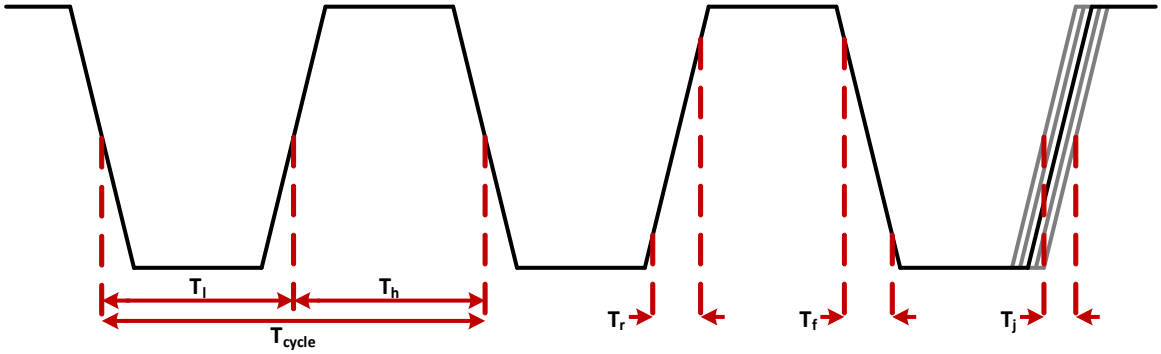
5.5.2 Power-Down Sequence

When the device is powered down and then powered on, to guarantee the POR reset is asserted, VDDC must ramp down to 0.1V and maintain this level for at least 20 ms.

5.5.3 Reference Clocks

The following figure applies to all reference clocks in this subsection.

Figure 16: Reference Clock AC Parameters



5.5.3.1 PCIe Reference Clock Timing (PCIe_REFCLK)

The following table shows the parameters for a 100-MHz differential input.

Table 24: PCIe_REFCLK Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)	C_{freq}	—	100	—	MHz
Tolerance	TOL	–300	—	+300	ppm
Duty cycle	T_h/T_l	40	—	60	%
Rise/fall time (20% to 80%)	T_R/T_F	—	—	1.0	ns/V_{ppd}
Jitter RMS max (10 kHz to 1.5 MHz) for Gen3 8.0-Gb/s operation	T_J	—	—	1.0	ps
Jitter RMS max (10 kHz to 1.5 MHz) for Gen2 5.0-Gb/s operation	T_J	—	—	3.0	ps
Cycle-to-Cycle Jitter for Gen1 2.5-Gb/s operation	—	—	—	150	ps

5.5.3.2 Core PLL Reference Clock Timing (CORE_PLL_FREF)

The following table shows the parameters for a 50-MHz differential input.

Table 25: CORE_PLL_FREF Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)	C_{freq}	—	50	—	MHz
Frequency Deviation	—	–50	—	+50	ppm
Duty cycle distortion	—	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	—	—	1	ns/V_{ppd}
RMS jitter (12 kHz to 20 MHz)	T_j	—	—	1	ps-rms

5.5.3.3 Blackhawk SerDes Core Reference Clock Timing (TSC*_REFCLK)

The following table shows the parameters for 156.25-MHz differential input and the following figure shows the input timing diagram.

Table 26: TSC*_REFCLK Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)	C_{freq}	—	156.25	—	MHz
Frequency Deviation	—	–50	—	+50	ppm
Duty cycle distortion	—	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	—	0.3	0.5	ns/V_{ppd}
RMS jitter (12 kHz to 20 MHz)	T_j	—	—	0.3	ps-rms

5.5.3.4 Merlin SerDes Core Reference Clock Timing (MGMT_REFCLK)

The following table shows the parameters for the 156.25-MHz differential input

Table 27: MGMT_REFCLK Clock Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)	C_{freq}	—	156.25	—	MHz
Frequency Deviation	—	–50	—	+50	ppm
Duty cycle distortion	—	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	0.2	—	0.9	ns/V_{ppd}
RMS jitter (12 kHz to 20 MHz)	T_j	—	—	0.3	ps-rms

5.5.3.5 Time Sync Reference Clock Timing (TS_PLL_FREF)

The TS_PLL_FREFP/N clock supports a 50-MHz differential source with characteristics shown in the following table.

Table 28: TS_PLL_FREF Clock Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)	C_{freq}	—	50	—	MHz
Frequency deviation	—	–50	—	+50	ppm
Duty cycle	T_h/T_l	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	—	—	1	ns/V_{ppd}
RMS jitter maximum (12 kHz to 20 MHz)	T_j	—	—	1	ps-rms
NOTE: The ±50 ppm accuracy is the minimum requirement for the operation of Transparent Clock (TC) functionality only. Input clock accuracy may be application dependent.					

NOTE: Do not use PLL-based oscillators or zero-delay buffers as a source for TS_PLL_FREF because this introduces excessive jitter that may result in unacceptable bit error rate performance.

5.5.3.6 BroadSync PLL Reference Clocks Timing (BS_PLL0_FREF / BS_PLL1_FREF)

The BS_PLL0/1_FREFp/n supports differential source with characteristics shown in the following table.

Table 29: BS_PLL0_FREF / BS_PLL1_FREF

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)[a]	—	—	12.8	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	20	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	25	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	32	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	50	—	MHz
Tolerance	—	–50	——	50	PPM
Duty cycle	T_h/T_l	40	50	60	%
Rise/fall time (20% to 80%)	T_r/T^f	—	—	1	ns/V_{ppd}
RMS Jitter (12kHz to 20MHz)	T_J	—	—	1	ps

a. The Broadcom SDK automatically programs the PLL appropriately for the provided reference clock frequency.

5.5.4 Blackhawk (TSC) Interface

The device serial interface conforms to IEEE 802.3bs and 802.3cd specifications and includes the following features:

- Octal SerDes block supporting eight serial links.
- Line rates from 10.3125 Gb/s to 56.25 Gb/s (PAM4 56.25 Gb/s or NRZ 28.125 Gb/s).
- CML driver with 2 × 50Ω internal termination.
- Controlled peak-to-peak amplitude.

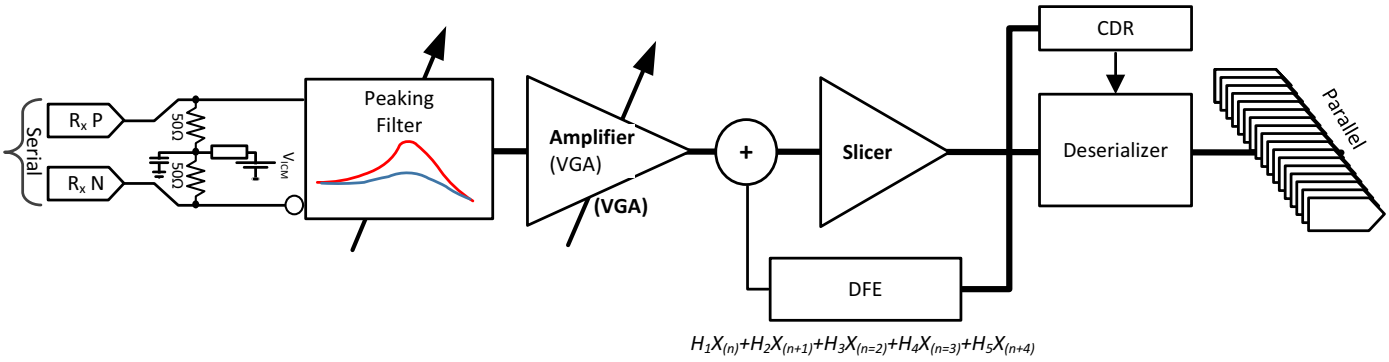
The serial interface operating conditions are shown in the following table.

Table 30: Blackhawk Serial Interface Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud, symbol rate	B_{PS}	3.75	—	28.3	Gbaud
Unit interval	UI	35.33	—	266.6	ps

5.5.4.1 Blackhawk Receiver

Figure 17: SerDes Receiver Conceptual Diagram



The serial interface receive characteristics are shown in the following table.

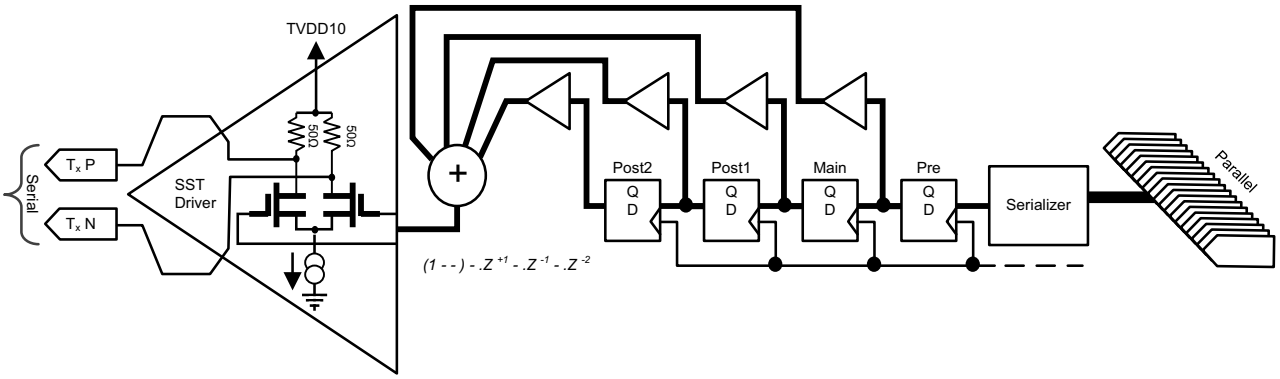
Table 31: Blackhawk Serial Interface Receive Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Units
Jitter tolerance	Δt_{RXtot}	Total, peak-to-peak	—	—	0.65	UI
	Δt_{RXdet}	Deterministic, peak-to-peak	—	—	0.37	UI
Input common mode	VCM-RX	AC cap is included on die, and the input Vcm is floating.[a]	—	500	750	mV
Input differential swing	VId	Input eye must meet RX Eye Templates from applicable standards. For Vid = 1.6Vppd, input Vcm-RX voltage should be adjusted down.	85	—	1600	mVppd

a. For inputs with a higher Vcm voltage than the Max, an external 100 nF AC capacitor is needed.

5.5.4.2 Blackhawk Transmitter

Figure 18: Blackhawk SerDes Transmitter Conceptual Diagram



The serial interface transmit characteristics are shown in the following table.

Table 32: Blackhawk Serial Interface Transmit Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Output voltage fall time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, eight 1's and eight 0's)	—	a	—	ps
Output voltage rise time	t_{rise}	20% to 80% (based on 10GBASE-KR waveform, eight 1's and eight 0's)	—	a	—	ps
Output differential skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	—	—	1	ps
Transmit output jitter	Δt_{TXRND}	Random, wideband, RMS	—	0.008	0.010	UI
	Δt_{TXtot}	Total, peak-to-peak	—	0.15	0.28	UI
	Δt_{TXdet}	Deterministic, peak-to-peak	—	0.05	—	UI

a. The value depends on the package and board routings.

5.5.5 Merlin (TSCm) Interface

The device serial interface supports the following features:

- Quad SerDes block supporting four serial links.
- Line rates of 1.25G, with up to 10.3125 Gbaud per serial link. Oversampling mode is used if the speed is below 2.5G.
- SST driver with 2 × 50Ω internal termination.
- Controlled peak-to-peak amplitude.

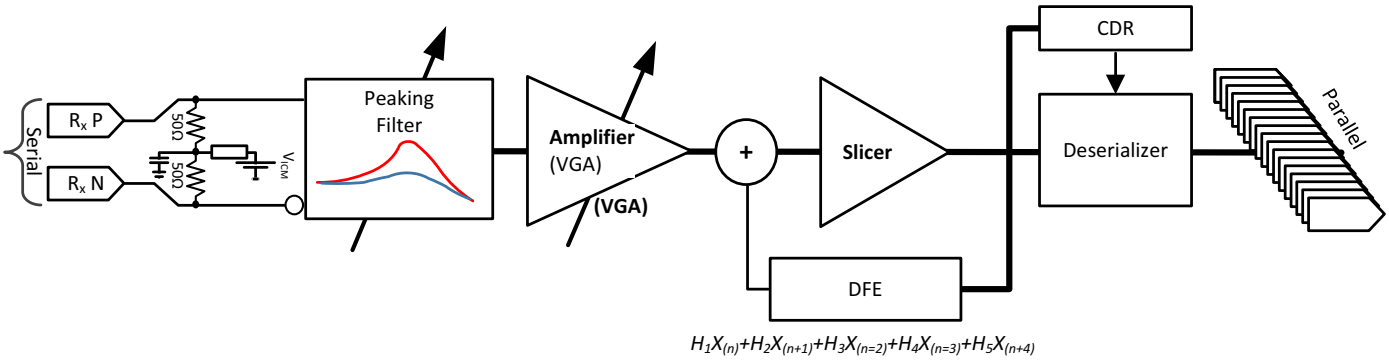
The serial interface operating conditions are shown in the following table and figure.

Table 33: Merlin Technology Serial Interface Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud, symbol rate	B_{PS}	1.25	—	10.3125	Gbaud
Unit interval	UI	—	97	—	ps

5.5.5.1 Merlin Receiver

Figure 19: SerDes Receiver Conceptual Diagram



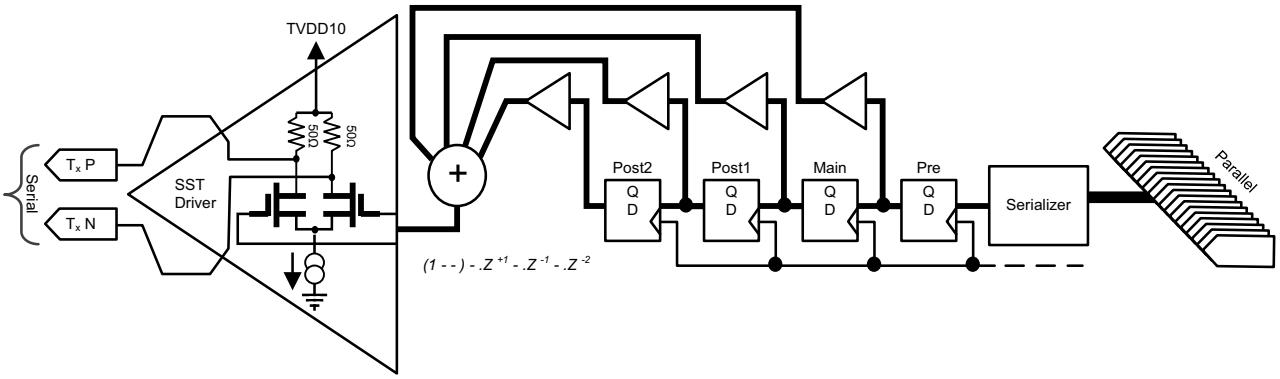
The serial interface receive characteristics are shown in the following table and figure.

Table 34: Serial Interface Receive Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Jitter tolerance	Δt_{RXtot}	Total, peak-to-peak	—	—	0.65	UI
	Δt_{RXdet}	Deterministic, peak-to-peak	—	—	0.42	UI

5.5.5.2 Merlin Transmitter

Figure 20: SerDes Transmitter Conceptual Diagram



The serial interface transmit characteristics are shown in the following table.

Table 35: Serial Interface Transmit Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Output voltage fall time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, eight 1's and eight 0's)	24	—	36	ps
Output voltage rise time	t_{rise}	20% to 80% (based on 10GBASE-KR waveform, eight 1's and eight 0's)	24	—	36	ps
Output differential skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	—	—	5	ps
Transmit output jitter	Δt_{TXRND}	Random, wideband, RMS	—	0.008	0.130	UI
	Δt_{TXtot}	Total, peak-to-peak	—	—	0.18	UI
	Δt_{TXdet}	Deterministic, peak-to-peak	—	0.05	—	UI

5.5.6 PCIe Interface

5.5.6.1 PCIe Receiver Input

Figure 21: PCIe_RX Timing Diagram

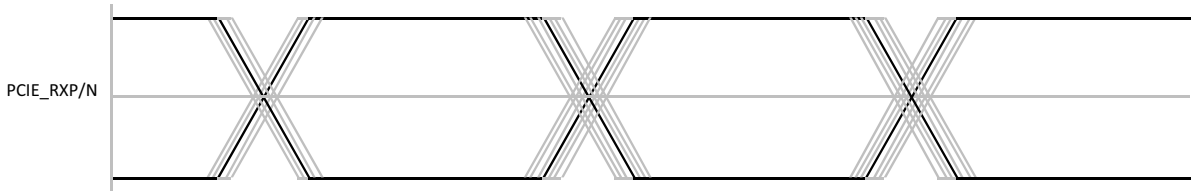


Table 36: PCIe_RX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Baud rate	FREQ	—	2.5, 5.0, or 8.0	—	Gbaud
Minimum RX total jitter	T_J	0.6	—	—	UI
NOTE: Includes on-chip AC coupling capacitors.					

5.5.6.2 PCIe Transmitter Output

Figure 22: PCIe_TX Timing Diagram

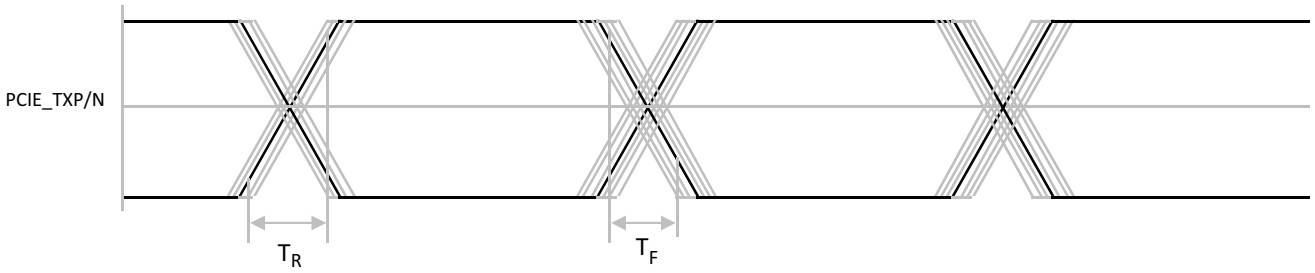


Table 37: PCIe_Transmitter Output Timing

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Baud rate	FREQ	—	—	2.5, 5.0, or 8.0	—	Gbaud
Output rise/fall time (20% to 80%)	T_R/T_F	—	30	—	90	ps
Output deemphasis[a]	V_{OEQ}	Gen1 2.5 Gb/s Gen1 5.0 Gb/s	–3.0 –5.5	–3.5 –6.0	–4.0 –6.5	dB
Minimum TX total jitter	T_J	—	0.75	—	—	UI

a. The output deemphasis values listed in this table are the default settings. TX deemphasis can be software configured in the range of 0 db to 8 dB, overriding the defaults.

5.5.7 BroadSync Interface

The following figure and table show the slave mode input timing.

Figure 23: BroadSync Input Timing: Slave Mode

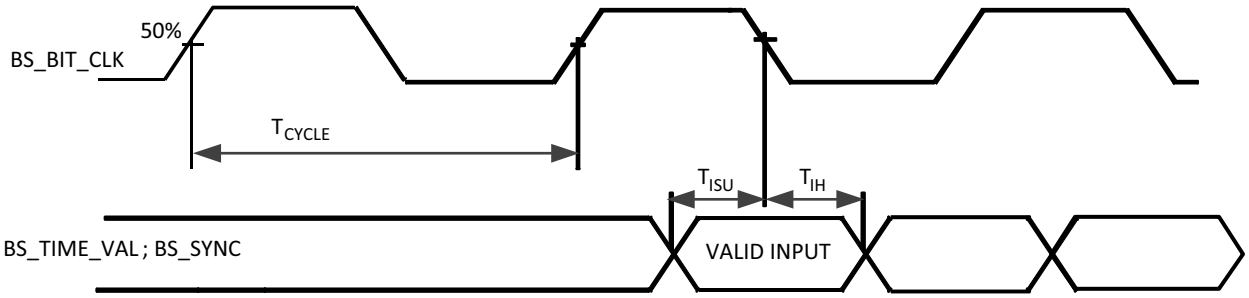


Table 38: BroadSync Input Timing: Slave Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	500	—	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	%
BS_TIME_VAL; BS_SYNC input setup time	t_{ISU}	20	—	—	ns
BS_TIME_VAL; BS_SYNC input hold time	t_{IH}	0	—	—	ns

The following figure and table show the master mode input timing.

Figure 24: BroadSync Output Timing: Master Mode

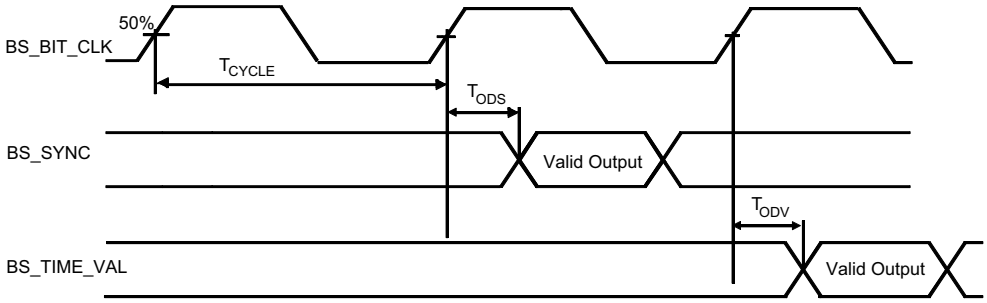


Table 39: BroadSync Output Timing: Master Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	500	—	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	%
BS_SYNC output delay	t_{ODS}	0	—	25	ns
BS_TIME_VAL output delay	t_{ODV}	0	—	25	ns

5.5.8 BSC Interface

The BSC interface can operate in the following two modes:

- Slave mode
- CPU-controlled master/slave mode

The external master drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

Figure 25: BSC Timing Diagram

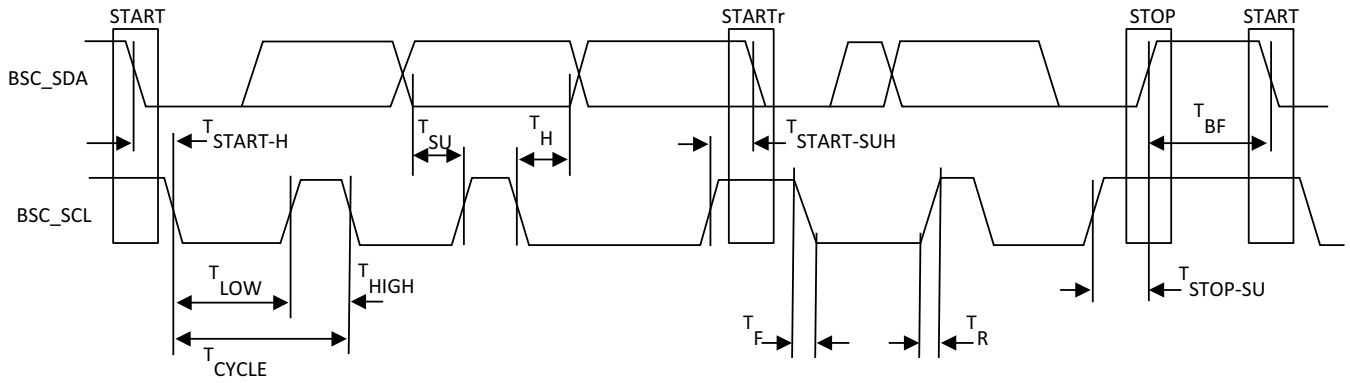


Table 40: BSC Master/Slave Fast-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	400	kHz
BSC_SCL cycle time	T_{CYCLE}	2.5	—	—	µs
BSC_SCL low time	T_{LOW}	1.3	—	—	µs
BSC_SCL high time	T_{HIGH}	0.6	—	—	µs
Data hold time	T_{H}	0	—	—	µs
Data setup time	T_{SU}	100	—	—	ns
Rise time, clock, and data (see note)	T_{R}	—	—	300	ns
Fall time, clock, and data (GBD)	T_{F}	—	—	300	ns
Hold time, start or repeated start	$T_{START–H}$	0.6	—	—	µs
Setup time, repeated start	$T_{START–SU}$	0.6	—	—	µs
Setup time, stop	$T_{STOP–SU}$	0.6	—	—	µs
Bus free time (between stop and start)	T_{BF}	1.3	—	—	µs

Table 41: BSC Master/Slave Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	100	kHz
BSC_SCL cycle time	T_{CYCLE}	10	—	—	µs
BSC_SCL low time	T_{LOW}	4.7	—	—	µs
BSC_SCL high time	T_{HIGH}	4.0	—	—	µs
Data hold time	T_H	0.0	—	—	µs
Data setup time	T_{SU}	250	—	—	ns
Rise time, clock, and data (see note)	T_R	—	—	1000	ns
Fall time, clock, and data (GBD)	T_F	—	—	300	ns
Hold time, start, or repeated start	$T_{START–H}$	4.0	—	—	µs
Setup time, repeated start	$T_{START–SU}$	4.7	—	—	µs
Setup time, stop	$T_{STOP–SU}$	4.0	—	—	µs
Bus free time (between stop and start)	T_{BF}	4.7	—	—	µs

NOTE: BSC_SCL and BSC_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which must be selected to meet the rise-time requirement.

The device drives the BSC_SCL clock with a programmable speed of 100 kHz or 400 kHz based on the mode bit called MODE_400. The device drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

5.5.9 LED Interface

LED[4:0]_CLK and LED[4:0]_DATA are outputs. The LED[4:0]_CLK output clock period is 200 ns (5.0 MHz).

Figure 26: LED Timing Diagram

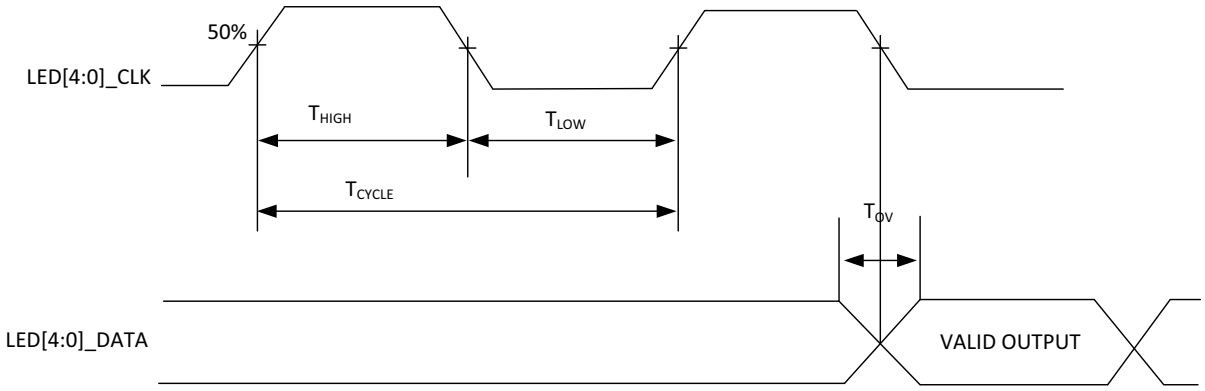


Table 42: LED Timing[a]

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED[4:0]_CLK clock frequency	f_{CLK}	—	5	5	MHz
LED[4:0]_CLK cycle time	T_{CYCLE}	200	—	—	ns
LED[4:0]_CLK high time	T_{HIGH}	70	100	130	ns
LED[4:0]_CLK low time	T_{LOW}	70	100	130	ns
LED[4:0]_DATA output valid time	T_{OV}	–15	—	15	ns

a. Timing values are specified at the 50% crossing thresholds.

5.5.10 Management Interface (MIIM)

5.5.10.1 MDIO AC Characteristics

Figure 27: MIIM Interface Timing Diagram

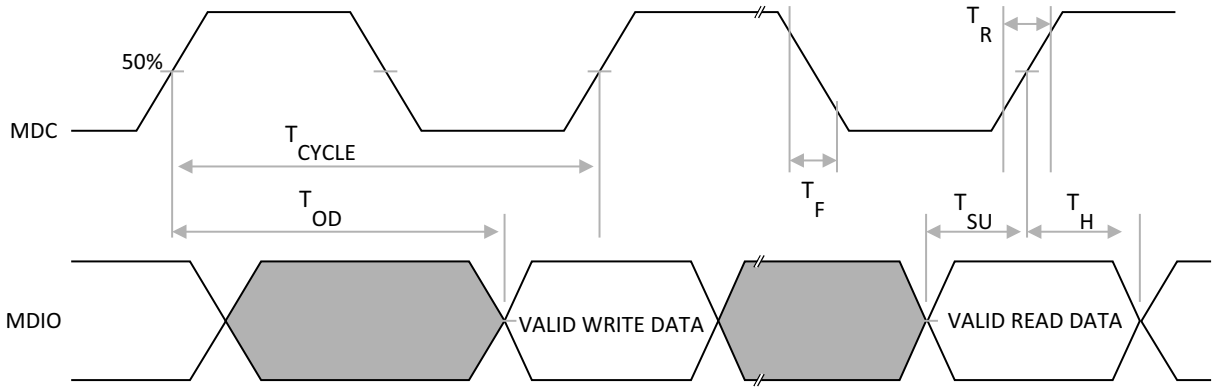


Table 43: 1.2V MDC/MDIO Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
MDC clock frequency	f_{CLK}	—	2.5	12.5	MHz
MDC cycle time	T_{CYCLE}	80	400	—	ns
MDC duty cycle	—	40	—	60	%
MDIO setup time	T_{SU}	20	—	—	ns
MDIO hold time	T_H	0	—	—	ns
MDIO output delay	T_{OD}	10	—	30	ns

NOTE: The following notes apply to MDC/MDIO timing:

- Output load conditions = 25 pF.
- External device to conform to IEEE specifications.
- MDIO output delay is programmable.

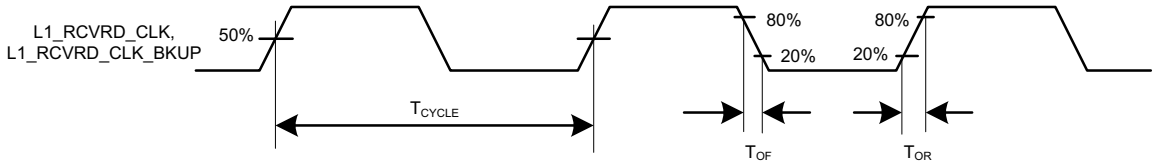
5.5.11 Synchronous Ethernet Interface

The following table and figure describe the L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP output timing.

Table 44: L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP cycle time	T_{CYCLE}	6.4	—	40	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP duty cycle	T_{HIGH}	45	—	55	%

Figure 28: Synchronous Ethernet Output Timing Diagram



5.5.12 JTAG Interface

Figure 29: JTAG Timing Diagram

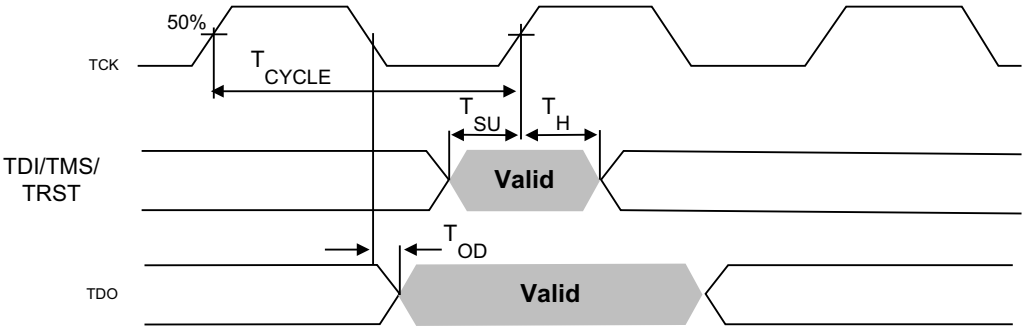


Table 45: JTAG AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
JTCK clock frequency	f_{CLK}	—	—	12.5	MHz
JTCK duty cycle	—	45	—	55	%
JTCK cycle time	t_{CYCLE}	80.0	—	—	ns
JTCK falling edge to output valid (applicable to *JTDO)*	t_{OD}	0	—	25	ns
Data input setup time before *JTCK (*applicable to *JTDI and JTMS)*	t_{SU_JT}	15	—	—	ns
Data hold time after *JTCK* rise (applicable to *JTDI and JTMS)*	t_{H_JT}	5	—	—	ns
Input setup time before *JTCK* rising edge (applicable to *JTRST_N)*	t_{SU_JTRS}	15	—	—	ns
Input hold time after *JTCK* rising edge (applicable to *JTRST_N)*	t_{H_JTRS}	5	—	—	ns

NOTE: Unless otherwise noted, the specifications are valid across the following operating conditions:

- The threshold value is at 50% of the applicable I/O rail voltage.
- The default loading on an output is 5 pF.

5.5.13 QSPI Interface

Figure 30: IP_QSPI Timing (Read/Write Mode Using MSPI Controller)

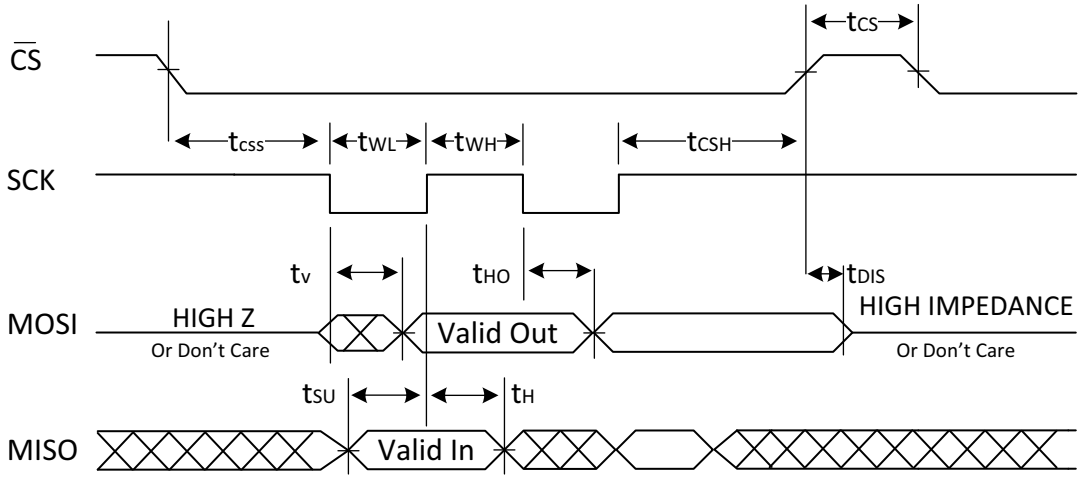
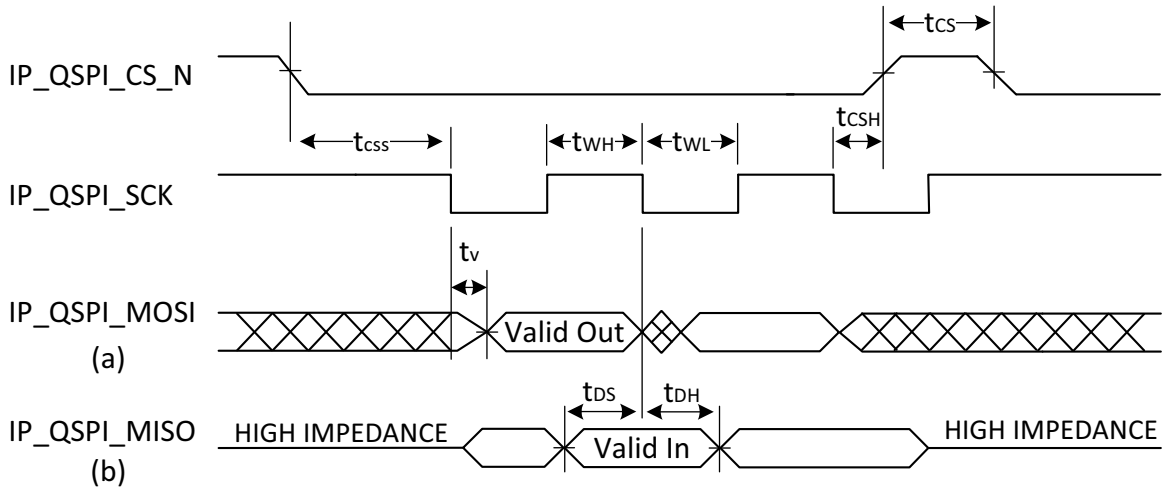


Table 46: IP_QSPI Timing (Read/Write Mode Using MSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	15.625	MHz
SCK clock LOW period	t_{WL}	0.5 / Fsck – 0.5	—	—	ns
SCK clock HIGH period	t_{WH}	0.5 / Fsck – 0.7	—	—	ns
CS lead time	t_{CSS}	0.5 / Fsck – 4	—	—	ns
CS trail time	t_{CSH}	9.6	—	—	ns
CS high time	t_{CS}	81	—	—	ns
MOSI output valid	t_V	—	—	13	ns
MOSI output hold	t_{HO}	4	—	—	ns
MISO input setup	t_{SU}	9	—	—	ns
MISO input hold	t_H	4	—	—	ns
MOSI output disable[a]	t_{DIS}	—	—	—	ns

a. The IP_QSPI_MOSI signal is always driven.

Figure 31: IP_QSPI Timing (Boot Read Mode Using BSPI Controller)



a): also valid for IP_QSPI_MISO in dual/quad mode; also valid for IP_QSPI_WP_N, IP_QSPI_HOLD_N in quad mode
b): also valid for IP_QSPI_MOSI in dual/quad mode; also valid for IP_QSPI_WP_N, IP_QSPI_HOLD_N in quad mode

Table 47: IP_QSPI Timing (Boot Read Mode Using BSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	50	MHz
SCK clock LOW period	t_{WL}	0.5 / Fsck – 0.5	—	—	ns
SCK clock HIGH period	t_{WH}	0.5 / Fsck – 0.5	—	—	ns
CS lead time	t_{CSS}	1 / Fsck – 2.9	—	—	ns
CS trail time	t_{CSH}	–1.6	—	—	ns
MOSI output valid	t_V	–1.6	—	3	ns
MISO input setup	t_{SU}	4	—	—	ns
MISO input hold	t_H	1.3	—	—	ns

5.5.14 SPI Interface

Figure 32: IP_SPI Timing (SPI Master: Mode 0)

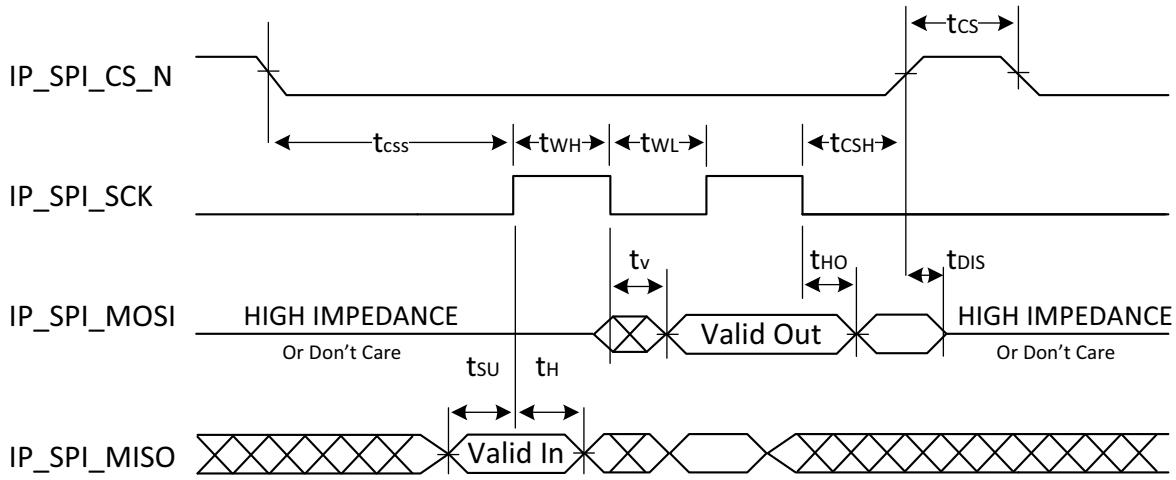


Figure 33: IP_SPI Timing (SPI Master: Mode 3)

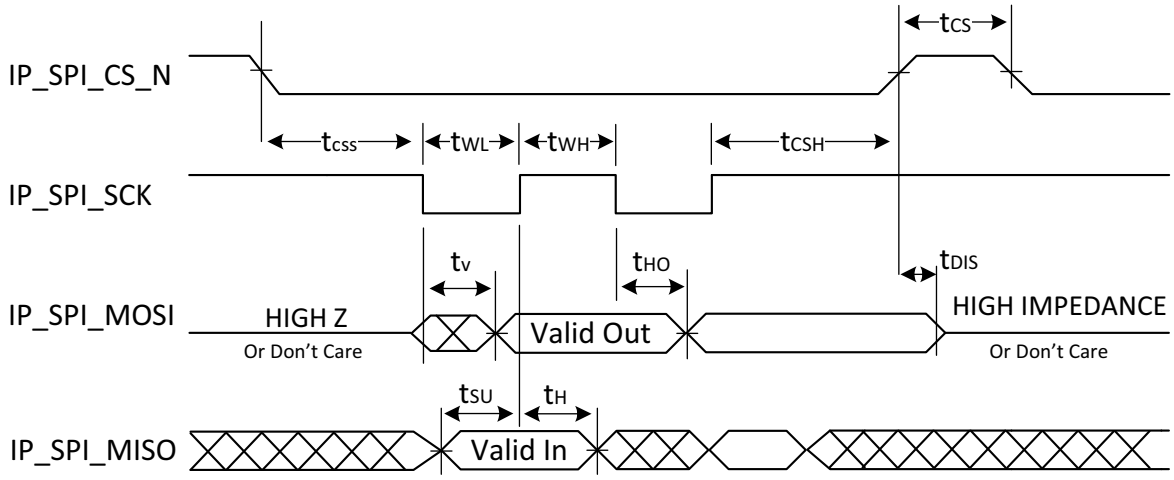


Table 48: IP_SPI Timing (Master Mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	31.25	MHz
SCK clock LOW period	t_{WL}	0.5 / Fsck – 1	—	—	ns
SCK clock HIGH period	t_{WH}	0.5 / Fsck – 1	—	—	ns
CS lead time	t_{CSS}	0.5 / Fsck – 4	—	—	ns
CS trail time	t_{CSH}	0.5 / Fsck – 4	—	—	ns
CS high time (SPH = 0)	t_{CS}	0.5 / Fsck	—	—	ns
CS high time (SPH = 1)	t_{CS}	0	—	—	ns

Table 48: IP_SPI Timing (Master Mode) (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MOSI output valid	t_V	—	—	4	ns
MOSI output hold	t_{HO}	–4	—	—	ns
MISO input setup	t_{SU}	9	—	—	ns
MISO input hold	t_H	0	—	—	ns
MOSI output disable	t_{DIS}	—	—	4	ns

Chapter 6: Standard Electrical Characteristics

6.1 PAM4 Electrical Characteristics

The device is designed in compliance with CEI-56G-VSR, CEI-56G-LR, IEEE 802.3bs CDAUI-8 C2C/C2M, and IEEE 802.3cd standards.

6.2 40G XLAUI Electrical Characteristics

6.2.1 Transmitter

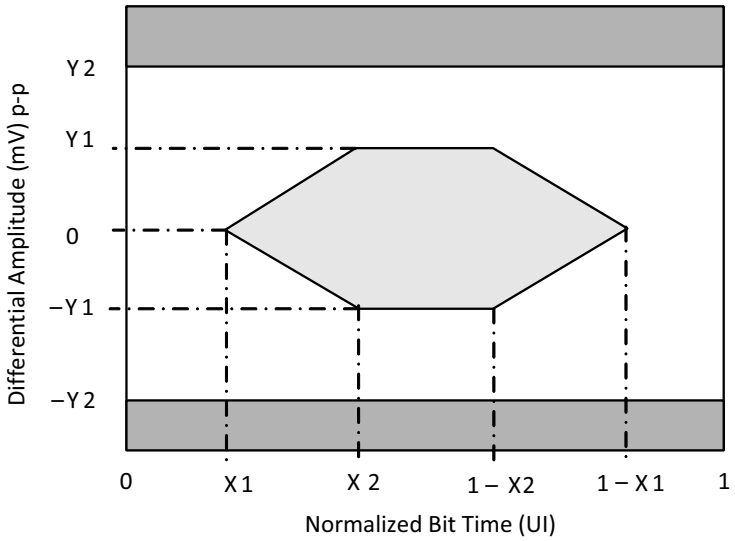
Table 49: XLAUI TX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Output speed per lane	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Differential output voltage (peak-to-peak)	VOD	—	—	760	mVp-p
Transmit eye mask (Figure 34)	X1	—	—	0.16	UI
Transmit eye mask (Figure 34)	X2	—	—	0.38	UI
Transmit eye mask (Figure 34)	Y1	200	—	—	mV
Transmit eye mask (Figure 34)	Y2	—	—	380	mV
Common mode voltage	VCM	—	0.65	—	V
Differential output return loss (minimum)	Equation[a]	—	—	—	dB
Common-mode output return loss (minimum)	Equation[b]	—	—	—	dB
Output rise time (20% to 80%)	Tr	24	—	—	ps
Output fall time (20% to 80%)	Tf	24	—	—	ps
Output jitter at $1e^{-12}$ BER					
Deterministic	sDJ	—	—	0.17	UI
Total	sTJ	—	—	0.32	UI

a. Return loss (f) ≤ 12 dB for 10 MHz ≤ f < 2.125 GHz.
Return loss ≤ [6.5 – 13.33 log (f / 5.5)] dB for 2.125 GHz ≤ f ≤ 11.1 GHz.

b. Return loss (f) ≤ 9 dB for 10 MHz ≤ f < 2.125 GHz.
Return loss ≤ [3.5 – 13.33 log (f / 5.5)] dB for 2.125 GHz ≤ f ≤ 7.1 GHz.
Return loss ≤ 2 dB for 7.1 GHz < f < 11.1 GHz.

Figure 34: XLAUI Transmit Eye Mask



6.2.2 Receiver

Table 50: XLAUI RX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Receiver coupling	AC	0.05	—	0.1	µF
Receive eye mask (Figure 35)	X1	—	—	0.31	UI
Receive eye mask (Figure 35)	X2	—	—	0.5	UI
Receive eye mask (Figure 35)	Y1	42.5	—	—	mV
Receive eye mask (Figure 35)	Y2	—	—	425	mV
Differential input return loss	Equation[a]	—	—	—	dB
Common mode input return loss	Equation[b]	—	—	—	dB
Receiving speed per lane	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Sinusoidal jitter tolerance	Figure 36	—	—	—	bps
Bit error rate based channel characteristics per Clause 83A in IEEE 802.3ba.	—	—	—	1e-12	bps

a. Return loss (f) ≤ 12 dB for 10 MHz ≤ f < 2.125 GHz.
Return loss ≤ [6.5 – 13.33 log (f / 5.5)] dB for 2.125 GHz ≤ f ≤ 11.1 GHz, where f is in GHz.

b. Return loss (f) ≤ 15 dB for 10 MHz ≤ f < 11.1 GHz, where f is in GHz.

Figure 35: XLAUI Receive Eye Mask

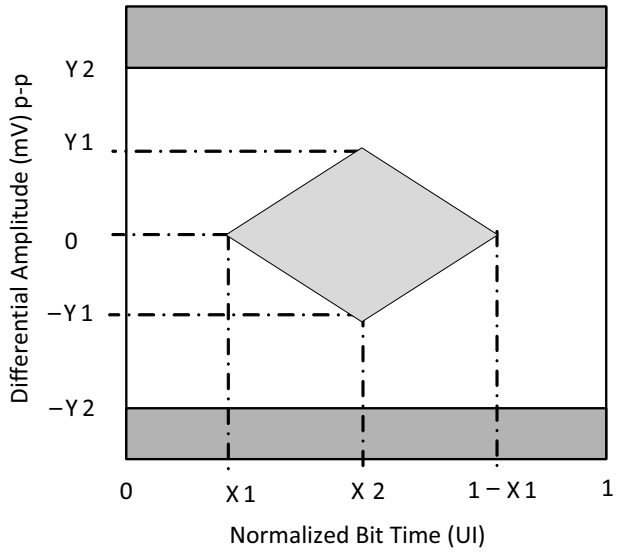
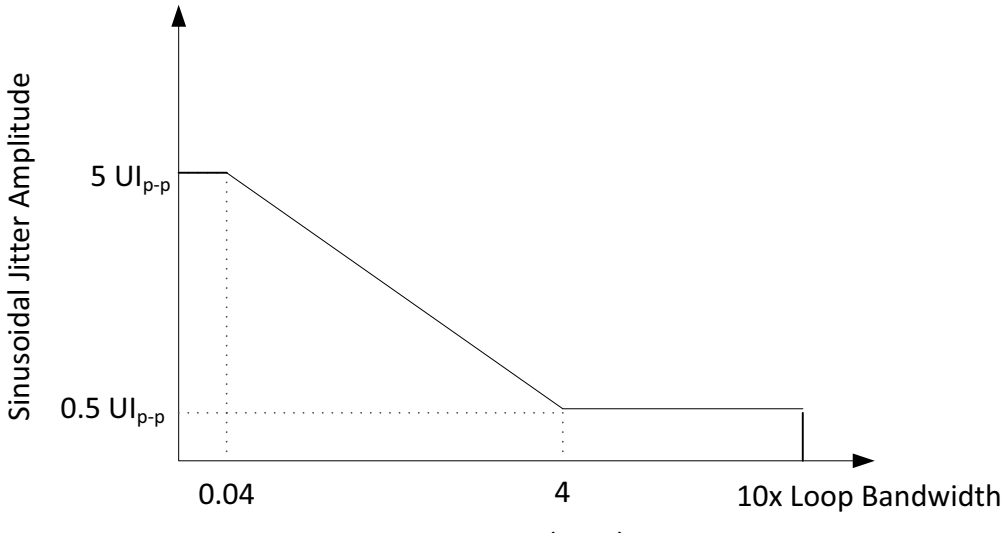


Figure 36: Single-Tone Sinusoidal Jitter Mask



6.3 10GBASE-KR Electrical Characteristics

6.3.1 Transmitter

Table 51: 10GBASE-KR TX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Output speed	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Differential output voltage (peak-to-peak) based on 101010 pattern	VOD	—	—	1200	mVp-p
Output voltage (peak-to-peak) when TX is disabled	VOD	—	—	30	mVp-p
Common mode voltage	VCM	0	—	1.9	V
Differential output return loss (minimum)	Equation[a]	—	—	—	dB
Common-mode output return loss (minimum)	Equation[b]	—	—	—	dB
Output rise time (20% to 80%)	Tr	24	—	47	ps
Output fall time (20% to 80%)	Tf	24	—	47	ps
Output jitter @ 1e-12 BER					
Random	sRJ	—	—	0.15	UI
Deterministic	sDJ	—	—	0.15	UI
Duty cycle distortion	sDCD	—	—	0.035	UI
Total	sTJ	—	—	0.28	UI

a. Return loss (f) ≥ 9 dB for 50 MHz ≤ f < 2500 MHz.
Return loss ≥ [9 – 12 log (f / 2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz.

b. Return loss (f) ≥ 6 dB for 50 MHz ≤ f < 2500 MHz.
Return Loss ≥ [6 – 12 log (f / 2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz.

6.3.2 Receiver

Table 52: 10GBASE-KR RX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Receiver coupling	AC	0.05	—	0.1	µF
Differential input voltage (peak-to-peak)	VID	—	—	1200	mVp-p
Differential input return loss (min)	Equation[a]	—	—	—	dB
Receiving speed	—	–100 ppm	10.3125 ppm	+100 ppm	Gbaud

a. Return loss (f) ≥ 9 dB for 50 MHz ≤ f < 2500 MHz.
Return loss ≥ [9 – 12 log (f / 2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz.

Chapter 7: Thermal Specifications

7.1 Thermal Requirements

The following tables provide device thermal specifications. The maximum θ_{JA} is a function of the maximum allowed ambient air temperature of the system and is given for ambient air temperatures of 50°C and 70°C. The device requires a steady state maximum junction temperature at 105°C. The device allows a junction temperature excursion of up to 115°C for a maximum period of 15 (< 96 hours contiguous) days per year. During the excursion period, the device continues to operate but its performance may degrade.

Table 53: Estimated Package Thermal Specifications for T_A = 70°C

Parameters	Symbol	Min.	Typ.	Max.	Unit
Power dissipation	P	—	—	530	W
Maximum junction temperature	T	—	—	105	°C
Maximum ambient temperature	A	—	—	70	°C
Maximum calculated θ_{JA}: (T-A)/P	O	—	—	0.066	°C/W

Table 54: Estimated Thermal Specifications for T_A = 50°C

Parameters	Symbol	Min.	Typ.	Max.	Unit
Power dissipation	P	—	—	530	W
Maximum junction temperature	T	—	—	105	°C
Maximum ambient temperature	A	—	—	50	°C
Maximum calculated θ_{JA}: (T-A)/P	O	—	—	0.104	°C/W

7.2 Package Thermal Specifications

To maintain a junction temperature below the maximum specified junction temperature, the Theta-JA (θ_{JA}) must be smaller than the maximum calculated θ_{JA} for the device. A heat sink and airflow is required.

7.3 Heat Sink

7.3.1 Heat Sink Selection

The device must be used with a heat sink. The end-use thermal environment combined with the operating mode of the device dictates the required thermal characteristics (size, thermal resistance, and so forth) of the heat sink.

7.3.2 Heat Sink Attachment

For heat sink attachment guidelines, including loading forces, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).

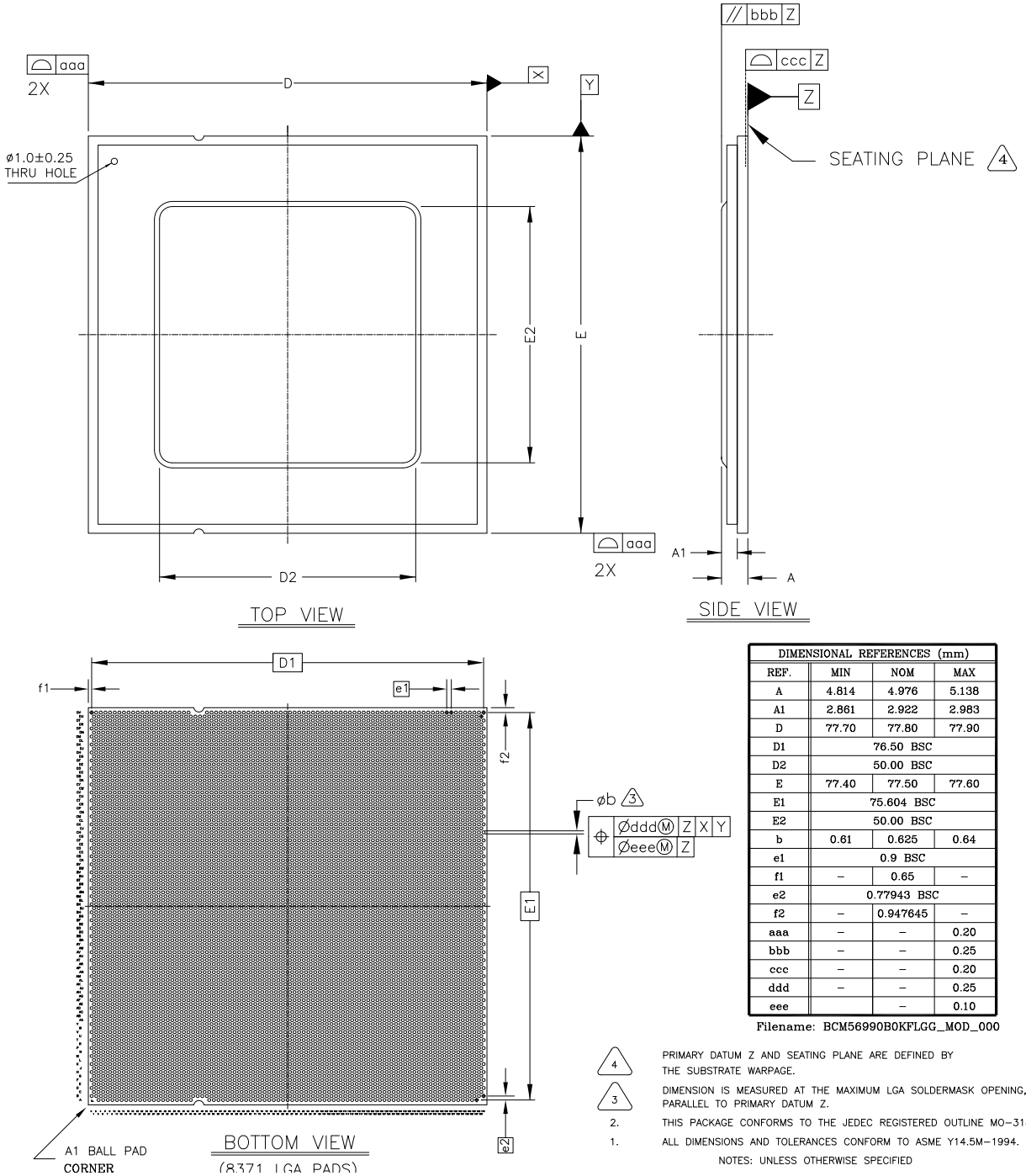
7.4 Socket Attachment

For socket attachment guidelines, refer to the *BCM56990 Hardware Design Guidelines* (56990-DG1xx).

Chapter 8: Mechanical Information

8.1 8371-Ball LGA

Figure 37: BCM5699x 8371-Ball LGA (77.8 mm × 77.5 mm)



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	4.814	4.976	5.138
A1	2.861	2.922	2.983
D	77.70	77.80	77.90
D1		76.50 BSC	
D2		50.00 BSC	
E	77.40	77.50	77.60
E1		75.604 BSC	
E2		50.00 BSC	
b	0.61	0.625	0.64
e1		0.9 BSC	
f1	–	0.65	–
e2		0.77943 BSC	
f2	–	0.947645	–
aaa	–	–	0.20
bbb	–	–	0.25
ccc	–	–	0.20
ddd	–	–	0.25
eee		–	0.10

Filename: BCM56990B0KFLGG_MOD_000

4 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SUBSTRATE WARPAGE.

3 DIMENSION IS MEASURED AT THE MAXIMUM LGA SOLDERMASK OPENING, PARALLEL TO PRIMARY DATUM Z.

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–318B.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Related Documents

The references in this section may be used in conjunction with this document.

NOTE: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (docSAFE) and Downloads and Support site.

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
BCM56990 Hardware Design Guidelines	56990-DG1xx	Broadcom CSP
IBIS-AMI model for BlackHawk7	BRCM_AMI_BlackHawk7_vx.x.zip	Broadcom CSP
IBIS-AMI model for Merlin	BRCM_AMI_Merlin_vx.x.zip	Broadcom CSP
BCM56990_ballout_revx.x.xlsx	BRCM56990_ballout_revx.x	Broadcom CSP
Delphi Thermal Model	BCM56990_Delphi_Model_r0.pdf	Broadcom CSP
StrataXGS® 64x 400GbE Switch SVK Schematic	956990KS-PB10x	Broadcom CSP
Heat Sink Attachment and Rework Guidelines Using Thermal Epoxy	PACKAGING-AN7xx	Broadcom CSP
Heat Sink Application Note	Heat_Sink-AN1xx	Broadcom CSP

Glossary

Table 55: Acronyms and Abbreviations

Term	Description
ACL	Access Control List
AGC	Automatic Gain Control
ARM	Advanced RISC Machines
ARP	Address Resolution Protocol
ASF	Alternate Store and Forward
AUI	Attachment Unit Interface
B-MAC	Backbone MAC
BCB	Backbone Core Bridge
BH7	Blackhawk7 PAM4 SerDes Core
BPDU	Bridge Protocol Data Unit
BSC	Broadcom Serial Controller
C-MAC	Customer MAC
CAUI	100 Gb/s Attachment Unit Interface
CFI	Canonical Field Indicator
CMIC	CPU Management Interface Controller
CML	Computer Managed Learning
CMOS	Complimentary Metal-Oxide Semiconductor
CoS	Class of Service
CPPI	100 Gb/s Parallel Physical Interface at the PMD layer
DCBX	Decision-Feedback Equalization
DFE	Decision-Feedback Equalization
DHCP	Dynamic Host Configuration Protocol
DIP	Destination IP address
DLF	Destination Lookup Failure
DNAT	Destination NAT
DSCP	Differentiated Services Code Point
DVMRP	Distance Vector Multicast Routing Protocol
DVMVO	Distance Vector
DXAUI	Altera's XAUI PHY Solution
ECMP	Equal Cost Multiple Paths
ECN	Explicit Congestion Notification
ENNI	External Network to Network Interface
EPON	Ethernet Passive Optical Network
ERSPAN	Encapsulated Remote SPAN
ETS	Enhanced Transmission Selection
FCID	Fibre Channel ID
FCoE	Fiber Channel over Ethernet
FEC	Forward Error Correction
FIP	FCoE Initialization Protocol

Table 55: Acronyms and Abbreviations (Continued)

Term	Description
FRR	Fast ReRoute
GBD	Guaranteed by Design
GPIO	General-Purpose Input/Output
GPON	Gigabit PON
GRE	Generic Routing Encapsulation
HiGig3	HiGig Version 3
HOL	Head of Line
HOLB	Head of Line Blocking
HPAE	Host Posture Assessment and Enforcement
HTLS	Hierarchical Transparent LAN Services
I-SID	I Domain SID
IETF	Internet Engineering Task Force
IGMP	Internet Group Management Protocol
IPMC	IP Muliticast
ITM	Ingress Traffic Manager
JTAG	Joint Test Action Group
KR	A specification defining a single backplane lane/physical layer coding as defined in IEEE 802.3 Clause 49
L2MC	Layer 2 Multicast
LAG	Link Aggregation Group
LGA	Land Grid Array
LLS	Linked List Scheduler
LoF	Loss of Frame
LoS	Loss of Signal
LPM	Longest Prefix Match
MAC	Media Access Control
MAC_DA	MAC Destination Address
MAC_SA	MAC Source Address
MDIO	Management Data Input/Output
MIIM	Media Independent Interface Management
MLD	Multicast Listener Discovery
MPLS	Multi-Protocol Label Switching
MTP	Mirror to Port
NAND	Special Form of Flash Memory
NAPT	Network Address Port Translator
NAT	Network address translation
NVGRE	Network Virtualized Generic Route Encapsulation (GRE)
OLT	Optical Line Termination
OOBFC	Out-of-Band Flow Control
PAM4	Four-Level Pulse Amplitude Modulation
PBB	Provider Backbone Bridges
PBB-TE	Provider Backbone Bridging with Traffic Engineering
PCIe	Peripheral Component Interconnect Express (PC bus)
PFC	Priority-based Flow Control

Table 55: Acronyms and Abbreviations (Continued)

Term	Description
PFM	Port Filter Mode
PHY	Physical Layer Interface
PIM	Protocol-Independent Multicast
PIM-BIDR	Protocol-Independent Multicast BiDirectional
PIM-DM	Protocol-Independent Multicast Dense Mode
PIM-SM	Protocol-Independent Multicast Sparse Mode
PIM-SSM	Protocol-Independent Multicast Single Source Multicast
PLL	Phase Loop Lock
QCN	Quantized Congestion Notification/Notifier
QoS	Quality of Service
QSGMII	Quad Serial Gigabit Media Independent Interface
RIOT	Routing In and Out of Tunnel
RMON MIB	Remote Monitoring Management Information Base
RSPAN	Remote Switched Port Analyzer
RSSI	Receive Signal Strength Indication
RX	Receiver
RXAUI	Reduced XAUI
S-VID	Service VLAN ID
SAFC	Service Aware Flow Control
SerDes	Serialize Deserialize
SFI	SerDes Framer Interface
SGMII	Serial Gigabit Media Independent Interface
SIP	Source IP address
SLA	Service Level Agreement
SMON MIB	Switched network MONitoring Management Information Base
SNAT	Source NAT
SNMP	Simple Network Management Protocol
SP	Strict Priority
srTCM	single rate Three Color Marker/Marking
SSTL	Stub Series Terminated Logic
TCAM	Ternary Content Addressable Memory
TDM	Time Division Multiplexor
ToR	Top of Rack
TPID	Tag Protocol ID
TRILL	Transparent Interconnection of Lots of Links
trTCM	two rate Three Color Marker/Marking
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
uRPF	unicast Reverse Path Forwarding
VCO	Voltage Controlled Oscillator
VFI	Virtual Forwarding Instance
VFP	VLAN Field Processor
VLAN	Virtual Local Area Network

Table 55: Acronyms and Abbreviations (Continued)

Term	Description
VOQ	Virtual Output Queue
VRF	Virtual Route Forwarding or VPN Routing and Forwarding
WCMP	Weighted Cost Multiple Paths
WDRR	Weighted Deficit Round-Robin
WEEE	Waste Electrical and Electronic Equipment
WRED	Weighted Random Early Detection
WRR	Weighted Round-Robin
XFI	10-Gigabit Serial Electrical Interface
XGMII	XGMII Extender Sublayer
XLPPI	40G (XL) Parallel Physical Interface

Revision History

56990-DS105-PUB; July 22, 2020

Initial release.