BA1356

FM stereo demodulator with noise controller

The BA1356 is an FM stereo demodulator.

Since the IC has a soft-muting function built-in, separation control, which lowers stereo noise when receiving weak RF signals by using the IF meter output voltage, and high frequency filtering, which decreases the treble frequency element noise, can be conducted independently of each other.

Features

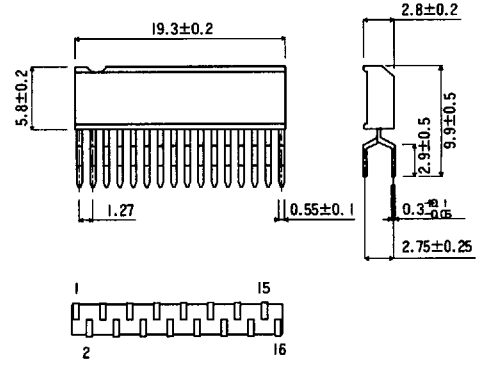
- available in a ZIP16 package
- wide operating voltage range (5.0 V ~ 12.0 V)
- low distortion (typically 0.2%)
- input/output gain is 3 dB
- separation value con be set with a control input. Internal resistance is set so that the separation is a maximum for a particular phase shift of the input signal.
- high frequency cutoff can be set by a control input
- terminals for VCO oscillation, forced monaural operation and high frequency cut-off are available
- protected against surging when modes are switched
- designed for compatibility with soft muting FM-IF BA4110

Applications

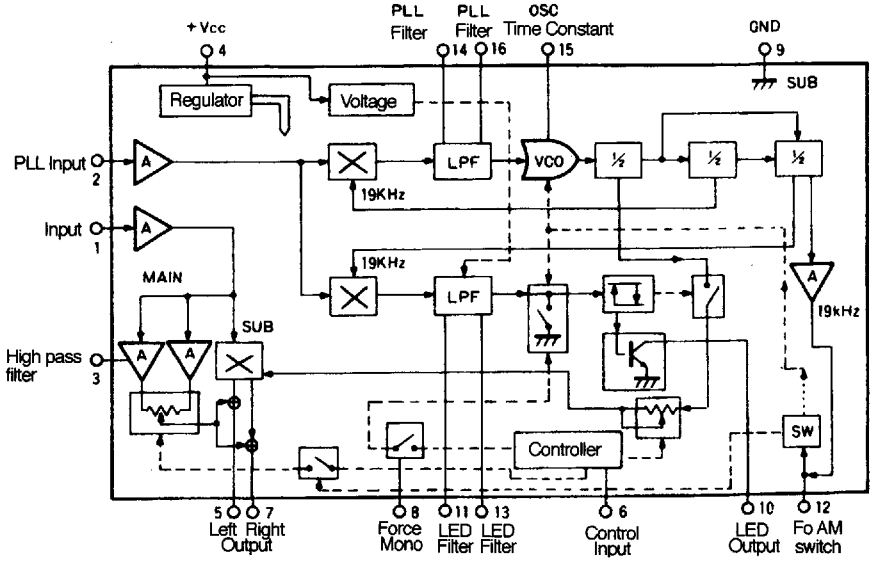
- car stereos
- high fidelity stereos

Dimensions (Units : mm)

BA1356 (ZIP16)



Block diagram



Absolute maximum ratings (T_a = 25°C)

Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V_{CC}	14	V	
Power dissipation	P_d	400	mW	Reduce power by 4.0 mW for each degree above 25°C
Operating temperature	T_{opr}	−25 ~ +75	°C	
Storage temperature	T_{stg}	−55 ~ +125	°C	

Electrical characteristics (unless otherwise noted, T_a = 25°C, V_{CC} = 9V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Operating voltage range	V_{CC}	5.0	9	12	V	
Quiescent current	I_Q	5	9	13	mA	
Maximum input signal	V_{IN}	500			mV_{rms}	
Input impedance	Z_{IN}	20	40	80	kΩ	
Channel separation	Sep	35	45		dB	Phase shift
Total harmonic distortion	THD		0.2	0.9	%	200 mV MAIN signal
Input/output gain	G_V	1.3	3		dB	Mono 200 mV_{rms}
Lamp lighting voltage	P_{IN}	6	10	14	mV_{rms}	Pilot level

Note: For test circuit, see Figure 1.

Figure 1 Test circuit

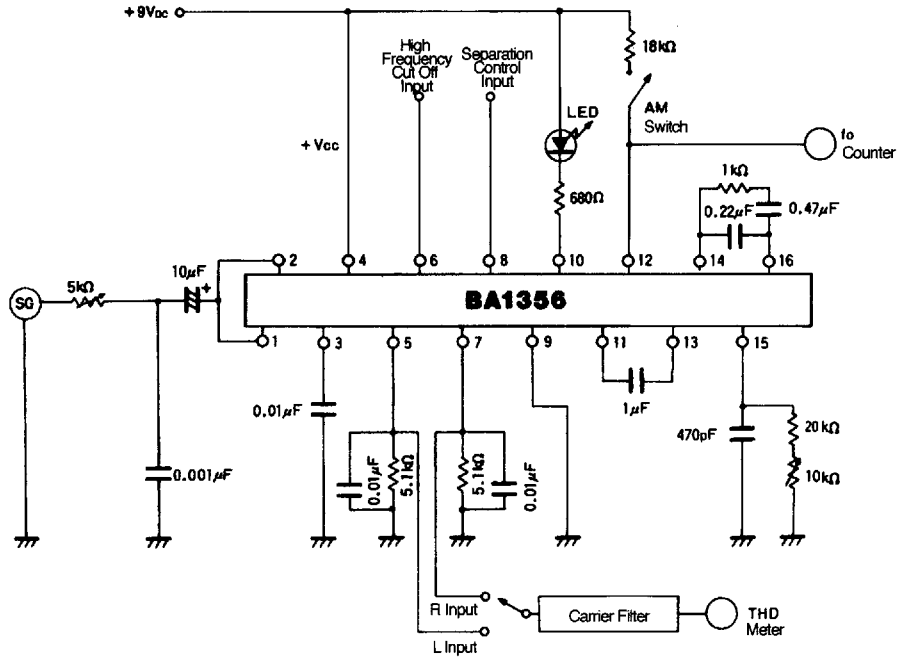
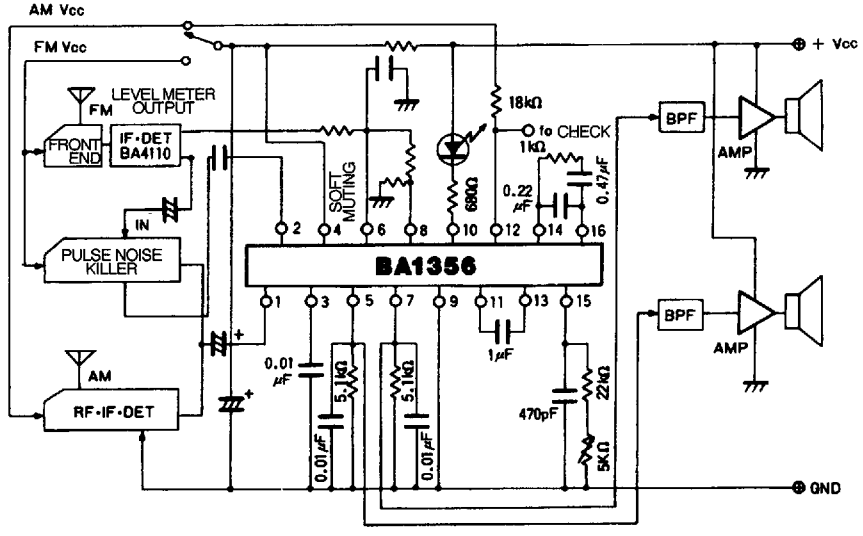


Figure 2 Application example



Note: When pin 12 is between 2 ~ 4 V, VCO oscillation can be terminated, and forced mono operation and high frequency cutoff can be cancelled.

BA1362F
BA1362FS

1.5 V FM stereo demodulator

The BA1362F and BA1362FS are PLL system FM stereo demodulators primarily for use with portable stereos operating at voltages as low as 1.5 V.

The BA1362F and BA1362FS use a PLL circuit that creates a 19 kHz or a 38 kHz signal synchronized with the input signal; a synchronized detection circuit, which detects the presence or absence of the 19 kHz pilot signal in the input signal; and a demodulation circuit, which is divided into right and left channels by an input signal switching operation. In addition, it has a built-in circuit to force monaural operation when the RF signal is weak. It also has an LED driver circuit for stereo operation display.

Features

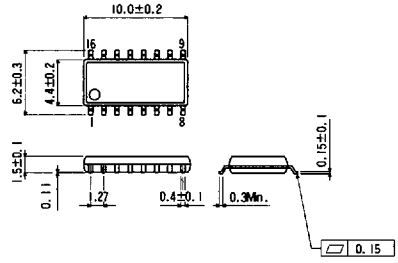
- available in a SOP16 and SSOP-A16 packages
- low operating voltage range (1.0 V ~ 2.5 V). Mono operation down to 0.9 V
- low distortion (typically 0.1%)
- gain can be set to 0 dB or +2.5 dB on input connection, no external parts
- provided with VCO stop terminal to prevent beats when in AM mode
- channel separation is controlled by the high frequency cut-off filter of the input unit
- built in output resistor determines de-emphasis (R_{OUT} = 5 kΩ)
- compatible with the BA4230AF 1.5 V FM/AM IF system IC

Applications

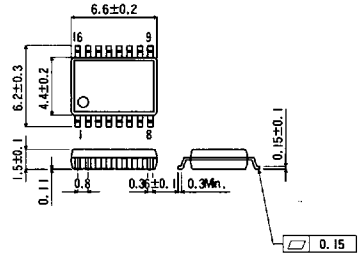
- 1.5 V headphone stereos

Dimensions (Units : mm)

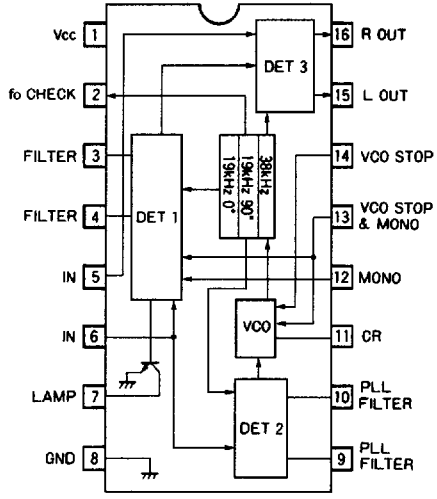
BA1362F (SOP16)



BA1362FS (SSOP-A16)



Block diagram



Absolute maximum ratings (T_a = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Power supply voltage		V_{CC}	3	V	
Power dissipation	BA1362F	P_d	300	mW	Reduce power by 3 mW for each degree above 25°C.
	BA1362FS		500		Reduce power by 5 mW for each degree above 25°C.
Operating temperature		T_{opr}	−25 ~ +75	°C	
Storage temperature		T_{stg}	−55 ~ +125	°C	

Recommended operating condition (T_a = 25°C)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Power supply voltage	V_{CC}	1.0	1.25	2.5	V	

Electrical characteristics (T_a = 25°C, V_{CC} = 1.25 V, f = 1 kHz, V_{IN} = 100 mV, L+R = 90%, Pilot = 10%) (Sheet 1 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Quiescent current	I_Q	1.6	4	6.2	mA	
Channel separation	Sep	30	35		dB	Input phase shift
Total harmonic distortion	THD		0.3	0.8	%	Main signal
Channel balance	CB	−2	0	2	dB	Mono signal
LED lighting level	V_P	2.5	4.5	7.0	mV_{rms}	Pilot signal only

Electrical characteristics (T_a = 25°C, V_{CC} = 1.25 V, f = 1 kHz, V_{IN} = 100 mV, L+R = 90%, Pilot = 10%) (Sheet 2 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
LED hysteresis	Hys		4.3	9.5	dB	
Input resistance	R_{IN}	4.5	8.2	12.0	kΩ	Short between pin 5 and pin 6
Output resistance	R_{Out}	3.6	5.1	6.6	kΩ	
Input/output gain	G_V		2.5		dB	
Signal-to-noise ratio	S/N		68		dB	
Capture range	CR		±3		%	Main signal
Forced monaural switch voltage	V_{CP12}		OPEN			Force cancel using ground connection
VCO stop voltage	V_{VCO14}		0.9		V	
Pilot detector output pin	I_P		5		mA	
Input level	V_{IN}	150			mV	THD = 6%

Note: For test circuit, see Figure 1.

Figure 1 Test circuit

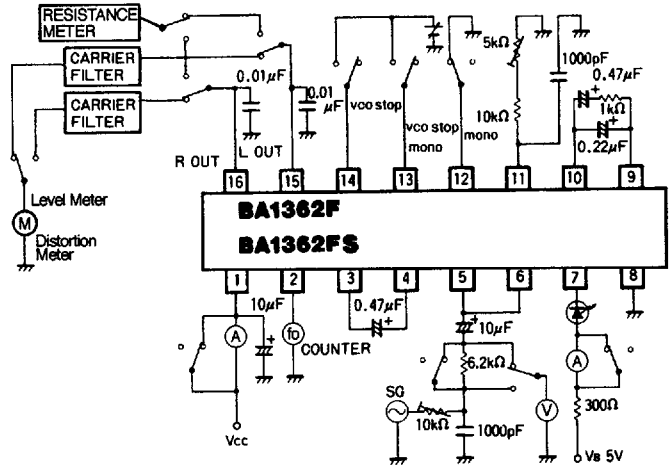
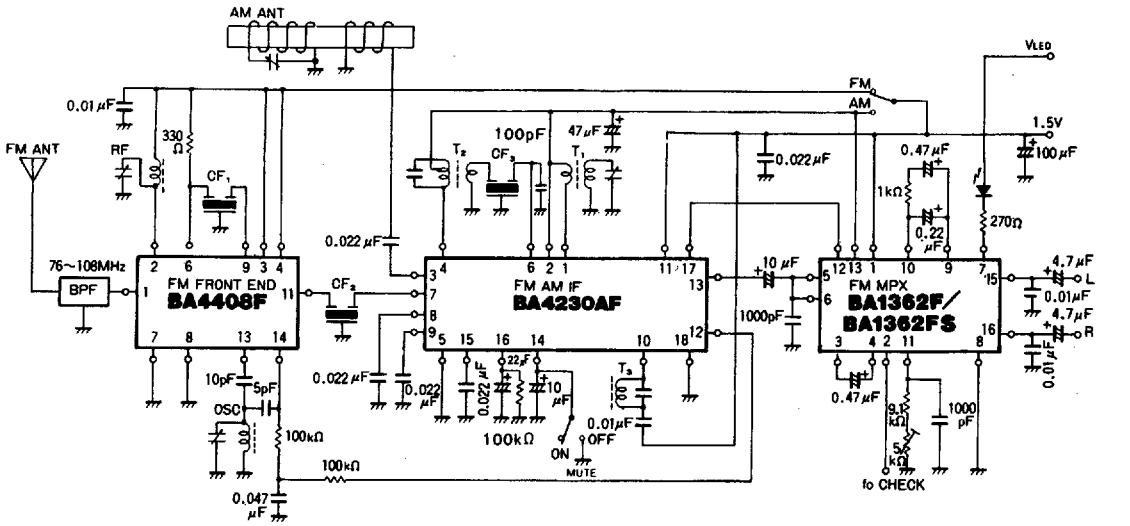


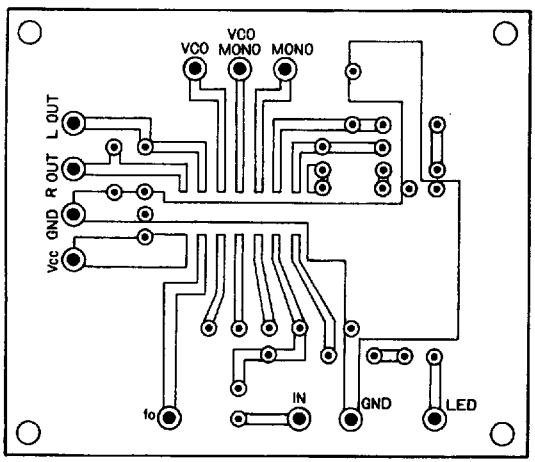
Figure 2 Application example (circuit diagram)



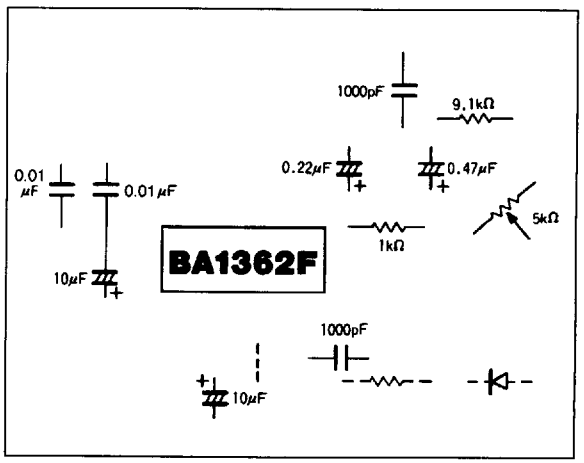
T1:AM OSC 4177-216(SUMIDA) CF1,CF2:FM SFE10.7MA5(MURATA)
T2:AM IFT 4175-352(SUMIDA) CF3:AM PFB455J (MURATA)
T3:FM DET 4176-303(SUMIDA)

Figure 3 PCB layout for application example

Solder side



Component side



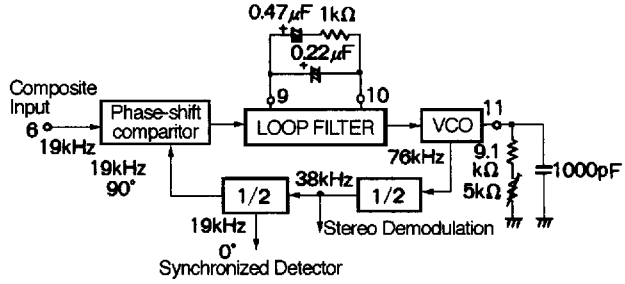
Description of operation

PLL circuit

The PLL circuit creates 19 kHz and 38 kHz signals that are synchronized with the 19 kHz pilot signal included in the composite signal that is used as a synchronized detector and stereo demodulation signal. (See Figure 4)

The circuit consists of a phase-shift comparator, a low-pass filter, a VCO and a half-frequency separator. The capture range is determined by the RC filter between pin 9 and pin 10, and both the lock range and the VCO frequency (f_O) are determined by the RC time constant between pin 11 and ground.

Figure 4

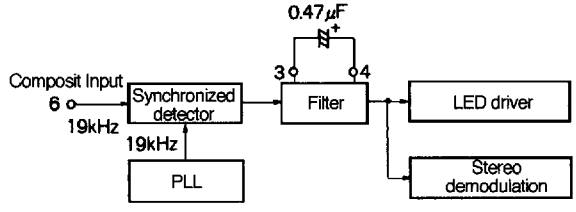


Synchronized detector

This circuit detects the presence or absence of the pilot signal by carrying out a synchronized detection of the pilot signal (19 kHz) in the composite signal and the 19 kHz signal created by the PLL circuit using the phase comparator. The LED driver and the demodulator circuit are turned ON and OFF by the output signal (after it has been smoothed to a dc level).

As the value of the capacitor between pin 3 and pin 4 is changed, the time to switch between stereo and monaural operation changes.

Figure 5



Stereo demodulator

The stereo demodulator switches the composite signal at a frequency of 38 kHz between the left and right channels and carries out stereo demodulation.

The composite signal is derived according to the following formula:

$$C(t) = (L+R) + (L-R)\cos\omega t + pc\cos\frac{\omega t}{2}$$

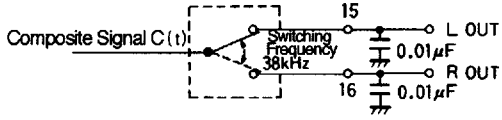
where ω = Sub-carrier frequency and p = pilot signal amplitude

When $\omega t = 2n\pi$, $C(t) = (L+R) + (L-R) = 2L$

and when $\omega t = (2n+1)\pi$, $C(t) = (L+R) - (L-R) = 2R$

The output impedance is set at 5 kΩ, and the capacitor is connected between pin 15 (16) and the ground. This is the band pass filter for the de-emphasis circuit.

Figure 6



Monaural circuit

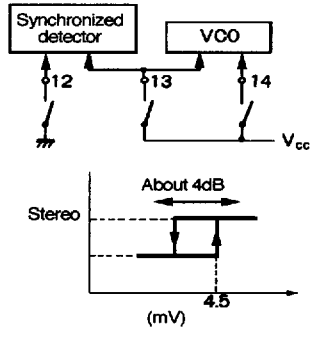
Monaural to stereo operation switching can be done automatically or it can be set manually. The dc voltage of the pilot level is used to switch the IC between these modes automatically. There is some built-in hysteresis to prevent excessive mode switching.

Manual switching occurs when the input to pins 12, 13, and 14 is changed

When pin 12 is opened, the IC is forced to monaural operation. When pin 12 is pulled down to ground, forced monaural operation is inhibited. When pin 14 is pulled up to the V_{CC}, VCO oscillations stop, and when pin 14 is opened, VCO stop is inhibited.

When pin 13 is pulled up to the V_{CC}, the IC is switched to monaural operation and the VCO oscillations stop. When pin 13 is opened, monaural operation and VSO stop are inhibited.

Figure 7



Electrical characteristic curves

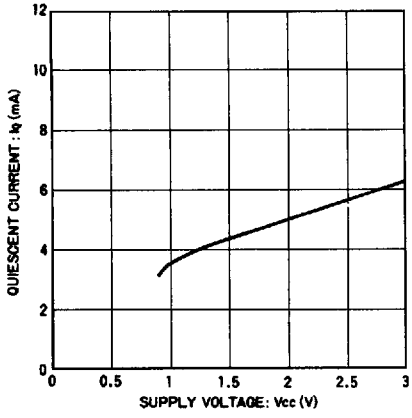


Figure 8

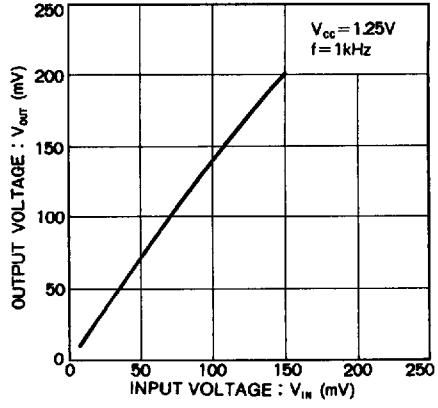


Figure 9

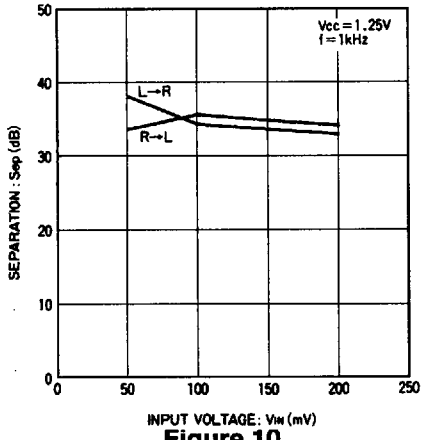


Figure 10

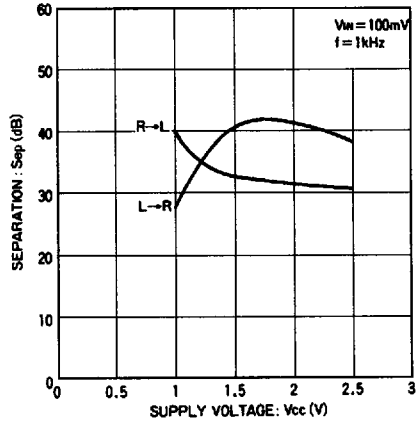


Figure 11

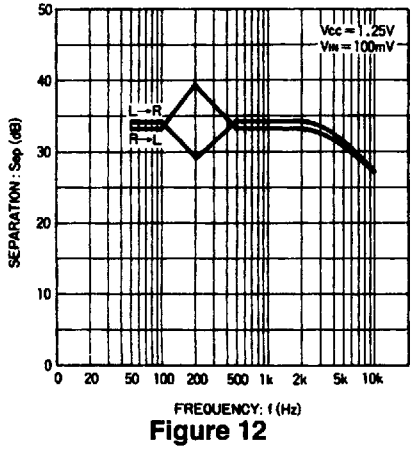


Figure 12

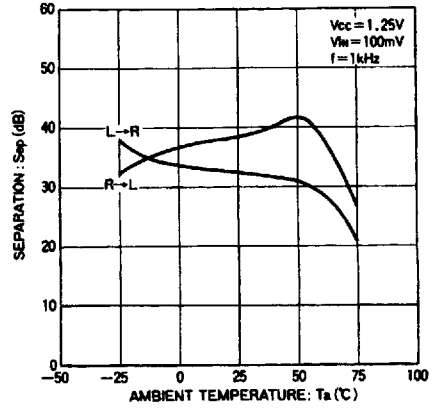


Figure 13

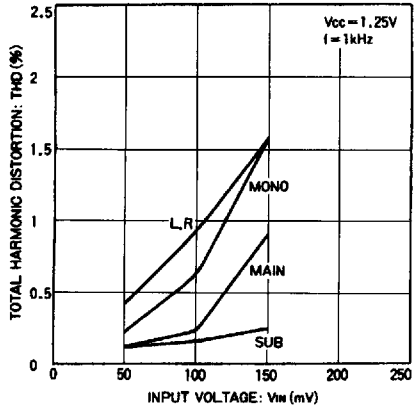


Figure 14

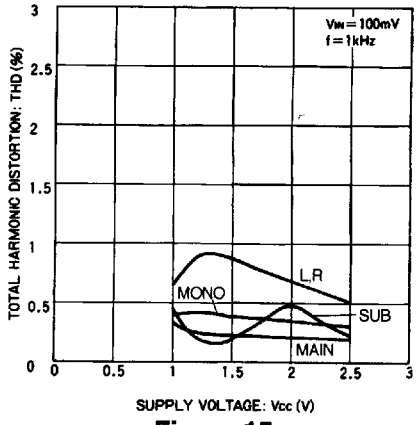


Figure 15

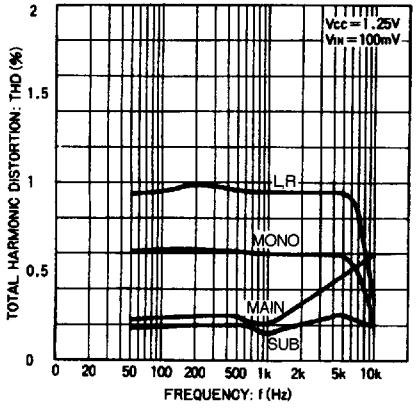


Figure 16

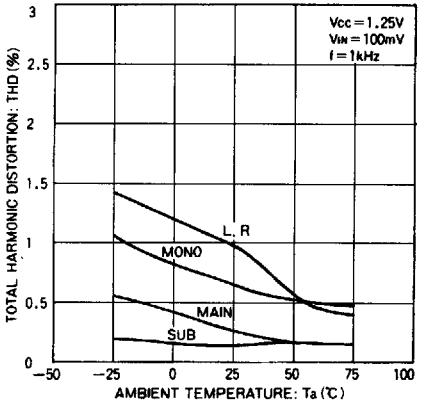


Figure 17

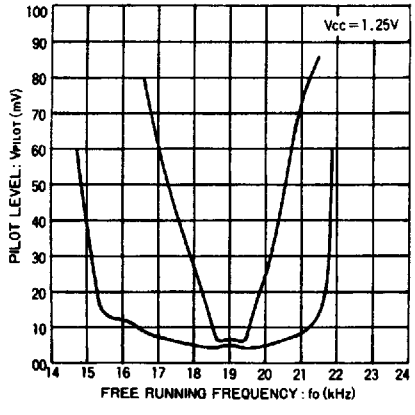


Figure 18

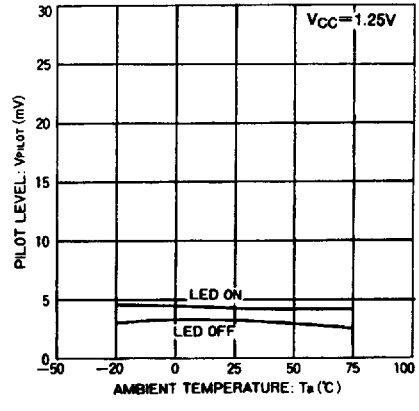


Figure 19

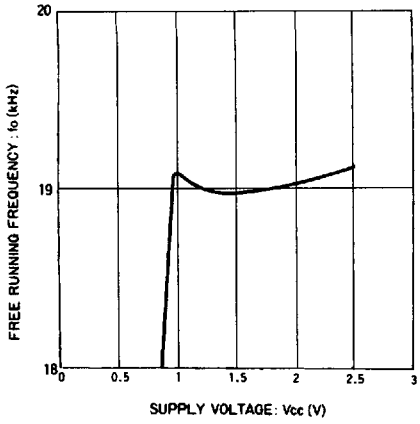


Figure 20

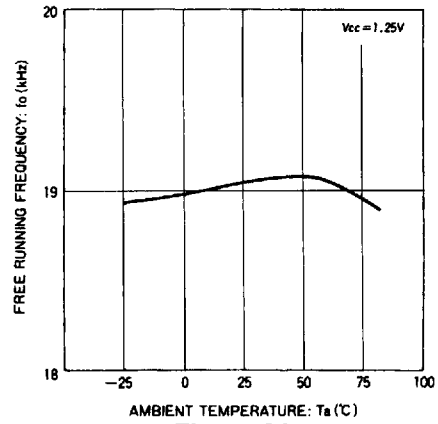


Figure 21

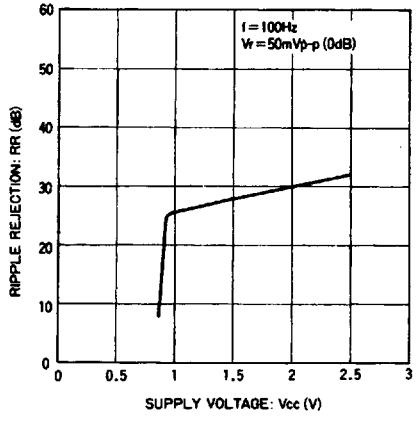


Figure 22

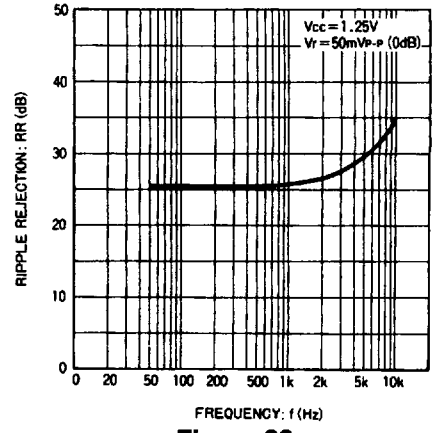


Figure 23