Ver 1.1

14-Bit 10MSPS Analog to Digital Converter

Datasheet

Part Number：B9240MGRH

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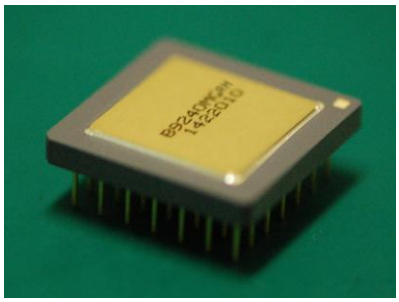
1. Unique Features



- Monolithic 14-Bit, 10 MSPS A/D Converter
- Power Dissipation: 320 mW
- Single +5 V Supply
- Integral Nonlinearity Error: 1.5 LSB
- Differential Nonlinearity Error: 0.8 LSB
- On-Chip Sample-and-Hold Amplifier and Voltage Reference
- Signal-to-Noise and Distortion Ratio: 73 dB
- Spurious-Free Dynamic Range: 75 dB
- Out-of-Range Indicator
- Straight Binary Output Data
- CPGA40 package
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV cm^2/mg

2. Product Description

The B9240MGRH is a radiation hardened, 10 MSPS, single supply, 14-bit analog-to-digital converter (ADC). It combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid implementations at a fraction of the power consumption and cost. It is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and-hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the DC accuracy and temperature drift requirements of the application. The device uses a multistage differential pipelined architecture with digital output error correction logic to guarantee no missing codes over the full operating temperature range.

The input of the B9240MGRH is highly flexible, allowing for easy interfacing to imaging, communications, medical, and data acquisition systems. A truly differential input structure allows for both single-ended and differential input interfaces of varying input spans. The sample-and-hold amplifier (SHA) is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels as well as sampling single channel inputs at frequencies up to and beyond the Nyquist rate. Also, the B9240MGRH performs well in communication systems employing Direct-IF Down Conversion since the SHA in the differential input mode can achieve excellent dynamic performance well beyond its specified Nyquist frequency of

1.5MHz.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

3. Functional Block Diagram

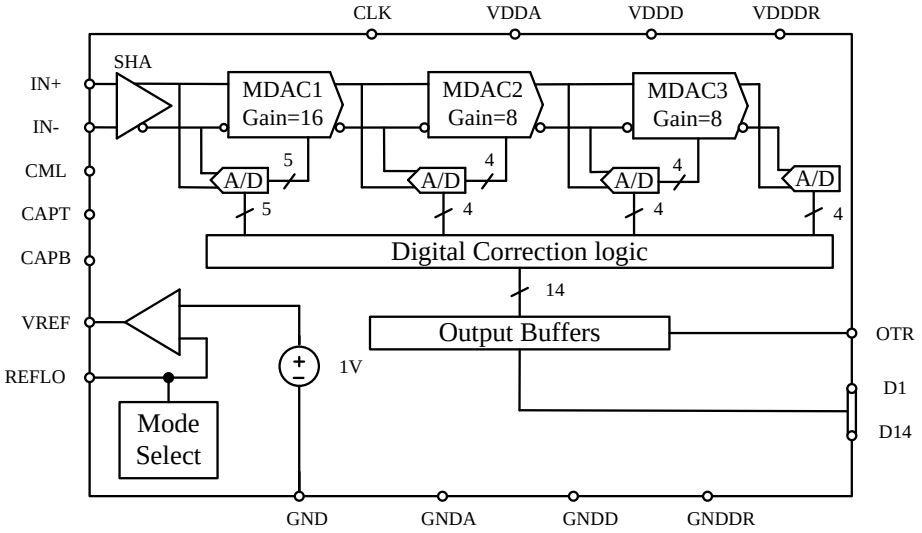


Figure 3-1. Functional Block Diagram

4. Pin Description

The B9240MGRH is packaged in CPGA40 package, as is shown in figure 4-1.

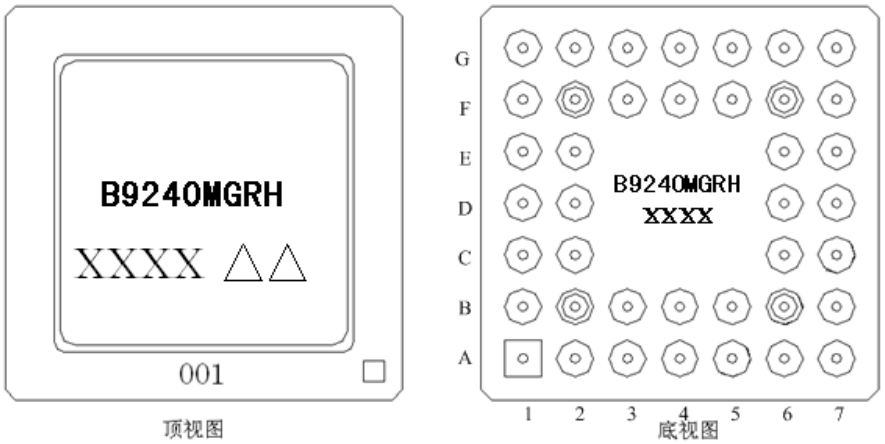


Figure 4-1. B9240MGRH pin description

B9240MGRH pin description table

Symbol	Attribute	Description
D1~14	O	Digital output

CML	O	Common mode
IN+、IN-	I	Analog input
CLK	I	Clock input
OTR	O	Out of range
REFLO	I	Reference select
V_{REF}	I/O	Reference input/output
BIAS	I	Power/Speed programming
CAPB	O	Noise reduction pin
CAPT	O	Noise reduction pin
GND	GND	Reference common ground
GND_A	GND	Analog ground
GND_{DR}	GND	Digital output driver ground
GND_D	GND	Digital ground
V_{DDA}	VDD	+5V analog supply
V_{DDD}	VDD	+5V digital supply
V_{DDDR}	VDD	Digital Output Driver Supply
NC	——	No connect

5. Pin Definition（Appendix 1）

6. Definitions of Specification

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from “negative full scale” through “positive full scale.” The point used as “negative full scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSINGCODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes, respectively, must be present overall operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below IN+ =

IN-. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, N = (SINAD – 1.76)/6.02 it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and DC. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

7. Product Description

The B9240MGRH utilizes a four-stage pipeline architecture with a wideband input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last stage, consists of a low resolution flash A/D connected to a switched capacitor DAC and inter stage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of

redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D. The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This latency is not a concern in most applications. The digital output, together with the out-of-range indicator (OTR), is latched into an output buffer to drive the output pins. The output drivers can be configured to interface with +5 V or +3.3 V logic families. The B9240MGRH uses both edges of the clock in its internal timing circuitry. The A/D samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock), the input SHA is in the sample mode; during the clock high time it is in the hold mode. System disturbances just prior to the rising edge of the clock and/or excessive clock jitter may cause the input SHA to acquire the wrong value, and should be minimized.

7.1 Power/Speed Programmability

The B9240MGRH's maximum conversion rate and associated power dissipation can be set using the part's BIAS pin. A simplified diagram of the on-chip circuitry associated with the BIAS pin is shown in Figure 7-1.

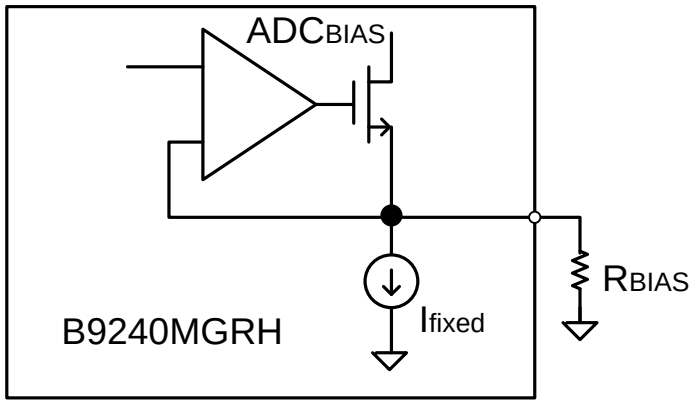


Figure 7-1. power/speed programmability

The value of R_{BIAS} can be varied over a limited range to set the maximum sample rate and power dissipation of the B9240MGRH. Note that all other plots and specifications in this data sheet reflect performance at a fixed R_{BIAS} = 2 kΩ.

7.2 Analog Input and Reference Overview

Figure 7-2, a simplified model of the B9240MGRH, highlights the relationship between the analog inputs, IN+, IN-, and the reference voltage, V_{REF}. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value V_{REF} defines.

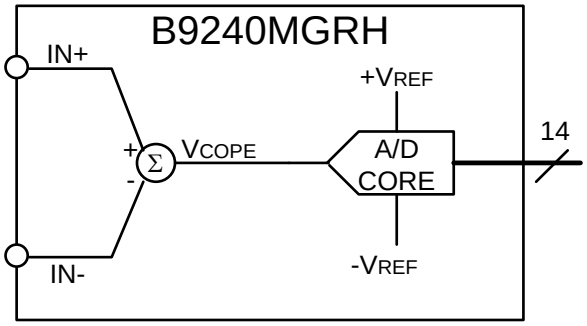


Figure 7-2. B9240MGRH Equivalent Functional Input Circuit

The addition of a differential input structure gives the user an additional level of flexibility that is not possible with traditional flash converters. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D's input structure allows the DC offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the A/D core is the difference of the voltages applied at the IN+ and IN- input pins.

Therefore, the equation,

$$V_{CORE} = IN+ - IN- \quad (1)$$

Defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE}, must satisfy the condition,

$$-V_{REF} \le V_{CORE} \le V_{REF} \quad (2)$$

Where V_{REF} is the voltage at the V_{REF} pin.

While an infinite combination of IN+ and IN- inputs exist that satisfy Equation (2), there is an additional limitation placed on the inputs by the power supply voltages of the B9240MGRH. The power supplies bound the valid operating range for IN+ and IN-. The condition,

$$GND_A - 0.3\ V < IN+ < V_{DDA} + 0.3\ V \quad (3)$$

$$GND_A - 0.3\ V < IN- < V_{DDA} + 0.3\ V \quad (4)$$

where GND_A is nominally 0V and V_{DDA} is nominally +5V, defines this requirement. Thus, the range of valid inputs for IN+ and IN- is any combination that satisfies both Equations (3),(4).

7.3 Analog Input Operation

Figure 7-3 shows the equivalent analog input of the B9240MGRH which consists of a differential sample-and-hold amplifier (SHA). The differential input structure of the SHA is highly flexible, allowing the devices to be easily configured for either a differential or single-ended input. The DC offset, or common-mode voltage, of the input(s) can be set to accommodate either single-supply or dual supply systems. Also, note that the analog inputs, IN+ and IN-, are interchangeable with the exception that reversing the inputs to the IN+ and IN- pins results in a polarity inversion.

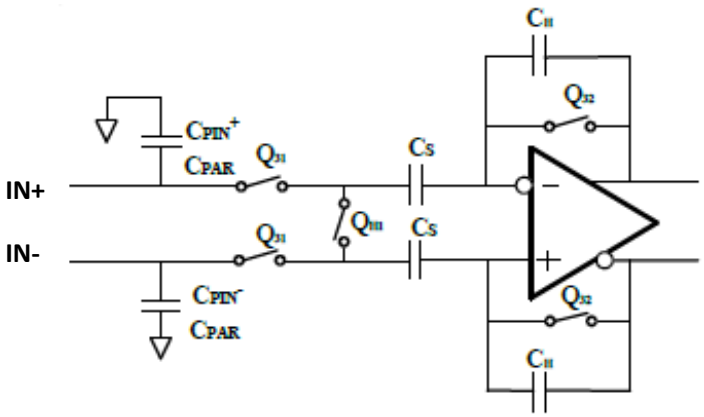


Figure 7-3. B9240MGRH Simplified Input Circuit

The input SHA of the B9240MGRH is optimized to meet the performance requirements for some of the most demanding communication, imaging, and data acquisition applications while maintaining low power dissipation.

The SHA's optimum distortion performance for a differential or single-ended input is achieved under the following two conditions: (1) the common-mode voltage is centered around midsupply (i.e., $V_{DDA}/2$ or approximately 2.5 V) and (2) the input signal voltage span of the SHA is set at its lowest (i.e., 2 V input span). This is due to the sampling switches, Q_{S1}, being CMOS switches whose R_{ON} resistance is very low but has some signal dependency which causes frequency dependent AC distortion while the SHA is in the track mode. The R_{ON} resistance of a CMOS switch is typically lowest at its midsupply but increases symmetrically as the input signal approaches either V_{DDA} or GND_A. A lower input signal voltage span centered at midsupply reduces the degree of R_{ON} modulation.

Due to the high degree of symmetry within the SHA topology, a significant improvement in distortion performance for differential input signals with frequencies up to and beyond Nyquist can be realized. This inherent symmetry provides excellent cancellation of both common-mode distortion and noise. Also, the required input

signal voltage span is reduced by a half which further reduces the degree of R_{ON} modulation and its effects on distortion.

The optimum noise and DC linearity performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 5 V input span) and matched input impedance for IN+ and IN-. Note that only a slight degradation in DC linearity performance exists between the 2 V and 5 V input span.

The differential SHA is implemented using a switched-capacitor topology. Hence, its input impedance and its subsequent effects on the input drive source should be understood to maximize the converter's performance. The combination of the pin capacitance, C_{PIN}, parasitic capacitance C_{PAR}, and the sampling capacitance, C_S, is typically less than 16 pF. When the SHA goes into track mode, the input source must charge or discharge the voltage stored on C_S to the new input voltage. This action of charging and discharging C_S which is approximately 4pF, averaged over a period of time and for a given sampling frequency, F_S, makes the input impedance appear to have a benign resistive component (i.e., 83 kΩ at F_S = 10.0 MSPS). However, if this action is analyzed within a sampling period (i.e., T = <1/FS), the input impedance is dynamic due to the instantaneous requirement of charging and discharging C_S. A series resistor inserted between the input drive source and the SHA input as shown in Figure 7-4 provides the effective isolation.

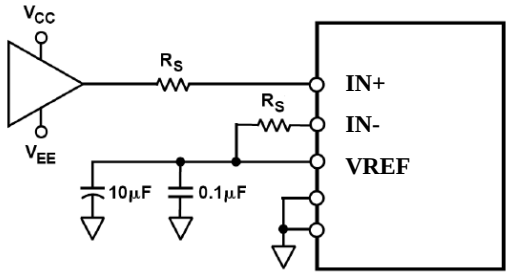


Figure 7-4. Series Resistor Isolates Switched-Capacitor SHA Input from Op Amp.

Matching Resistors Improve SNR Performance

The optimum size of this resistor is dependent on several factors which include the B9240MGRH sampling rate, the selected op amp, and the particular application. In most applications, a 30Ω to 50Ω resistor is sufficient. However, some applications may require a larger resistor value to reduce the noise bandwidth or possibly limit the fault current in an overvoltage condition. Other applications may require a larger resistor value as part of an anti-aliasing filter. In any case, since the THD performance is dependent on the series resistance and the above mentioned factors, optimizing this resistor value for a given application is encouraged.

A slight improvement in SNR performance and DC offset performance is achieved by matching the input resistance connected to IN+ and IN-. The degree of improvement is dependent on the resistor value and the sampling rate. For series resistor values greater than 100Ω, the use of a matching resistor is encouraged.

The noise or small-signal bandwidth of the B9240MGRH is the same as its full-power bandwidth. For noise sensitive applications, the excessive bandwidth may be detrimental and the addition of a series resistor and/or shunt capacitor can help limit the wide-band noise at the A/D's input by forming a low-pass filter. Note, however, that the combination of this series resistance with the equivalent input capacitance of the B9240MGRH should be evaluated for those time-domain applications that are sensitive to the input signal's absolute settling time. In applications where harmonic distortion is not a primary concern, the series resistance may be selected in combination with the SHA's nominal 16 pF of input capacitance to set the filter's 3 dB cutoff frequency.

A better method of reducing the noise bandwidth, while possibly establishing a real pole for an anti-alias filter, is to add some additional shunt capacitance between the input (i.e., IN+ and/or IN-) and analog ground. Since this additional shunt capacitance combines with the equivalent input capacitance of the B9240MGRH, a lower series resistance can be selected to establish the filter's cutoff frequency while not degrading the distortion performance of the device. The shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the hold capacitor, C_H, further reducing current transients seen at the op amp's output.

The effect of this increased capacitive load on the op amp driving the B9240MGRH should be evaluated. To optimize performance when noise is the primary consideration, increase the shunt capacitance as much as the transient response of the input signal will allow. Increasing the capacitance too much may adversely affect the op amp's settling time, frequency response, and distortion performance.

7.4 Reference Operation

The B9240MGRH contains an onboard bandgap reference that provides a pin-strappable option to generate either a 1 V or 2.5 V output. With the addition of two external resistors, the user can generate reference voltages other than 1 V and 2.5 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. Figure 7-7 shows a simplified model of the

internal voltage reference of the B9240MGRH. A pin-strappable reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the V_{REF} pin. The voltage on the V_{REF} pin determines the full-scale input span of the A/D. This input span equals,

$$\text{Full-Scale Input Span} = 2 \times V_{REF}$$

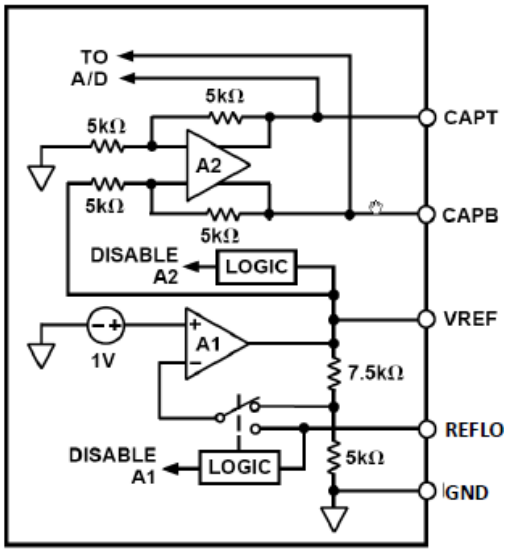


Figure 7-5. Equivalent Reference Circuit

The voltage appearing at the V_{REF} pin as well as the state of the internal reference amplifier, A1, are determined by the voltage appearing at the REFLO pin. The logic circuitry contains two comparators which monitor the voltage at the REFLO pin. The comparator with the lowest set point (approximately 0.3 V) controls the position of the switch within the feedback path of A1. If the REFLO pin is tied to GND, the switch is connected to the internal resistor network thus providing a V_{REF} of 2.5 V. If the REFLO pin is tied to the V_{REF} pin via a short or resistor, the switch is connected to the REFLO pin. A short will provide a V_{REF} of 1.0 V while an external resistor network will provide an alternative V_{REF} between 1.0 V and 2.5 V. The other comparator controls internal circuitry which will disable the reference amplifier if the REFLO pin is tied V_{DDA}. Disabling the reference amplifier allows the V_{REF} pin to be driven by an external voltage reference.

The actual reference voltages used by the internal circuitry of the B9240MGRH appear on the CAPT and CAPB pins. For proper operation when using the internal or an external reference, it is necessary to add a capacitor network to decouple these pins. Figure 7-6 shows the recommended decoupling network. This capacitive network performs the following three functions: (1) along with the reference amplifier, A2, it provides a low source impedance over a large frequency range to drive the A/D

internal circuitry, (2) it provides the necessary compensation for A2, (3) it band limits the noise contribution from the reference. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 15ms and should be evaluated in any power-down mode of operation.

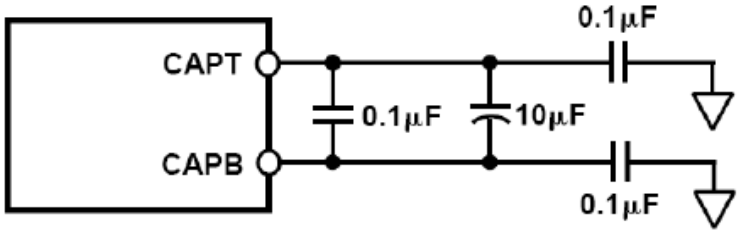


Figure 7-6. Recommended CAPT/CAPB Decoupling Network

The A/D's input span may be varied dynamically by changing the differential reference voltage appearing across CAPT and CAPB symmetrically around 2.5 V (i.e., mid-supply). To change the reference at speeds beyond the capabilities of A2, it will be necessary to drive CAPT and CAPB with two high speed, low noise amplifiers. In this case, both internal amplifiers (i.e., A1 and A2) must be disabled by connecting REFLO to V_{DDA} and V_{REF} to GND and the capacitive decoupling network removed. The external voltages applied to CAPT and CAPB must be 2.5 V + Input Span/4 and 2.5 V – Input Span/4 respectively in which the input span can be varied between 2 V and 5 V. Note that those samples within the pipeline A/D during any reference transition will be corrupted and should be discarded.

7.5 Driving The Analog Inputs Introduction

The B9240MGRH has a highly flexible input structure allowing it to interface with single-ended or differential input interface circuitry. The applications shown in sections "Driving the Analog Inputs" and "Reference Configurations" along with the information presented in "Input and Reference Overview" of this data sheet, give examples of both single-ended and differential operation.

The optimum mode of operation, analog input range, and associated interface circuitry will be determined by the particular applications performance requirements as well as power supply options. For example, a DC coupled single-ended input may be appropriate for many data acquisition and imaging applications. Also, many communication applications which require a DC coupled input for proper demodulation can take advantage of the excellent single-ended distortion performance of the B9240MGRH. The input span should be configured such that the system's performance objectives and the headroom requirements of the driving op amp are simultaneously met.

Alternatively, the differential mode of operation provides the best THD and SFDR performance over a wide frequency range. A transformer coupled differential input should be considered for the most demanding spectral-based applications which allow AC coupling (e.g., Direct IF to Digital Conversion). The DC coupled differential mode of operation also provides an enhancement in distortion and noise performance at higher input spans. Furthermore, it allows the B9240MGRH to be configured for a 5 V span using op amps specified for +5 V or ±5 V operation.

Single-ended operation requires that IN+ be AC or DC coupled to the input signal source while IN- of the B9240MGRH be biased to the appropriate voltage corresponding to a midscale code transition. Note that signal inversion may be easily accomplished by transposing IN+ and IN-.

Differential operation requires that IN+ and IN- be simultaneously driven with two equal signals that are in and out of phase versions of the input signal. Differential operation of the B9240MGRH offers the following benefits: (1) Signal swings are smaller and therefore linearity requirements placed on the input signal source may be easier to achieve, (2) Signal swings are smaller and therefore may allow the use of op amps which may otherwise have been constrained by headroom limitations, (3) Differential operation minimizes even-order harmonic products, and (4) Differential operation offers noise immunity based on the device's common-mode rejection.

As is typical of most CMOS devices, exceeding the supply limits will turn on internal parasitic diodes resulting in transient currents within the device. Figure 7-7 shows a simple means of clamping a DC coupled input with the addition of two series resistors and two diodes. Note that a larger series resistor could be used to limit the fault current through D1 and D2 but should be evaluated since it can cause a degradation in overall performance.

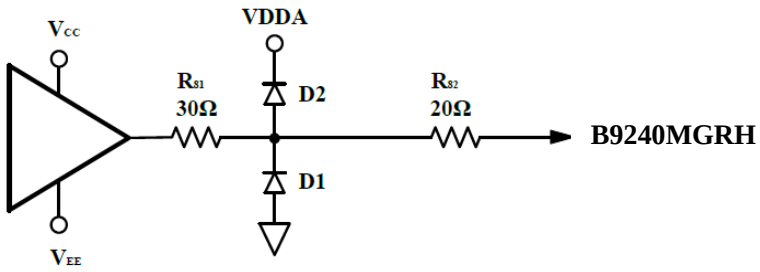


Figure 7-7. Sample Clamping Circuit

7.6 Differential Mode of Operation

Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended to differential conversion. A

single-ended to differential conversion can be realized with an RF transformer or a dual op amp differential driver. The optimum method depends on whether the application requires the input signal to be AC or DC coupled to B9240MGRH.

AC Coupling via an RF Transformer

In applications that do not need to be DC coupled, an RF transformer with a center tap is the best method to generate differential inputs for the B9240MGRH. It provides all the benefits of operating the A/D in the differential mode without contributing additional noise or distortion. An RF transformer has the added benefit of providing electrical isolation between the signal source and the A/D.

Figure 7-8 shows the schematic of the suggested transformer circuit. The circuit uses a Mini-Circuits RF transformer, model #T4-6T, which has an impedance ratio of four (turns ratio of 2). The schematic assumes that the signal source has a 50Ω source impedance. The 1:4 impedance ratio requires the 200Ω secondary termination for optimum power transfer and VSWR. The centertap of the transformer provides a convenient means of level shifting the input signal to a desired common-mode voltage. Optimum performance can be realized when the centertap is tied to CML of the B9240MGRH which is the common mode bias level of the internal SHA.

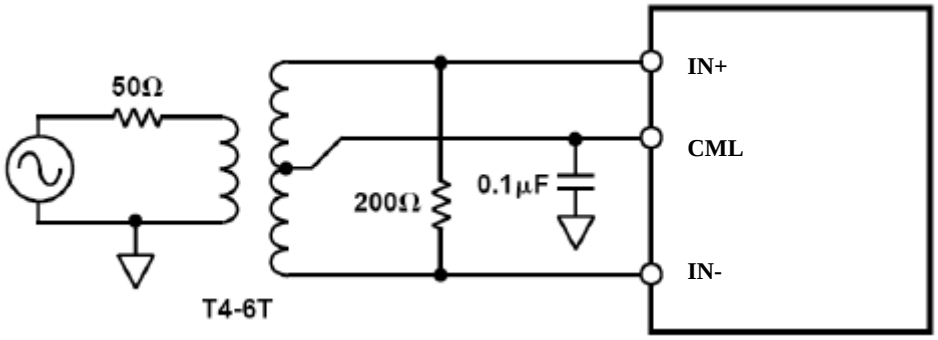


Figure 7-8. Transformer Coupled Input

Transformers with other turns ratios may also be selected to optimize the performance of a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Hence, selecting a transformer with a higher impedance ratio (i.e., Mini-Circuits T16-6T with a 1:16 impedance ratio) effectively "steps up" the signal level, further reducing the driving requirements of the signal source.

DC Coupling with Op Amps

Applications that require DC coupling can also benefit by driving the B9240MGRH differentially. Since the signal swing requirements of each input is

reduced by a factor of two in the differential mode, the B9240MGRH can be configured for a 5 V input span in a +5 V or ± 5 V system. This allows various high performance op amps specified for +5 V and ±5 V operation to be configured in various differential driver topologies. The optimum op amp driver topology depends on whether the common-mode voltage of the single-ended-input signal requires level-shifting.

Figure 7-9 shows a cross-coupled differential driver circuit best suited for systems in which the common-mode signal of the input is already biased to approximately mid-supply (i.e., 2.5 V). The common-mode voltage of the differential output is set by the voltage applied to the "+" input of A2. The closed loop gain of this symmetrical driver can be easily set by R_{IN} and R_F.

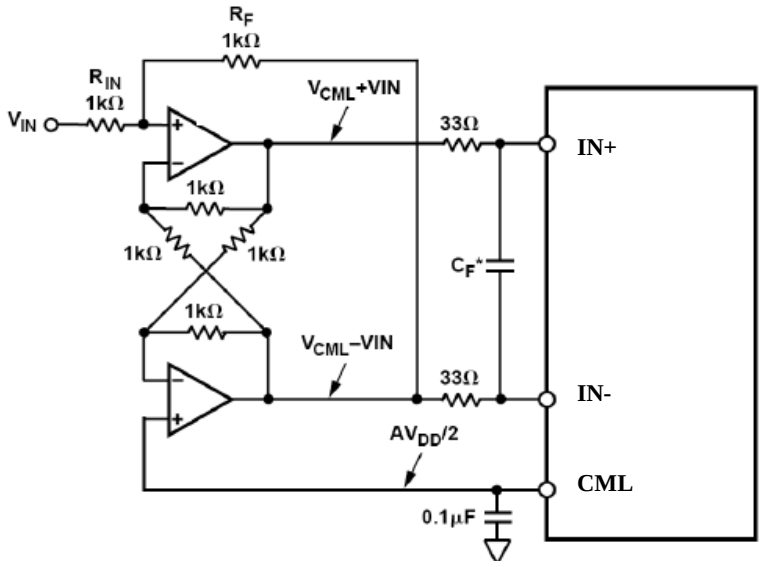


Figure 7-9. Cross-Coupled Differential Driver

The driver circuit shown in Figure 7-10 is best suited for systems in which the bipolar input signal is referenced to GND_A and requires proper level shifting. This driver circuit provides the ability to level-shift the input signal to within the common-mode range of the B9240MGRH. The two op amps are configured as matched difference amplifiers with the input signal applied to opposing inputs to provide the differential output. The common-mode offset voltage is applied to the non-inverting resistor network which provides the proper level shifting. The circuit also employs optional diodes and pull-up resistors which may help improve the op amps' distortion performance by reducing their headroom requirements.

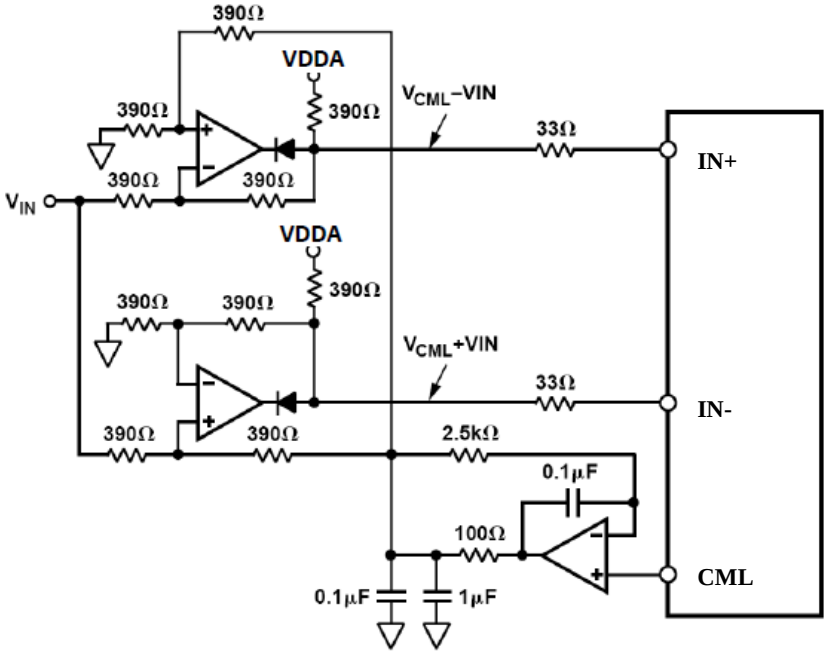


Figure 7-10. Differential Driver with Level-Shifting

7.7 Single-Ended Mode of Operation

The B9240MGRH can be configured for single-ended operation using DC or AC coupling. In either case, the input of the A/D must be driven from an operational amplifier that will not degrade the A/D's performance. Because the A/D operates from a single supply, it will be necessary to level shift ground-based bipolar signals to comply with its input requirements. Both DC and AC coupling provide this necessary function, but each method results in different interface issues which may influence the system design and performance.

DC Coupling and Interface Issues

Many applications require the analog input signal to be DC coupled to the B9240MGRH. An operational amplifier can be configured to rescale and level shift the input signal so that it is compatible with the selected input range of the A/D. The input range to the A/D should be selected on the basis of system performance objectives as well as the analog power supply availability since this will place certain constraints on the op amp selection.

Many of the new high performance op amps are specified for only ±5 V operation and have limited input/output swing capabilities. Hence, the selected input range of the B9240MGRH should be sensitive to the headroom requirements of the particular op amp to prevent clipping of the signal. Also, since the output of a dual supply amplifier can swing below –0.3V, clamping its output should be considered in some applications.

In some applications, it may be advantageous to use an op amp specified for single supply +5 V operation since it will inherently limit its output swing to within the power supply rails.

If the application requires the largest single-ended input range (i.e., 0 V to 5 V) of the B9240MGRH, the op amp will require larger supplies to drive it. Various high speed amplifiers in the "Op Amp Selection Guide" of this data sheet can be selected to accommodate a wide range of supply options. Once again, clamping the output of the amplifier should be considered for these applications.

Two DC coupled op amp circuits using a non-inverting and inverting topology are discussed below. Although not shown, the non-inverting and inverting topologies can be easily configured as part of an anti-alias filter by using a Sallen-Key or Multiple-Feedback topology, respectively. An additional R-C network can be inserted between the op amp's output and the B9240MGRH input to provide a real pole.

Simple Op Amp Buffer

In the simplest case, the input signal to the B9240MGRH will already be biased at levels in accordance with the selected input range. It is simply necessary to provide an adequately low source impedance for the IN+ and IN- analog input pins of the A/D. Figure 7-11 shows the recommended configuration for a single-ended drive using an op amp. In this case, the op amp is shown in a non-inverting unity gain configuration driving the IN+ pin. The internal reference drives the IN- pin. Note that the addition of a small series resistor of 30Ω to 50Ω connected to IN+ and IN- will be beneficial in nearly all cases. Figure 7-11 shows the proper connection for a 0V to 5 V input range. Alternative single ended input ranges of 0 V to 2 × V_{REF} can also be realized with the proper configuration of V_{REF}.

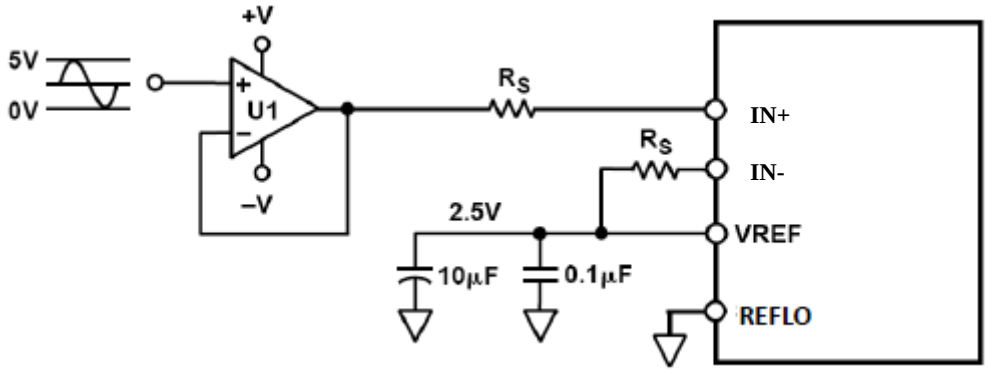


Figure 7-11. Single-Ended B9240MGRH Op Amp Drive Circuit

Op Amp with DC Level Shifting

Figure 7-12 shows a DC-coupled level shifting circuit employing an op amp, A1,

to sum the input signal with the desired DC offset. Configuring the op amp in the inverting mode with the given resistor values results in an AC signal gain of –1. If the signal inversion is undesirable, interchange the IN+ and IN- connections to reestablish the original signal polarity. The DC voltage at V_{REF} sets the common-mode voltage of the B9240MGRH. For example, when V_{REF} = 2.5 V, the output level from the op amp will also be centered around 2.5 V. The use of ratio matched, thin-film resistor networks will minimize gain and offset errors. Also, an optional pull-up resistor, RP, may be used to reduce the output load on V_{REF} to ±1 mA.

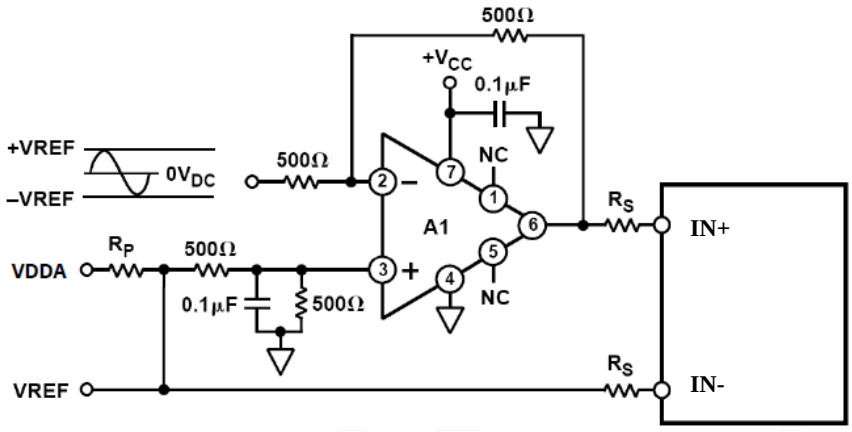


Figure 7-12. Single-Ended Input with DC-Coupled Level Shift

7.8 AC Coupling and Interface Issues

For applications where AC coupling is appropriate, the op amp's output can be easily level shifted to the common-mode voltage, V_{CM}, of the B9240MGRH via a coupling capacitor. This has the advantage of allowing the op amps common-mode level to be symmetrically biased to its mid-supply level (i.e., (VCC + VEE)/2). Op amps which operate symmetrically with respect to their power supplies typically provide the best AC performance as well as greatest input/output span. Hence, various high speed/performance amplifiers which are restricted to +5 V/–5 V operation and/or specified for +5 V single-supply operation can be easily configured for the 5 V or 2 V input span of the B9240MGRH, respectively. The best AC distortion performance is achieved when the A/D is configured for a 2V input span and common-mode voltage of 2.5V. Note that differential transformer coupling, which is another form of AC coupling, should be considered for optimum AC performance.

Simple AC Interface

Figure 7-13 shows a typical example of an AC-coupled, single-ended configuration. The bias voltage shifts the bipolar, ground-referenced input signal to approximately V_{REF}. The value for C1 and C2 will depend on the size of the resistor,

R. The capacitors, C1 and C2, are typically a 0.1 µF ceramic and 10 µF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. The combination of the capacitor and the resistor form a high-pass filter with a high-pass –3 dB frequency determined by the equation,

$$f_{-3\,dB} = 1/(2 \times \pi \times R \times (C1 + C2))$$

The low impedance V_{REF} voltage source biases both the IN- input and provides the bias voltage for the IN+ input. Figure 7-13 shows the V_{REF} configured for 2.5 V. Thus the input range of the A/D is 0 V to 5 V. Other input ranges could be selected by changing V_{REF} but the A/D's distortion performance will degrade slightly as the input common-mode voltage deviates from its optimum level of 2.5 V.

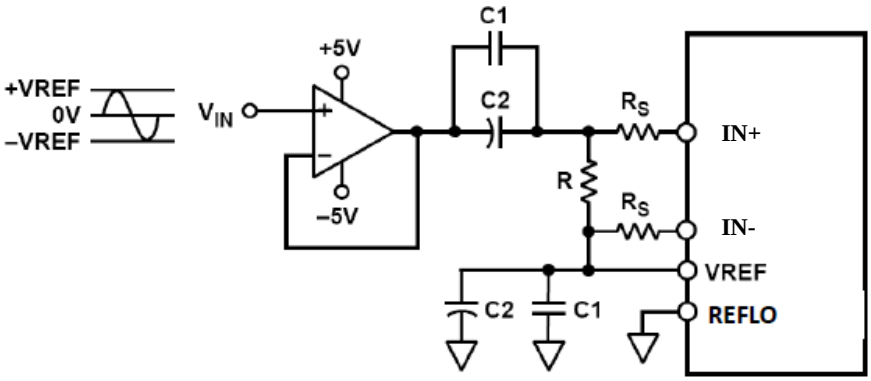


Figure 7-13. AC-Coupled Input

Alternative AC Interface

Figure 7-14 shows a flexible AC coupled circuit which can be configured for different input spans. Since the common-mode voltage of IN+ and IN- are biased to midsupply independent of V_{REF}, V_{REF} can be pin-strapped or reconfigured to achieve input spans between 2V and 5V p-p. The B9240MGRH's CMRR along with the symmetrical coupling R-C networks will reject both power supply variations and noise. The resistors, R, establish the common-mode voltage. They may have a high value (e.g., 5kΩ) to minimize power consumption and establish a low cutoff frequency. The capacitors, C1 and C2, are typically a 0.1 µF ceramic and 10 µF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. RS isolates the buffer amplifier from the A/D input. The optimum performance is achieved when IN+ and IN- are driven via symmetrical networks. The high pass f_{-3dB} point can be approximated by the equation,

$$f_{-3\,dB} = 1/(2 \times \pi \times R/2 \times (C1 + C2))$$

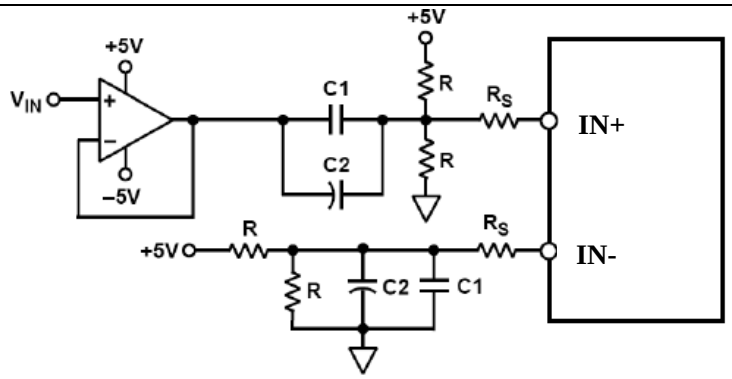


Figure 7-14. AC-Coupled Input-Flexible Input Span, V_{CM} = 2.5 V

7.9 Using the Internal Reference

Single-Ended Input with 0 to 2 × V_{REF} Range

Figure 7-15 shows how to connect the B9240MGRH for a 0V to 2V or 0V to 5V input range via pin strapping the REFLO pin. An intermediate input range of 0 to 2 × V_{REF} can be established using the resistor programmable configuration in Figure 7-17 and connecting V_{REF} to IN-.

In either case, both the common-mode voltage and input span are directly dependent on the value of V_{REF}. More specifically, the common-mode voltage is equal to V_{REF} while the input span is equal to 2 × V_{REF}. Thus, the valid input range extends from 0 to 2 × V_{REF}. When IN+ is ≤ 0 V, the digital output will be 0000 Hex; when IN+ is ≥ 2 × V_{REF}, the digital output will be 3FFF Hex.

Shorting the V_{REF} pin directly to the REFLO pin places the internal reference amplifier in unity-gain mode and the resultant VREF output is 1 V. Therefore, the valid input range is 0 V to2 V. However, shorting the REFLO pin directly to the GND pin configures the internal reference amplifier for a gain of 2.5 and the resultant V_{REF} output is 2.5 V. Thus, the valid input range becomes 0 V to 5 V. The V_{REF} pin should be bypassed to the GND pin with a 10 µF tantalum capacitor in parallel with a low-inductance 0.1 µF ceramic capacitor.

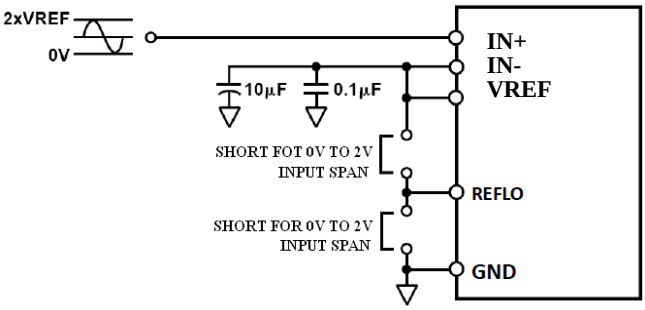


Figure 7-15. Internal Reference (2V p-p Input Span, V_{CM} = 1 V, or 5V p-p Input Span, V_{CM} = 2.5V)

Single-Ended or Differential Input, V_{CM} = 2.5 V

Figure 7-16 shows the single-ended configuration that gives the best SINAD performance. To optimize dynamic specifications, center the common-mode voltage of the analog input at approximately by 2.5 V by connecting IN- to V_{REF}, a low-impedance 2.5 V source. As described above, shorting the REFLO pin directly to the GND pin results in a 2.5V reference voltage and a 5V p-p input span. The valid range for input signals is 0V to 5V. The V_{REF} pin should be bypassed to the GND pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

This reference configuration could also be used for a differential input in which IN+ and IN- are driven via a transformer as shown in Figure 7-8. In this case, the common-mode voltage, V_{CM}, is set at midsupply by connecting the transformers center tap to CML of the B9240MGRH. V_{REF} can be configured for 1V or 2.5V by connecting REFLO to either V_{REF} or GND respectively. Note that the valid input range for each of the differential inputs is one half of the single-ended input and thus becomes VCM – V_{REF}/2 to VCM + V_{REF}/2.

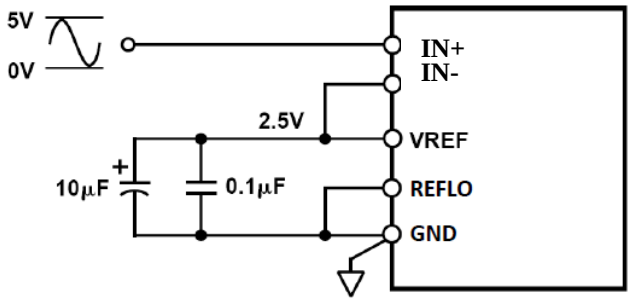


Figure 7-16. Internal Reference—5 V p-p Input Span, V_{CM} = 2.5 V

Resistor Programmable Reference

Figure 7-17 shows an example of how to generate a reference voltage other than 1 V or 2.5 V with the addition of two external resistors and a bypass capacitor. Use the equation,

$$V_{REF} = 1\ V \times (1 + R1/R2),$$

to determine appropriate values for R1 and R2. These resistors should be in the 2 kΩ to 100 kΩ range. For the example shown, R1 equals 2.5 kΩ and R2 equals 5 kΩ. From the equation above, the resultant reference voltage on the VREF pin is 1.5 V. This sets the input span to be 3 V p-p. To assure stability, place a 0.1 µF ceramic capacitor in parallel with R1.

The common-mode voltage can be set to V_{REF} by connecting IN- to V_{REF} to provide an input span of 0 to 2 × V_{REF}. Alternatively, the common-mode voltage can

be set to 2.5 V by connecting IN- to a low impedance 2.5 V source. For the example shown, the valid input single range for IN+ is 1 V to 4 V since IN- is set to an external, low impedance 2.5 V source. The V_{REF} pin should be bypassed to the GND pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

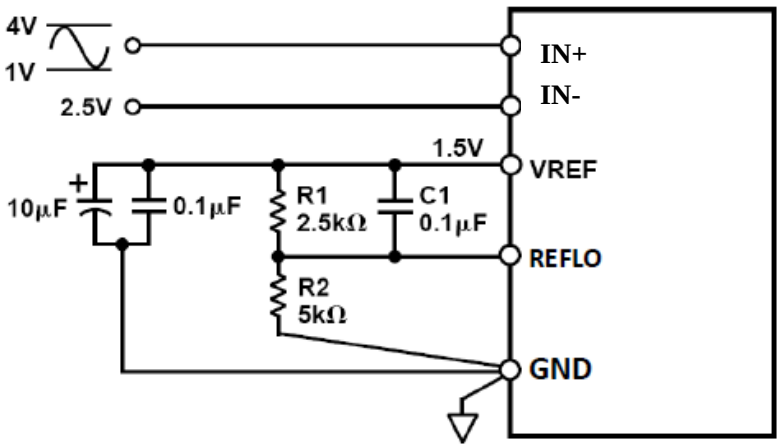


Figure 7-17. Resistor Programmable Reference (3V p-p Input Span, V_{CM} = 2.5V)

7.10 Using an External Reference

Using an external reference may enhance the DC performance of the B9240MGRH by improving drift and accuracy. To use an external reference, the user must disable the internal reference amplifier and drive the V_{REF} pin. Connecting the REFLO pin to V_{DDA} disables the internal reference amplifier.

The B9240MGRH contains an internal reference buffer, A2, that simplifies the drive requirements of an external reference. The external reference must be able to drive a ≈5kΩ (± 20%) load. Note that the bandwidth of the reference buffer is deliberately left small to minimize the reference noise contribution. As a result, it is not possible to change the reference voltage rapidly in this mode without the removal of the CAPT/ CAPB Decoupling Network, and driving these pins directly.

Variable Input Span with V_{CM} = 2.5 V

Figure 7-18 shows an example of the B9240MGRH configured for an input span of 2 × V_{REF} centered at 2.5V. An external 2.5V reference drives the IN- pin thus setting the common-mode voltage at 2.5V. The input span can be independently set by a voltage divider consisting of R1 and R2 which generates the V_{REF} signal. A1 buffers this resistor network and drives V_{REF}. Choose this op amp based on accuracy requirements. It is essential that a minimum of a 10 µF capacitor in parallel with a 0.1 µF low inductance ceramic capacitor decouple the reference output to ground.

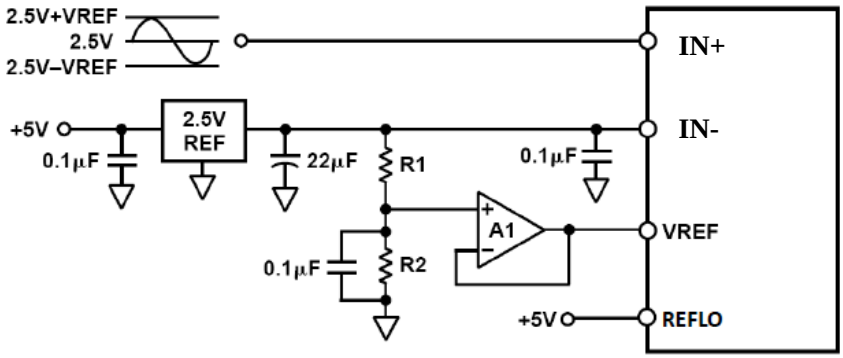


Figure 7-18. External Reference, V_{CM} = 2.5 V (2.5 V on IN-, Resistor Divider to Make V_{REF})

Single-Ended Input with 0 to 2 × V_{REF} Range

Figure 7-19 shows an example of an external reference driving both IN- and V_{REF}. In this case, both the common mode voltage and input span are directly dependent on the value of V_{REF}. More specifically, the common-mode voltage is equal to V_{REF} while the input span is equal to 2 × V_{REF}. Thus, the valid input range extends from 0 to 2 × V_{REF}. For example, a 2.048 external reference was selected, the valid input range extends from 0 V to 4.096V. In this case, 1 LSB of the B9240MGRH corresponds to 0.250 mV. It is essential that a minimum of a 10 µF capacitor in parallel with a 0.1 µF low inductance ceramic capacitor decouple the reference output to ground.

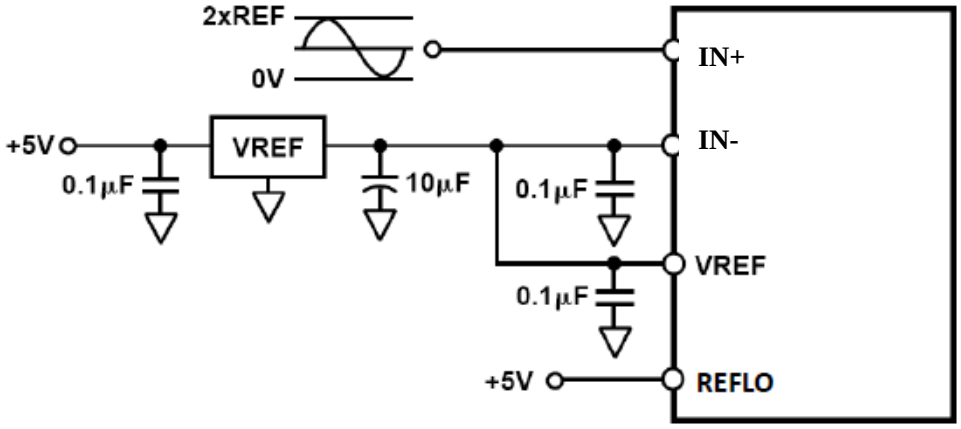


Figure 7-19. Input Range = 0V to 2 × V_{REF}

Low Cost/Power Reference

The external reference circuit shown in Figure 7-20 uses a low cost 1.225 V external reference along with an op amp and transistor. The transistor acts in conjunction with 1/2 of an OP282 to provide a very low impedance drive for IN-. The selected op amp need not be a high speed op amp and may be selected based on cost, power, and accuracy.

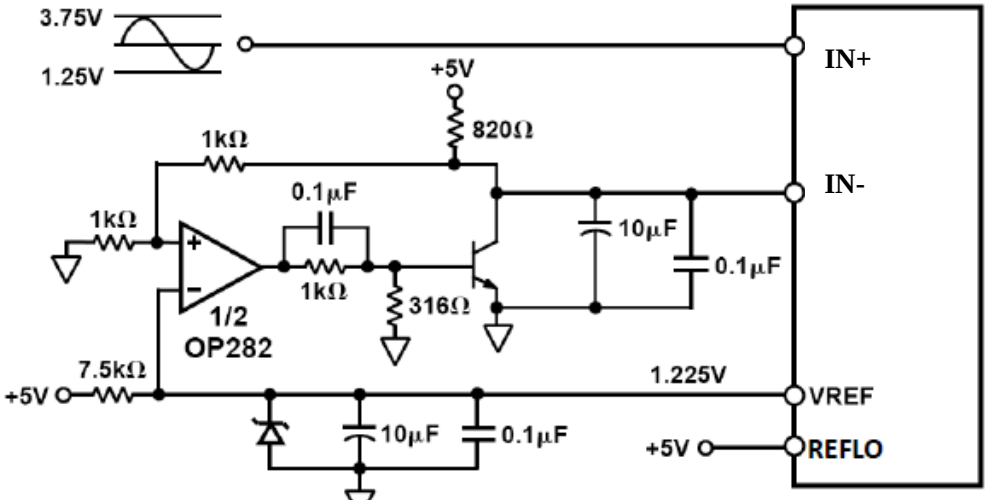


Figure 7-20. External Reference and Low Impedance Buffer

7.11 Digital Inputs and Outputs

Digital Outputs

The B9240MGRH output data is presented in positive true straight binary for all input ranges. Next table indicates the output data formats for various input ranges regardless of the selected input range. A twos complement output data format can be created by inverting the MSB.

Output Data Format

Input(V)	Condition(V)	Digital Output	OTR
IN+-IN-	$<-V_{REF}$	00 0000 0000 0000	1
IN+-IN-	$=-V_{REF}$	00 0000 0000 0000	0
IN+-IN-	=0	10 0000 0000 0000	0
IN+-IN-	$=+V_{REF}$-1LSB	11 1111 1111 1111	0
IN+-IN-	$\geq+V_{REF}$	11 1111 1111 1111	1

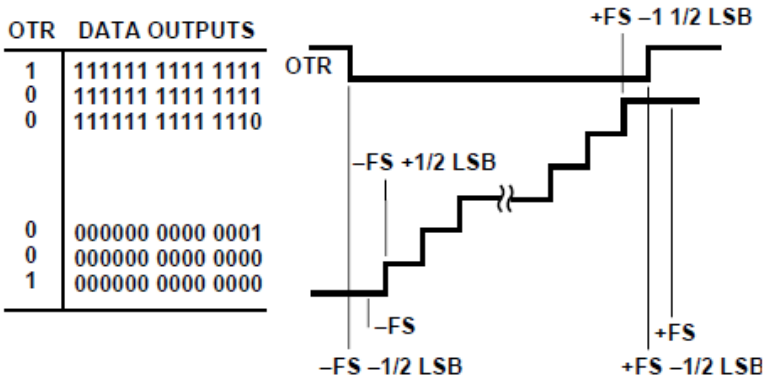


Figure 7-21. Output Data Format

Out Of Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the converter. OTR is a digital output that is updated along with the data output corresponding to the particular sampled analog input voltage. Hence, OTR has the same pipeline delay (latency) as the digital data. It is LOW when the analog input voltage is within the analog input range. It is HIGH when the analog input voltage exceeds the input range as shown in Figure 7-21. OTR will remain HIGH until the analog input returns within the input range and another conversion is completed. By logical operating OTR with the MSB and its complement, over-range high or under-range low conditions can be detected. Next table is a truth table for the over/under-range circuit in Figure 7-22 which uses NAND gates. Systems requiring programmable gain conditioning of the B9240MGRH input signal can immediately detect an out-of-range condition, thus eliminating gain selection iterations. Also, OTR can be used for digital offset and gain calibration.

Out-of Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Under-range
1	1	Over-range

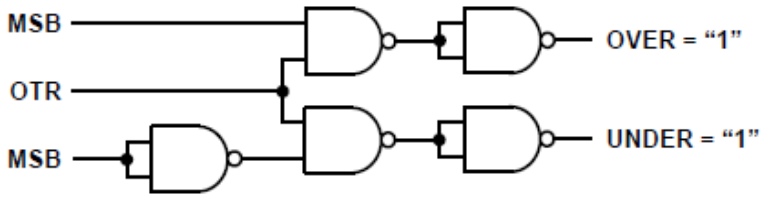


Figure 7-22. Over-range or Under-range Logic

Digital Output Driver Considerations (V_{DDDR})

The B9240MGRH output drivers can be configured to interface with +5 V or 3.3 V logic families by setting V_{DDDR} to +5 V or 3.3 V respectively. The B9240MGRH output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect SINAD performance. Applications requiring the B9240MGRH to drive large capacitive loads or large fan out may require additional decoupling capacitors on V_{DDDR}. In extreme cases, external buffers or latches may be required.

Clock Input and Considerations

The B9240MGRH internal timing uses the two edges of the clock input to generate a variety of internal timing signals. The clock input must meet or exceed the minimum specified pulse width high and low (t_{CH} and t_{CL}) specifications for the given A/D as defined in the Switching Specifications at the beginning of the data sheet to meet the rated performance specifications. For example, the clock input to the B9240MGRH operating at 3 MSPS may have a duty cycle between 45% to 55% to meet this timing requirement since the minimum specified t_{CH} and t_{CL} is 150 ns.

For clock rates below 3 MSPS, the duty cycle may deviate from this range to the extent that both t_{CH} and t_{CL} are satisfied.

All high speed high resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due to only aperture jitter (t_A) can be calculated with the following equation:

$$SNR = 20 \log10 [1/(2 \times \pi \times f_{IN} \times t_A)]$$

In the equation, the rms aperture jitter, t_A, represents the rootsum square of all the jitter sources which include the clock input, analog input signal, and A/D aperture jitter specification. For example, if a 1.5 MHz full-scale sine wave is sampled by an A/D with a total rms jitter of 15 ps, the SNR performance of the A/D will be limited to 77 dB. Under-sampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the B9240MGRH. As such, supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other method), it should be retimed by the original clock at the last step.

7.12 Grounding and Decoupling

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the B9240MGRH features separate analog and digital ground pins, it should be treated as an analog component. The GND_A, GND_D and GND_{DR} pins must be joined together directly under the B9240MGRH. A solid ground plane under the A/D is acceptable if the power and ground return currents are managed carefully. Alternatively, the ground plane under the A/D may contain serrations to steer currents in predictable directions where cross-coupling between analog and digital would otherwise be unavoidable. The analog and digital grounds are connected by a jumper below the A/D.

Analog and Digital Supply Decoupling

The B9240MGRH features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals.

In general, V_{DDA}, the analog supply, should be decoupled to GND_A, the analog common, as close to the chip as physically possible. Figure 7-23 shows the recommended decoupling for the analog supplies; 0.1 µF ceramic chip capacitors should provide adequately low impedance over a wide frequency range. Note that the V_{DDA} and GND_A pins are co-located on the B9240MGRH to simplify the layout of the decoupling capacitors and provide the shortest possible PCB trace lengths.

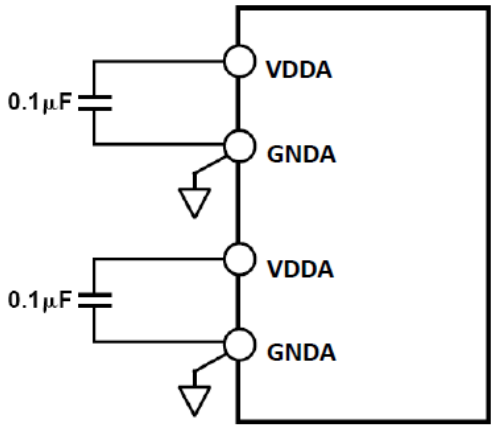


Figure 7-23. Analog Supply Decoupling

The CML is an internal analog bias point used internally by the B9240MGRH. This pin must be decoupled with at least a 0.1 µF capacitor as shown in Figure 7-24. The DC level of CML is approximately $V_{DDA}/2$. This voltage should be buffered if it

is to be used for any external biasing.

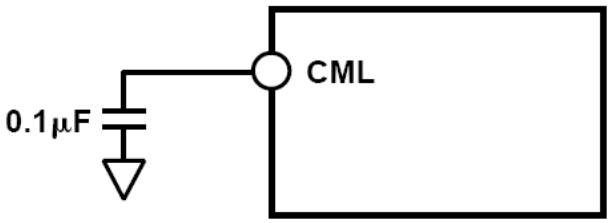


Figure 7-24. CML Decoupling

The digital activity on the B9240MGRH chip falls into two general categories: correction logic, and output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits: large capacitive loads are to be avoided. Note that the internal correction logic of the B9240MGRH is referenced V_{DDD} while the output drivers are referenced to V_{DDDR}.

The decoupling shown in Figure 7-25, a 0.1 μF ceramic chip capacitor, is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionally, and/or using external buffers/ latches.

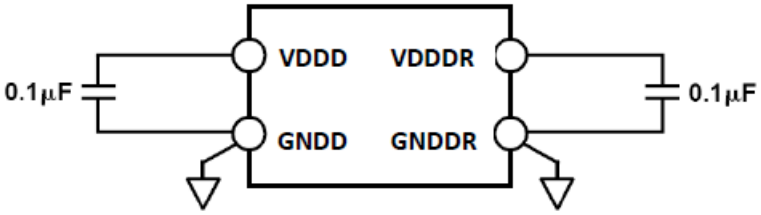


Figure 7-25. Digital Supply Decoupling

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the PCB to reduce low-frequency ripple to negligible levels.

8. Specifications

8.1 Storage Condition

The warehouse environment of B9240MGRH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

8.2 Absolute Maximum Ratings

1)Power Voltage（V_{DD}）…… -0.3V～6.5V

2)Digital Input Voltage（V_{ID}）…… -0.3V～V_{DDD}+0.3V

3) Digital Output Voltage（V_{OD}）…… -0.3V～V_{DDD}+0.3V

4)Analog Input&Output Voltage （V_{IA}、V_{OA}）…… -0.3V～V_{DDA}+0.3V

5)Reference Voltage（V_{REF}）…… -0.3V～V_{DDA}+0.3V

6) Storage Temperature (T_{STG})：…… -65℃~+ 150℃

7) Thermal Resistance（$R_{th\ (jc)}$） …… 8℃/W

8) Lead Temperature(10 sec)（T_h） …… 260℃（10s）

9) Junction Temperature（T_J） …… 150℃

8.3 Recommended Operating conditions

1) Power Voltage（V_{DD}）…… 5V

2) Temperature（T_A）…… -55℃～125℃

8.4 Radiation hardened performance

a) Total Ionizing Dose ≥ 100 Krad(Si)

b) SEL threshold ≥ 75 MeV cm^2/mg

8.5 Electrical Characteristic

Electrical Characteristic Table

Parameter	**Symbol**	***Conditions*** ***(Unless otherwise specified*** V_{DDD} = V_{DDA} = V_{DDDR}5V, GND = GND_A = GND_D = GND_{DR} = 0V, R_{BIAS} = 2KΩ, -55℃ ≤ T_A ≤ 125℃)	**Value**			**Units**
			Min	**Type**	**Max**	
Resolution	*RES*			14		bits
Integral Nonlinearity (INL)	E_L		-3.5	±1.5	+3.5	LSB

Parameter	Symbol	Conditions (Unless otherwise specified V_{DDD} = V_{DDA} = V_{DDDR}5V, GND = GND_A = GND_D = GND_{DR} = 0V, R_{BIAS} = 2KΩ, -55℃ ≤ T_A ≤ 125℃)	Value			Units
			Min	Type	Max	
Differential Nonlinearity (DNL)	E_{DL}		-1.5	±0.8	+1.5	LSB
Zero Error	E_O	(T_A=25℃)	—	0.01	0.4	%FS
Gain Error	E_G	(T_A=25℃)	—	0.2	1.5	%FS
Clock input capacitance	$C_{IN,CL}$	V_{DDA}=V_{DDD}=V_{DDDR}=0V	—	—	8	pF
Logic output capacitance	$C_{OUT,CL}$	V_{DDA}=V_{DDD}=V_{DDDR}=0V	—	—	8	pF
Reference input resistance	$R_{REF,in}$	V_{DDA}=V_{DDD}=V_{DDDR}=0V	—	—	20	kΩ
Analog input capacitance	C_{IN}	V_{DDA}=V_{DDD}=V_{DDDR}=0V	—	—	10	pF
Output Voltage Reference	V_{REF}	2.5V mode	2.465	2.5	2.535	V
Reference load regulation	V_{LR}	Load = 1mA	-5	0.36	5	mV
Power supply Restrain	*PSR*	±5% power change	—	0.02	0.1	%FS
High Level Input Voltage	V_{IH}		3.5	—	—	V
Low Level Input Voltage	V_{IL}		—	—	1.0	V
High Level Output Voltage	V_{OH}	V_{DDDR} =5V，I_{OH} =0.5mA	2.4	4.9	—	V
		V_{DDDR} =5V，I_{OH} =0.05mA	4.5	4.99	—	
		V_{DDDR} =3V，I_{OH} =0.05mA	2.4	2.99	—	
High Level Output Voltage	V_{OL}	V_{DDDR} =5V，I_{OL} =1.6mA	—	0.25	0.4	V
		V_{DDDR} =5V，I_{OL} =0.05mA	—	0.01	0.1	
		V_{DDDR} =3V，I_{OL} =0.05mA	—	0.09	0.7	
High Level Input Current	I_{IH}	V_{IN}= V_{DDD}	—	0.01	1	μA
Low Level Input Current	I_{IL}	V_{IN}=0V	—	0.01	1	μA
Digital Supply Current	I_{DDD}		—	11.4	20	mA
Analog supply Current	I_{DDA}		—	50	60	mA
Output driver current	I_{DDDR}	No load	—	2.6	10	mA
Power consumption	P_W		—	320	450	mW
Zero Error by Temperature	α_{EO}		—	—	0.02	%FS/℃
Gain Error by Temperature	α_{EG}		—	—	0.1	%FS/℃
Clock input capacitance	C_{IN}，C_L	V_{DDA}=V_{DDD}=V_{DDDR}=0V	—	—	8	pF

Parameter	Symbol	*Conditions* (*Unless otherwise specified* V_{DDD} = V_{DDA} = V_{DDDR}5V, GND = GND_A = GND_D = GND_{DR} = 0V, R_{BIAS} = 2KΩ, -55℃ ≤ T_A ≤ 125℃)	Value			Units
			Min	Type	Max	
Logic output capactiance	C_{OUT}, C_L	V_{DDA}=V_{DDD}=V_{DDDR}=0V	—	—	8	pF
Signal-to-noise and distortion ratio	*SINAD*	f_{IN}=500kHz, Diff. input, A_{IN} = -0.5dBFS, f_{SAMPLE} = 10 MSPS	67	73.4	—	dB
Effective number of bits	*ENOB*	f_{IN}=500kHz, Diff. input, A_{IN} = -0.5dBFS, f_{SAMPLE} = 10 MSPS	10.8	11.9	—	Bits
Signal-to-noise ratio	*SNR*	f_{IN}=500kHz, Diff. input, A_{IN} = -0.5dBFS, f_{SAMPLE} = 10 MSPS	68	75.5	—	dB
Spurious free dynamic range	*SFDR*	f_{IN}=500kHz, Diff. input, A_{IN} = -0.5dBFS, f_{SAMPLE} = 10 MSPS	71.0	—	—	dB
Total harmonic distortion	*THD*	f_{IN}=500kHz, Diff. input, A_{IN} = -0.5dBFS, f_{SAMPLE} = 10 MSPS	—	-75	-70	dB
Max work frequence	f_{max}		10	—	—	MHz
Output delay	T_{OD}		8	15	24	ns

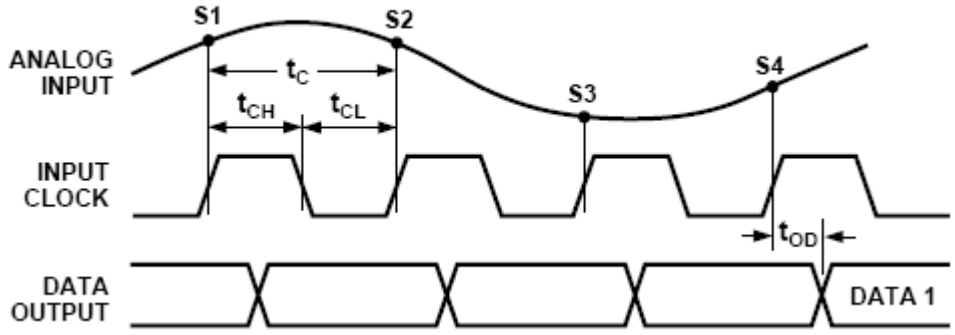


Figure 8-1. Timing Diagram

9. Outline Dimensions

The B9240MGRH is packaged in CPGA40 package, as is shown in figure 9-1:

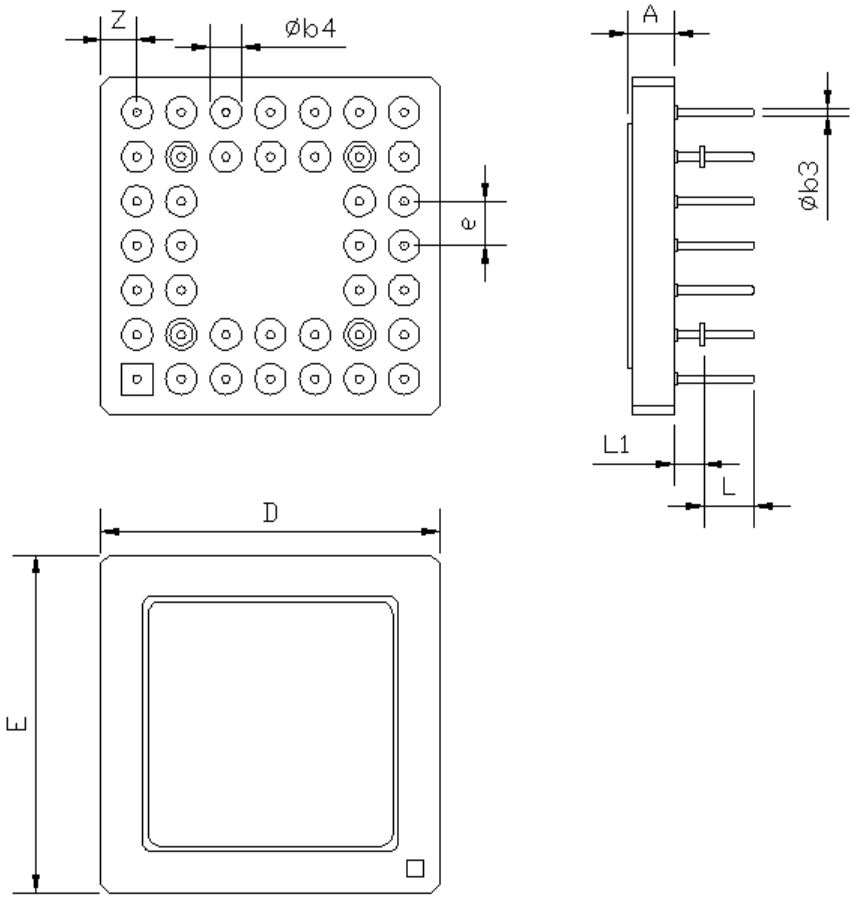


Figure 9-1. Outline dimensions

Symbol	Value（Unit:mm）		
	Min.	Typ.	Max.
D	19.10	——	19.50
E	19.10	——	19.50
Z	——	——	2.54
A	1.78	——	3.68
e	——	2.54	——
L1	1.50	——	1.90
L	2.54	——	5.08
Φb3	0.41	——	0.51
Φb4	1.50	——	2.00

Appendix 1 Pin Definition

NO.	Pin No.	Symbol	Attribute	Description	NO.	Pin No.	Symbol	Attribute	Description
1	A4	CML	O	Common mode	21	G4	D7	O	Digital output
2	B3	NC	—	No connect	22	F5	D6	O	Digital output
3	A3	IN+	I	Analog input（+）	23	G5	D5	O	Digital output
4	A2	IN-	I	Analog input（-）	24	G6	D4	O	Digital output
5	B2	NC	—	No connect	25	F6	D3	O	Digital output
6	A1	NC	—	No connect	26	G7	NC	O	No connect
7	B1	GND_D	GND	Digital ground	27	F7	D2	O	Digital output
8	C2	GND_A	GND	Analog ground	28	E6	D1	O	Digital
9	C1	V_{DDD}	VDD	+5V digital supply	29	E7	OTR	O	Out of range
10	D2	V_{DDA}	VDD	+5V analog supply	30	D6	V_{DDA}	VDD	+5V analog
11	D1	GND_{DR}	GND	Digital output driver ground	31	D7	GND_A	GND	Analog ground
12	E2	V_{DDDR}	VDD	Digital output driver supply	32	C6	REFLO	I	Reference select
13	E1	CLK	I	Clock input pin	33	C7	V_{REF}	I/O	Reference input/output
14	F1	D14	O	Digital output(LSB)	34	B7	GND	GND	Reference common ground
15	F2	D13	O	Digital output	35	B6	NC	—	No connect
16	G1	D12	O	Digital output	36	A7	BIAS	I	Power/Speed programming
17	G2	D11	O	Digital output	37	A6	CAPB	O	Noise reduction
18	F3	D10	O	Digital output	38	B5	NC	—	No connect
19	G3	D9	O	Digital output	39	A5	CAPT	O	Noise reduction
20	F4	D8	O	Digital output	40	B4	NC	—	No connect

Appendix 2 Typical Applications

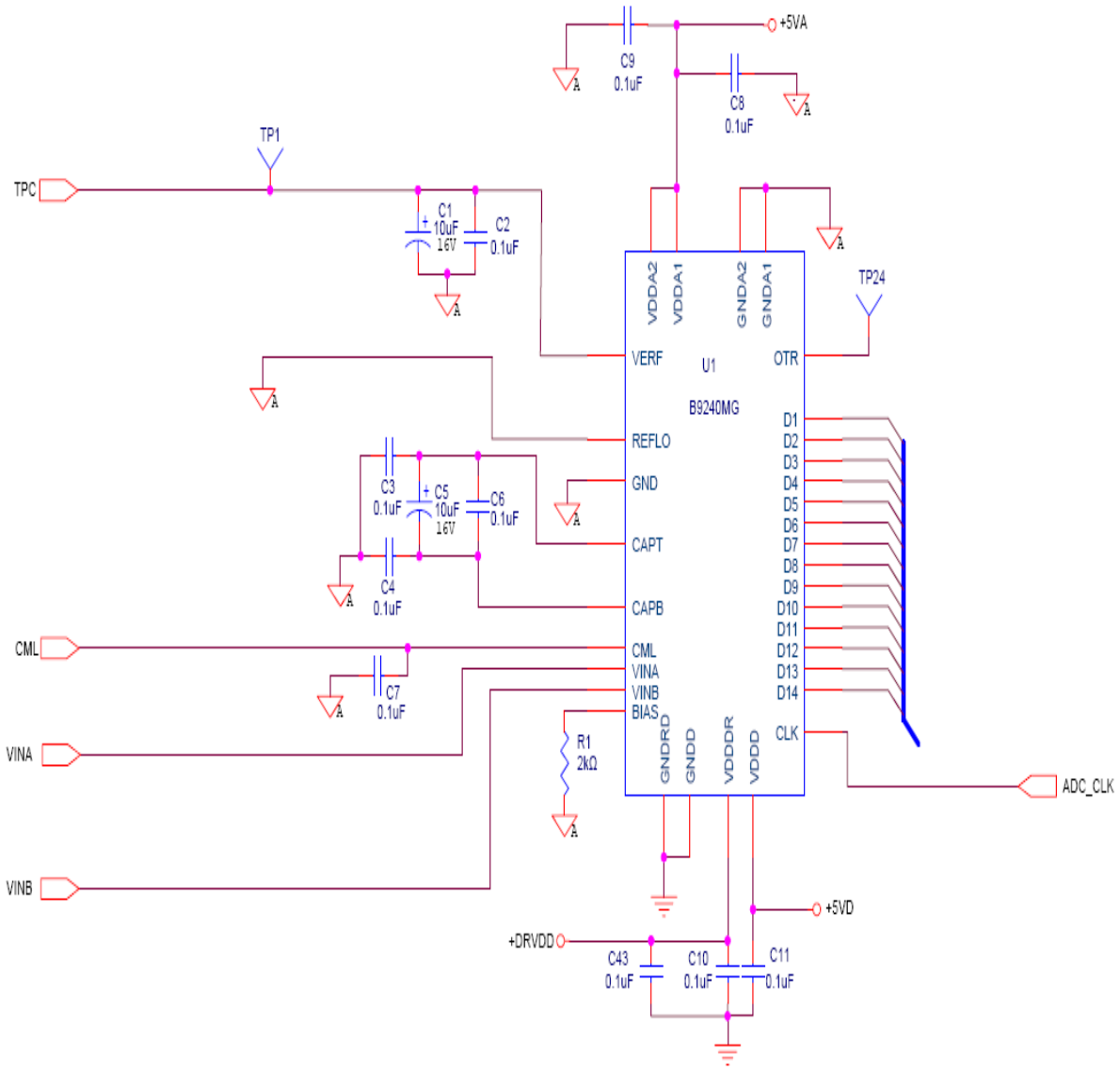
DIRECT IF DOWN CONVERSION USING THE B9240MGRH

The B9240MGRH's performance in the differential mode of operation extends well beyond its baseband region and into several Nyquist zone regions. Hence, the B9240MGRH may be well suited as a mix down converter in both narrow and wideband applications. Various IF frequencies exist over the frequency range in which the B9240MGRH maintains excellent dynamic performance (e.g., refer to Figure 5 and 6). The IF signal will be aliased to the ADC's baseband region due to the sampling process in a similar manner that a mixer will down convert an IF signal. For signals in various Nyquist zones, the following equation may be used to determine the final frequency after aliasing.

$$f_{1NYQUIST} = f_{SIGNAL}$$
$$f_{2NYQUIST} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{3NYQUIST} = abs(f_{SAMPLE} - f_{SIGNAL})$$
$$f_{4NYQUIST} = 2 \times f_{SAMPLE} - f_{SIGNAL}$$
$$f_{5NYQUIST} = abs(2 \times f_{SAMPLE} - f_{SIGNAL})$$

There are several potential benefits in using the ADC to alias (i.e., mix) down a narrowband or wideband IF signal. First and foremost is the elimination of a complete mixer stage with its associated amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction, and detection.

One common example is the digitization of a 10.7 MHz IF using a low jitter 2.5 MHz sample clock. Using the equation above for the fifth Nyquist zone, the resultant frequency after sampling is700 kHz.



App 2-1. B9240MGRH typical application

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