

Ver 1.2

Radiation-Hardened SRAM

Datasheet

Part Number: B7156ARH



中国航天

北京微电子技术研究所

Beijing Microelectronics Technology Institute



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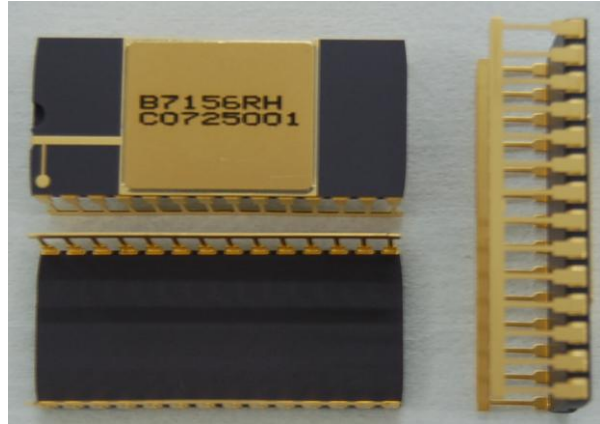


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1. Features

- ✧ 40ns maximum address access time
- ✧ Asynchronous operation for compatibility with industry standard 32K x 8 SRAM
- ✧ CMOS compatible inputs/outputs
- ✧ Three-state bidirectional data bus
- ✧ Low operating and standby current
- ✧ Radiation-hardened design
 - total-dose : 300krads
 - SEL Immune ≥ 80 Mev-cm²/mg
 - SEU LET_{TH} ≥ 32 Mev-cm²/mg
- ✧ Package : DIP28
- ✧ 5-volt operation



2. General Description

The B7156RH SRAM is a high performance, asynchronous, 32K x 8 random access memory conforming to industry-standard fit, form, and function. The B7156RH SRAM features fully static operation requiring no external clocks or timing strobes. Implemented using an standard commercial CMOS process and a device enable/disable function the B7156RH is a high performance, powersaving SRAM. The combination of fast access time and low power consumption make B7156RH ideal for high-speed systems.

3. Block Diagram

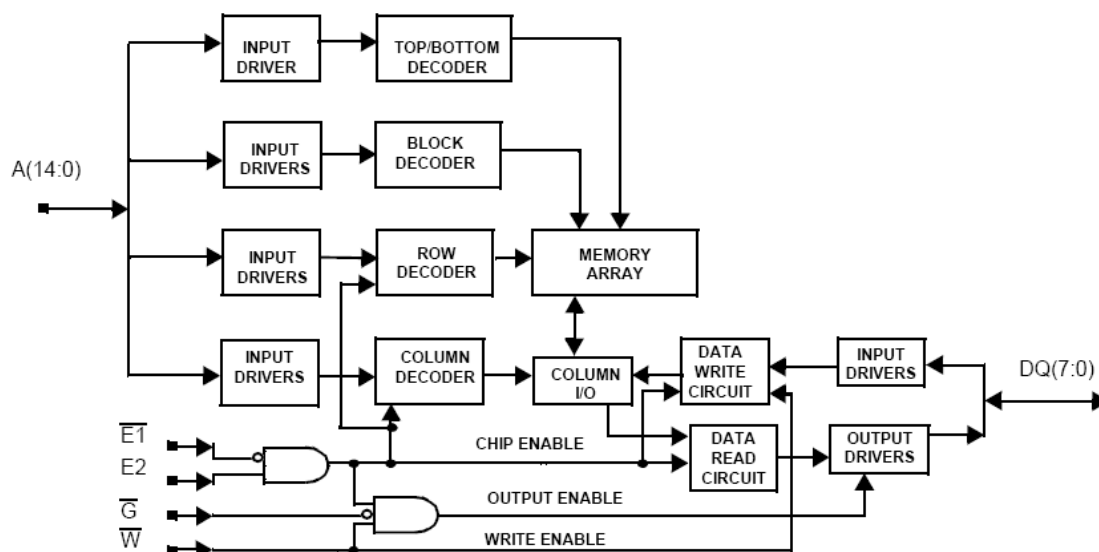


Figure 1. B7156ARH Block Diagram

4. Pin Description

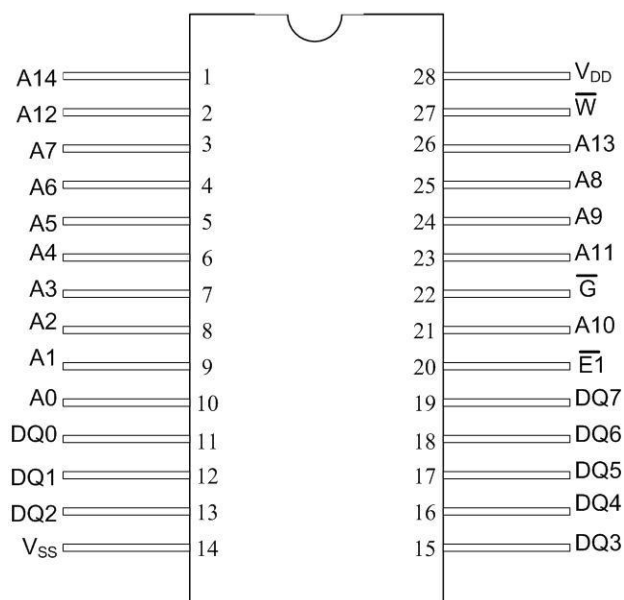


Figure 2. B7156ARH SRAM Pinout (28)

Table 1. Pin Names

| Pin Names | Functions |
|-----------------|--|
| A0~A14 | Address |
| DQ0~DQ7 | Data Input / Output |
| $\overline{E1}$ | Chip Enable 1 (Active Low) |
| \overline{W} | Write Enable (Low Write Enable, and High Read Enable) |
| \overline{G} | Output Enable (Active Low) |
| VDD | Power (5 V) |
| VSS | Ground |

5. Pin Configurations (Appendix 1)

6. Product Description

6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B7156ARH is GJB597A-1996 B. And B7156ARH is up to the Q/Zt 20198-2011 semiconductor IC standard and CASTPSW11/337-2011 standard.

6.2 Function Description

The B7156RH has four control inputs called Enable 1 ($\overline{E1}$), Write Enable (\overline{W}), and Output Enable (\overline{G}); 15 address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). $\overline{E1}$ are device enable inputs that control device selection, active, and standby modes. Asserting both $\overline{E1}$ enables the device, causes I_{DD} to rise to its active value, and decodes the 15 address inputs to select one of 32,768 words in the memory. \overline{W} controls read and write operations. During a read cycle, \overline{G} must be asserted to

enable the outputs.

Table 2. Device Operation Truth Table

| Inputs | | | Outputs | |
|----------------|----------------|-----------------|------------------|--------------------|
| \overline{G} | \overline{W} | $\overline{E1}$ | I/O Mode | Mode |
| X | X | 1 | DQ(7:0) 3-State | Standby |
| 0 | 1 | 0 | DQ(7:0) Data out | Read |
| X | 0 | 0 | DQ(7:0) Data in | Write |
| 1 | 1 | 0 | DQ(7:0) 3-State | Read DQ 3-State |

Notes:

1. X = Don't care

◆ Read Cycle

A combination of \overline{W} greater than $V_{IH}(\min)$ and $\overline{E1}$ less than $V_{IL}(\max)$ defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is enabled with \overline{G} asserted and \overline{W} deasserted. Valid data appears on data outputs DQ (7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by the latter of $\overline{E1}$ going active while \overline{G} remains asserted, \overline{W} remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 8-bit word addressed by A (18:0) is accessed and appears at the data outputs DQ (7:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by \overline{G} going active while $\overline{E1}$ are asserted, \overline{W} is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

◆ Write Cycle

A combination of \overline{W} and $\overline{E\overline{I}}$ less than $V_{IL(max)}$ defines a write cycle. The state of \overline{G} is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either \overline{G} is greater than $V_{IH(min)}$, or when \overline{W} is less than $V_{IL(max)}$.

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by \overline{W} going high, with $\overline{E\overline{I}}$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by \overline{W} , and by t_{ETWH} when the write is initiated by $\overline{E\overline{I}}$. Unless the outputs have been previously placed in the high-impedance state by \overline{G} , the user must wait t_{WLQZ} before applying data to the 8 bidirectional pins DQ (7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by either of $\overline{E\overline{I}}$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by \overline{W} , and by t_{ETEF} when the write is initiated by either $\overline{E\overline{I}}$ going active. For the \overline{W} initiated write, unless the outputs have been previously placed in the high-impedance state by \overline{G} , the user must wait t_{WLQZ} before applying data to the 8 bidirectional pins DQ (7:0) to avoid bus contention.

6.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

| Symbol | Parameter | Limits |
|----------|------------------------|----------------|
| V_{DD} | supply voltage | 4.5 V ~ 5.5 V |
| T_C | Case temperature range | -55°C ~ +125°C |
| V_I | DC input voltage | 0 V ~ V_{DD} |

7. Electrical Characteristics

7.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 4. DC Parameter Table (I)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|-----------------|------------------------------------|---|---------------|------|---------|
| V_{IH} | High-level input voltage | (CMOS) | 3.5 | | V |
| V_{IL} | Low-level input voltage | (CMOS) | | 1.5 | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 200\mu A$, $V_{DD} = 4.5V$ (CMOS) | | 0.05 | V |
| V_{OH} | High-level output voltage | $I_{OH} = -200\mu A$, $V_{DD} = 4.5V$ (CMOS) | $V_{DD}-0.05$ | | V |
| V_{OH} | High-level output voltage | $I_{OH} = -4mA$, $V_{DD} = 4.5V$ (CMOS) | 4.2 | | V |
| C_{IN}^1 | Input capacitance | $f = 1MHz @ 0V$ | | 20 | pF |
| C_{IO}^1 | Bidirectional I/O capacitance | $f = 1MHz @ 0V$ | | 20 | pF |
| I_{IN} | Input leakage current | $V_{IN} = V_{DD}$ and V_{SS} | -5 | 5 | μA |
| I_{OZ} | Three-state output leakage current | $V_O = V_{DD}$ and V_{SS} $V_{DD} = 5.5V$ $\overline{G} = 5.5V$ | -10 | 10 | μA |
| $I_{DD}(OP)$ | Supply current operating @1MHz | CMOS inputs ($I_{OUT} = 0$) $V_{DD} = 5.5V$ | | 50 | mA |
| $I_{DD1}(OP)$ | Supply current operating @ 25MHz | CMOS inputs ($I_{OUT} = 0$) $V_{DD} = 5.5V$ | | 120 | mA |
| $I_{DD3}(SB)^2$ | Supply current standby @ 0Hz | CMOS inputs ($I_{OUT} = 0$) $\overline{EI} = V_{DD} - 0.5$, $V_{DD} = 5.5V$ | | 1.2 | mA |

Notes:

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. $V_{IH} = 5.5V$, $V_{IL} = 0V$.

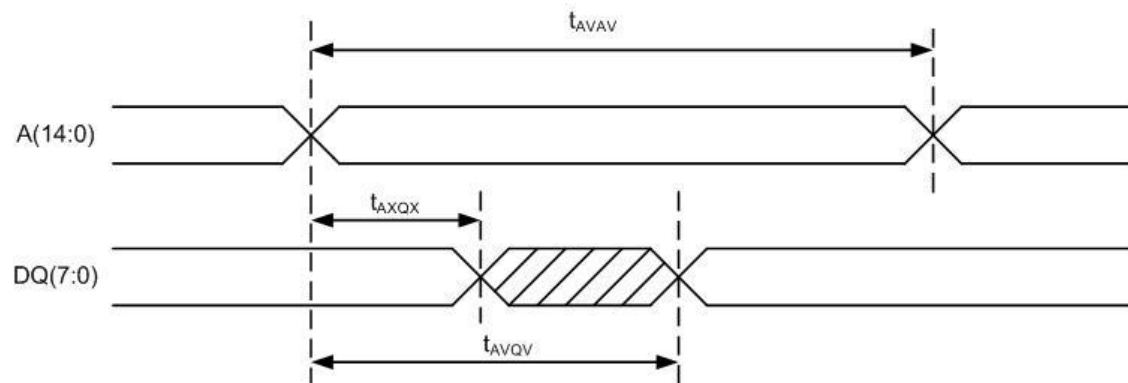
7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 5. Read Cycle AC Parameters

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| t_{AVAV}^1 | Read cycle time | 40 | | ns |
| t_{AVQV} | Read access time | | 40 | ns |
| t_{AXQX}^2 | Output hold time | 5 | | ns |
| t_{GLQX}^2 | \overline{G} -controlled output enable time | 3 | | ns |
| t_{GLQV} | \overline{G} -controlled output enable time (Read Cycle 3) | | 15 | ns |
| t_{GHQZ}^2 | \overline{G} -controlled output three-state time | | 15 | ns |
| t_{ETQX}^2 | $\overline{E1}$ -controlled output enable time | 3 | | ns |
| t_{ETQV} | $\overline{E1}$ -controlled access time | | 40 | ns |
| t_{EFQZ}^1 | $\overline{E1}$ -controlled output three-state time ² | | 15 | ns |

Notes:

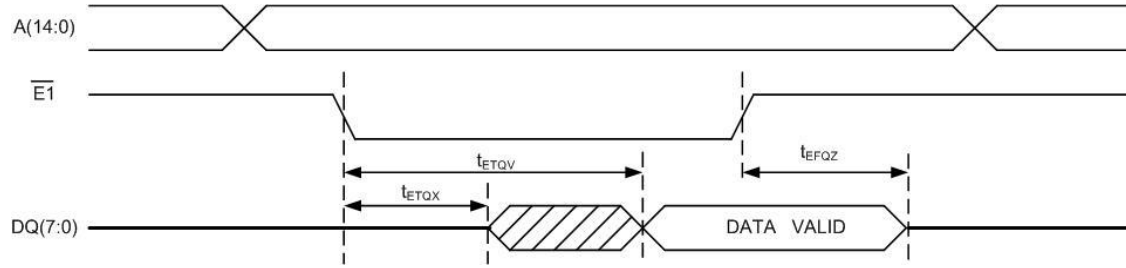
1. Functional test.
2. Three-state is defined as a 500mV change from steady-state output voltage.
3. (VDD = 5.0V ±10%) (-55C to +125C)



Assumptions:

1. $\overline{E1} \leq V_{IL}(\max)$ 、 $\overline{G} \leq V_{IL}(\max)$
2. $\overline{W} \geq V_{IH}(\min)$

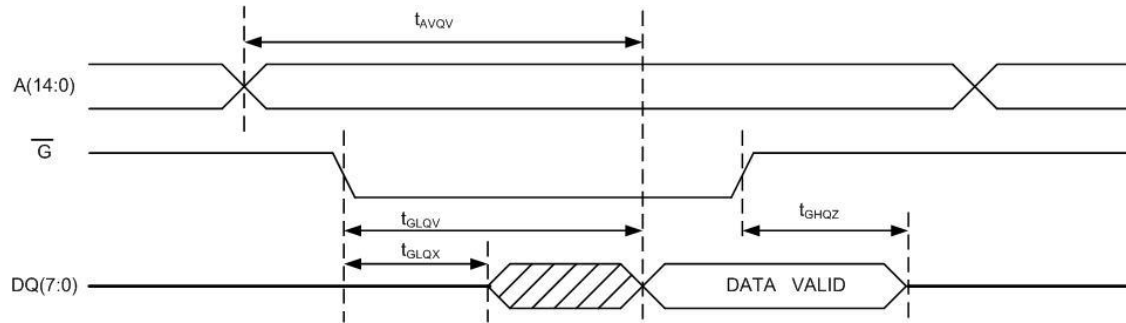
Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:

1. $\bar{G} \leq V_{IL}(\max)$ and $\bar{W} \geq V_{IH}(\min)$

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:

1. $\bar{E1} \leq V_{IL}(\max)$
2. $\bar{W} \geq V_{IH}(\min)$

Figure 3c. SRAM Read Cycle 3: Output Enable Access

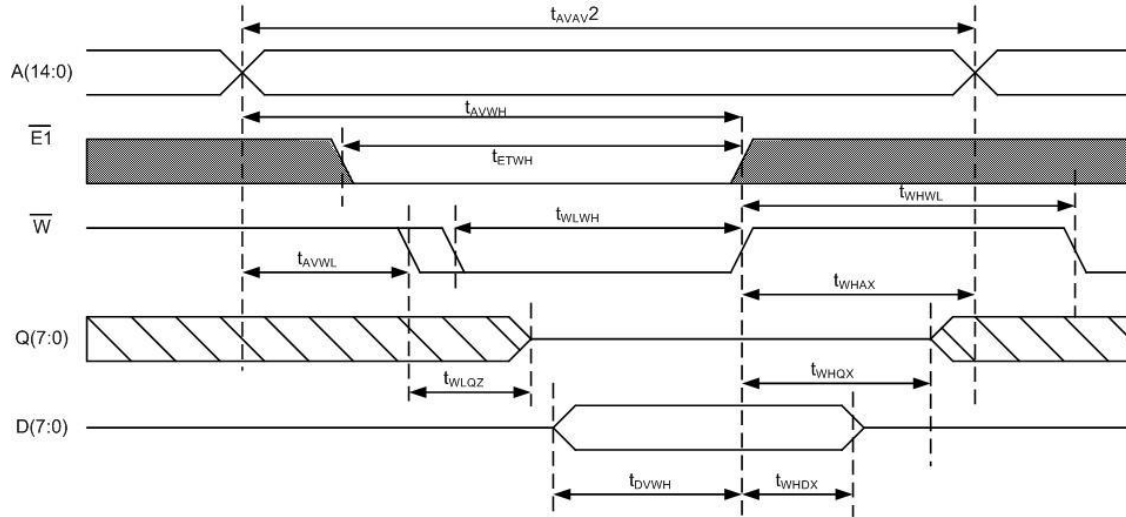
7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 6. Write Cycle AC Parameter

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|---|-----|-----|------|
| t_{AVAV}^1 | Write cycle time | 40 | | ns |
| t_{ETWH} | Device enable to end of write | 35 | | ns |
| t_{AVET} | Address setup time for write (\overline{EI} - controlled) | 0 | | ns |
| t_{AVWL} | Address setup time for write (\overline{W} - controlled) | 0 | | ns |
| t_{WLWH} | Write pulse width | 35 | | ns |
| t_{WHAX} | Address hold time for write (\overline{W} - controlled) | 0 | | ns |
| t_{EFAX} | Address hold time for device enable (\overline{EI} controlled) | 0 | | ns |
| t_{WLQZ}^2 | \overline{W} - controlled three-state time | | 15 | ns |
| t_{WHQX}^2 | \overline{W} - controlled output enable time | 1 | | ns |
| t_{ETEF} | Device enable pulse width (\overline{EI} - controlled) | 35 | | ns |
| t_{DVWH} | Data setup time | 30 | | ns |
| t_{WHDX} | Data hold time | 3 | | ns |
| t_{WLEF} | Device enable controlled write pulse width | 35 | | ns |
| t_{DVEF} | Data setup time | 35 | | ns |
| t_{EFDX} | Data hold time | 0 | | ns |
| t_{AVWH} | Address valid to end of write | 35 | | ns |
| t_{WHWL}^1 | Write disable time | 5 | | ns |

Notes:

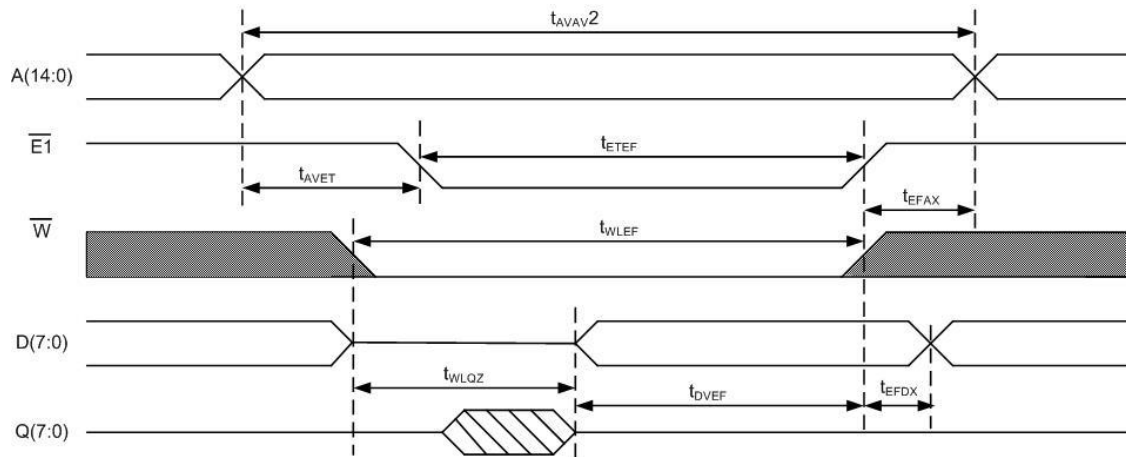
1. Functional test performed with outputs disabled (\overline{G} high).
2. Three-state is defined as 500mV change from steady-state output voltage.
3. (VDD = 5.0V \pm 10%) (-55C to +125C)



Assumptions:

1. $\bar{G} \leq V_{IL}(\max)$. If $\bar{G} \geq V_{IH}(\min)$ then Q(7:0) will be in three-state for the entire cycle.
2. \bar{G} high for t_{AVAV} cycle.

Figure 4a. SRAM Write Cycle 1: W - Controlled Access



Assumptions & Notes:

1. $\bar{G} \leq V_{IL}(\max)$. If $\bar{G} \geq V_{IH}(\min)$ then Q(7:0) will be in three-state for the entire cycle.
2. \bar{G} high for t_{AVAV} cycle.

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access

7.4 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

(Referenced to VSS)

| SYMBOL | PARAMETER | LIMITS |
|---------------|---|-----------------------------|
| V_{DD} | DC supply voltage | -0.5 to 7.0V |
| V_{IO} | Voltage on any pin | -0.5 to ($V_{DD} + 0.3$)V |
| T_{STG} | Storage temperature | -65 to +150°C |
| P_D | Maximum power dissipation | 2.0W |
| T_J | Maximum junction temperature ² | +150°C |
| Θ_{JC} | Thermal resistance, junction-to-case | 28°C/W |
| I_I | DC input current | ±10 mA |

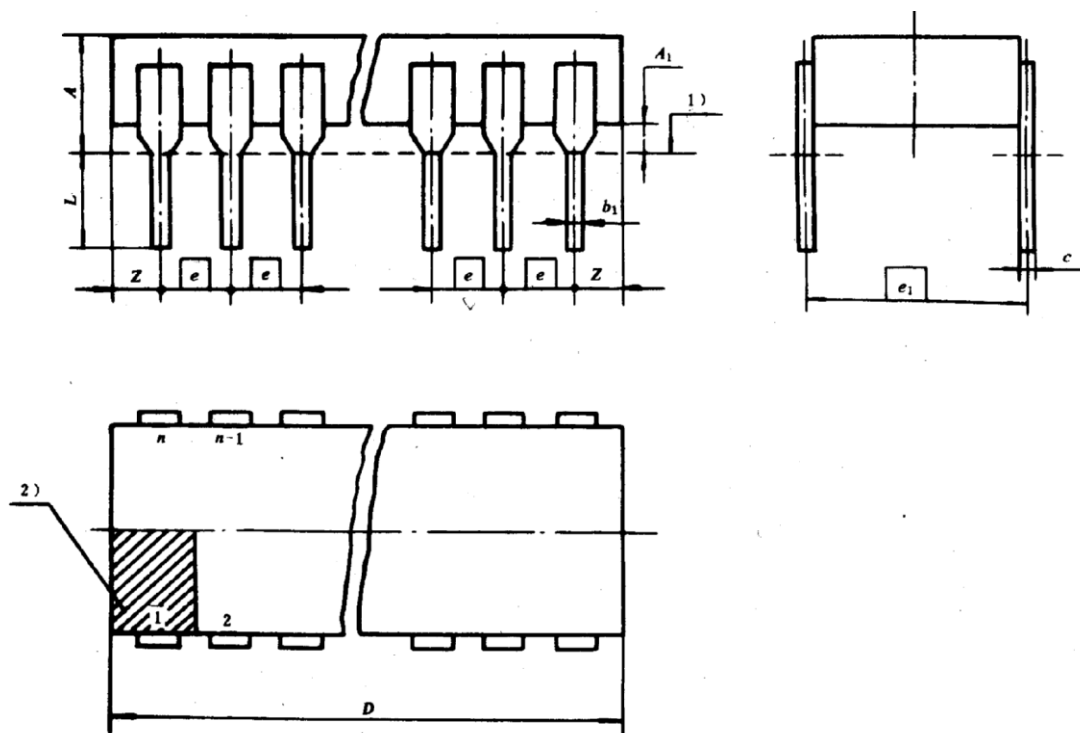
Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Maximum junction temperature may be increased to +175 °C during burn-in and steady-static life.

8. Typical Application (Appendix 2)

9. Packaging

The SRAM B7156ARH utilizes 28-Lead Ceramic Flatpack as shown in Figure 5 and the corresponding dimensions are listed in Table 8, which is accordance with GB/T7092.



Notes: 1) Fitting plane.

2) Pin NO. 1 ID.

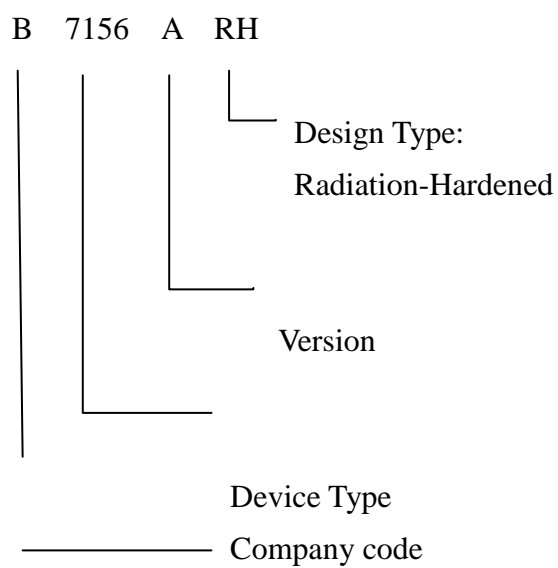
Figure 5. Package Outline

Table 8. Package Dimensions

Unit: mm

| SYMBOL | Value | | |
|--------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | — | — | 5.1 |
| A_1 | 0.51 | — | — |
| b_1 | 0.35 | — | 0.59 |
| c | 0.20 | — | 0.36 |
| e | — | 2.54 | — |
| e_1 | — | 15.24 | — |
| L | 2.54 | — | 5.00 |
| D | — | — | 36.12 |
| Z | — | — | 1.78 |

10. Naming Rule



B7156ARH

Appendix 1

Pin Descriptions are listed in Table 9:

Table 9. Pin Symbols and Functions

| Pin NO. | Symbol | Functions | Pin NO. | Symbol | Functions |
|---------|-----------------|-----------|---------|-----------------|---------------|
| 1 | A14 | Address | 28 | V _{DD} | Power(5V) |
| 2 | A12 | Address | 27 | \overline{W} | Write Enable |
| 3 | A7 | Address | 26 | A13 | Address |
| 4 | A6 | Address | 25 | A8 | Address |
| 5 | A5 | Address | 24 | A9 | Address |
| 6 | A4 | Address | 23 | A11 | Address |
| 7 | A3 | Address | 22 | \overline{G} | Output Enable |
| 8 | A2 | Address | 21 | A10 | Address |
| 9 | A1 | Address | 20 | $\overline{E1}$ | Chip Enable 1 |
| 10 | A0 | Address | 19 | DQ7 | I/O |
| 11 | DQ0 | I/O | 18 | DQ6 | I/O |
| 12 | DQ1 | I/O | 17 | DQ5 | I/O |
| 13 | DQ2 | I/O | 16 | DQ4 | I/O |
| 14 | V _{SS} | Ground | 15 | DQ3 | I/O |

Appendix 2

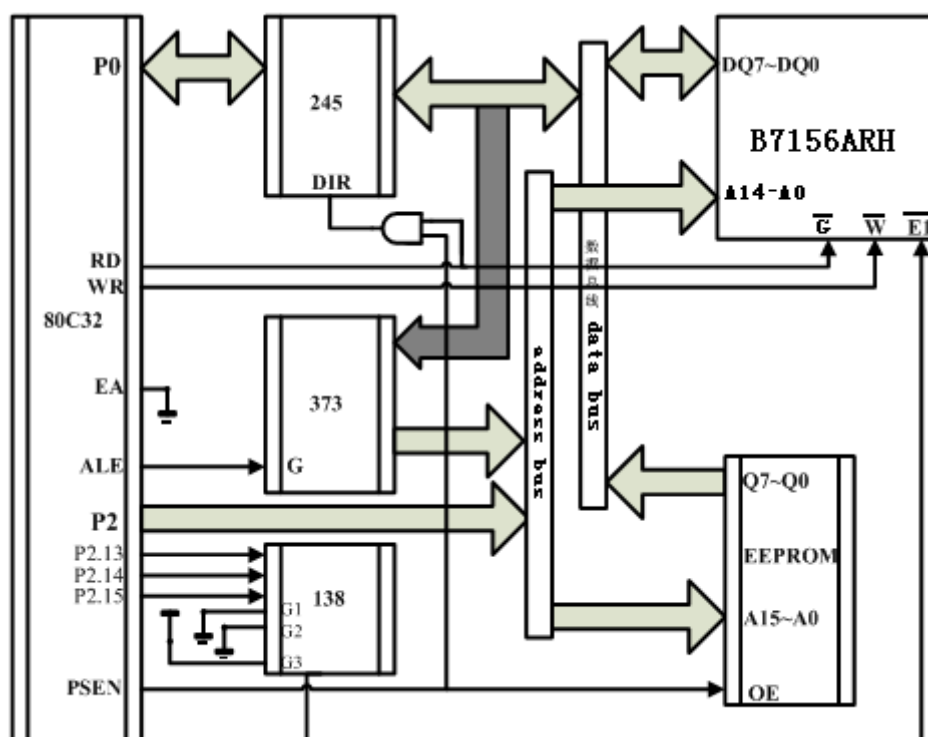


Figure 6. Typical Application

Figure 6 illustrates a typical application system, which consists of a CPU(80c32) and an SRAM (B7156ARH) chip. The B7156ARH serves as a parity check memory. The CPU is configured in standard mode for memory accessed. Besides address and data, the main signal include Chip Enable 、 Output Enable(RD) and Write Enable(WR).

The access timing is fixed for CPU. Base on the access timing of the SRAM(Fig3~Fig4), one should properly configure the control signal .

Notes:

1. Supply voltage is required to be as stable as possible.
2. The input should not be suspend in midair.
3. The output should not be connected to supply voltage or V_{SS} .

There are varied processor in different application, the access timing of SRAM will be different. Such condition requires the system designer to consider the timing carefully.

Service & Supply

Address: No.2. Siyingmen N.Rd. Donggaodi Fengtai District, BeiJing, China

Department: Department of international cooperation

Telephone: +86(0)10-67968115-6751

Email: gjhz@mxtronics.com

Fax: +86(0)10-68757706

Zip code: 100076