NEC®

500 MHz DUAL-MODULUS PRESCALER

UPB571C

DESCRIPTION

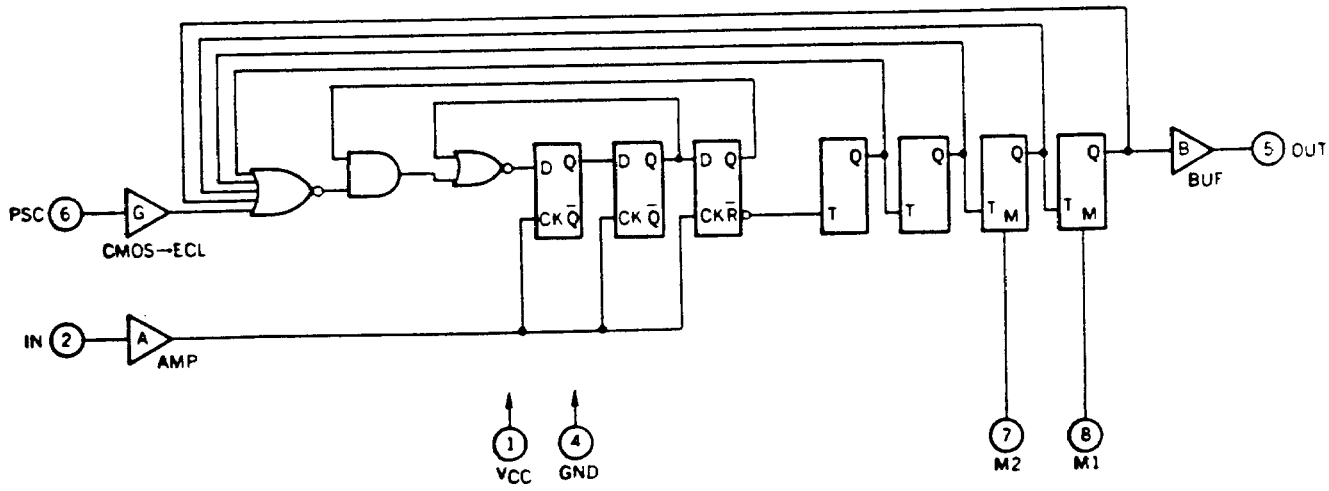
The UPB571C is a 500 MHz Low Power Dual - modulus prescaler intended for use in PLL digital tuning systems in connection with NEC PLL LSI ICs.

The device provides 1/64, 1/65, 1/32, 1/33, 1/16 and 1/17 division ratio for pulse swallowing method and is guaranteed to operate up to 500 MHz over a -35°C to +75°C temperature range.

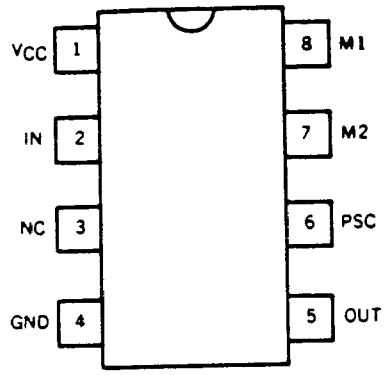
FEATURES

- High frequency operation: 500 MHz MAX. (V_{IN} = 400 mV_{p-p})
- Dual mode operation with pulse swallowing method
  ÷64/÷65 , ÷32/÷33 , ÷16/÷17
- Single supply Voltage: V_{CC} = 5.0 V ± 10 %
- Low supply current: I_{CC} = 11 mA (TYP.)
- Small package: 8 pin plastic dual in-line package (DIP)

BLOCK DIAGRAM



CONNECTION DIAGRAM



1	V_{CC}	Power Supply
2	IN	Signal Input
3	NC	No Connection
4	GND	Ground
5	OUT	Signal Out
6	PSC	Modulus Control Input
7	M2	Divide Ratio Control 2
8	M1	Divide Ratio Control 1

DIVIDE RATIO

M1	M2	PSC	DIVIDE RATIO
L	L	H	64
L	L	L	65
L	H	H	32
L	H	L	33
H	H	H	16
H	H	L	17

M Terminal

"H" : Connect to V_{CC}

"L" : Open

PSC Terminal

"H" : 0.8 V_{CC} to V_{CC} [V]

"L" : 0 to 0.2 V_{CC} [V]

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +6.0	V
Input Voltage	V_I	−0.5 to V_{CC} +0.5	V
Output Current	I_o	−10	mA
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_{opt}	−35 to +75	°C

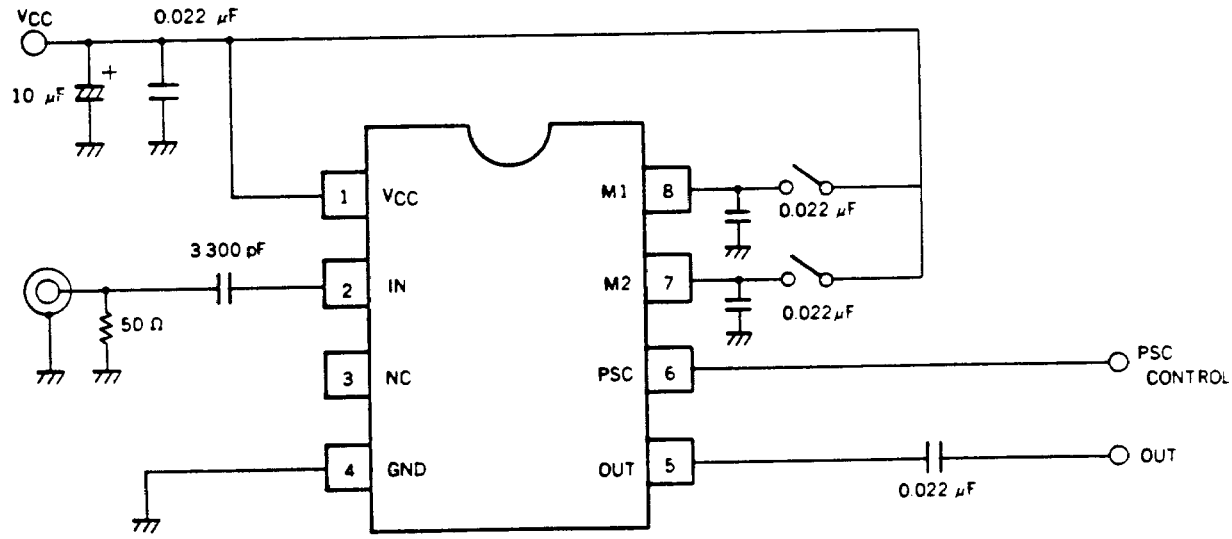
RECOMMENDED OPERATING CONDITIONS

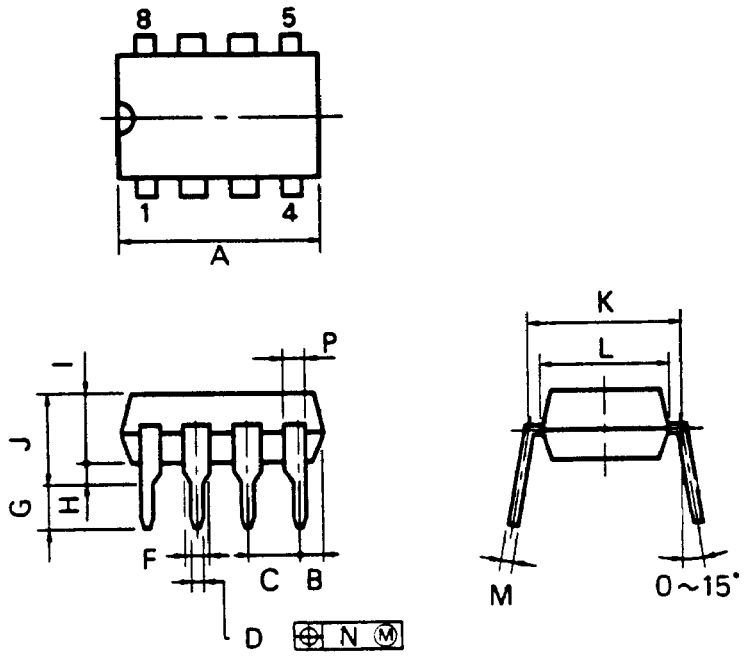
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Amplitude	V_{in}	0.4		1.2	V_{p-p}	IN Terminal
High Level Input Voltage	V_{IH}	0.8 V_{CC}			V	PSC Terminal
Low Level Input Voltage	V_{IL}			0.2 V_{CC}	V	PSC Terminal
Frequency Response	f_{in}	100		500	MHz	IN Terminal, V_{in} = 0.4 V_{p-p}
Output Load Capacitance	CL			10	pF	
Operating Temperature	T_{opt}	−35		75	°C	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5±0.5 [V], T_a = −35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{CC}		11	15.7	mA	
Output Amplitude	V_o	0.9	1.2		V_{p-p}	Out Terminal
High Level Input Current	I_{IH}			5	μA	PSC, M, Terminal
Set-up Time	t_s			30	ns	PSC to Out
Output Rise Time	t_r	5		15	ns	C_L = 10 pF, 20 to 80 % Out Terminal

MEASUREMENT CIRCUIT





P8C-100-3008.C

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	$3.2^{-0.3}$	$0.126^{-0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.