Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(✓) Final Specifications

Module	**15.6" (15.55) FHD 16:9 Color TFT-LCD with *LED Backlight* design**
Model Name	B156HW02 V1 (H/W:0A) / VNJVC
Note ( )	***LED Backlight with driving circuit design***

Customer	Date	Approved by	Date
		Vicki Chai	02/08/2011
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Aries SH Hsu	02/08/2011

Note: This Specification is subject to change without notice.

NBBU Marketing Division / AU Optronics corporation

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2010/06/29	All	Preliminary Edition for Customer		
0.2 2010/11/01	28 ; 30~33		X20 label and EDID updated	
0.3 2010/11/26	22		Remove T10 max value	
1.0 2011/01/12	28 ; 30~33	X20 label and EDID	A00 label and EDID updated	
	25~27		LCM drawing updated	
1.1 2011/02/08	30~33		A00 EDID updated	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electros tic breakdown.

2. General Description

B156HW02 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD (1920(H) x 1080(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B156HW02 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

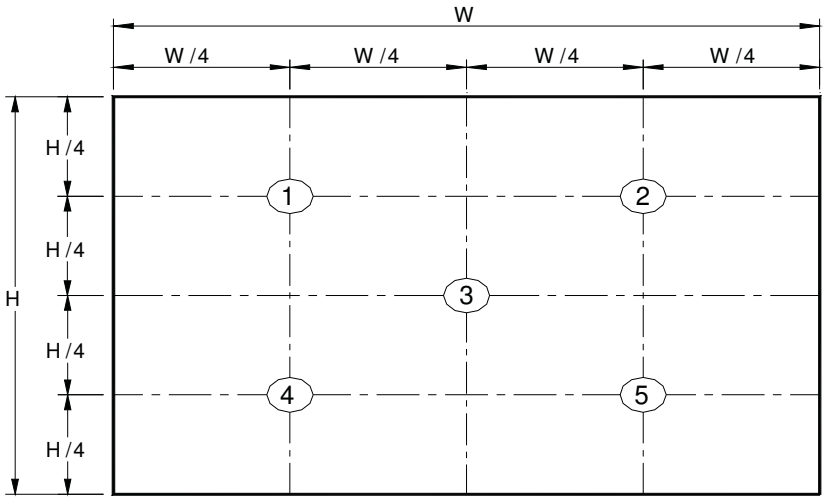
Items	Unit	Specifications			
Screen Diagonal	[mm]	15.6" (15.55)			
Active Area	[mm]	344.16 x 193.59			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	**[mm]**	0.17925 x 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance **(I_{LED}=6.5mA)** **(Note: I_{LED} is LED current)**	[cd/m²]	300 typ. (5 points average) 255 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 :1 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	8.0 max. (Include Logic and Blu power)			
Weight	[Grams]	470 max.			
Physical Size **Without inverter, bracket.**	[mm]		Min.	Typ.	Max.
		Length	358.8	359.3	359.8
		Width	209.0	209.5	210.0
		Thickness	-	-	5.7
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-Glare			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

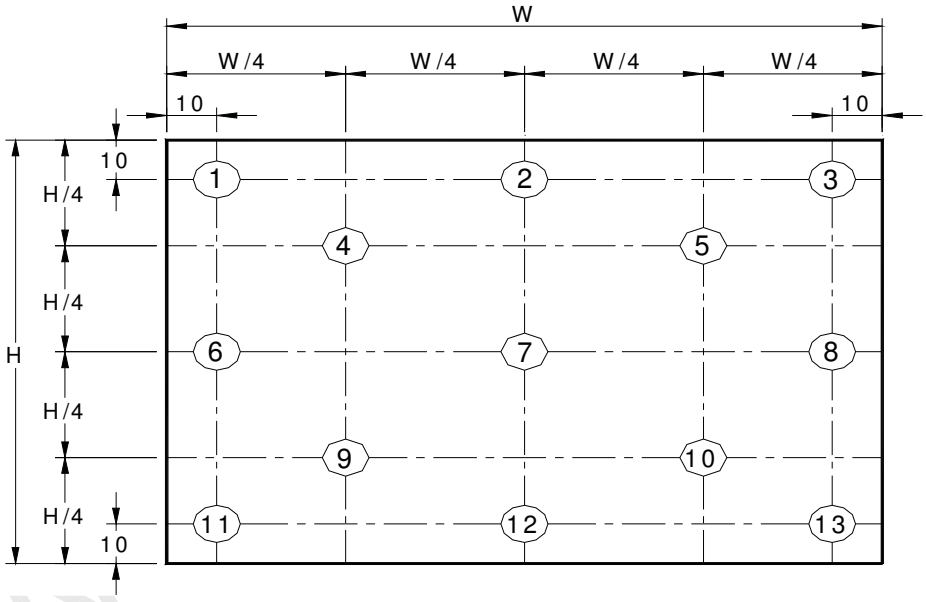
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA			5 points average	255	300	-	cd/m²	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	60	70	-	degree	4, 9
		θ_L	(Left)	60	70	-		
		ψ_H	Vertical (Upper) CR = 10	45	60	-		
		ψ_L	(Lower)	50	60	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		500	600	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.59	0.62	0.65	-	4
		Ry		0.32	0.35	0.38		
	Green	Gx		0.29	0.32	0.35		
		Gy		0.57	0.6	0.63		
	Blue	Bx		0.12	0.15	0.18		
		By		0.09	0.12	0.15		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		--	60			

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

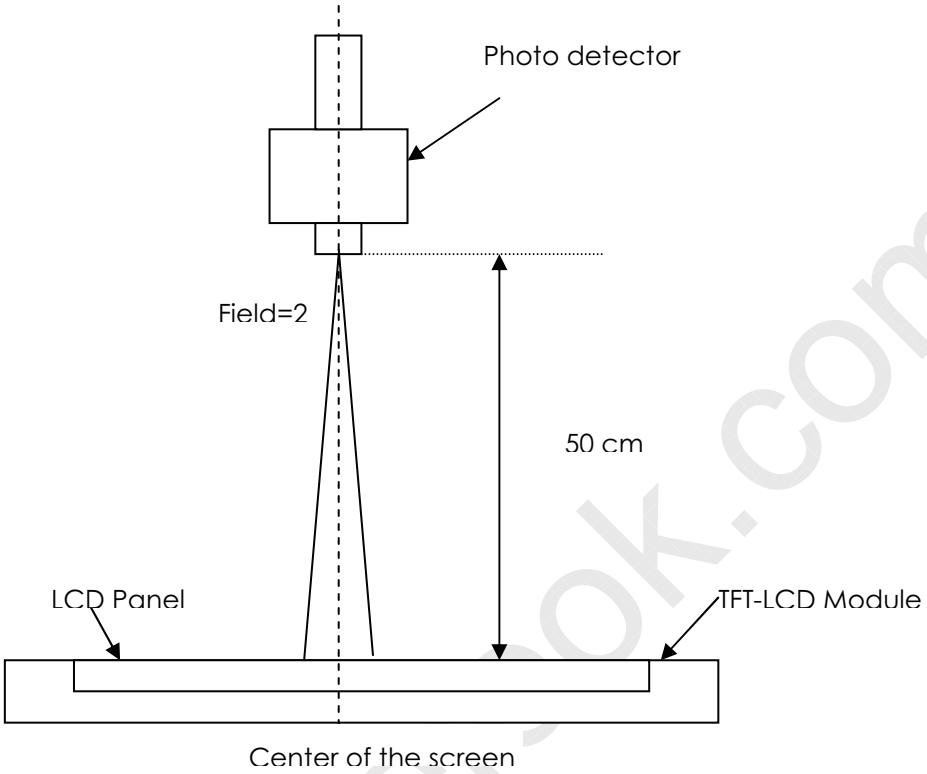
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after

lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

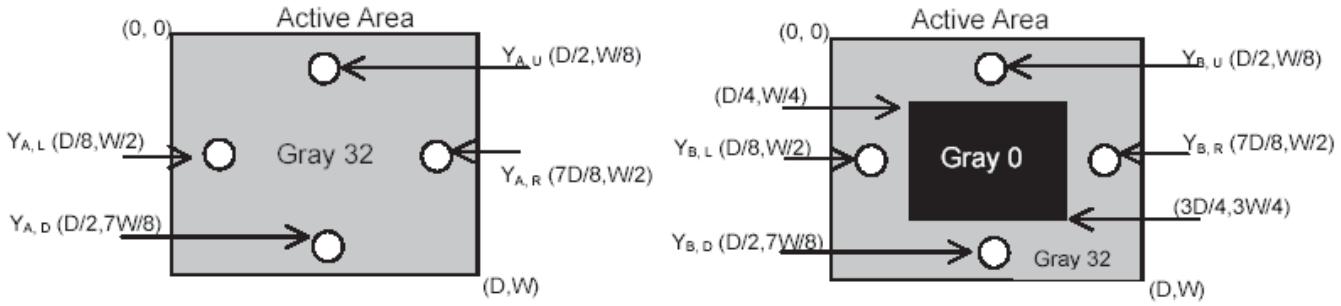
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

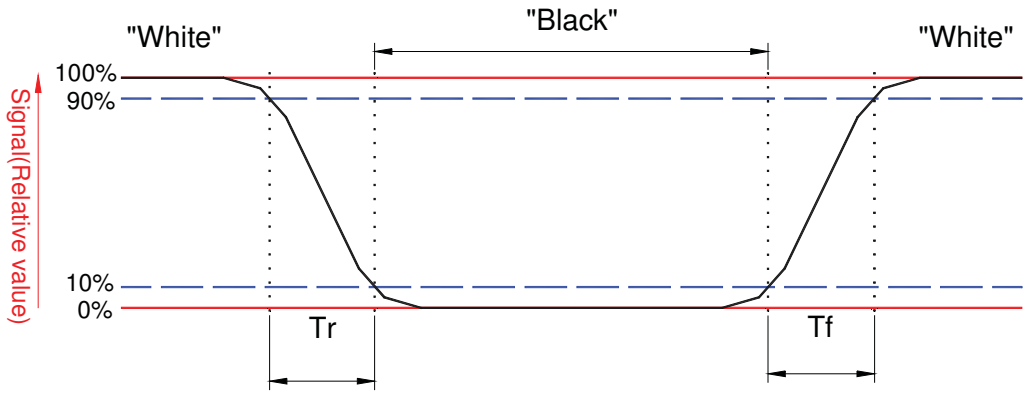
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



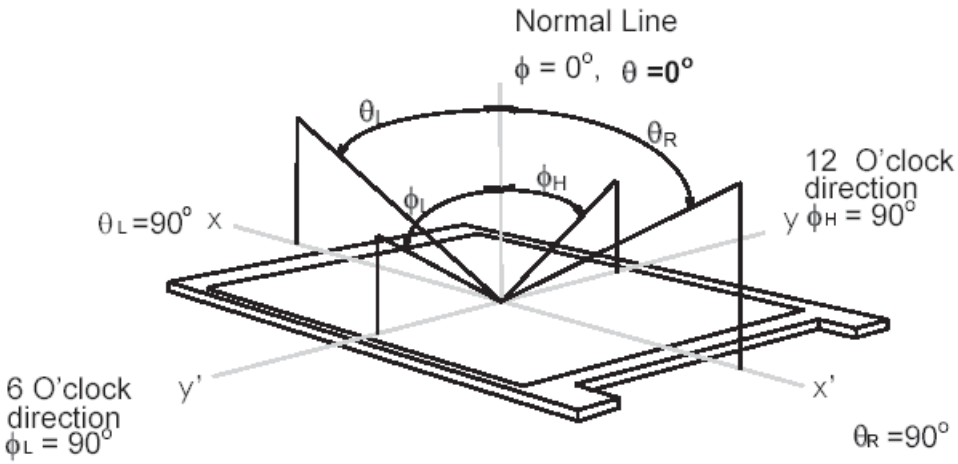
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



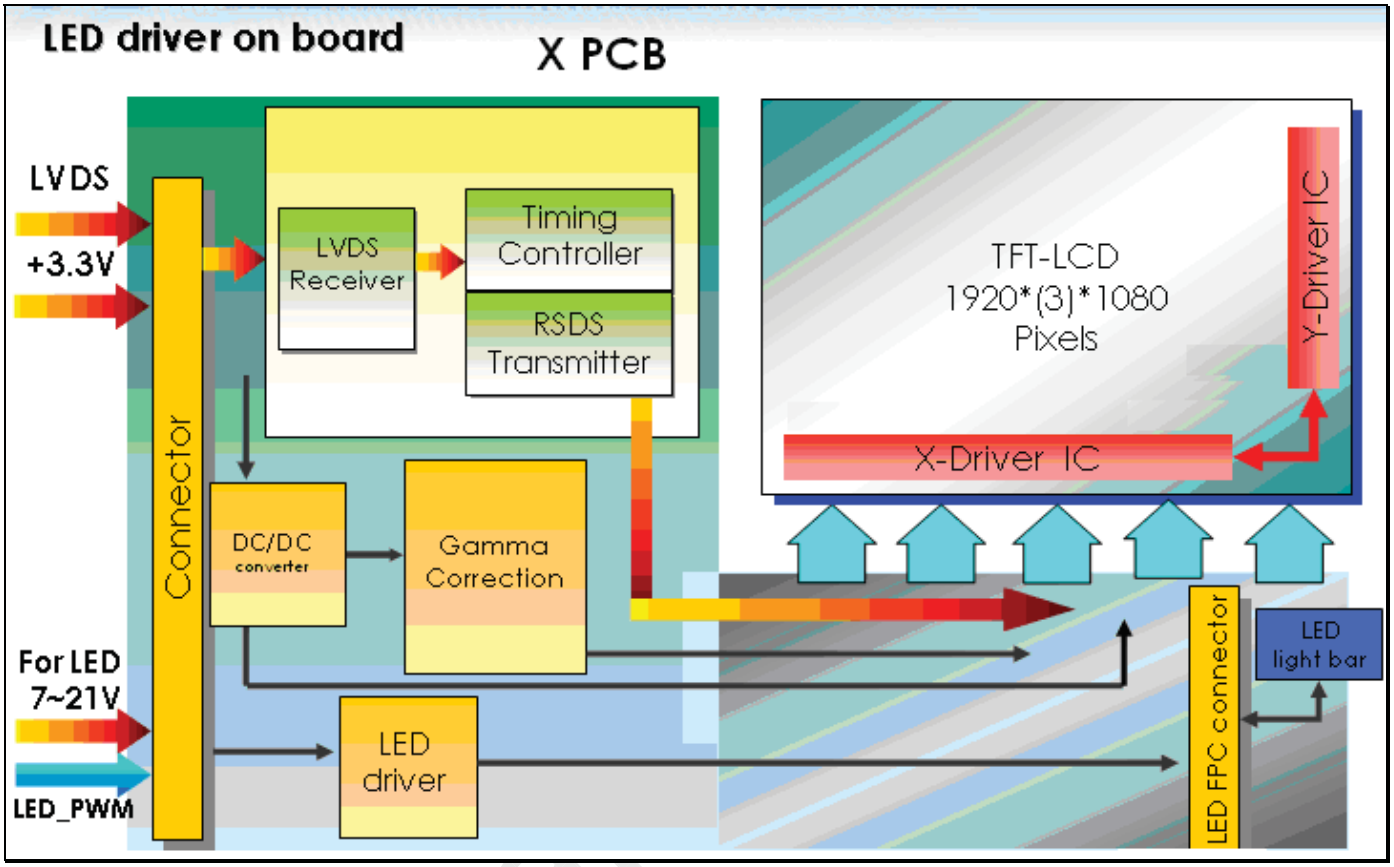
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin.



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

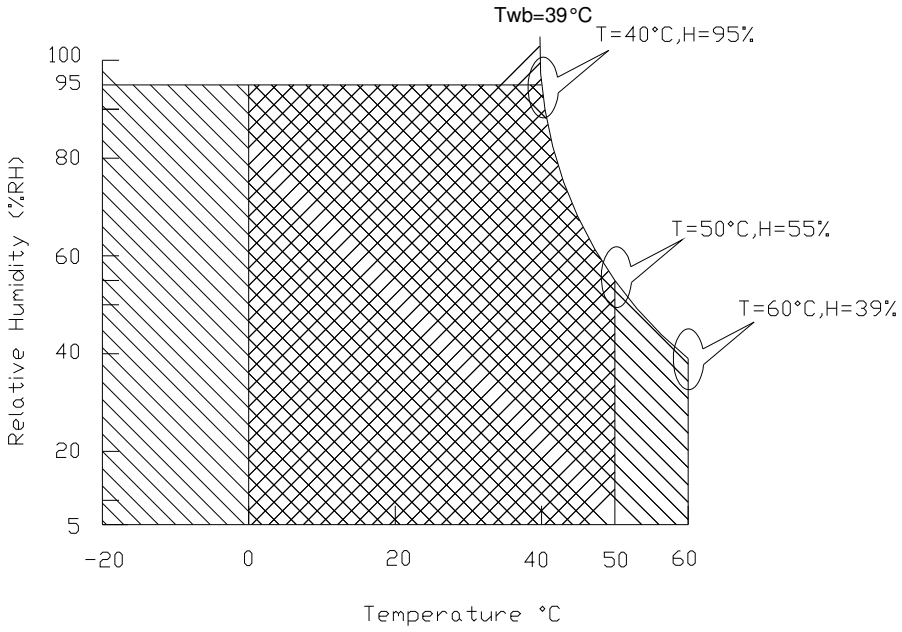
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	8	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

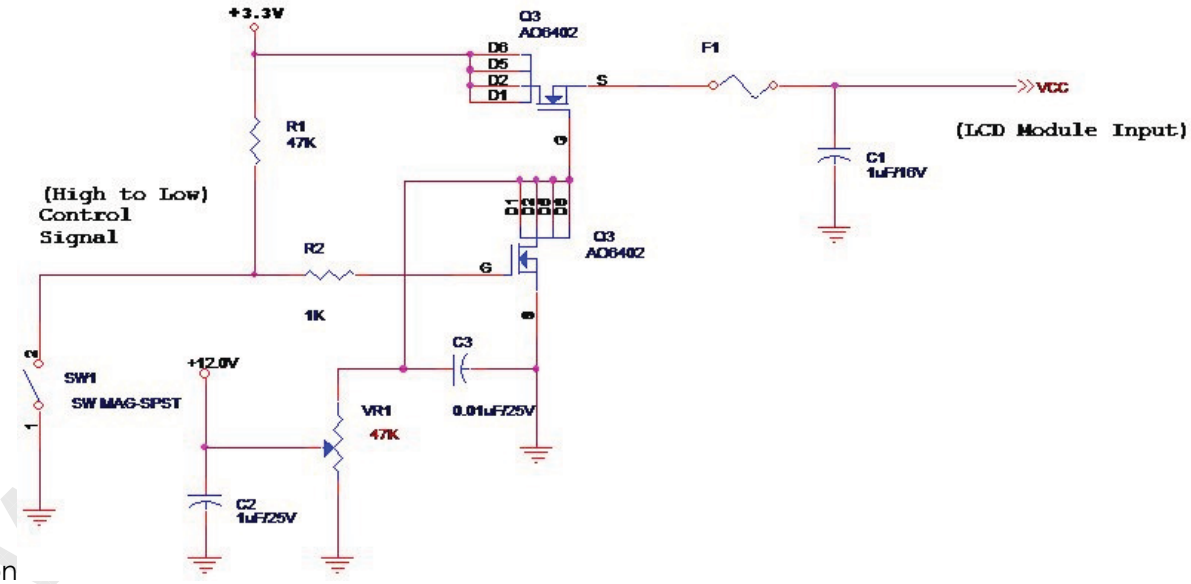
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2.0	[Watt]	Note 1/2
IDD	IDD Current	-	-	606	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

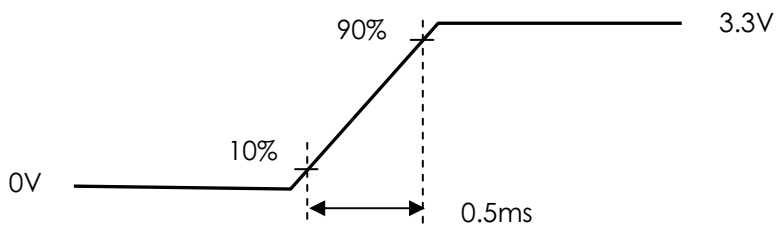
Note 1 : Maximum Measurement Condition：Black Pattern, XP Desktop Pattern

Note 2：Typical Measurement Condition: Mosaic Pattern, XP Desktop Pattern

Note 3：Measure



Condition



Vin rising time

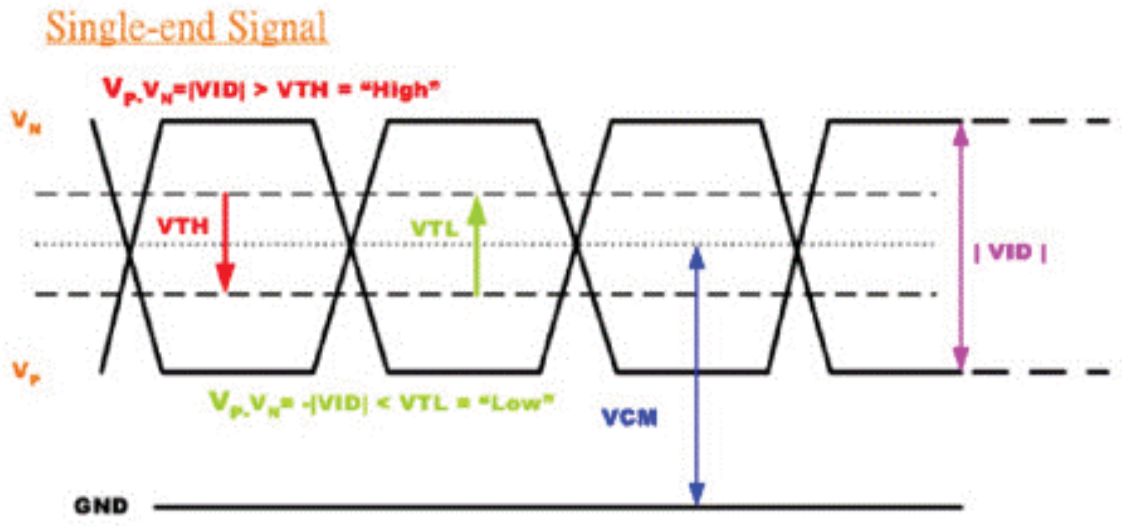
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
$\lvert V_{ID} \rvert$	Differential Input Voltage	100	600	[mV]
V_{CM}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-		6.0	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

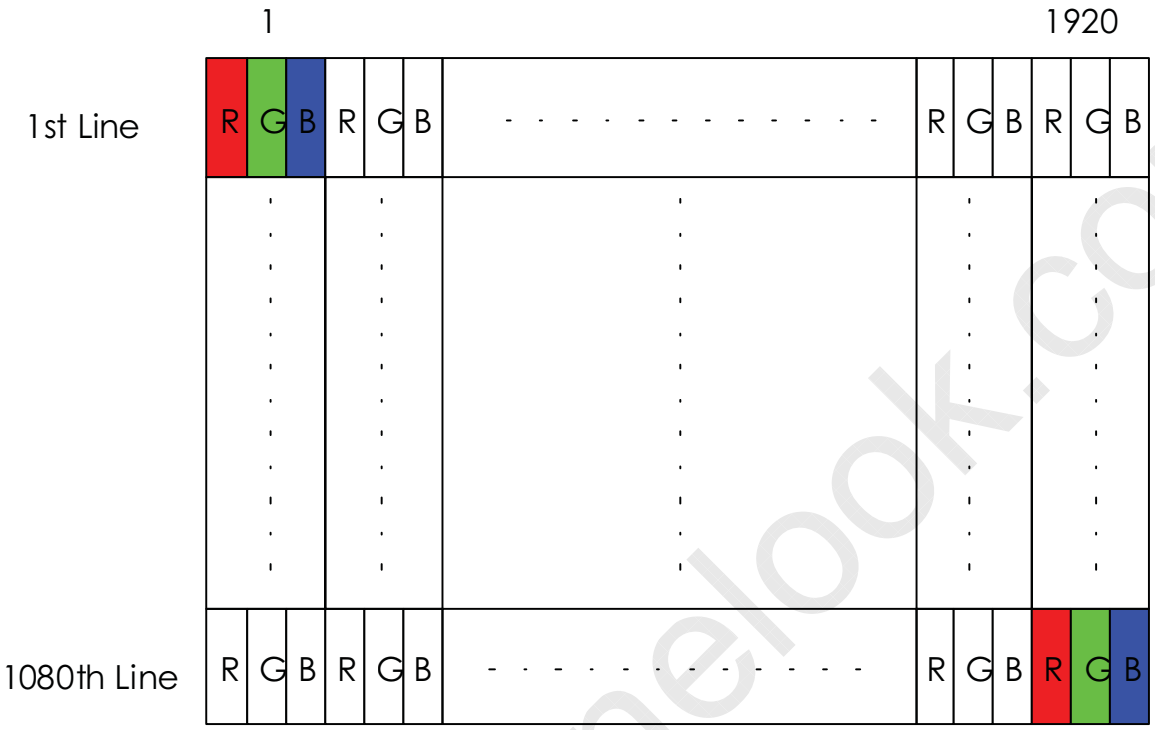
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	200	20k	Hz	
PWM Duty Ratio	Duty	1	--	100	%	

Note 1: Calculator Value for refence IFx VFx 36 efficency (85%) = P(typ);P(max) estimated with Lf and VF tolerance.
Note2: The LED life-time define as the estimated time to 50% degradation of iinitial luminous.
Note3: Output PWM frequency< 5k Hz

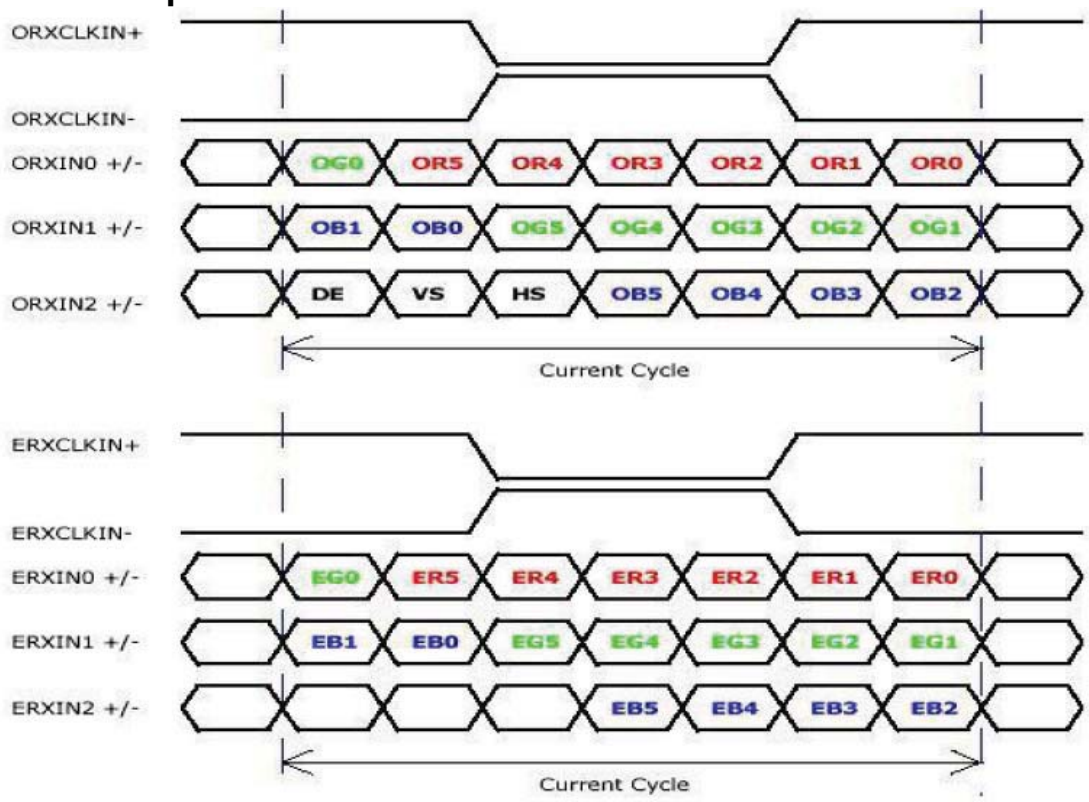
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX
Type / Part Number	IPEX 20455-040E-12R or compatible
Mating Housing/Part Number	IPEX 20353-040T-11 or compatible

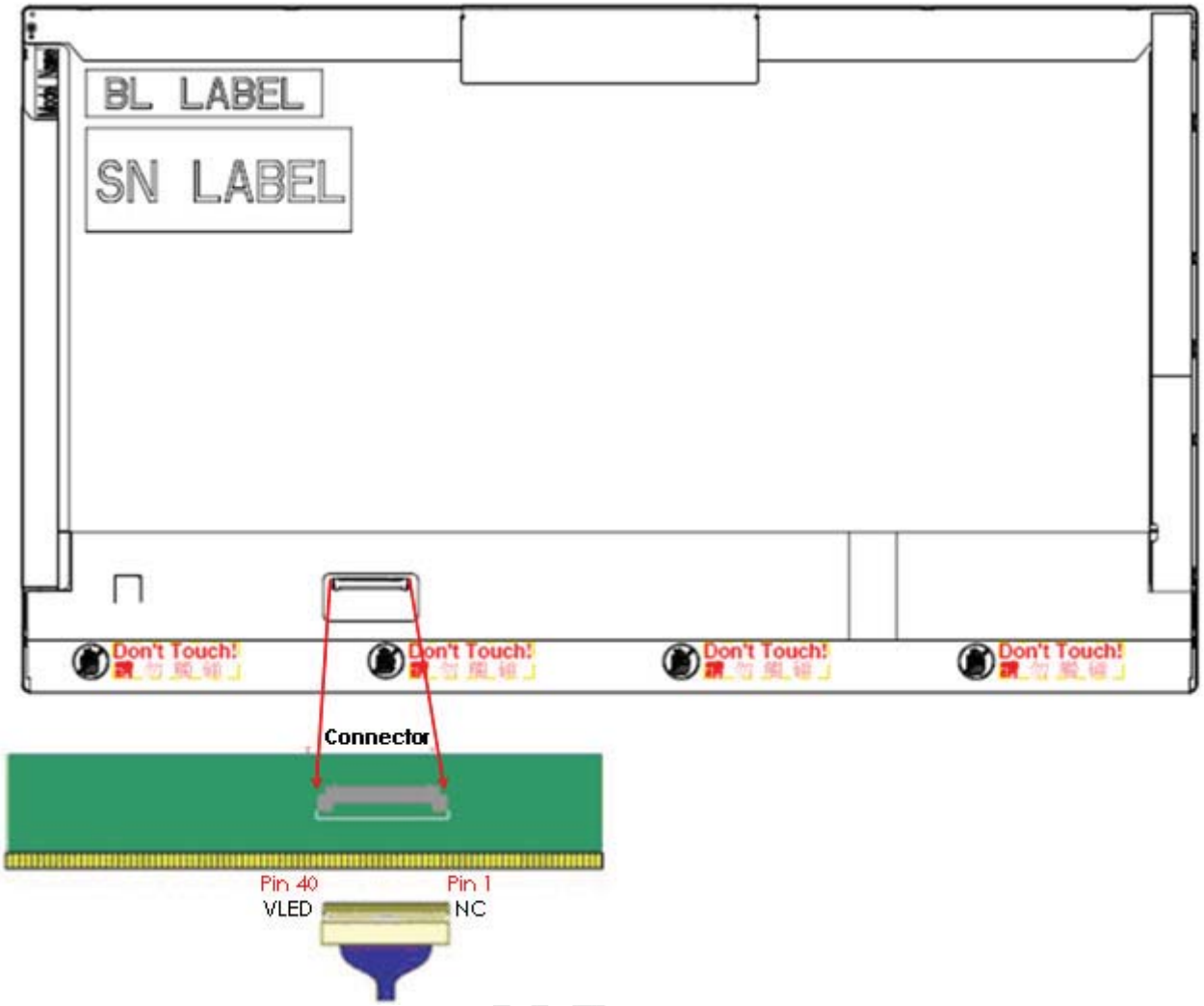
6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	NC	No connection (Reserve)
2	AVDD	PowerSupply,3.3V(typical)
3	AVDD	PowerSupply,3.3V(typical)
4	DVDD	DDC 3.3Vpower
5	Test	Panel Self Test
6	SCL	DDCClock
7	SDA	DDCData
8	Odd_Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Odd_Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Odd_Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Odd_Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Odd_Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Odd_Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	Odd_ClkIN-	-LVDSdifferential clock input
18	Odd_ClkIN+	+LVDSdifferential clock input
19	GND	Ground–Shield
20	Even_Rin0-	-LVDSdifferential data input(R0-R5,G0)
21	Even_Rin0+	+LVDSdifferential data input(R0-R5,G0)
22	GND	Ground
23	Even_Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)

24	Even_Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
25	GND	Ground
26	Even_Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
27	Even_Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
28	GND	Ground
29	Even_ClkIN-	-LVDSdifferential clock input
30	Even_ClkIN+	+LVDSdifferential clock input
31	GND	Ground–Shield
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No connection (Reserve)
35	PWM	System PWM Logic Input level
36	LED_EN	LED enable input level
37	NC	No Connection (Reserve)
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.

internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input

6.4 Interface Timing

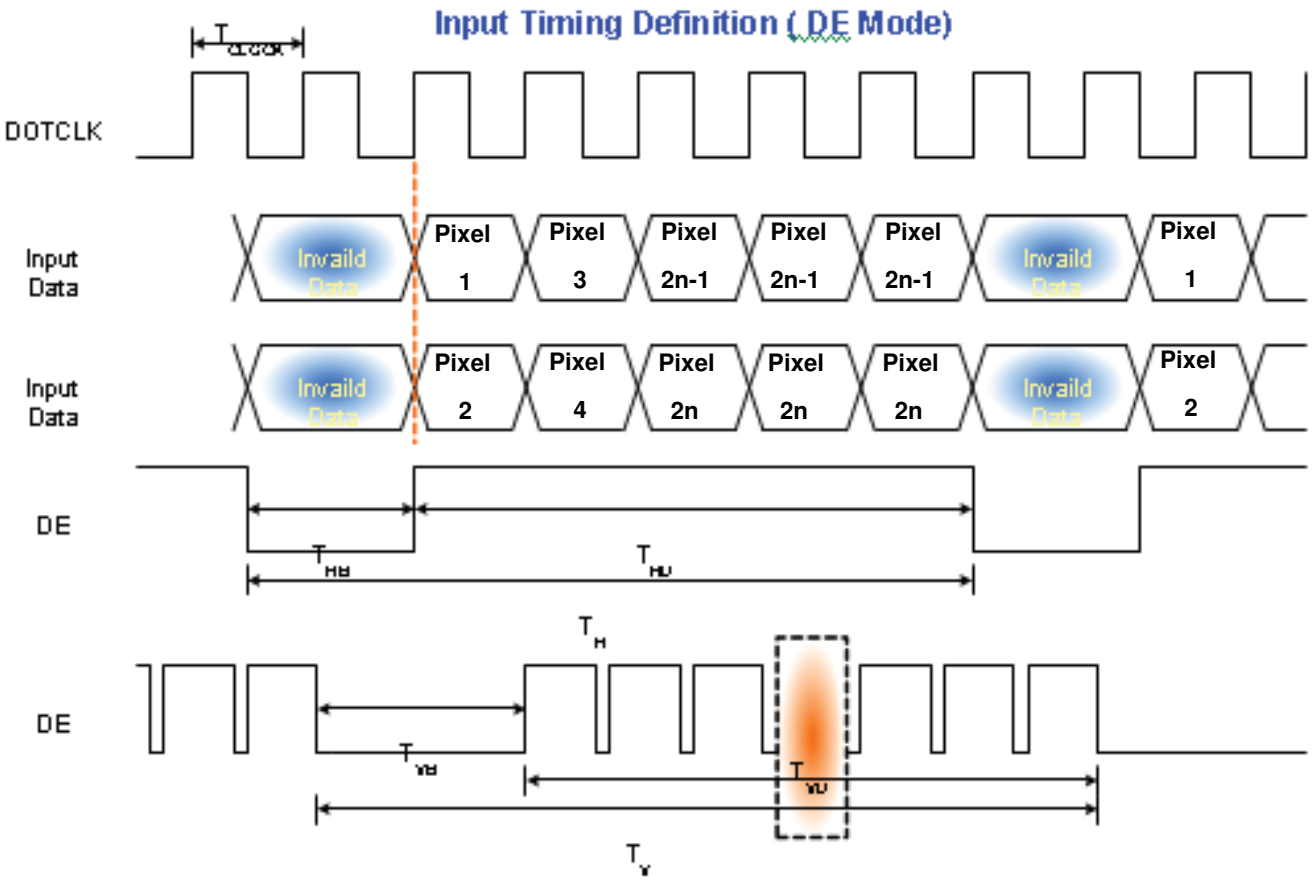
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	40	60	-	Hz
Clock frequency		1/ T_{Clock}	-	71.19	85	MHz
Vertical Section	Period	T_V	1088	1130	-	T_{Line}
	Active	T_{VD}		1080		
	Blanking	T_{VB}	8	50	-	
Horizontal Section	Period	T_H	990	1050	-	T_{Clock}
	Active	T_{HD}		960		
	Blanking	T_{HB}	30	90	-	

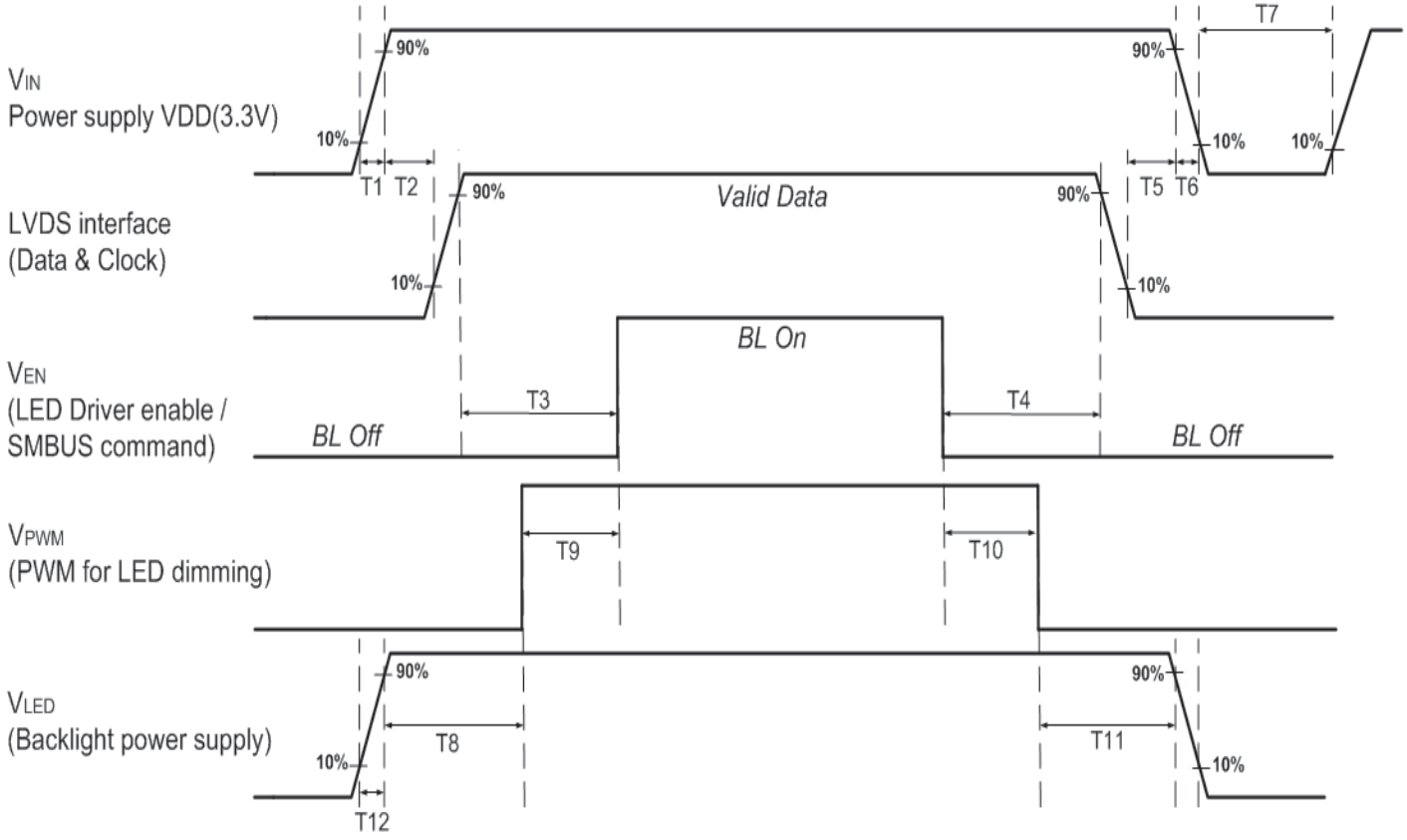
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

LED on/off sequence is as follows. Interface signals are also shown in the chart.



	Min (ms)	Max (ms)
T1	0.5	10
T2	0	50
T3	250	-
T4	200	-
T5	0	50
T6	0	10
T7	500	-
T8	10	-
T9	10	-
T10	10	-
T11	10	-
T12	0.5	10

Note 1 : If T4<200ms，The display garbage may occur. We suggest T4>200ms to avoid the display garbage.

Note 2：If T1 or T12<0.5ms，the inrush current may cause the damage of fuse. If T1 or T12<0.5ms，the inrush current I^2t is under typical melt of fuse Spec.，there is no mentioned problem.

7. Vibration and Shock Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3. Reliability

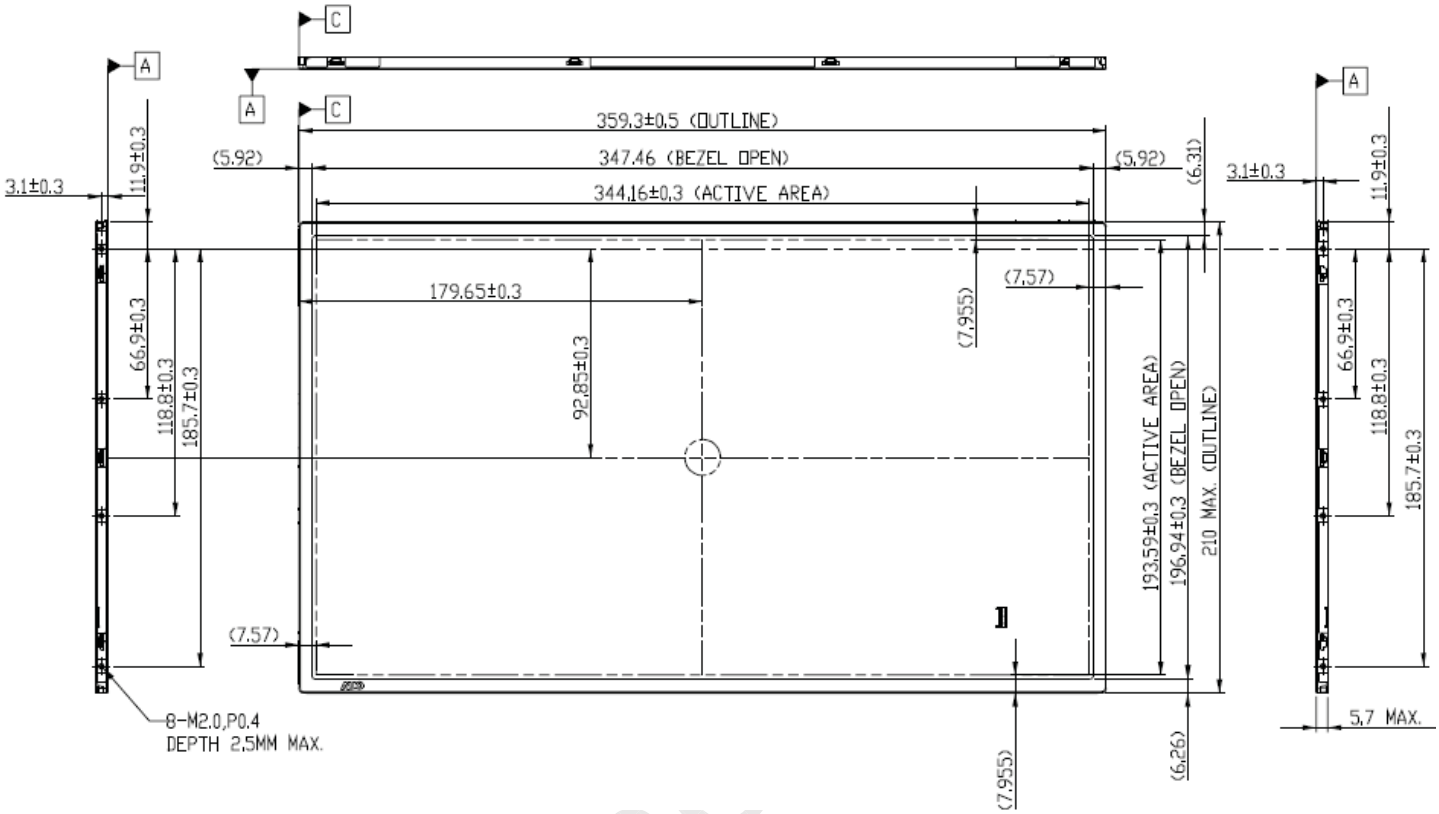
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension



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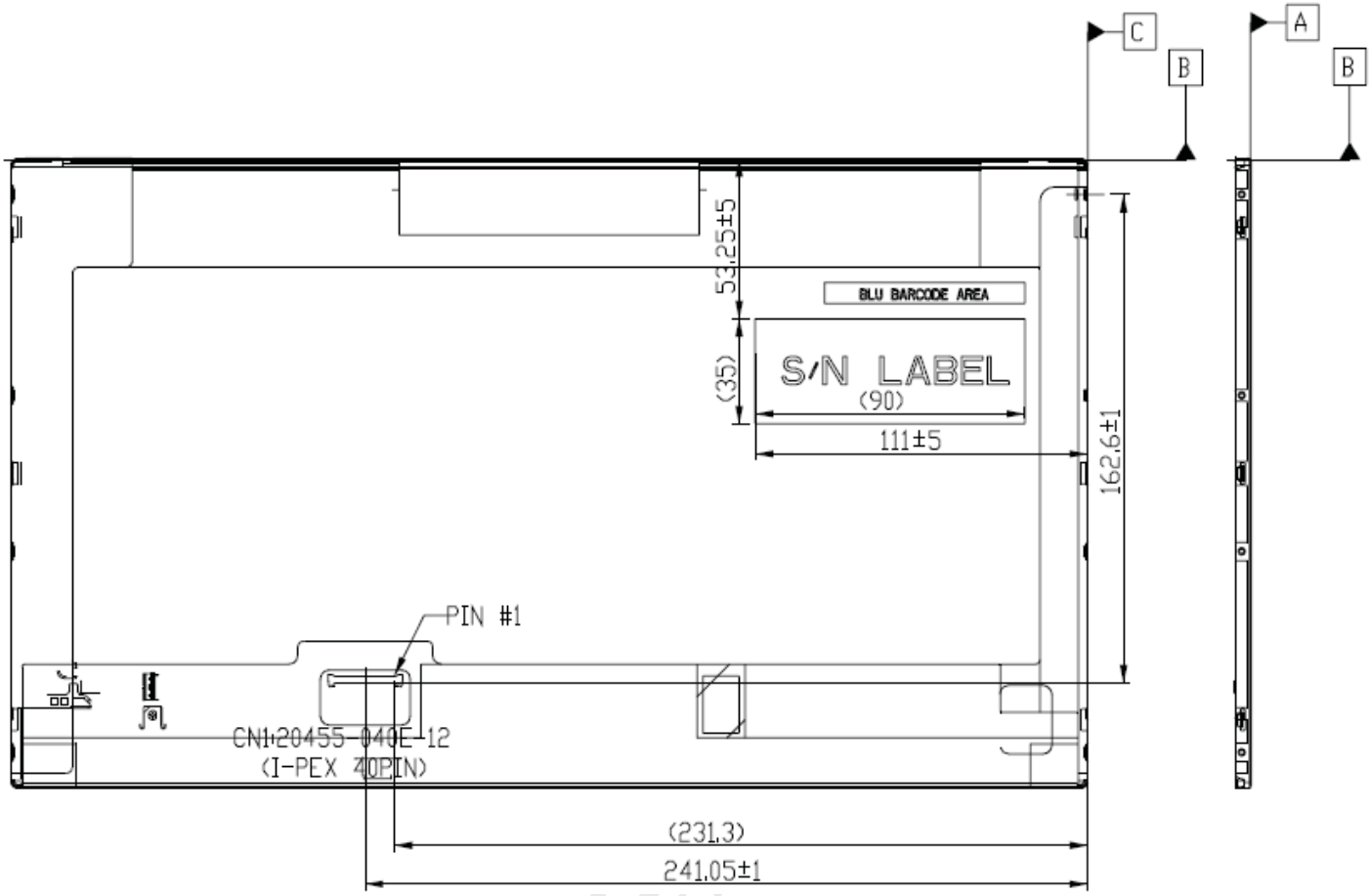
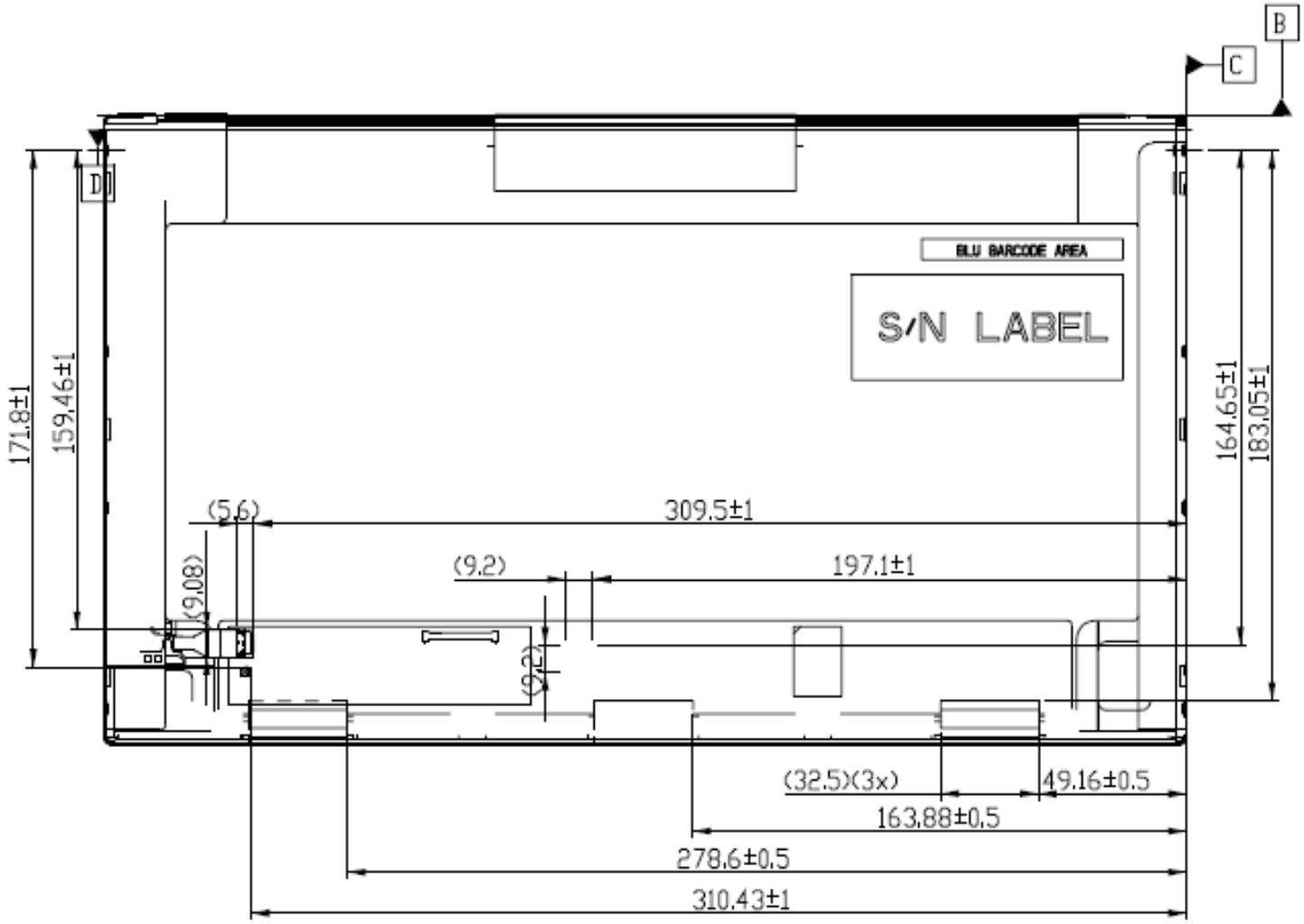
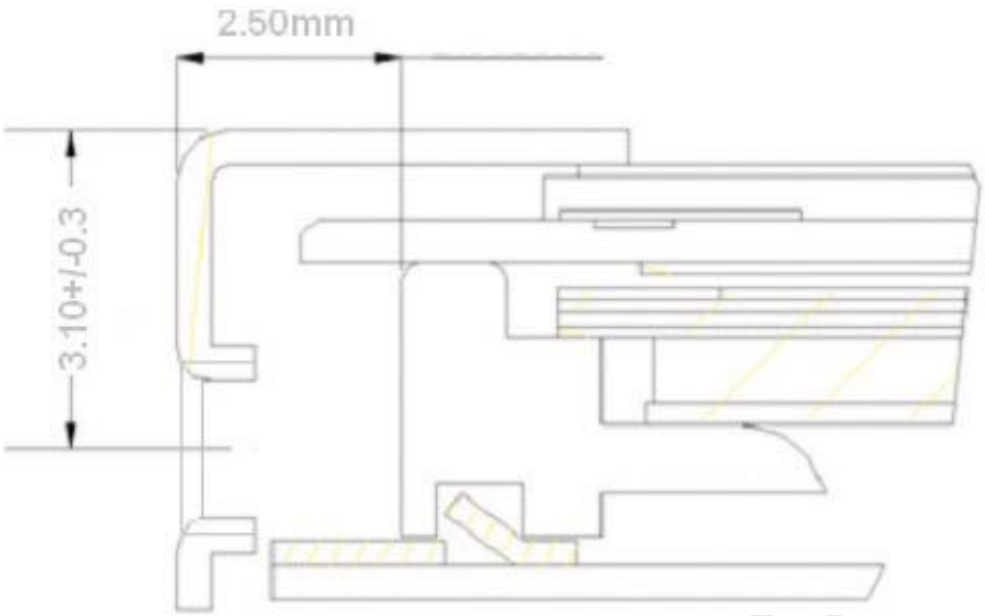
AU OPTRONICS CORPORATION





Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

8.2 Screw Hole Depth and Center Position



9. Shipping and Package

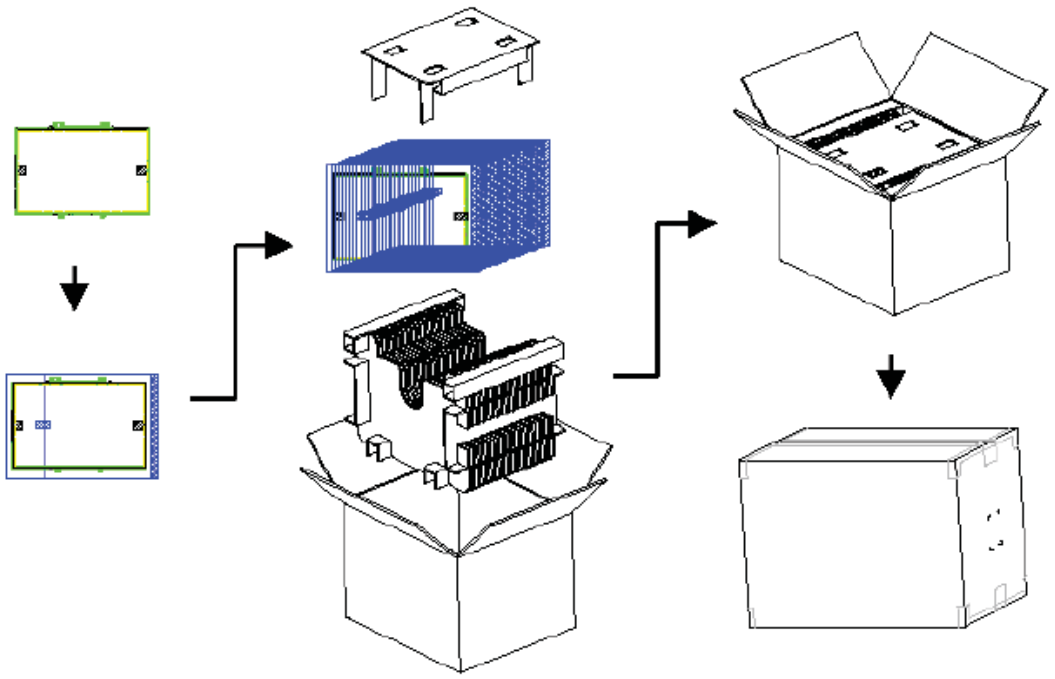
9.1 Shipping Label Format

9.2 Definition of customer PPID Label and Revision Code

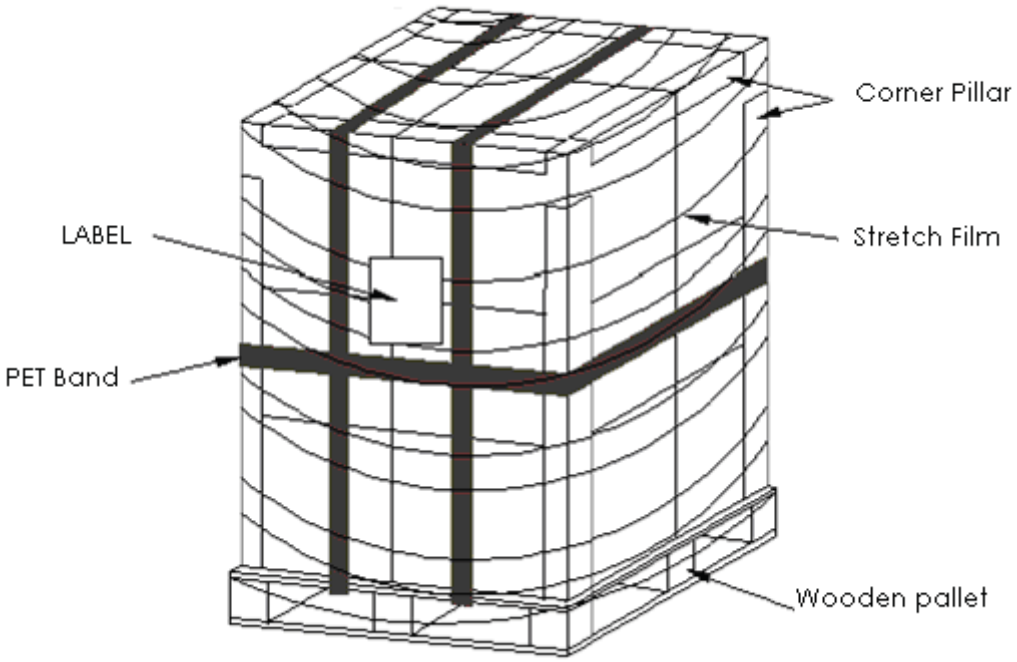
Please refer to the Dell Part identification Label Specification, Number:13190

Build Name(s):	PPID Revision Code(s):
Sub System Test (SST) Working Sample (WS) ENG 2	X00, X01, X02, ..., X0n
Product Test (PT) Engineering Sample (ES) ENG 3	X10, X11, X12, ..., X1n
System Test (ST) Customer Sample (CS) ENG 4	X20, X21, X22, ... X2n
X-Build (XB) Mass Production (MP) ENG 5	A00, A01, A02, ... A0n

9.2. Carton package



9.3 Shipping package of palletizing sequence



10. Appendix: EDID description

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
Header	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	ED	11101101	237
	0B	Panel Supplier Reserved – Product Code	21	00100001	33
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	10	Week of manufacture	04	00000100	4
	11	Year of manufacture	15	00010101	21
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 4	04	00000100	4
Display Parameters	14	Video I/P definition	90	10010000	144
	15	Max H image size = ?? cm (Rounded to cm)	22	00100010	34
	16	Max V image size = ?? cm (Rounded to cm)	13	00010011	19
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
	18	Feature support	02	00000010	2
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	E2	11100010	226
	1A	Blue/White Low bit (BxBy/WxWy)	B5	10110101	181
	1B	Red X Rx = 0.???	9E	10011110	158
	1C	Red Y Ry = 0.???	59	01011001	89
	1D	Green X Rx = 0.???	52	01010010	82
	1E	Green Y Ry = 0.???	99	10011001	153
	1F	Blue X Rx = 0.???	26	00100110	38
	20	Blue Y Ry = 0.???	1E	00011110	30
	21	White X Rx = 0.???	50	01010000	80

	22	White Y Ry = 0.???	54	01010100	84
Established Timing	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer's timings (00h if not used)	00	00000000	0
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1
	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1
	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	78	01111000	120
	37	Pixel Clock/10,000 (MSB)	37	00110111	55
	38	Horizontal Active = ???? pixels (lower 8 bits)	80	10000000	128
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	AE	10101110	174
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	70	01110000	112
	3B	Vertical Active = ??? lines	38	00111000	56
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	32	00110010	50
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64
	3E	Horizontal Sync, Offset (Thfp) = ?? pixels	3C	00111100	60
	3F	Horizontal Sync, Pulse Width = ??? pixels	30	00110000	48
	40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	AA	10101010	170
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	42	Horizontal Image Size = ??? mm	58	01011000	88
	43	Vertical image Size = ??? mm	C2	11000010	194
	44	Horizontal Image Size / Vertical image size	10	00010000	16
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0

	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descripter #2 (=Timing Descripter #1)	48	Pixel Clock/10,000 (LSB)	78	01111000	120
	49	Pixel Clock/10,000 (MSB)	37	00110111	55
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	80	10000000	128
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	0C	00001100	12
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	73	01110011	115
	4D	Vertical Active = xxxx lines	38	00111000	56
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	EA	11101010	234
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	40	01000000	64
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	C8	11001000	200
	51	Horizontal Sync, Pulse Width = xxxx pixels	64	01100100	100
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	AA	10101010	170
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	54	Horizontal Image Size =xxx mm	58	01011000	88
	55	Vertical image Size = xxx mm	C2	11000010	194
	56	Horizontal Image Size / Vertical image size	10	00010000	16
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descripter #3 Dell specific	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1st Character	56	01010110	86

	60	Dell P/N 2nd Character	4E	01001110	78
	61	Dell P/N 3rd Character	4A	01001010	74
	62	Dell P/N 4th Character	56	01010110	86
	63	Dell P/N 5th Character	43	01000011	67
	64	**EDID Revision** **Bit[6:0] See charts below** **Bit[7] 0: X-rev, 1: A-rev**	80	10000000	128
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	35	00110101	53
	68	Manufacturer P/N	36	00110110	54
	69	Manufacturer P/N	48	01001000	72
	6A	Manufacturer P/N	57	01010111	87
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	32	00110010	50
Timing Descripter #4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
	70	Flag	00	00000000	0
	71	Color Management	00	00000000	0
	72	Panel Structure	41	01000001	65
	73	Frame Rate	21	00100001	33
	74	Light Controller Interface and Luminance	9E	10011110	158
	75	Outdoor Features	00	00000000	0
	76	Multi-Media Features	00	00000000	0
	77	Multi-Media Features	00	00000000	0
	78	Special Features #1	00	00000000	0
	79	Special Features #2	02	00000010	2
	7A	Special Features #3	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	F9	11111001	249