Ver 1.2

14-Bit 20MSPS Analog to Digital Converter

Datasheet

Part Number：B1401RH

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Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.1	-	-	
1.1	2017.9	Chapter 7	Modified parameter list	
1.2	2018.3	-	Changed the template	

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1. Unique features

- Power Supply：2.5V
- Sample Frequency：≤20MSPS
- Input Voltage：2V p-p
- Resolution：14bit
- INL：≤±4LSB
- DNL：≤±1 LSB
- SNR：≥61dB
- SINAD：≥60dB
- ENOB：≥9.7bit
- THD：≤-64dB
- Power Dissipation：≤100mW
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV·cm^2/mg

2. General Description

The B1401RH is a14-Bit, radiation hardened, optional sample frequency ADC. The typical sample frequency is 20MSPS and normal below 30MSPS. The power supply of B1401RH is 2.5V and the output driver include 2.5V and 3.3V. The polarization current in the input stage is set by an external resistor (Rpol). When selecting the resistor value, it is possible to optimize the power consumption according to the sampling frequency of the application. Internal and external voltage reference can all be used for B1401RH and maintained a high level of performance.

The B1401RH is based on a pipeline structure and digital error correction to provide excellent static linearity. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. A single clock input is used to control all internal conversion cycles. The digital output data is presented in either straight binary output format or twos complement output data format. An out-of-range (OR) signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

3. Block Diagram

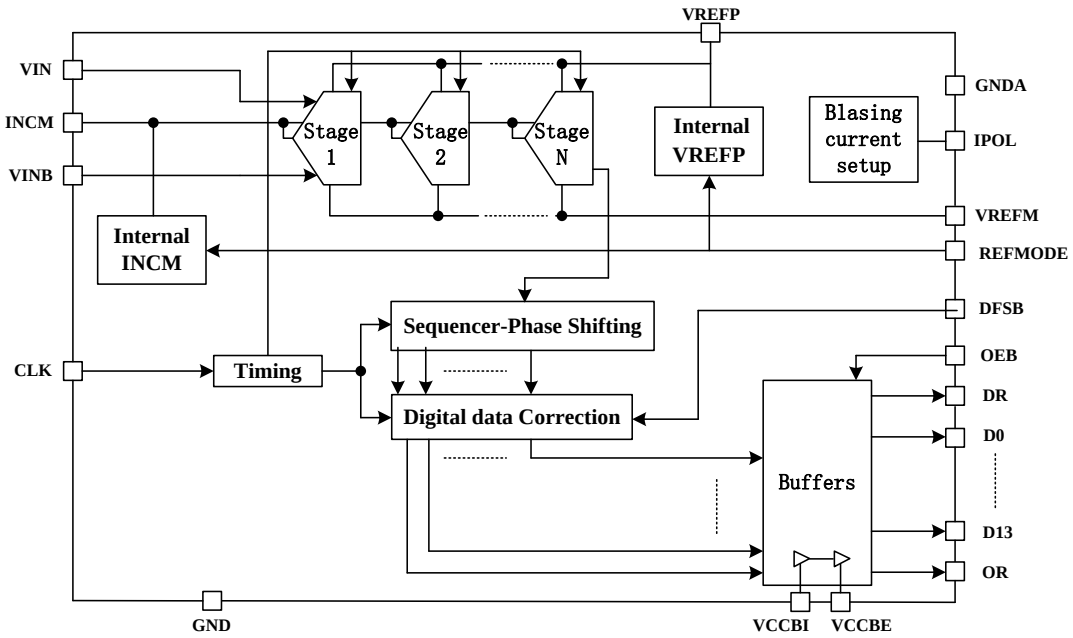

Figure 3-1. Block Diagram

4. Pin Description

The B1401RH is packaged in FP48 package, as is shown in figure 4-1.

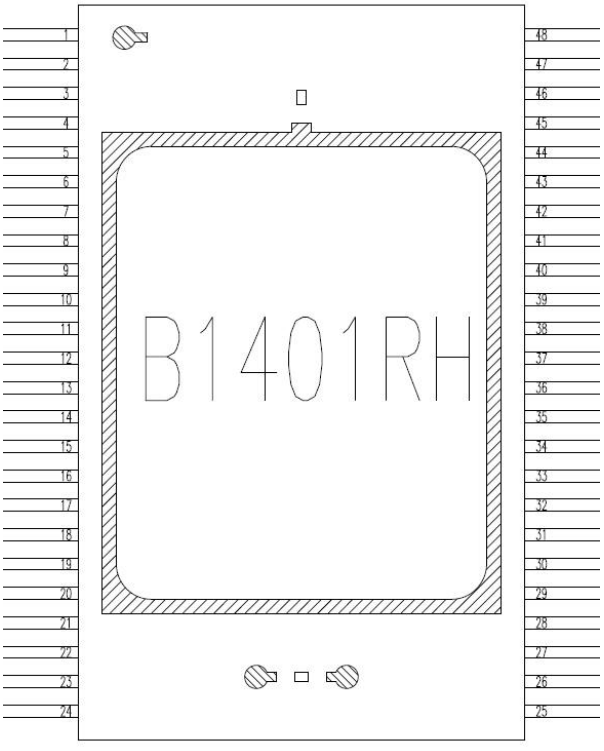

Figure 4-1. B1401RH Top View

Table 4-1. Pin Description

Symbol	Attribute	Description
D0~13	CMOS output(2.5V/3.3V)	Digital output（LSB~MSB）
DR	CMOS output(2.5V/3.3V)	Data ready output
VIN、VINB	1Vpp	Analog input
CLK	2.5 V compatible CMOS input	Clock input
OR	CMOS output(2.5V/3.3V)	Out of range output
REFMODE	2.5 V/3.3 V CMOS input	Ref. mode control input
OEB	2.5 V/3.3 V CMOS input	Output enable input
DFSB	2.5 V/3.3 V CMOS input	Data format select input
IPOL	I	Analog bias current input
VREFP	Can be external or internal	Top voltage reference
VREFM	0V	Bottom voltage reference
INCM	Can be external or internal	Input common mode
GNDBI	0V	Digital buffer ground
GNDBE	0V	Digital buffer ground
AGND	0V	Analog ground
DGND	0V	Digital ground
VCCBE	2.5V/3.3V	Digital buffer power supply
VCCBI	2.5V	Digital buffer power supply
AVCC	2.5V	Analog power supply
DVCC	2.5V	Digital power supply
NC	——	No connection

5. Pin Definition

Table 5-1. The pin configuration

Pin NO.	Symbol	Function	Pin NO.	Symbol	Function
1	GNDBI	Digital buffer ground	25	REFMODE	Ref. mode control input
2	GNDBE	Digital buffer ground	26	OEB	Output enable input
3	VCCBE	Digital buffer power supply	27	DFSB	Data format select input
4	NC	No connection	28	AVCC	Analog power supply
5	NC	No connection	29	AVCC	Analog power supply
6	OR	Out of range output	30	AGND	Analog ground
7	D13(MSB)	Digital output(MSB)	31	IPOL	Analog bias current input
8	D12	Digital output	32	VREFP	Top voltage reference
9	D11	Digital output	33	VREFM	Bottom voltage reference
10	D10	Digital output	34	AGND	Analog ground
11	D9	Digital output	35	VIN	Analog input
12	D8	Digital output	36	AGND	Analog ground
13	D7	Digital output	37	VINB	Inverted analog input
14	D6	Digital output	38	AGND	Analog ground
15	D5	Digital output	39	INCM	Input common mode
16	D4	Digital output	40	AGND	Analog ground

17	D3	Digital output	41	AVCC	Analog power supply
18	D2	Digital output	42	AVCC	Analog power supply
19	D1	Digital output	43	DVCC	Digital power supply
20	D0(LSB)	Digital output(LSB)	44	DVCC	Digital power supply
21	DR	Data ready output	45	DGND	Digital ground
22	VCCBE	Digital buffer power supply	46	CLK	Clock input
23	GNDBE	Digital buffer ground	47	DGND	Digital ground
24	VCCBI	Digital buffer power supply	48	DGND	Digital ground

6. Product Description

6.1 Application Description

6.1.1 Optimizing the power consumption

The polarization current in the input stage is set by an external resistor (Rpol). When selecting the resistor value, it is possible to optimize the power consumption according to the sampling frequency of the application. For this purpose, an external Rpol resistor is placed between the IPOL pin and the analog ground.

The values in Figure 6-1 are achieved with VREFP = 1 V, VREFM = 0 V, INCM = 0.5 V and the input signal is 2 Vpp with a differential DC connection. If the conditions are changed, the Rpol resistor varies slightly.

Figure 6-1 shows the optimum Rpol resistor value to obtain the best ENOB value. It also shows the minimum and maximum values to get good results. ENOB decreases by approximately 0.2 dB when you change Rpol from optimum to maximum or minimum.

If Rpol is higher than the maximum value, there is not enough polarization current in the analog stage to obtain good results. If Rpol is below the minimum, THD increases significantly.

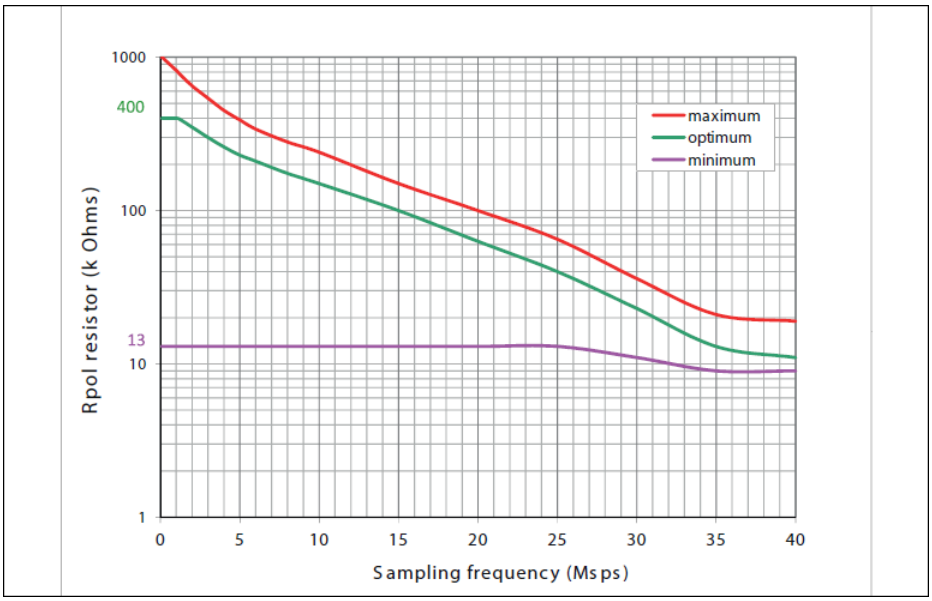

Figure 6-1. Rpol values vs. Fs

Therefore, the total dissipation can be adjusted across the entire sampling range to fulfill the requirements of applications where power saving is critical.

The power consumption depends on the Rpol value and the sampling frequency. In Figure 6-2, it is shown with the internal references disabled (REFMODE = 1) and Rpol defined in Figure 6-1 as the optimum.

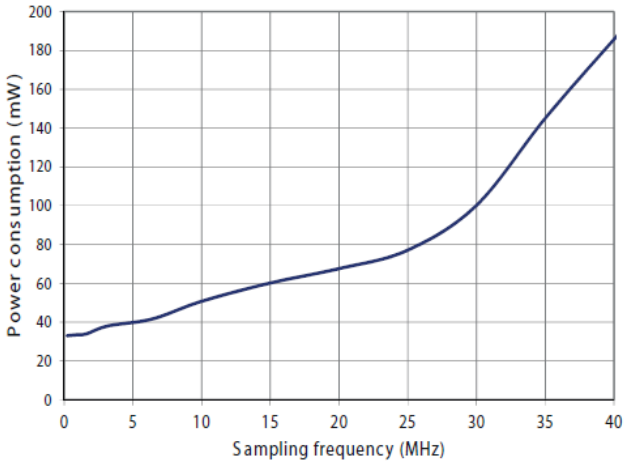

Figure 6-2. Power consumption values vs. Fs with internal references disabled

6.1.2 Driving the analog input

The input frequency can range from DC to tens of MHz.

The input stages (VIN and VINB) have a special design that limits the input amplitude. For each of them, the maximum input voltage is about 1.6 V for low sampling frequencies and less for high sampling frequencies. Low voltage is ground.

Consequently, the maximum input voltage read by the ADC for Single-ended mode is 1.6 V regardless of the VREFP and VREFM voltages.

6.1.2.1 Differential mode

The INCM value must be equal to the medium input voltage value.

In differential mode, high sampling limitation is seen in Figure 6-3.

For all input frequencies, it is mandatory to add a capacitor on the PCB (between VIN and VINB) to cut the HF noise. The lower the frequency, the higher the capacitor.

The full-scale range is twice the difference between VREP and VREFM.

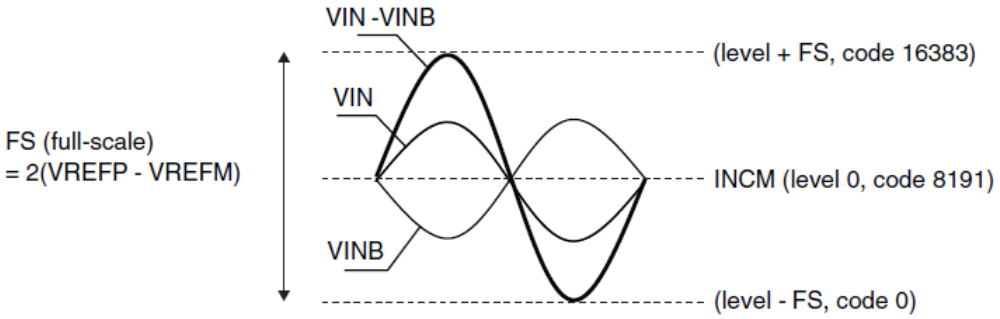

Figure 6-3. Equivalent VIN-VINB(differential input)

Table 6-1. Differential mode output codes

VIN-VINB=	DFSB=1	DFSB=0
+（VREFP-VREFM）	3FFF	1FFF
0	1FFF	3FFF
-（VREFP-VREFM）	0000	2000

The B1401RH is designed to obtain optimum performance when driven on differential inputs with a differential amplitude of two volts peak-to-peak (2 Vpp). This is the result of 1 Vpp on the VIN and VINB inputs in phase opposition.

The B1401RH is specifically designed to meet sampling requirements for intermediate frequency (IF) input signals. In particular, the track-and-hold in the first stage of the pipeline is designed to minimize the linearity limitations as the analog frequency increases.

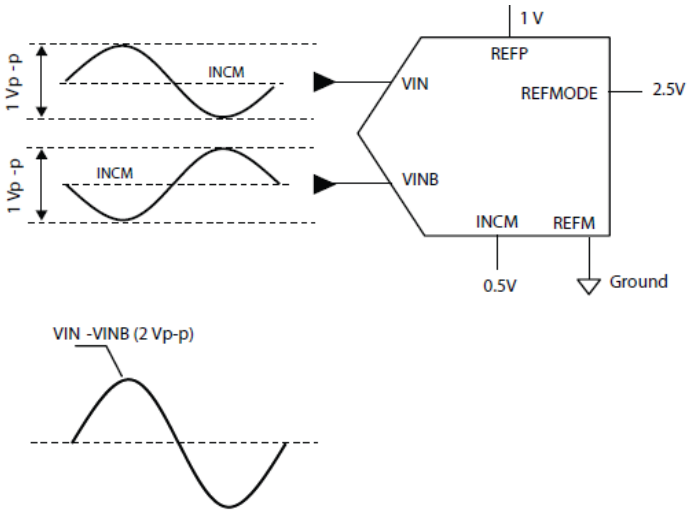

Figure 6-4. 2Vpp differential input

Figure 6-4 shows a differential input solution. The input signal is fed to the transformer's primary, while the secondary drives both ADC inputs. The transformer must be matched with generator output impedance: 50Ω in this case for proper matching with a 50Ω generator. The tracks between the secondary and VIN and VINB pins must be as short as possible.

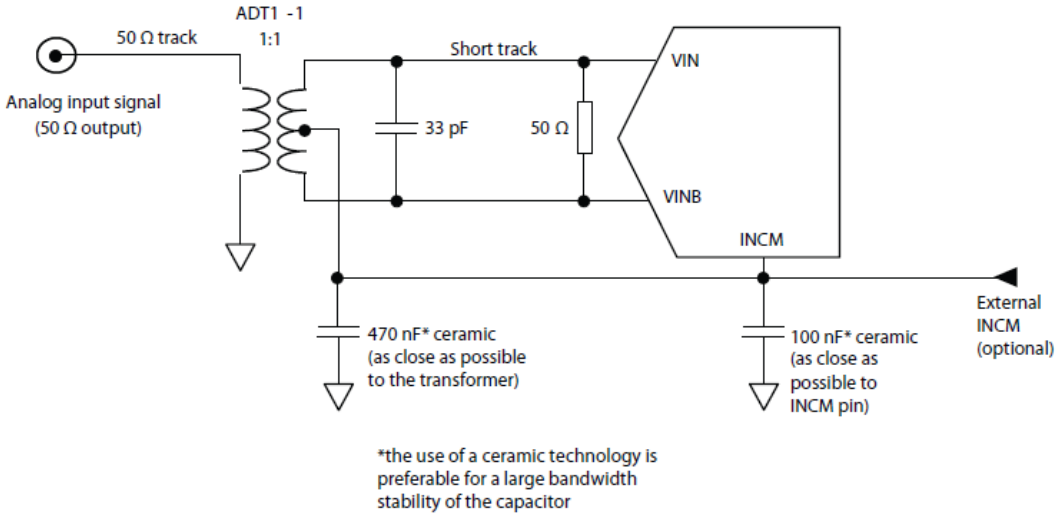

Figure 6-5. Differential implementation using a balun

The input common-mode voltage of the ADC (INCM) is connected to the center tap of the transformer's secondary in order to bias the input signal around the common voltage. The INCM is decoupled to maintain a low noise level on this node. Ceramic technology for decoupling provides good capacitor stability across a wide bandwidth.

6.1.2.2 Single-ended mode

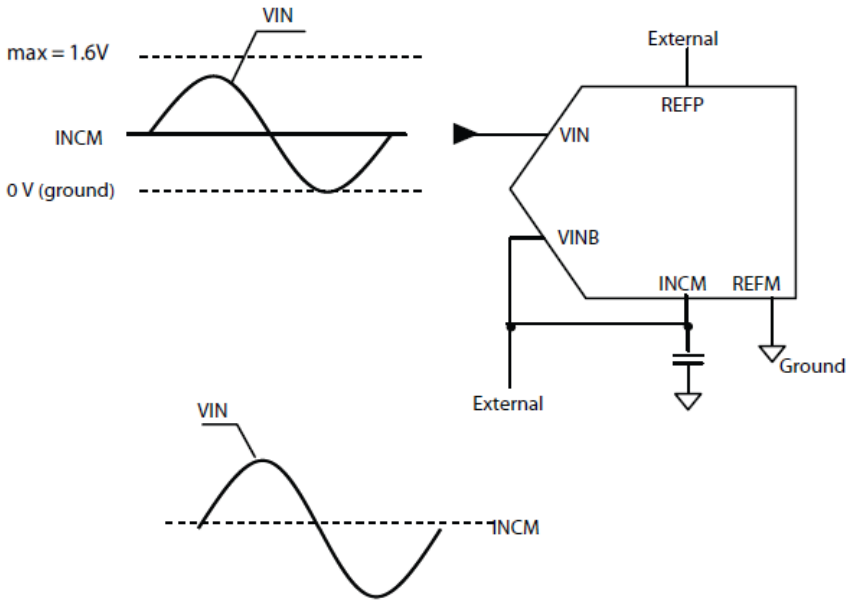

Figure 6-6. Optimized single-ended configuration(DC coupling), external REFP

Table 6-2 Single-ended mode output codes with VINB = INCM

VIN =	DFSB=1	DFSB=0
INCM+（VREFP-VREFM）	3FFF	1FFF
0	1FFF	3FFF
INCM -（VREFP-VREFM）	0000	2000

The B1401RH is designed for use in a differential input configuration. Nevertheless, it can achieve good performance in a single-ended input configuration. In single-ended, performances depend on the input voltage, input frequency, voltage of references and sampling frequency.

VREFP and INCM internal voltage references are not adapted to Single-ended mode.

Some applications may require a single-ended input, which can easily be achieved with the configuration shown in Figure 6-7, Figure 6-8 for AC coupling or Figure 6-16. for DC coupling. However, with this type of configuration, a degradation in the rated performance of the B1401RH may occur compared with a differential configuration. A sufficiently decoupled DC reference should be used to bias the B1401RH inputs. An AC-coupled analog input can also be used and the DC analog level set with a high value resistor R (6kΩ to 100kΩ) connected to a proper DC source. Cin and R behave like a high-pass filter and are calculated to set the lowest possible cut-off frequency.

Each input is limited to about 1.6 V due to the CMOS transistor on the input path.

Voltage can be a bit more or less than 1.6 V depending on temperature, AVCC, and variations from one die to another. This “input limitation” is independent of the VREFP and VREFM values.

The OR pin should rise to 1 when the signal is out of range. However, when VREFP = 0.8 V, VREFM = 0 V, and input voltage max = 1.6 V, the ADC may not read the maximum input voltage due to the CMOS input transistor. Consequently, the OR pin does not rise to 1. To avoid this situation occurring, it is recommended to limit the input amplitude to 1.5 V, VREFP to 0.75 V, and VREFM to 0 V.

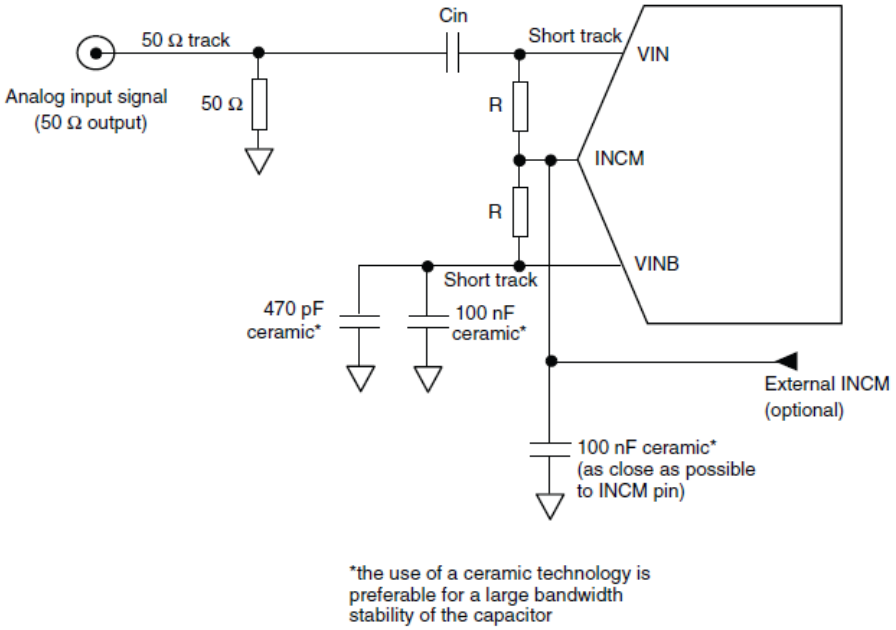

Figure 6-7. AC-coupling single-ended input configuration

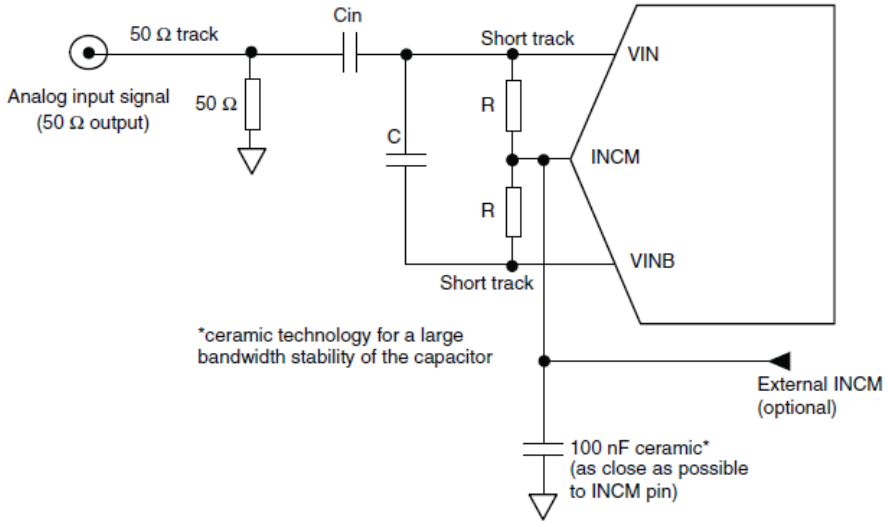

Figure 6-8. AC-coupling single-ended input configuration for low frequencies

The C capacitor is efficient in reducing noise at high frequencies. When coupled

with the resistors, R and C together behave like a high-pass filter. For example, if R = 10 k and C = 33 pF, the cut-off frequency of this filter equals 482 kHz.

6.1.3 Reference connections

6.1.3.1 Internal voltage reference

In standard configuration, the ADC is biased with two internal voltage references: VREFP and INCM. They should be decoupled to minimize low and high frequency noise. When the REFMODE pin is set to 0 both internal voltage references are enabled and they can drive external components or be forced by an external value.

The VREFM pin has no internal reference and must be connected to a voltage reference. It is usually connected to the analog ground.

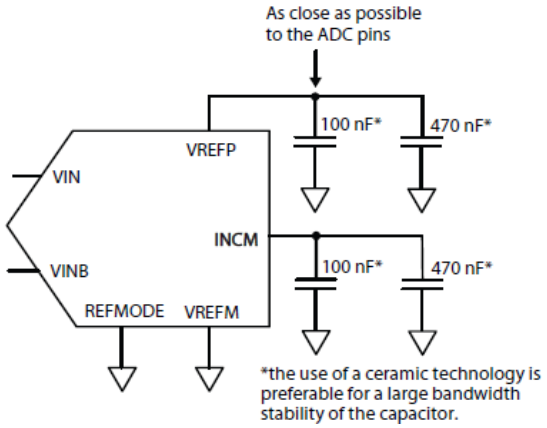

Figure 6-9. Internal voltage reference setting

6.1.3.2 External voltage reference

External voltage references can be used for specific applications requiring better linearity, enhanced temperature behavior, or different voltage values. Internal voltage references are disabled when the REFMODE pin is equal to 1. In this case, external voltage references must be applied to the device.

External voltage references can be applied when internal voltage references are disabled or not.

The external voltage references with the configuration shown in Figure 6-10 and Figure6-11 can be used to obtain optimum performance. Decoupling is achieved by using ceramic capacitors, which provide optimum linearity versus frequency.

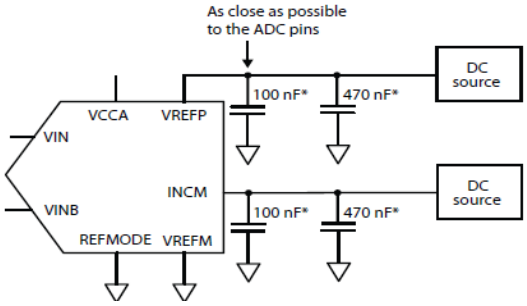

Figure 6-10. External voltage reference setting

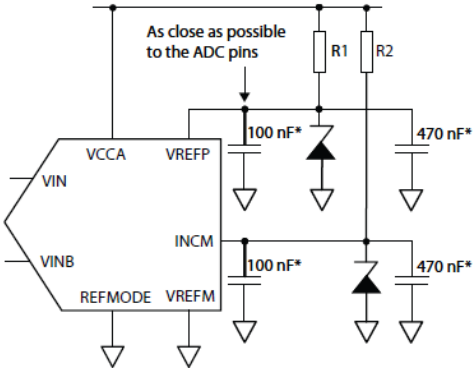

Figure 6-11. Example with zeners

Note：*The use of ceramic technology is preferable to ensure large bandwidth stability of the capacitor*

In multi-channel applications, the high impedance input (when REFMODE = 1) of the references allows one to drive several ADCs with only two voltage reference devices.

In Differential mode the voltage of the analog input common mode (INCM) should be around VREFP/2. Higher levels introduce more distortion.

6.1.4 Clock input

The quality of the converter very much depends on the accuracy of the clock input in terms of jitter. The use of a low-jitter, crystal-controlled oscillator is recommended.

The following points should also be considered.

● The clock's power supplies must be independent of the ADC's output supplies to avoid digital noise modulation at the output.

● When powered-on, the circuit needs several clock periods to reach its normal operating conditions.

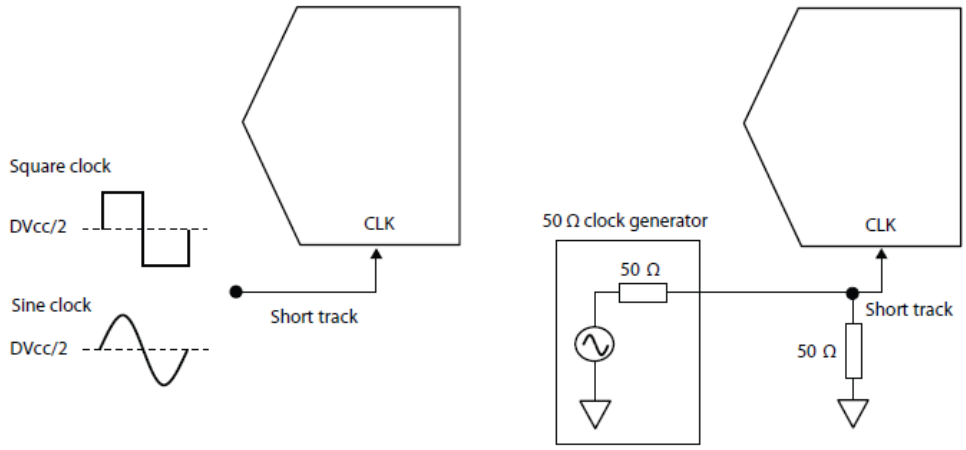

Figure 6-12. Clock input schematic

The signal applied to the CLK pin is critical to obtain full performance from the B1401RH. Below 10 MHz, the sine clock does not have transition times fast enough to achieve good performances. It is recommended to use a square signal with fast transition times and to place proper termination resistors as close as possible to the device.

The sampling instant is determined by the clock signal's rising edge. The jitter associated with this instant must be as low as possible to avoid SNR degradation on fast moving input signals. To make sure any error is less than 0.5 LSB, the total jitter Tj must satisfy the following condition for a full-scale input signal.

$$T_j < \frac{1}{\pi \cdot F_{in} \cdot 2^{n+1}}$$

For example, the total jitter with a 14-bit resolution for a 10 MHz full-scale input should be no more than 1 picosecond (rms).

In most cases, the clock signal jitter is responsible for noise. Therefore, you must pay attention to the clock signal when fast signals are acquired with a low frequency clock.

6.1.5 Operating modes

Extra functionalities are provided to simplify the application board as much as possible. The operating modes offered by the B1401RH are described in Table 6-3.

Table 6-3. B1401RH operating modes

Inputs			Outputs		
Analog input differential amplitude	DFSB	OEB	OR	DR	MSB
VIN- VINB above maximum range	H	L	H	CLK	D13

	L	L	H	CLK	D13
VIN- VINB below minimum range	H	L	H	CLK	D13
	L	L	H	CLK	D13
VIN- VINB with in range	H	L	L	CLK	D13
	L	L	L	CLK	D13
X	X	H	HZ(High impedance)	HZ	HZ

6.1.5.1 Digital Inputs

Data format select bit (DFSB): when set to low level (VIL), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing. When set to high level (VIH), DFSB provides standard binary output coding.

Output enable bit (OEB): when set to low level (VIL), all digital outputs remain active. When set to high level (VIH), all digital output buffers are in a high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short Ton delay. This feature enables the chip select of the device. Figure 6-13.

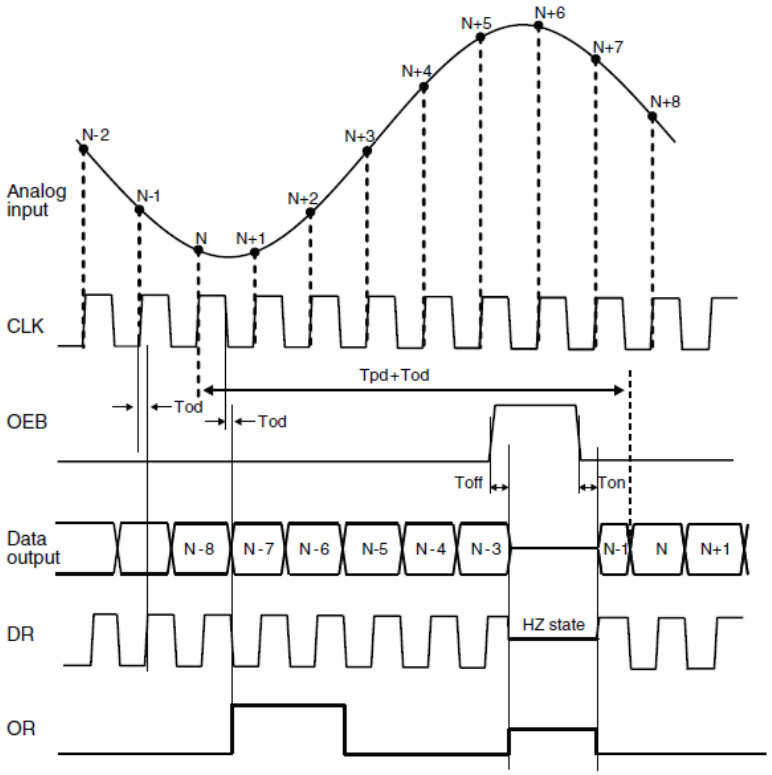

Figure 6-13. Timing diagram

The input signal is sampled on the rising edge of the clock while the digital outputs are synchronized on the falling edge of the clock. The duty cycles on DR and

CLK are the same.

The rising and falling edges of the OR pin are synchronized with the falling edge of the DR pin.

Reference mode control (REFMODE): this allows the internal or external settings of the voltage references VREFP and INCM. REFMODE = 0 for internal references, REFMODE = 1 for external references (and disables both references VREFP and INCM).

6.1.5.2 Digital outputs

Out of range (OR): this function is implemented on the output stage in order to set an "out-of-range" flag whenever the digital data is over the full-scale range. Typically, there is a detection of all data at '0' or all data at '1'. It sets an output signal OR, which is in a low level state (VOL) when the data stays within the range, or in a high-level state (VOH) when the data read by the ADC is out of range.

Data ready (DR): the Data Ready output is an image of the clock being synchronized on the output data (D0 to D13). This is a very helpful signal that simplifies the synchronization of the measurement equipment of the controlling DSP. Like all other digital outputs, DR goes into high impedance when OEB is set to a high level, as shown in Figure 6-13: Timing diagram.

6.1.5.3 Digital output load considerations

The features of the internal output buffers limit the maximum load on the digital data output. In particular, the shape and amplitude of the Data Ready signal, toggling at the clock frequency, can be weakened by a higher equivalent load.

In applications that impose higher load conditions, it is recommended to use the falling edge of the master clock instead of the Data Ready signal. This is possible because the output transitions are internally synchronized with the falling edge of the clock.

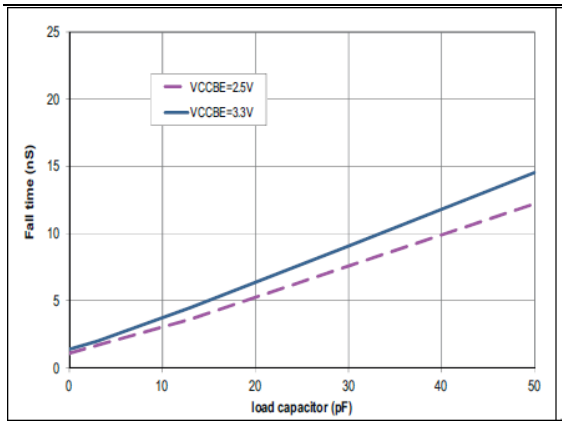

Figure 6-14. Output buffer fall time

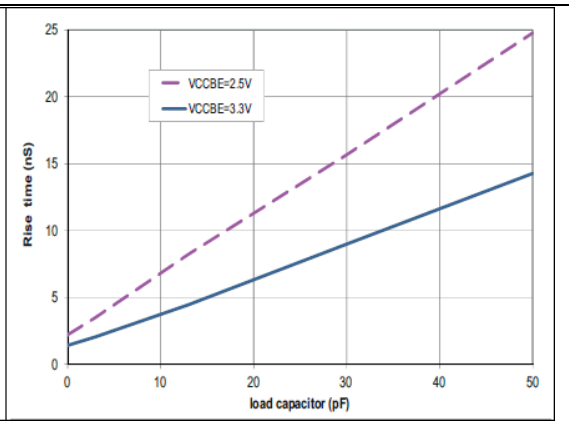

Figure 6-15. Output buffer rise time

6.1.6 PCB layout precautions

- The use of dedicated analog and digital ground planes on the PCB is recommended for high-speed circuit applications to provide low parasitic inductance and resistance. AGND is connected to the analog ground plane and DGND, GNDBI, GNDBE are connected to the digital ground plane.
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest-possible routing tracks. One way to reduce the capacitive load is to remove the ground plane under the output digital pins and layers at high sampling frequencies.
- The separation of the analog signal from the clock signal and digital outputs is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high-frequency bypassing and reduce harmonic distortion.
- All leads must be as short as possible, especially for the analog input, so as to decrease parasitic capacitance and inductance.
- Choose the smallest-possible component sizes (SMD).

6.2 Characterization Curves/Plots

Setup

- AVCC=DVCC=VCCBI=VCCBE=2.5V
- VREFM=0V
- REFMODE=0(internal reference are disabled)
- VIN=full scale-1dB，differential input
- Tamb=25 ℃
- A square clock is applied

- Unless other test conditions are specified

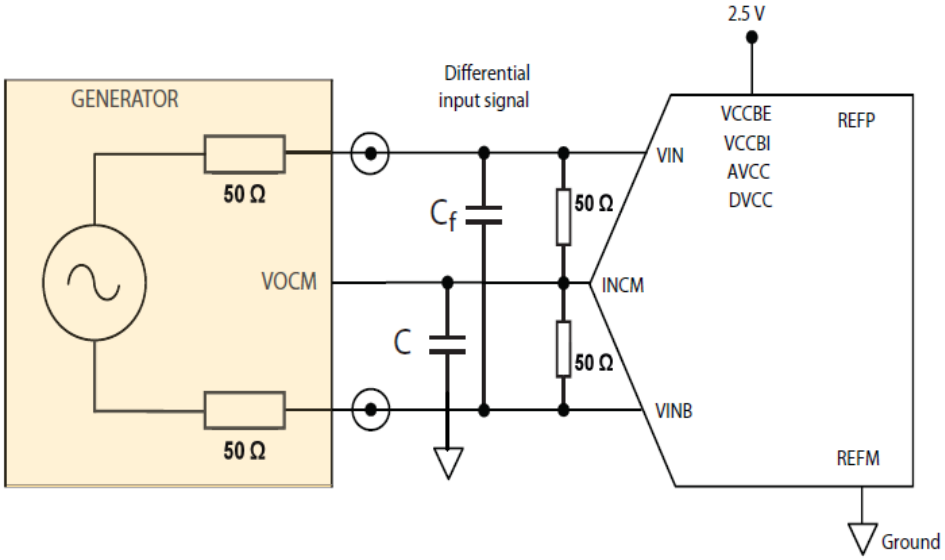

Figure 6-16. Differential configuration

Cf is a filter capacitor to cut the HF noise. Its value is 10 nF for input frequencies equal to or below 20 kHz. The value of the capacitor is divided by two when the input frequency is multiplied by 2.

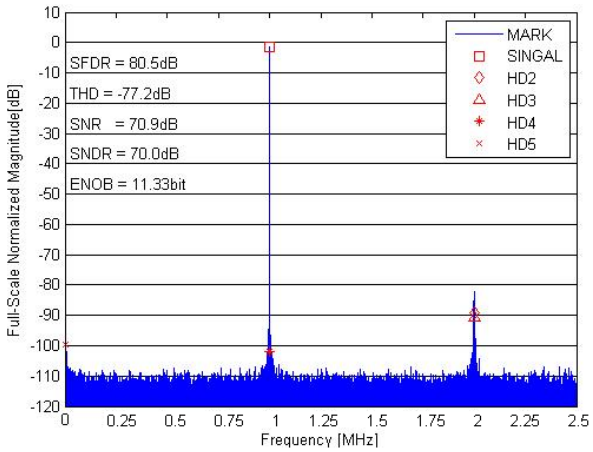

Figure 6-17. FFT vs. sample frequency = 5MSPS, input frequency = 1MHz

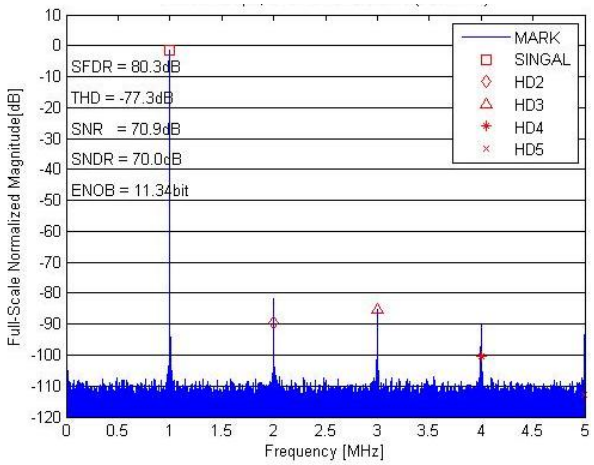

Figure 6-18. FFT vs. sample frequency = 10MSPS, input frequency = 1MHz

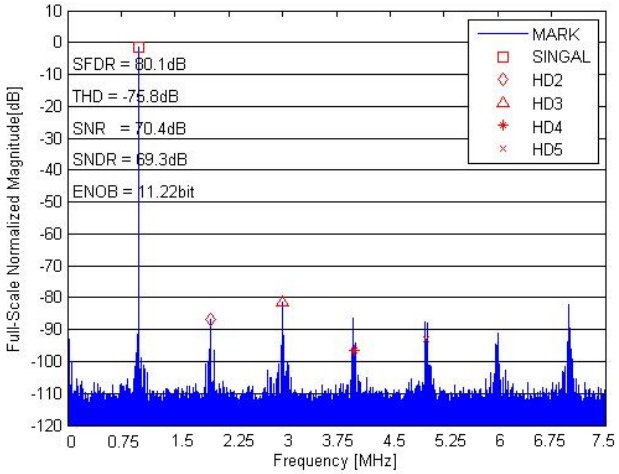

Figure 6-19. FFT vs. sample frequency = 15MSPS, input frequency = 1MHz

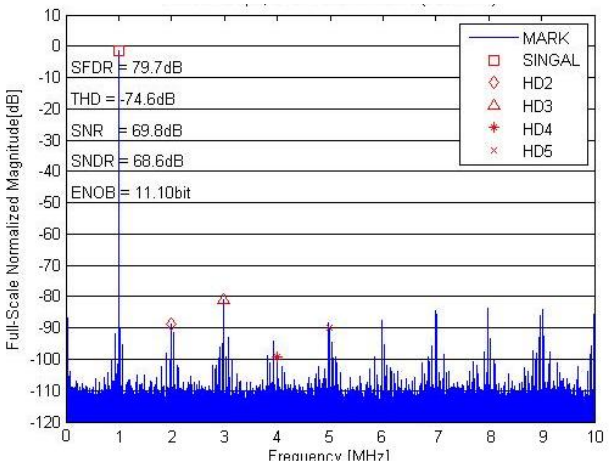

Figure 6-20. FFT vs. sample frequency = 20MSPS, input frequency = 1MHz

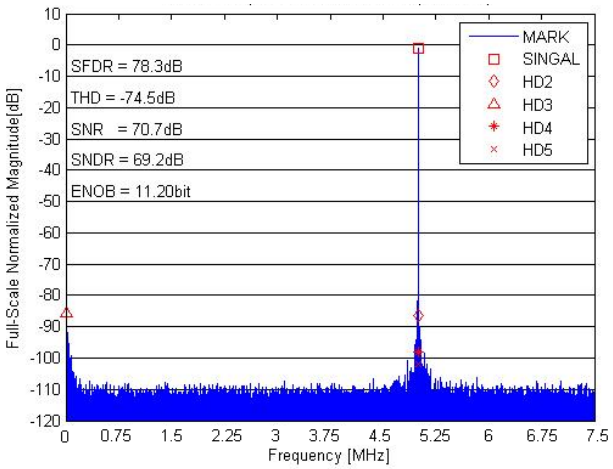

Figure 6-21. FFT vs. sample frequency = 15MSPS, input frequency = 5MHz

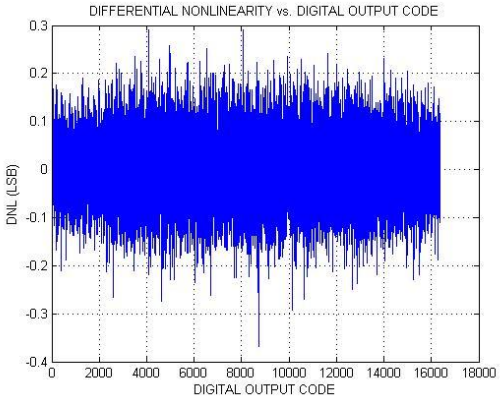

Figure 6-22. DNL vs. differential input

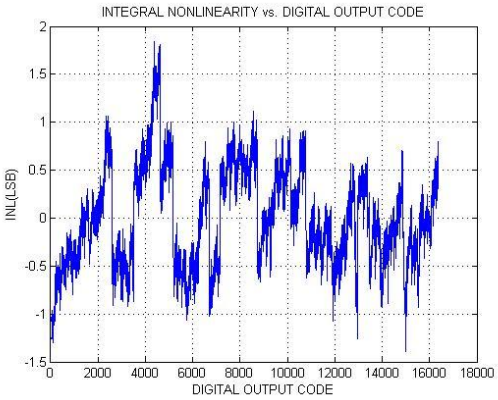

Figure 6-23. INL vs. differential input

6.3 Storage Condition

The warehouse environment of B1401RH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

Table 6-4. The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

6.4 Absolute maximum ratings

a) Analog supply voltage(AVCC) 3.3V

b) Digital supply voltage (DVCC) 3.3V

c) Digital buffer supply voltage (VCCVBI) 3.3V

d) Digital buffer supply voltage（VCCBE）.....3.6V

e) Digital DC input voltage range.....–0.3V ~ (VCCBE+ 0.3V)

f) Lead welding temperatrue（T_H）..... 260 ℃(10s)

g) Junction temperatrue（T_J） ..... 150 ℃

h) Storage temperatrue（Tstg）..... –65 ℃ ~ 150 ℃

6.5 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVCC	Analog supply voltage	2.3	2.5	2.7	V
DVCC	Digital supply voltage	2.3	2.5	2.7	V
VCCBI	Digital buffer supply voltage	2.3	2.5	2.7	V
VCCBE	Digital buffer supply voltage	2.3	2.5	3.4	V
VINCM	Forced common mode voltage	0.2	0.5	1.1	V
VREFP	Forced top voltage reference	0.5	1	1.3	V
VREFM	Bottom external reference voltage	0	0	0.5	V
Operation Temperature	T_A	-55℃	25℃	+125℃	℃

6.6 Radiation hardened performance

a) Total Ionizing Dose ≥ 100 Krad(Si)

b) SEL threshold ≥ 75 MeV·cm^2/mg

7. Electrical Characteristic

Table 7-1. Electrical Characteristic

Parameter	Symbol	Conditions (Unless otherwise specified,-55℃≤ T_A ≤ 125℃ AVCC=DVCC=VCCBI=VCCBE=2.5V, VREFM=0V)	Min	Max	Unit
Resolution	RES		14		bits
Integral non-linearity	E_L		-4.0	4.0	LSB
Differential non-linearity	E_{DL}		-1.0	1.0	LSB
Top internal reference voltage	VREFP	$V_{REFMODE}$ = 0	0.7	1.0	V

Parameter	Symbol	Conditions (Unless otherwise specified,-55℃≤ T_A ≤ 125℃ AVCC=DVCC=VCCBI=VCCBE=2.5V, VREFM=0V)	Min	Max	Unit
Input common mode voltage	VINCM	$V_{REFMODE}$ = 0	0.35	0.55	V
Logic"1"voltage	V_{IH}		1.875	—	V
Logic"0"voltage	V_{IL}		—	0.625	V
Logic"1"voltage	V_{OH}	IOH =-10uA	2.25	—	V
Logic"0"voltage	V_{OL}	IOL =10uA	—	0.25	V
High impedance leakage current	I_{OZ}	OBE set to V_{IH}	-15	15	uA
Power Dissipation	P_W	f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, input range = 2V, V_{IN} = -1dBFS, external reference, $V_{REFMODE}$ = 1,VREFP = 1V, VINCM = 0.5V	—	100	mW
Signal to noise radio	SNR	f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, V_{IN}=-1dBFS, internal reference, $V_{REFMODE}$=0	61	—	dB
		f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, nput range = 2V, V_{IN}=-1dBFS, external reference, $V_{REFMODE}$ = 1,VREFP = 1V, VINCM = 0.5V	61	—	dB
Signal to noise and distortion	SINAD	f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, V_{IN}=-1dBFS, internal reference, $V_{REFMODE}$=0	60	—	dB
		f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, nput range = 2V, V_{IN}=-1dBFS, external reference, $V_{REFMODE}$ = 1,VREFP = 1V, VINCM = 0.5V	60	—	dB
Total harmonic distortion	THD	f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, V_{IN}=-1dBFS, internal reference, $V_{REFMODE}$=0	—	-64	dB
		f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, nput range = 2V, V_{IN}=-1dBFS, external reference, $V_{REFMODE}$ = 1,VREFP = 1V, VINCM = 0.5V	—	-64	dB
Spurious free dynamic range	SFDR	f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, V_{IN}=-1dBFS, internal reference, $V_{REFMODE}$=0	65	—	dBFS
		f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, nput range = 2V, V_{IN}=-1dBFS, external reference, $V_{REFMODE}$ = 1,VREFP = 1V, VINCM = 0.5V	65	—	dBFS
Effective number of bits	ENOB	f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, V_{IN}=-1dBFS, internal reference, $V_{REFMODE}$=0	9.7	—	Bit

Parameter	Symbol	Conditions (Unless otherwise specified,-55℃≤ T_A ≤ 125℃ AVCC=DVCC=VCCBI=VCCBE=2.5V, VREFM=0V)	Min	Max	Unit
		f_{SAMPLE}=20MSPS, f_{IN}=5MHz, differential input, nput range = 2V, V_{IN}=-1dBFS, external reference, $V_{REFMODE}$ = 1,VREFP = 1V, VINCM = 0.5V	9.7	—	Bit
Data output delay (Figure 6-13)	T_{od}	Fall of clock to data valid	2	10	ns
Convert frequency	Fs		1.5	20	MHz

Note 1 : The typical value is test in T_A = 25℃.

Note 2 : If the duty cycle does not equal 50%: T_{pd} = 7 cycles + CLK pulse width.

8. Applications Field

- Telecommunication
- Receiver
- Cellular base station
- Frequency analysis
- Image – forming system
- ATE

9. Package Outline Dimensions

The B1401RH is packaged in FP48 package, as is shown in figure 9-1：

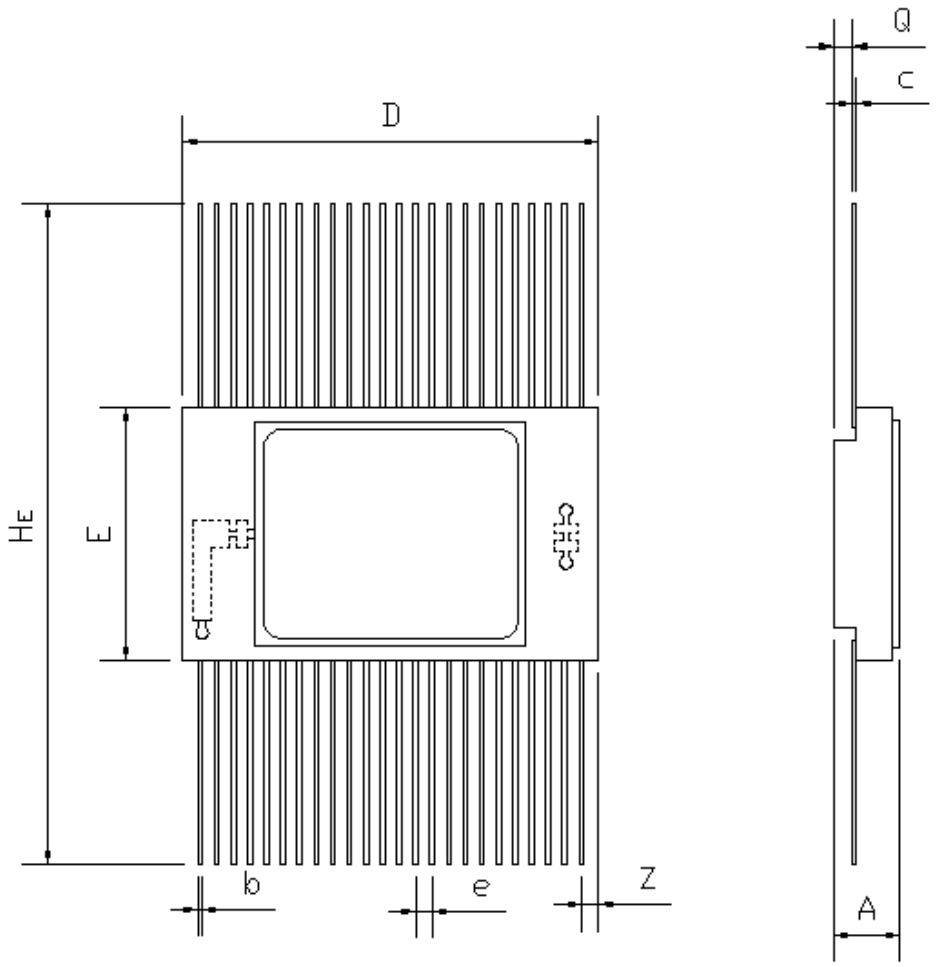

Figure 9-1. Outline dimensions

Symbol	Data（Units：mm）		
	Min	Typ	Max
A	2．02	—	2.74
b	0.20	—	0.31
c	0.10	—	0.20
e	—	0．635	—
D	15.675	—	16.075
E	9．452	—	9．852
H_E	13．70	—	25.50
Q	0.13	—	0.55
Z	—	—	1.27

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