AmZ8148

Chip Select Address Decoder With Acknowledge

DISTINCTIVE CHARACTERISTICS

- One-of-Eight Decoder provides eight chip select outputs
- Acknowledge output responds to enables and acknowledge input command
- Open-collector Acknowledge output for wired-OR application
- Inverting and non-inverting enable inputs for upper address decoding
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

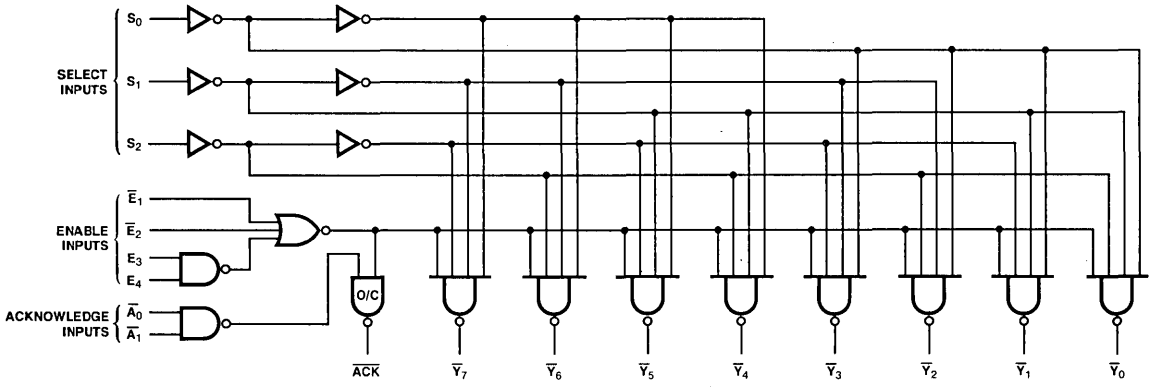
The AmZ8148 Address Decoder combines a three-line to eight-line decoder with four qualifying enable inputs (two active HIGH and two active LOW) and the acknowledge output required for "ready" or "wait state" control of all popular MOS microprocessors.

The acknowledge output, ACK, is active LOW and responds to the combination of all enables and an acknowledge active, input command.

The eight chip select outputs are individually active LOW in response to the combination of all enables active and the corresponding 3-bit input code at the S inputs.

The AmZ8148 is intended for chip select decoding in small, medium or large systems where multiple chip selects must be generated and address space must be allocated conservatively.

LOGIC DIAGRAM



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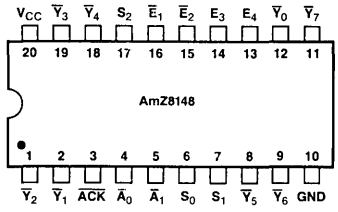
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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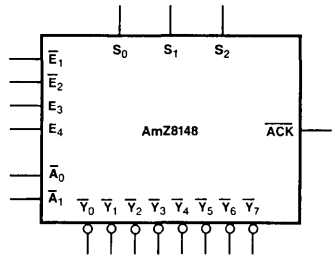
LOGIC SYMBOL



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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V					0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	20	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. TEST CONDITIONS: S_0 = S_1 = S_2 = $\overline{E}_1$ = $\overline{E}_2$ = GND: $\overline{A}_0$ = $\overline{A}_1$ = E_3 = E_4 = 4.5V.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	S_i to $\overline{Y_i}$ (Three Level Delay)		14	20	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			19	27	ns	
t_{PLH}	S_i to Y_i (Two Level Delay)		13	18	ns	
t_{PHL}			15	21	ns	
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to $\overline{Y_i}$		13	18	ns	
t_{PHL}			16	23	ns	
t_{PLH}	E_3, E_4 to $\overline{Y_i}$		15	21	ns	
t_{PHL}			19	27	ns	
t_{PLH}	$\overline{A_i}$ to ACK		25	35	ns	
t_{PHL}			16	22	ns	
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to $\overline{ACK}$		29	40	ns	
t_{PHL}			25	35	ns	
t_{PLH}	E_3, E_4 to $\overline{ACK}$		29	40	ns	
t_{PHL}			25	35	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		COM'L		MIL			
		T_A = 0°C to +70°C V_{CC} = 5.0V ±5%		T_A = −55°C to +125°C V_{CC} = 5.0V ±10%			
Parameters	Description	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{PLH}	S_i to Y_i (Three Level Delay)		27		30	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			34		36	ns	
t_{PLH}	S_i to Y_i (Two Level Delay)		23		25	ns	
t_{PHL}			28		31	ns	
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to $\overline{Y_i}$		23		25	ns	
t_{PHL}			29		31	ns	
t_{PLH}	E_3, E_4 to $\overline{Y_i}$		27		28	ns	
t_{PHL}			34		36	ns	
t_{PLH}	$\overline{A_i}$ to ACK		45		45	ns	
t_{PHL}			31		35	ns	
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to $\overline{ACK}$		45		45	ns	
t_{PHL}			39		40	ns	
t_{PLH}	E_3, E_4 to $\overline{ACK}$		45		45	ns	
t_{PHL}			39		40	ns	

DEFINITION OF FUNCTIONAL TERMS

S_0, S_1, S_2 Three-line to eight-line chip select decoder inputs.

$\overline{E}_1$, $\overline{E}_2$ The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled, and forces $\overline{ACK}$ HIGH.

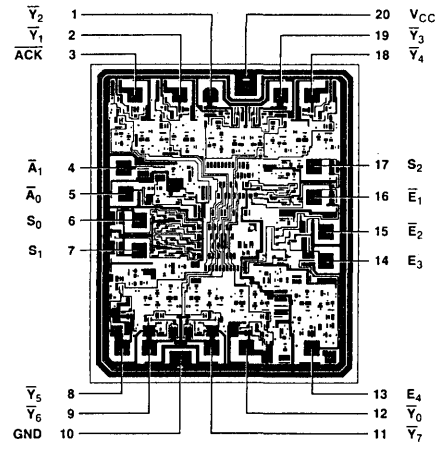
E_3, E_4 The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited, and forces $\overline{ACK}$ HIGH.

A_0, A_1 The acknowledge inputs, A_0 and A_1, are active LOW inputs used as conditions for an active LOW output at the acknowledge, $\overline{ACK}$, output.

$\overline{ACK}$ The acknowledge output, $\overline{ACK}$, is an active LOW output used to signal the microprocessor that specific devices have been selected. $\overline{ACK}$ goes LOW only when $\overline{E}_1$ and $\overline{E}_2$ are LOW, E_3 and E_4 are HIGH and $\overline{A}_0$ or $\overline{A}_1$ is LOW.

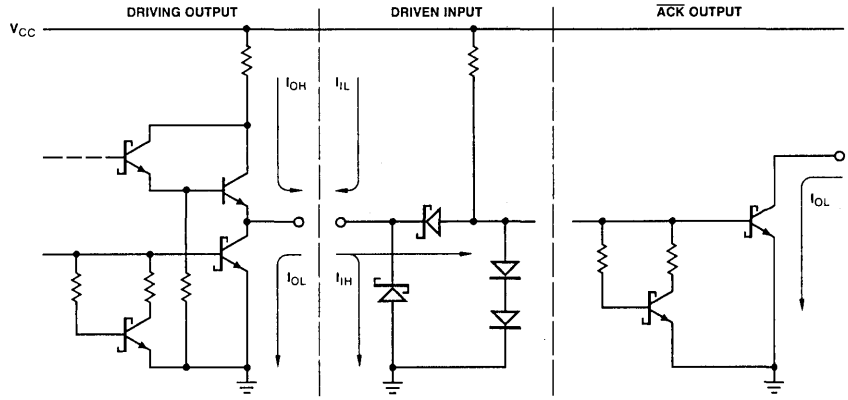
$\overline{Y}_i$ The eight active LOW chip select outputs.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.081" X 0.096"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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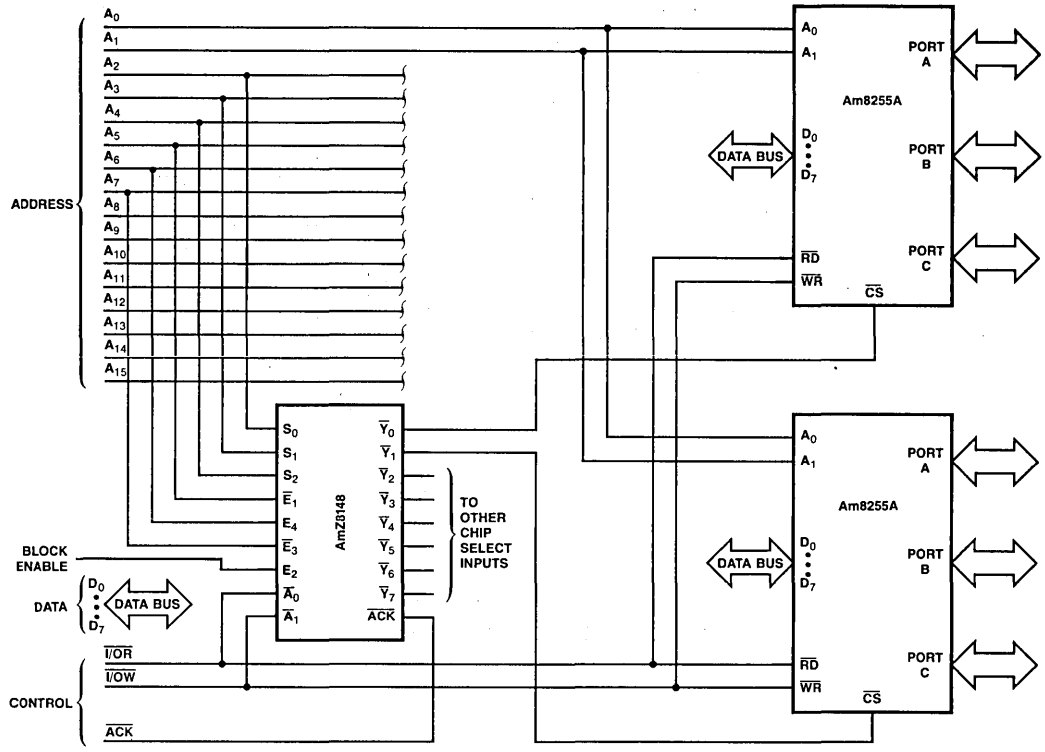
APPLICATION DIAGRAM



FUNCTION TABLES

CHIP SELECT OUTPUTS Y_i

S_2	S_1	S_0	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H	H
H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H	L
X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	X	H	H	H	H	H	H	H	H
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H

ACKNOWLEDGE OUTPUT $\overline{ACK}$

$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{A}_0$	$\overline{A}_1$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L