Am9147

4096 x 1 Static R/W Random Access Memory

PRELIMINARY

2

DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 55ns maximum
- 4K x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power-down when deselected
- Low power dissipation
  - Am9147: 880mW active, 110mW power down
- Standard 18-pin, .300 inch dual in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- No power-on current surge
- Polyplanar™ technology

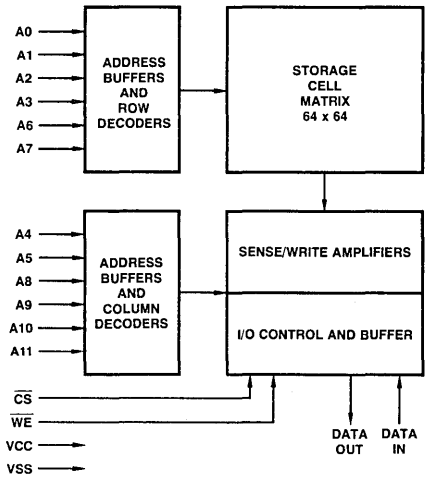
GENERAL DESCRIPTION

The Am9147 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single +5 volt power supply is required. When deselected (CS ≥ VIH), the Am9147 automatically enters a power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the Same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



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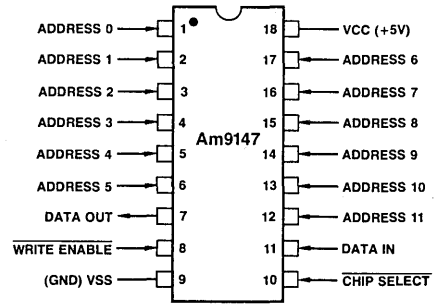
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ORDERING INFORMATION

	Am9147-55	Am9147-70
Maximum Access Time (ns)	55	70
Maximum Active Current (mA)	180	160
Maximum Standby Current (mA)	30	20

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
VCC with Respect to VSS	−0.5 to +7.0V
All Signal Voltages with Respect to VSS	−1.5 to +7.0V
Power Dissipation (Package Limitation)	1.2W
DC Output Current	20mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC	Part Number	Ambient Temperature	VSS	VCC
Am9147-55 PC/DC Am9147-70 PC/DC	0°C ≤ T_A ≤ +70°C	0V	+5.0V ± 10%	Am9147DM	−55°C ≤ T_A ≤ +125°C	0V	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over operating range (Note 6)

Parameter	Description	Test Conditions		Am9147-55 Min	Am9147-55 Typ (Note 1)	Am9147-55 Max	Am9147-70 Min	Am9147-70 Typ (Note 1)	Am9147-70 Max	Units
IOH	Output High Current	VOH = 2.4V	VCC = 4.5V	−4			−4			mA
IOL	Output Low Current	VOL = 0.4V	T_A = 70°C	12			12			mA
			T_A = 125°C							
VIH	Input High Voltage			2.0		6.0	2.0		6.0	Volts
VIL	Input Low Voltage			−1.0		0.8	−1.0		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC				10			10	μA
IOZ	Output Leakage Current	GND ≤ VO ≤ VCC Output Disabled	T_A = 125°C							μA
			T_A = 70°C	−50		50	−50		50	
IOS	Output Short Circuit Current	GND ≤ VO ≤ VCC (Note 2)	0 to + 70°C			200			200	mA
			−55 to +125°C							
CI	Input Capacitance (Note 1)	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V			3.0	5.0		3.0	5.0	pF
CO	Output Capacitance (Note 1)				5.0	6.0		5.0	6.0	
ICC	VCC Operating Supply Current	Max VCC, $\overline{CS}$ ≤ VIL	T_A = 25°C			170			150	mA
			T_A = 0°C			180			160	
			T_A = −55°C							
ISB	Automatic $\overline{CS}$ Power Down Current	Max VCC, ($\overline{CS}$ ≥ VIH) (Note 5)	T_A = 0°C			30			20	mA
			T_A = 70°C			30			20	
			T_A = 125°C							

Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.5V and output loading of the specified IOL/IOH and 30pF load capacitance.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. A pull up resistor to VCC on the $\overline{CS}$ input is required to keep the device deselected, otherwise ISB will exceed values given.
6. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
7. Chip deselected greater than 55ns prior to selection.
8. Chip deselected less than 55ns prior to selection.
9. At any given temperature and voltage condition, tHZ is less than tLZ for all devices.
10. $\overline{WE}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL.
12. Address valid prior to or coincident with $\overline{CS}$ transition low.

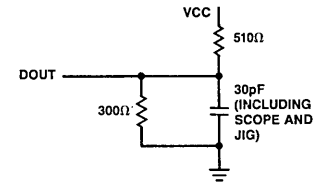

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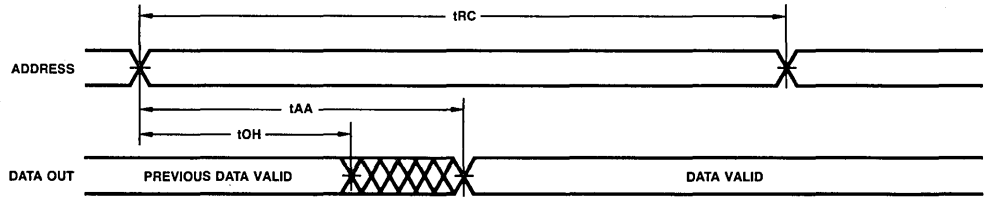
Figure 1. Output Load.

SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am9147-55 Min	Am9147-55 Max	Am9147-70 Min	Am9147-70 Max	Units
Read Cycle							
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		55		70		ns
tAA	Address Valid to Data Out Valid Delay (Address Access Time)			55		70	ns
tACS1	Chip Select Low to Data Out Valid (Note 5)	Note 7		55		70	ns
tACS2		Note 8		65		80	
tLZ	Chip Select Low to Data Out On	Note 9	10		10		ns
tHZ	Chip Select High to Data Out Off	Note 9	0	40	0	40	ns
tOH	Address Unknown to Data Out Unknown Time		5		5		ns
Write Cycle							
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		55		70		ns
tWP	Write Enable Low to Write Enable High Time (Note 4)		35		40		ns
tWR	Write Enable High to Address Do Not Care Time		10		15		ns
tWZ	Write Enable Low to Data Out Off Delay		0	30	0	35	ns
tDW	Data In Valid to Write Enable High Time		25		30		ns
tDH	Write Enable Low to Data In Do Not Care Time		10		10		ns
tAS	Address Valid to Write Enable Low Time		0		0		ns
tPD	Chip Select High to Power Low Delay			30		30	ns
tPU	Chip Select Low to Power High Delay		0		0		ns
tCW	Chip Select Low to Write Enable High Time (Note 4)		45		55		ns
tOW	Write Enable High to Output Turn On		0		0		ns
tAW	Address Valid to End of Write		45		55		ns

SWITCHING WAVEFORMS

READ CYCLE NO. 1 (Notes 10, 11)



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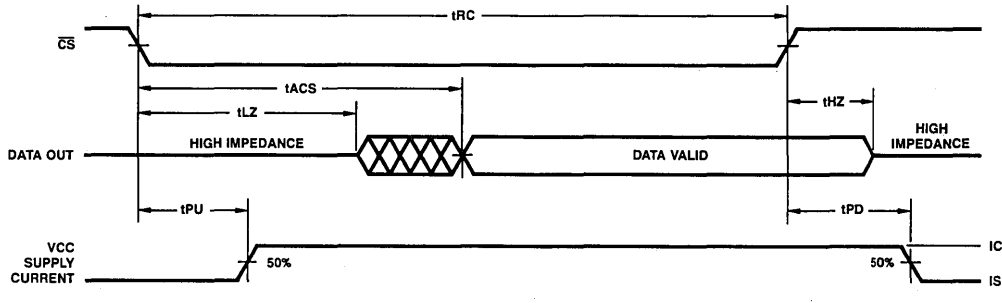
READ CYCLE NO. 2 (Notes 10, 12)



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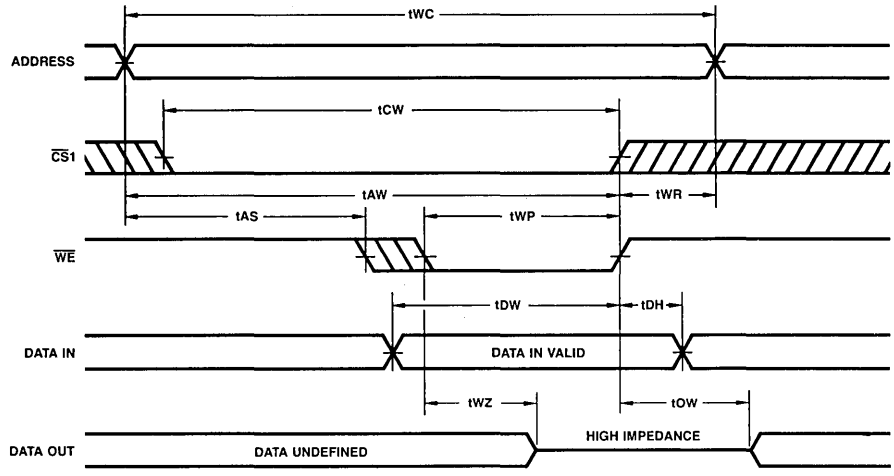
SWITCHING WAVEFORMS (Cont.)

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



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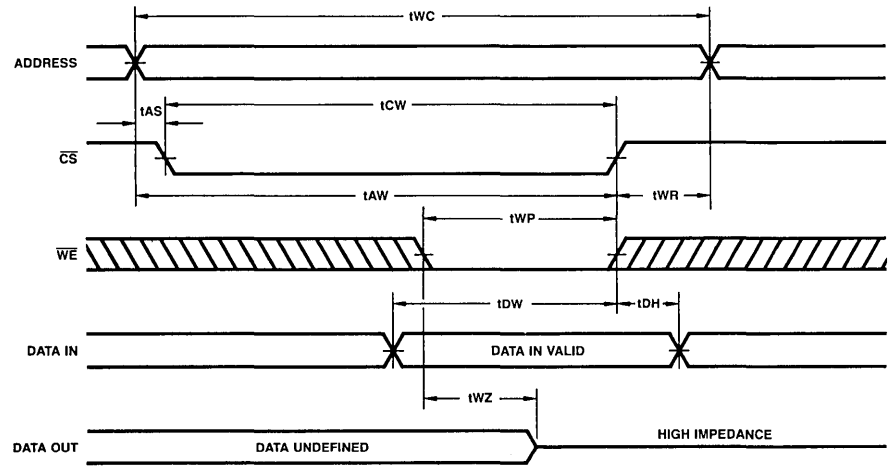
WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



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Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

BIT MAP

Address Designators	
External	Internal
A0	A2
A1	A5
A2	A4
A3	A3
A4	A7
A5	A8
A6	A1
A7	A0
A8	A6
A9	A9
A10	A11
A11	A10

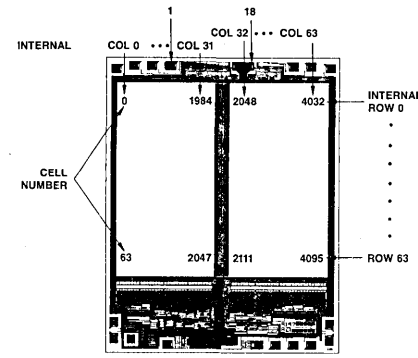
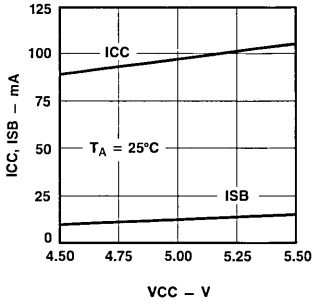


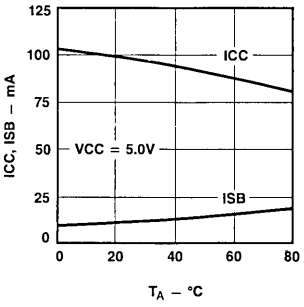
Figure 2. Bit Mapping Information.

TYPICAL DC AND AC CHARACTERISTICS

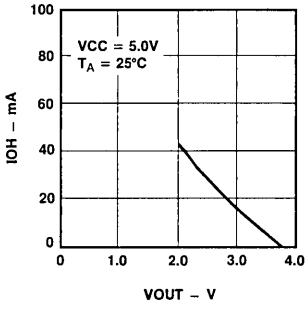
Supply Current Versus Supply Voltage



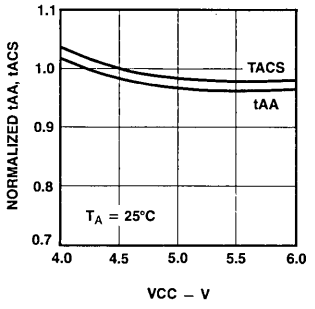
Supply Current Versus Ambient Temperature



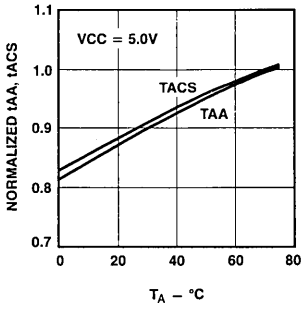
Output Source Current Versus Output Voltage



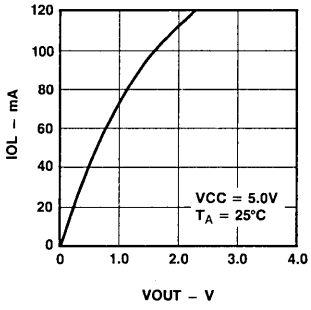
Normalized Access Time Versus Supply Voltage



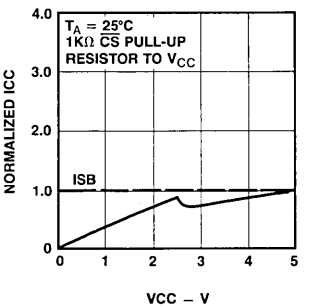
Normalized Access Time Versus Ambient Temperature



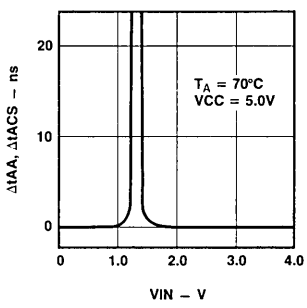
Output Sink Current Versus Output Voltage



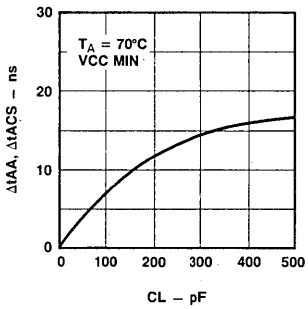
Typical Power-On Current Versus Power Supply



Access Time Change Versus Input Voltage



Access Time Change Versus Output Loading



Note: 1. The supply current shown in Graphs 1 and 2 are for the 9147-70. The supply current curves for the 9147-55 can be calculated by scaling proportionately.

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