

# Am9217/8316A

## 2048 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316A
- Access times as fast as 450 ns
- Fully capacitive inputs — simplified driving
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Drives two full TTL loads
- Single supply voltage — +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

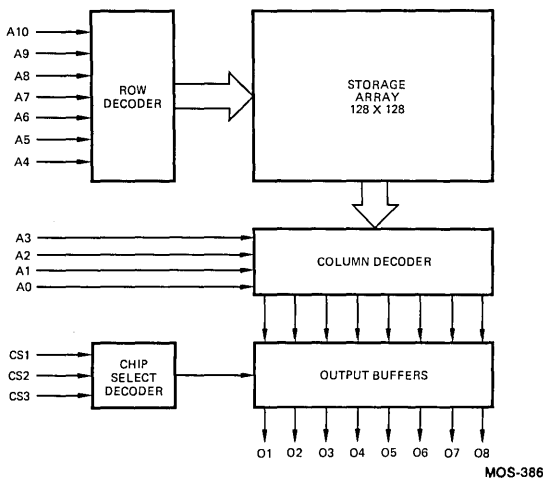
### FUNCTIONAL DESCRIPTION

The Am9217 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

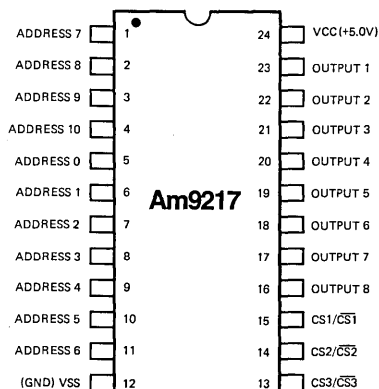
Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9217 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

### BLOCK DIAGRAM



### CONNECTION DIAGRAM



### ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		550ns	450ns
Hermetic DIP	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	AM9217ADC/C8316A	AM9217BDC
	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	AM9217ACC	AM9217BCC
Plastic DIP	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	AM9217ADM	AM9217BDM
		AM9217APC/P8316A	AM9217BPC

## Am9217/8316A

### MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature Under Bias	-55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

### ELECTRICAL CHARACTERISTICS

Am9217ADC       $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   
Am9217BDC       $V_{CC} = 5.0\text{V} \pm 5\%$   
C8316A

Parameters	Description	Test Conditions	Am9217XDC		C8316A		Units
			Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	9217      IOH = -200 $\mu$ A	2.4				Volts
		8316A      IOH = -100 $\mu$ A			2.2		
VOL	Output LOW Voltage	9217      IOL = 3.2mA		0.4			Volts
		8316A      IOL = 2.0mA				0.45	
VIH	Input HIGH Voltage		2.0	VCC + 1.0	2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage		-0.5	0.8	-0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled		10		10	$\mu$ A
ILI	Input Leakage Current			10		10	$\mu$ A
ICC	VCC Supply Current			70		98	mA

### ELECTRICAL CHARACTERISTICS

Am9217ADM       $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   
Am9217BDM       $V_{CC} = 5.0\text{V} \pm 10\%$

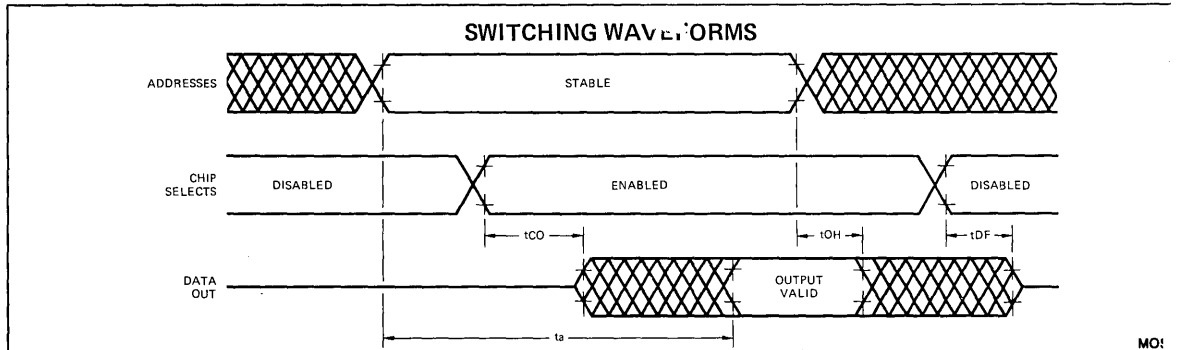
Parameters	Description	Test Conditions	Am9217XDM		Min.	Max.	Units
			Min.	Max.			
VOH	Output HIGH Voltage	9217      IOH = -200 $\mu$ A	2.2				Volts
VOL	Output LOW Voltage	9217      IOL = 3.2mA		0.45			Volts
VIH	Input HIGH Voltage		2.0	VCC + 1.0			Volts
VIL	Input LOW Voltage		-0.5	0.8			Volts
ILO	Output Leakage Current	Chip Disabled		10			$\mu$ A
ILI	Input Leakage Current			10			$\mu$ A
ICC	VCC Supply Current			80			mA

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Am9217XDC/C8316A       $T_A = 0^\circ\text{C to } +70^\circ\text{C}$        $V_{CC} = 5.0\text{V} \pm 5\%$   
Am9217XDM       $T_A = -55^\circ\text{C to } +125^\circ\text{C}$        $V_{CC} = 5.0\text{V} \pm 10\%$

Parameters	Description	Test Conditions	Am9217A		Am9217B		8316A		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
ta	Address to Output Access Time	tr = tf = 20ns Output load: one standard TTL gate plus 100pF (Note 1)		550		450		850	ns
tCO	Chip Select to Output ON Delay			180		150		300	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		-		ns
tDF	Chip Select to Output Off Delay			180		150		300	ns
CI	Input Capacitance	$T_A = 25^\circ\text{C}$ , f = 1.0MHz		7.0		7.0		10	pF
CO	Output Capacitance	All pins at 0V		7.0		7.0		15	pF

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.



### CUSTOM PATTERN ORDERING INFORMATION

Logic "1" = a more positive voltage (normally +5.0 V)

Logic "0" = a more negative voltage (normally 0 V)

**FIRST CARD**

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	8316A or 9217
65 thru 72	Optional information

## SECOND CARD

Column	Number	Description
	29	CS3 input required to select chip (0 or 1)
	31	CS2 input required to select chip (0 or 1)
	33	CS1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

Column Number	
10, 12, 14, 16, 18	Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30.
20, 22, 24, 26, 28, 30	
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

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