# Am8155/Am8156

## 2048-Bit Static MOS RAM With I/O Ports and Timer

### ADVANCE INFORMATION

#### DISTINCTIVE CHARACTERISTICS

- 256 word x 8-bits
- Single +5V power supply
- Completely static operation
- Internal address latch
- 2 programmable 8-bit I/O ports
- 1 programmable 6-bit I/O port
- Programmable 14-bit binary counter/timer
- Multiplexed address and data bus

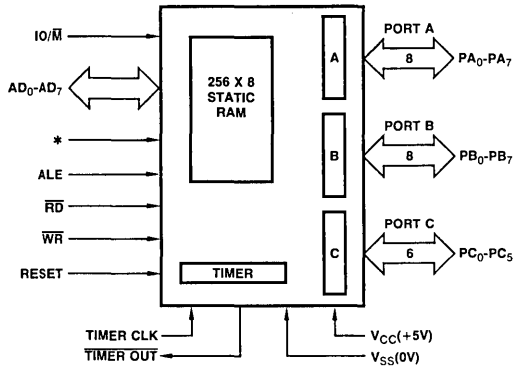
#### GENERAL DESCRIPTION

The Am8155 and Am8156 are RAM and I/O chips to be used in the Am8085A MPU system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. They have a maximum access time of 400ns to permit use with no wait states in Am8085A CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

#### BLOCK DIAGRAM




*Am8155 = $\overline{CE}$, Am8156 = CE

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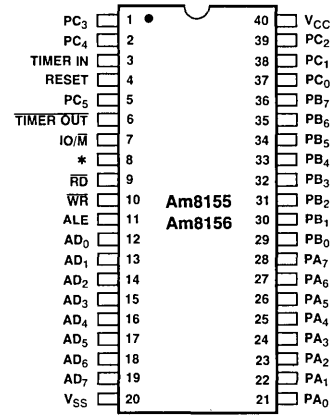
#### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

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#### ORDERING INFORMATION

| Package Type | Temperature Range | Order Numbers | |
|---|---|---|---|
| Hermetic DIP* | 0°C ≤ $T_A$ ≤ +70°C | AM8155DC or AM8155CC | AM8156DC or AM8156CC |
| Molded DIP | | AM8155PC | AM8156PC |

*Hermetic = Ceramic = DC = CC = D-40-1.

## FUNCTIONAL PIN DEFINITION

The following describes the functions of all of the Am8155/Am8156 pins.

### RESET

The Reset signal is a pulse provided by the Am8085 to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be 600ns. (Two Am8085A clock cycle times).

### $AD_0$-$AD_7$

These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/M input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.

### CE OR $\overline{CE}$

Chip Enable: On the Am8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the Am8156, this pin is CE and is ACTIVE HIGH.

### $\overline{RD}$

Input low on this line with the Chip Enable active enables the $AD_{0-7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port will be read to the AD bus.

### $\overline{WR}$

Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports depending on the polarity of IO/$\overline{M}$.

### ALE

Address Latch Enable: This control signal latches both the address on the $AD_{0-7}$ lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.

### IO/$\overline{M}$

IO/$\overline{Memory}$ Select: This line selects the memory if low and selects the IO if high.

### $PA_0$-$PA_7$

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.

### $PB_0$-$PB_7$

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.

### $PC_0$-$PC_5$

These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When $PC_{0-5}$ are used as control signals, they will provide the following:

- $PC_0$ – A INTR (Port A Interrupt)
- $PC_1$ – A BF (Port A Buffer full)
- $PC_2$ – $\overline{A\ STB}$ (Port A Strobe)
- $PC_3$ – B INTR (Port B Interrupt)
- $PC_4$ – B BF (Port B Buffer Full)
- $PC_5$ – $\overline{B\ STB}$ (Port B Strobe)

### TIMER IN

This is the input to the counter timer.

### $\overline{TIMER\ OUT}$

This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.

### $V_{CC}$

+5 volt supply.

### $V_{SS}$

Ground reference.

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## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## DC CHARACTERISTICS ($T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ± 5%)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | −0.5 | | 0.8 | Volts |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$+0.5 | Volts |
| $V_{OL}$ | Output Low Voltage | | $I_{OL}$ = 2mA | | | 0.45 | |
| $V_{OH}$ | Output High Voltage | | $I_{OH}$ = −400μA | 2.4 | | | Volts |
| $I_{IL}$ | Input Leakage | | $V_{IN}$ = $V_{CC}$ to 0V | | | ±10 | μA |
| $I_{LO}$ | Output Leakage Current | | 0.45V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | | ±10 | μA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | | | 180 | mA |
| $I_{IL}$(CE) | Chip Enable Leakage | Am8155<br>Am8156 | $V_{IN}$ = $V_{CC}$ to 0V | | +100<br>−100 | | μA |

## AC CHARACTERISTICS ($T_A$ = 0°C to + 70°C; $V_{CC}$ = 5V ± 5%)

| Parameters | Description | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{AL}$ | Address to Latch Set-up Time | | 50 | | ns |
| $t_{LA}$ | Address Hold Time After Latch | | 80 | | ns |
| $t_{LC}$ | Latch to READ/WRITE Control | | 100 | | ns |
| $t_{RD}$ | Valid Data Out Delay from READ Control | | | 170 | ns |
| $t_{AD}$ | Address Stable to Data Out Valid | | | 400 | ns |
| $t_{LL}$ | Latch Enable Width | | 100 | | ns |
| $t_{RDF}$ | Data Bus Float After Read | | 0 | 100 | ns |
| $t_{CL}$ | READ/WRITE Control to Latch Enable | | 20 | | ns |
| $t_{CC}$ | READ/WRITE Control Width | | 250 | | ns |
| $t_{DW}$ | Data In to WRITE Set-up Time | | 150 | | ns |
| $t_{WD}$ | Data In Hold Time After WRITE | | 0 | | ns |
| $t_{RV}$ | Recovery Time Between Controls | | 300 | | ns |
| $t_{WP}$ | WRITE to Port Output | | | 400 | ns |
| $t_{PR}$ | Port Input Set-up Time | 150pF Load | 70 | | ns |
| $t_{RP}$ | Port Input Hold Time | | 50 | | ns |
| $t_{SBF}$ | Strobe to Buffer Full | | | 400 | ns |
| $t_{SS}$ | Strobe Width | | 200 | | ns |
| $t_{RBE}$ | READ to Buffer Empty | | | 400 | ns |
| $t_{SI}$ | Strobe to INTR On | | | 400 | ns |
| $t_{RDI}$ | READ to INTR Off | | | 400 | ns |
| $t_{PSS}$ | Port Set-up Time to Strobe | | 50 | | ns |
| $t_{PHS}$ | Port Hold Time After Strobe | | 120 | | ns |
| $t_{SBE}$ | Strobe to Buffer Empty | | | 400 | ns |
| $t_{WBF}$ | WRITE to Buffer Full | | | 400 | ns |
| $t_{WI}$ | WRITE to INTR Off | | | 400 | ns |
| $t_{TL}$ | TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low | | | 400 | ns |
| $t_{TH}$ | TIMER-IN to $\overline{\text{TIMER-OUT}}$ High | | | 400 | ns |
| $t_{RDE}$ | Data Bus Enable from READ Control | | 10 | | ns |

Note: For Timer Input Specification, see Figure 10.

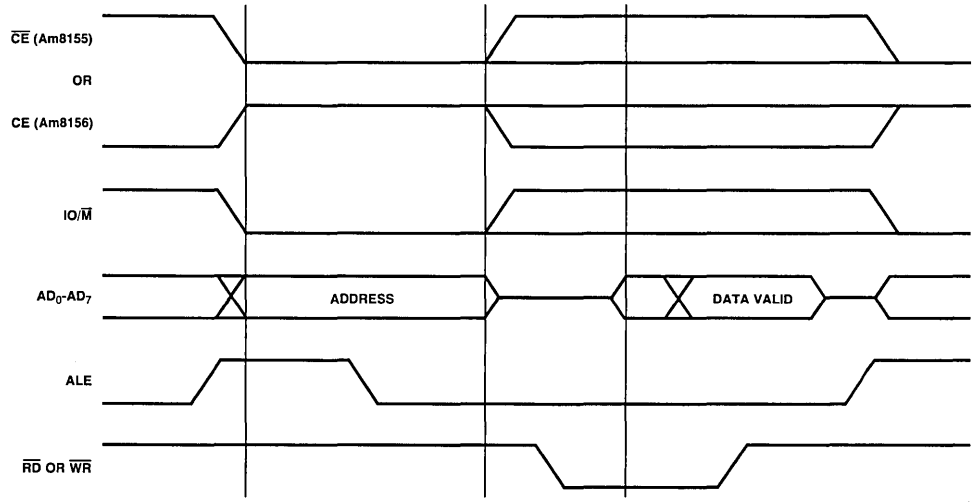
## OPERATIONAL DESCRIPTION

The Am8155/8156 includes the following operational features:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA and PB) and one 6-bit I/O port (PC)
- 14-bit down counter

The I/O portion contains four registers (Command/Status, $PA_{0-7}$, $PB_{0-7}$, $PC_{0-5}$). The IO/$\overline{M}$ (IO/$\overline{\text{Memory}}$ Select) pin selects the I/O or the memory (RAM) portion. Detailed descriptions of memory, I/O ports and timer functions will follow.

The 8-bit address on the AD lines, the Chip Enable input, and IO/$\overline{M}$ are all latched on chip at the falling edge of ALE. A low on the IO/$\overline{M}$ must be provided to select the memory section.




Note: For detailed timing diagram information, see Figure 7 and AC Characteristics.

**Figure 1. Memory Read/Write Cycle.**

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## PROGRAMMING OF THE COMMAND/STATUS REGISTER

The command register consists of eight latches, one for each bit. Four bits (0-3) define the mode of the ports. Two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The C/S register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation. The meaning of each bit of the command byte is defined as follows:

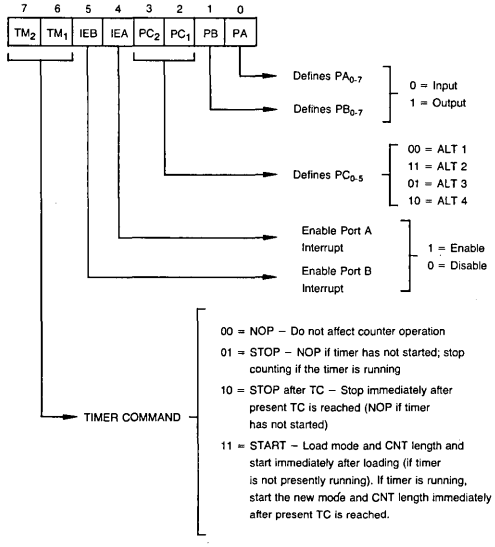


**Figure 2. Command/Status Register Bit Assignment.**

## READING THE COMMAND/STATUS REGISTER

The status register consists of seven latches, one for each bit: six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the C/S Register (Address XXXXX000). Status word format is shown below:

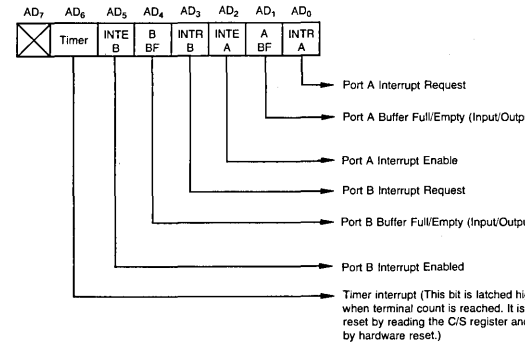


**Figure 3. Command/Status Register Status Word Format.**

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## INPUT/OUTPUT SECTION

The I/O section of the Am8155/8156 consists of four registers as described below.

- Command/Status Register (C/S) – This register is assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S register is selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer become available on the $AD_{0-7}$ lines.

- PA Register – This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are $PA_{0-7}$. The address of this register is XXXXX001.

- PB Register – This register functions the same as PA Register. The I/O pins assigned are $PB_{0-7}$. The address of this register is XXXXX010.

- PC Register – This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the $AD_2$ and $AD_3$ bits of the C/S register.

  When $PC_{0-5}$ is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the Am8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 1.

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

| Control | Input Mode | Output Mode |
|---|---|---|
| BF | Low | Low |
| INTR | Low | High |
| $\overline{STB}$ | Input Control | Input Control |

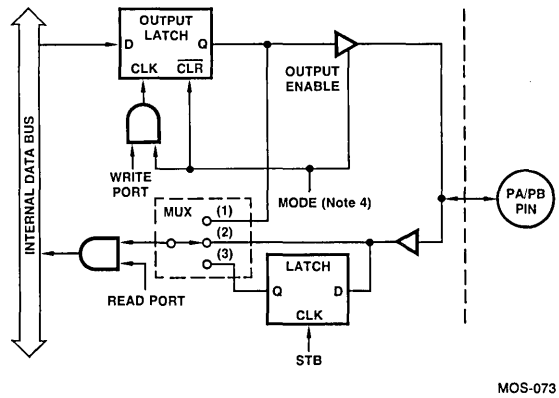
The set and reset of INTR and BF with respect to $\overline{STB}$, $\overline{WR}$ and $\overline{RD}$ timing is shown in Figure 8.

To summarize, the register's assignments are:

| Address | Pinouts | Functions | No. of Bits |
|---|---|---|---|
| XXXXX000 | Internal | Command/Status Register | 8 |
| XXXXX001 | $PA_{0-7}$ | General Purpose I/O Port | 8 |
| XXXXX010 | $PB_{0-7}$ | General Purpose I/O Port | 8 |
| XXXXX011 | $PC_{0-5}$ | General Purpose I/O Port or Control Lines | 6 |

The following diagram shows how I/O Ports A and B are structured within the Am8155 and Am8156:

**Am8155/Am8156**
**One Bit of Port A or Port B**




Notes: 1. Output Mode
2. Simple Input
3. Strobed Input
} Multiplexer Control
4. = 1 for output mode
= 0 for input mode.

Read Port = (IO/$\overline{M}$ = 1) • ($\overline{RD}$ = 0) • (CE active) • (Port address selected)

Write Port = (IO/$\overline{M}$ = 1) • ($\overline{WR}$ = 0) • (CE active) • (Port address selected)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to ouput, the output pins will go low. When the Am8155/8156 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

**Table 1. Table of Port Control Assignment.**

| Pin | ALT 1 | ALT 2 | ALT 3 | ALT 4 |
|---|---|---|---|---|
| PC0 | Input Port | Output Port | A INTR (Port A Interrupt) | A INTR (Port A Interrupt) |
| PC1 | Input Port | Output Port | A BF (Port A Buffer Full) | A BF (Port A Buffer Full) |
| PC2 | Input Port | Output Port | A $\overline{STB}$ (Port A Strobe) | A $\overline{STB}$ (Port A Strobe) |
| PC3 | Input Port | Output Port | Output Port | B INTR (Port B Interrupt) |
| PC4 | Input Port | Output Port | Output Port | B BF (Port B Buffer Full) |
| PC5 | Input Port | Output Port | Output Port | B $\overline{STB}$ (Port B Strobe) |

## TIMER SECTION

The timer is a 14-bit down counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode. The value loaded into the count length register can have any value from $2_H$ through $3FFF_H$ in bits 0-13.

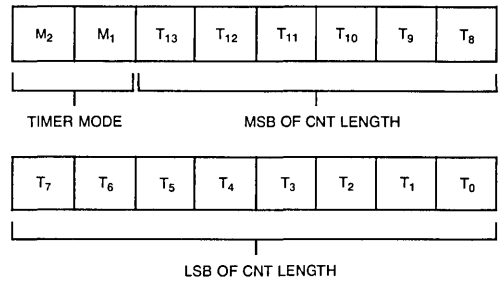



**Figure 4. Timer Format.**

There are four modes to choose from:

0 – Puts out low during second half of count
1 – Square wave
2 – Single pulse upon TC being reached
3 – Repetitive single pulse everytime TC is readied and automatic reload of counter upon TC being reached, until instructed to stop by a new command loaded into C/S.

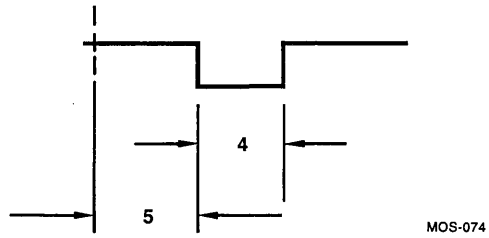
Bits 6-7 of Command/Status Register Contents are used to start and stop the counter. There are four commands to choose from (See the further description on Command/Status Register.).

| C/S7 | C/S6 | |
|---|---|---|
| 0 | 0 | NOP – Do not affect counter operation. |
| 0 | 1 | STOP – NOP if timer has not started; stop counting if the timer is running. |
| 1 | 0 | STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not started). |
| 1 | 1 | START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached. |

M2 and M1 define the timer mode as follows:

| M2 | M1 | |
|---|---|---|
| 0 | 0 | Puts out low during second half of count. |
| 0 | 1 | Square wave, i.e., the period of the square wave equals the count length programmed with automatic reload at terminal count. |
| 1 | 0 | Single pulse upon TC being reached. |
| 1 | 1 | Automatic reload, i.e., single pulse everytime TC is reached. |

Note: In case of an asymmetric count, i.e., 9, larger half of the count will be high, the larger count will stay active as shown in Figure 5.




Note: 5 and 4 refer to the number of clock cycles in that time period.

**Figure 5. Asymmetric Count.**

The counter in the Am8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

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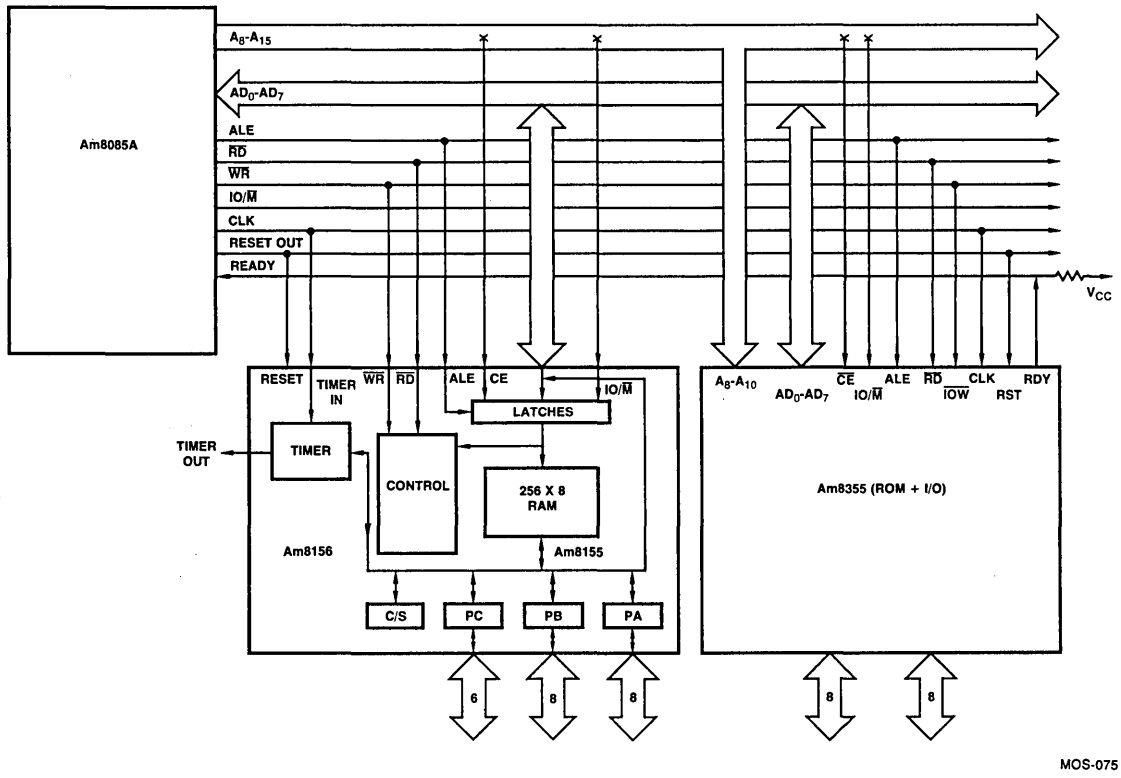


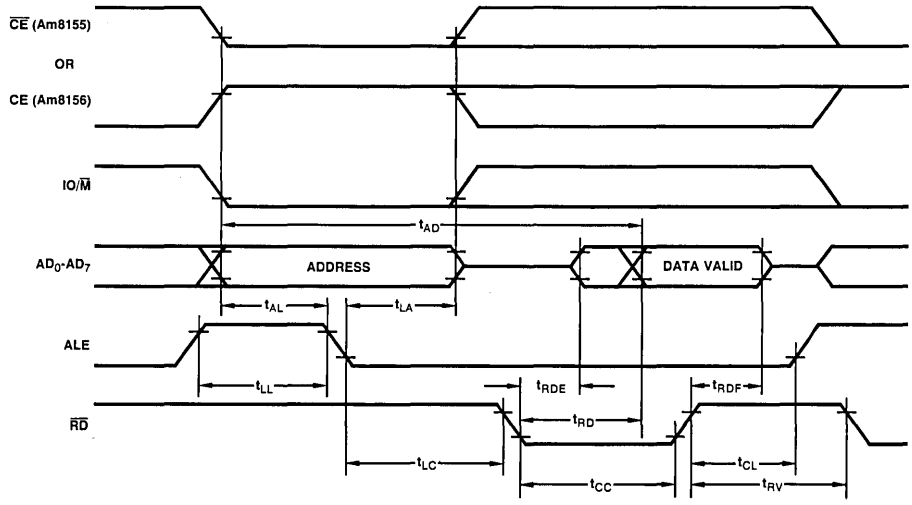

Figure 6 shows that a minimum system is possible using only three chips:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

**Figure 6. Am8085A Minimum System Configuration.**

## WAVEFORMS

### A. READ CYCLE.

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### B. WRITE CYCLE.

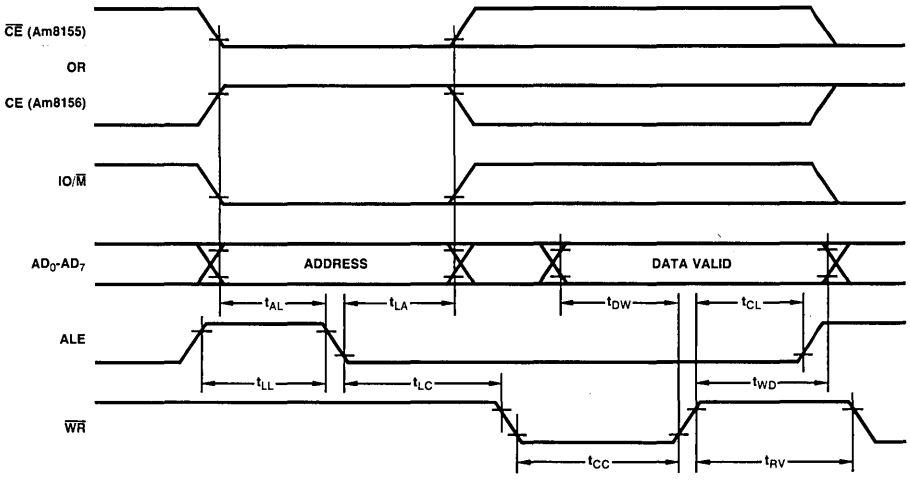


**Figure 7. Am8155/8156 Read/Write Timing Diagrams.**

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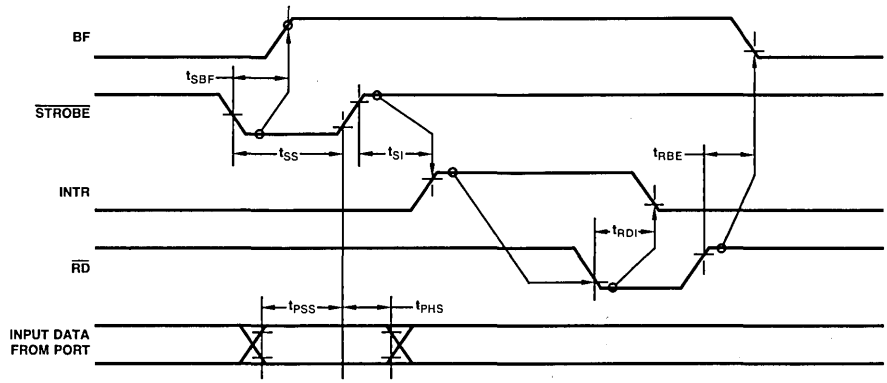
## WAVEFORMS (Cont.)

### A. STROBED INPUT MODE.

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### B. STROBED OUTPUT MODE.

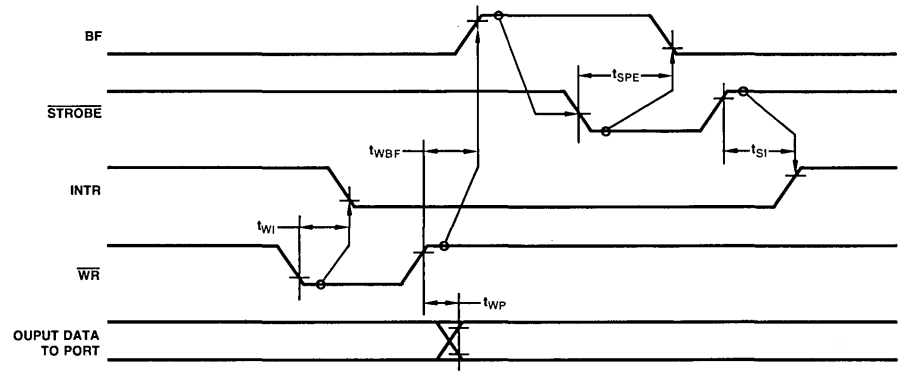


**Figure 8. Strobed I/O Timing.**

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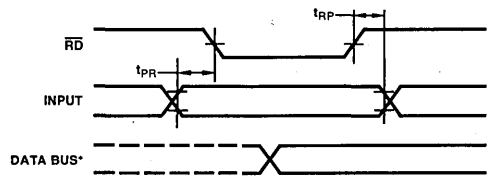
### BASIC INPUT MODE.

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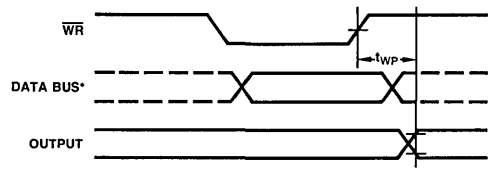
### BASIC OUTPUT MODE.

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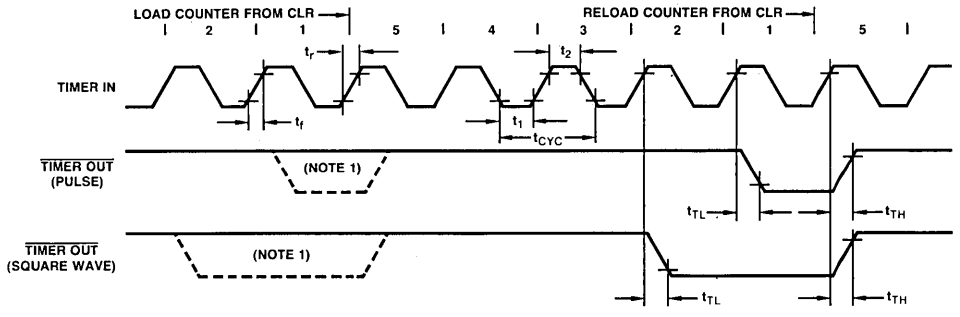
*Data bus timing is shown in Figure 7.

**Figure 9. Basic I/O Timing Waveform.**

## WAVEFORMS (Cont.)




Note 1: The timer output is periodic if in an automatic reload mode ($M_1$ mode bit = 1).

**Countdown from 5 to 1**

| | | |
|---|---|---|
| $t_{CYC}$ | 320ns | MIN. |
| $t_r$ and $t_f$ | 30ns | MAX. |
| $t_1$ | 80ns | MIN. |
| $t_2$ | 120ns | MIN. |
| $t_{TL}$ and $t_{TH}$ | 400ns | MAX. |

**Figure 10. Timer Output Waveform.**

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