Am4025/5025 • Am4026/5026 • Am4027/5027

2048-Bit Dynamic Shift Registers

Distinctive Characteristics

- 6 MHz data rate guaranteed
- Single 2048 and dual 1024-bit configurations
- Low power dissipation
- TTL compatible data inputs and outputs
- On chip recirculate and input select controls
- Alternate source to National parts
- Full military temperature range devices available
- 100% reliability assurance testing in compliance with MIL-STD-883

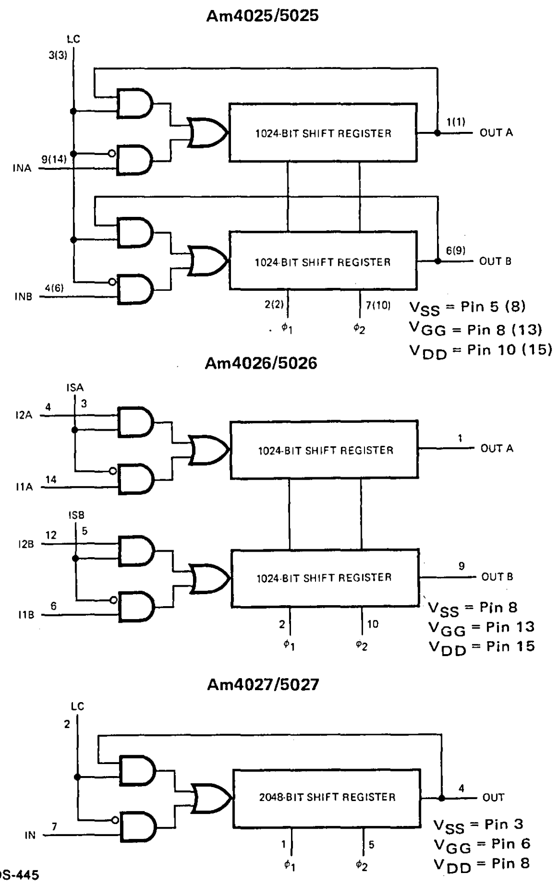
FUNCTIONAL DESCRIPTION

The Am4025/6/7 and Am5025/6/7 are military and commercial grade 2048-bit dynamic shift registers. The Am4025/5025 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The Am4026/5026 is similar, but each register has two data inputs, selected by separate input select (IS) signals. The Am4027/5027 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load or three Am93L series low-power TTL loads. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers, so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore, is double the frequency of either clock signal.

ORDERING INFORMATION

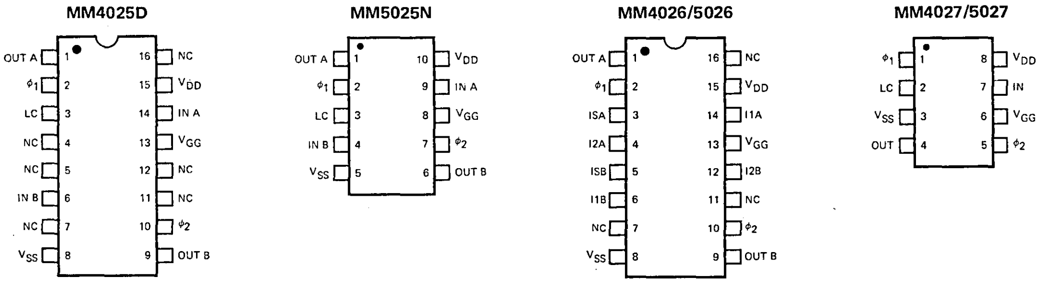
Package Type	Temperature Range	Order Number
10-Pin Molded	0°C to +70°C	MM5025N
16-Pin Hermetic	0°C to +70°C	MM5025D
16-Pin Hermetic	–55°C to +125°C	MM4025D
16-Pin Molded	0°C to +70°C	MM5026N
16-Pin Hermetic	0°C to +70°C	MM5026DC
16-Pin Hermetic	–55°C to +125°C	MM4026D
8-Pin Molded	0°C to +70°C	MM5027N
8-Pin Hermetic	0°C to +70°C	AM5027DC
8-Pin Hermetic	–55°C to +125°C	AM4027DM

LOGIC DIAGRAMS



MOS-445

CONNECTION DIAGRAMS
Top Views



MOS-44

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
DC Input Voltage with Respect to V_{CC}	−20V to +0.3V

OPERATING RANGE

Part Number	V_{SS}	V_{DD}	V_{GG}	T_A
MM4025/6/7	+5.0V ±5%	0V	−12V ±10%	−55°C to +125°C
MM5025/6/7	+5.0V ±5%	0V	−12V ±10%	0°C to +70°C

5

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = −0.5mA		2.4		V_{SS}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA		0.0		0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs except clocks		V_{SS} −1.7		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs except clocks		V_{SS} −10		V_{SS} −4.2	Volts
I_I	Input Leakage Current	V_{IN} = −10V, T_A = 25°C			10	500	nA
I_ϕ	Clock Input Leakage Current	V_ϕ = −15V, T_A = 25°C			50	1000	nA
$V_{\phi H}$	Clock HIGH Level			V_{SS} −1.0		V_{SS} +0.3	Volts
$V_{\phi L}$	Clock LOW Level			V_{SS} −18.5		V_{SS} −14.5	Volts
I_{GG}	V_{GG} Current	T_A = 25°C	.01MHz<f<0.1MHz		2	3.5	mA
		V_{SS}=5.0V, V_{GG}=−12.0V	f = 1.0MHz		2	3.5	
		$V_{\phi L}$ = −12.0V	f = 3.0MHz		2	3.5	
I_{DD}	V_{DD} Current	t = 115ns	.01MHz<f<0.1MHz		8	15	mA
		Data = 11110000...	f = 1.0MHz		22	32	
			f = 3.0MHz		48	70	

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12.0V and 25°C ambient.

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

Parameters	Definition	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
f_D	Data Rate (Note 2)	T_A = 0°C to +70°C	0.02		6.0	MHz
		T_A = −55°C to +125°C	0.12		2.0	
f_ϕ	Clock Frequency (Note 3)	T_A = 0°C to +70°C	.01		3.0	
		T_A = −55°C to +125°C	0.06		1.0	
$t_{\phi d}$	Delay Between Clocks (Note 3)		10		Note 3	ns
$t_{\phi pw}$	Clock LOW Time	$t_{\phi t}$ = 20ns	0.115		10	μs
$t_{\phi t}$	Clock Rise and Fall Times	10% to 90%			0.5	μs
t_s	Set-Up Time, Data and Select Inputs (See Definitions)				35	ns
t_h	Hold Time, Data and Select Inputs (See Definitions)		20			ns
$t_{\phi p}$	Period From Start of (Note 3) One Phase to Start of Other Phase	T_A = 0°C to +70°C	0.165		100	μs
		T_A = −55°C to +125°C	0.165		16.5	
t_{pd}	Delay, Clock to Data Out	C_L = 15pF			80	ns
C(D)	Capacitance, Data Input	V_{IN} = 0, f = 1MHz,			5	pF
C(S)	Capacitance, Select Input or L_C	All other pins GND (Note 4)			7	pF
C(φ)	Capacitance, Clock Input	V_ϕ = 0, f = 1MHz, All other pins GND		165	190	

Notes: 2. The Data Rate is twice the frequency of either clock phase.
3. The maximum delay between clocks (ϕ_1 and ϕ_2 both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.
4. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TRUTH TABLES

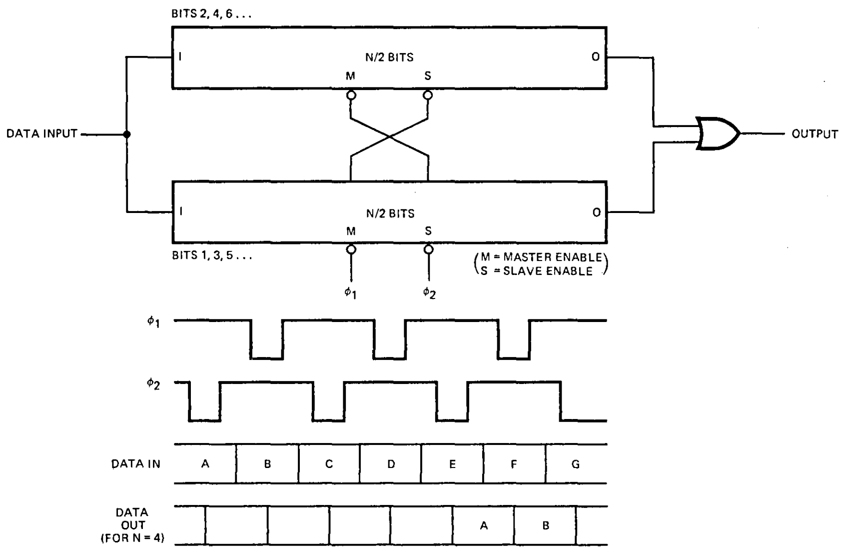
Am4025/5025 and Am4027/5027

LC	IN	OUT	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Am4026/5026

IS	INPUT 1	INPUT 2	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

FUNCTIONAL EQUIVALENT OF EACH REGISTER



Since the two registers shift on opposite clock pulses, a new data bit is entered on both ϕ_1 and ϕ_2. Data entering the register on ϕ_1 will appear at the output on ϕ_1 (from the negative edge of ϕ_1 to the negative edge of ϕ_2).

MOS-4

DEFINITION OF TERMS

Dynamic Shift Register A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

ϕ_1, ϕ_2 The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at V_{SS}. Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

$t_{\phi d}$ Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-toLOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

$t_{\phi pw}$ Clock pulse width. The LOW time of each clock sign During $t_{\phi pw}$ one of the clocks is ON, and data transfer betwe master and slave or slave and master occurs.

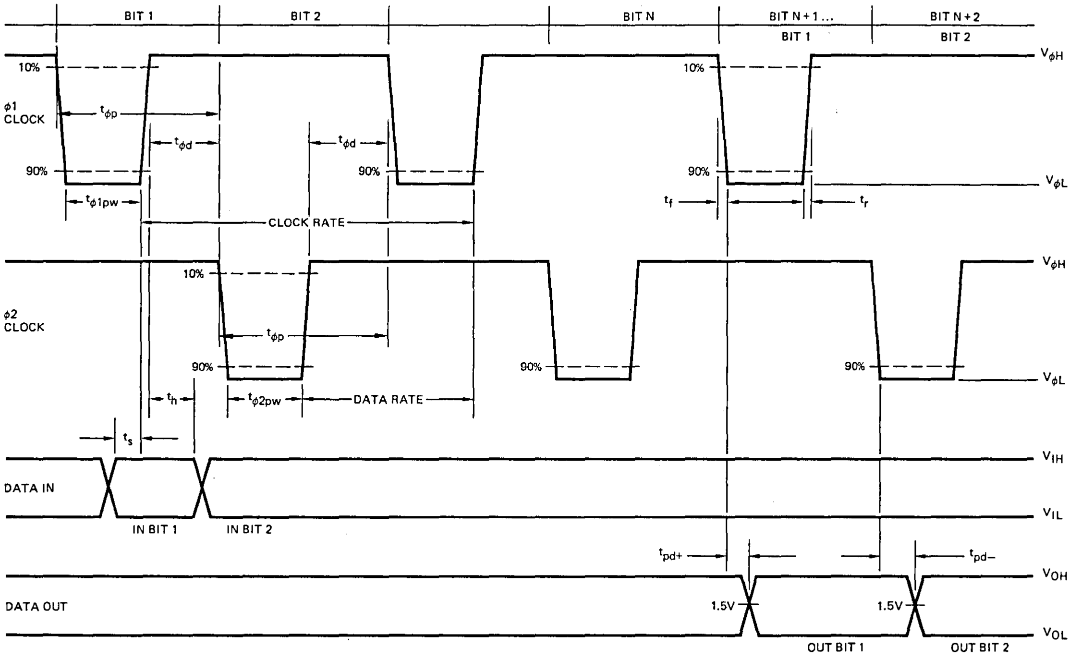
$t_{\phi t}$ Clock rise and fall times. The time required for the clc signals to change from 10% to 90% of the total level char occuring.

$t_s(D)$ Data set-up time. The time prior to the LOW-to-HI(transition of ϕ during which the data on the data input must steady to be correctly written into the memory.

$t_h(D)$ Data hold time. The time following the LOW-to-HI transition of ϕ during which the data must be steady. correctly write data into the register, the data must be applied $t_s(D)$ before this transition and must not be changed until t_h after this transition.

t_{pd} The delay from a HIGH-to-LOW clock transition to corı data present at the register output.

SWITCHING WAVEFORMS

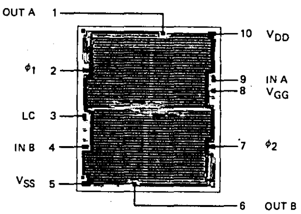


Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

MOS-448

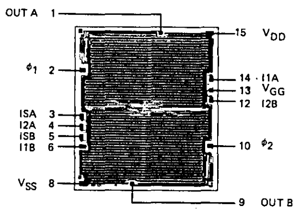
Metallization and Pad Layouts

Am4025/5025



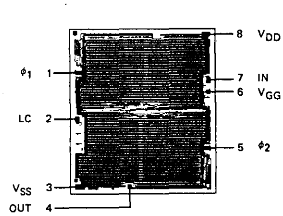
DIE SIZE 0.145" X 0.162"

Am4026/5026



DIE SIZE 0.145" X 0.162"

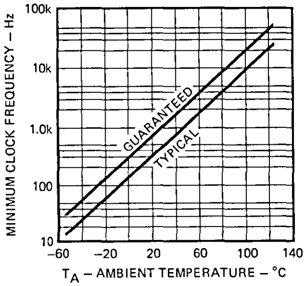
Am4027/5027



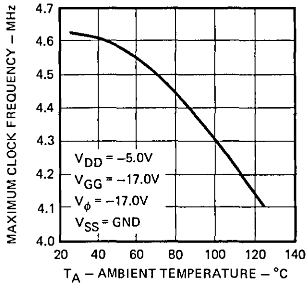
DIE SIZE 0.145" X 0.162"

OPERATING CHARACTERISTICS

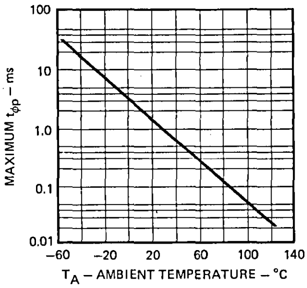
Guaranteed Minimum Clock Frequency Versus Temperature



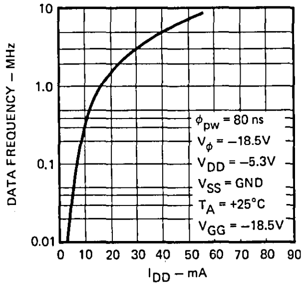
Maximum Clock Frequency Versus Temperature



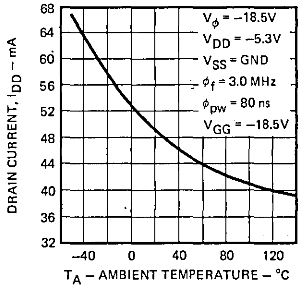
Guaranteed Maximum $t_{\phi p}$ Versus Temperature (Note 2)



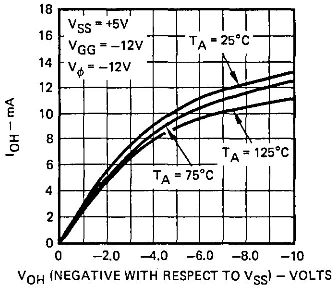
Typical Power Supply Current Versus Data Rate



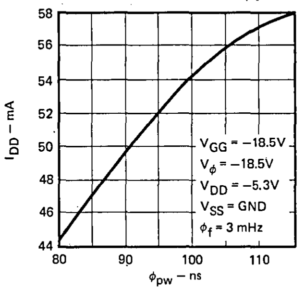
Typical Power Supply Current Versus Temperature



V_{OH} Versus I_{OH}



Typical Power Supply Current Versus Clock Pulse Width $t_{\phi pw}$



MOS-449