Am2810

Dual 128-Bit Static Shift Register

Distinctive Characteristics

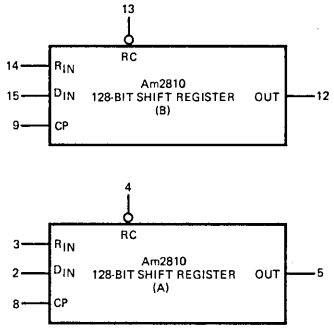
- 2nd Source to Mostek 1002P
- Built-in pull-up resistors
- 100% reliability assurance testing in compliance with MIL-STD-883
- Operation guaranteed from DC to 2MHz

FUNCTIONAL DESCRIPTION

The Am2810 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Each register has a separate clock input, and operates with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the R_{in} input; when RC is HIGH, data is accepted on the D_{in} input. The inputs to the registers have built-in pull-up resistors to provide total TTL compatibility. The V_{RA} pin controls the pull-up resistors for register A D_{in} and RC inputs. The V_{RB} pin controls the pull-up resistors for the register B D_{in} and RC inputs. The $V_{R\phi}$ pin controls the resistor on the clock input to both registers. When the resistor control pins are tied to V_{GG} (−12V), the resistors are enabled and pull the inputs they affect up to V_{SS}. When the resistor control pins are tied to V_{SS} the resistors are all very high impedance and the inputs they affect all exhibit normal MOS characteristics. The R_{in} inputs are intended to be the recirculate inputs from an MOS output and these inputs do not have pull-up resistors associated with them.

LOGIC SYMBOL



V_{RA} = Pin 16
V_{RB} = Pin 1
$V_{R\phi}$ = Pin 10

V_{SS} = Pin 7
V_{DD} = Pin 6
V_{GG} = Pin 11

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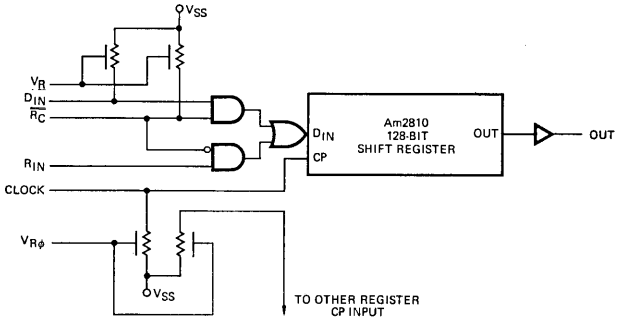
LOGIC BLOCK DIAGRAM (One Register Shown)



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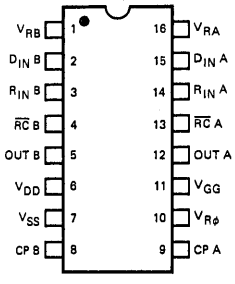
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM2810PC
Hermetic DIP	0°C to +75°C	AM2810DC
Hermetic DIP	−55°C to +125°C	AM2810DM

CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

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MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3V

OPERATING RANGE

Part Number	T_A	V_{SS}	V_{DD}	V_{GG}
Am2810XC Am1002P Am1002L	0°C to +75°C	5.0V ±5%	0 V	−12.0V ±5%
Am2810XM	−55°C to +125°C	5.0V ±5%	0 V	−12.0V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −100μA		V_{SS}−1			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		V_{SS}−1			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				V_{SS}−4	Volts
I_{IL} (Note 2)	Resistors Disabled Input LOW Current	V_{SS} = MAX., V_{IN} = 0V $V_{RA} = V_{RB} = V_{R\phi} = V_{SS}$				−40	μA
$I_{IL}(\Omega)$ (Note 2)	Resistors Enabled Input LOW Current	V_{SS} = MAX., V_{IN} = 0.4V, Am2810/Am1002P only $V_{RA} = V_{RB} = V_{R\phi} = V_{GG}$		−0.3		−2.0	mA
$I_{IL}(\phi)$	Input LOW Current Clock Input	1002L only		−0.6		−4.0	mA
I_{IH}	Input HIGH Current	$V_{RA} = V_{RB} = V_{R\phi} = V_{IN} = V_{SS}$				40	μA
I_{SS}	V_{SS} Power Supply Current	f = 1MHz Inputs and Outputs Open	0°C to +75°C		14	25	mA
			−55°C to +125°C			35	
I_{GG}	V_{GG} Power Supply Current		0°C to +75°C		−4	−10	
			−55°C to +125°C			−15	

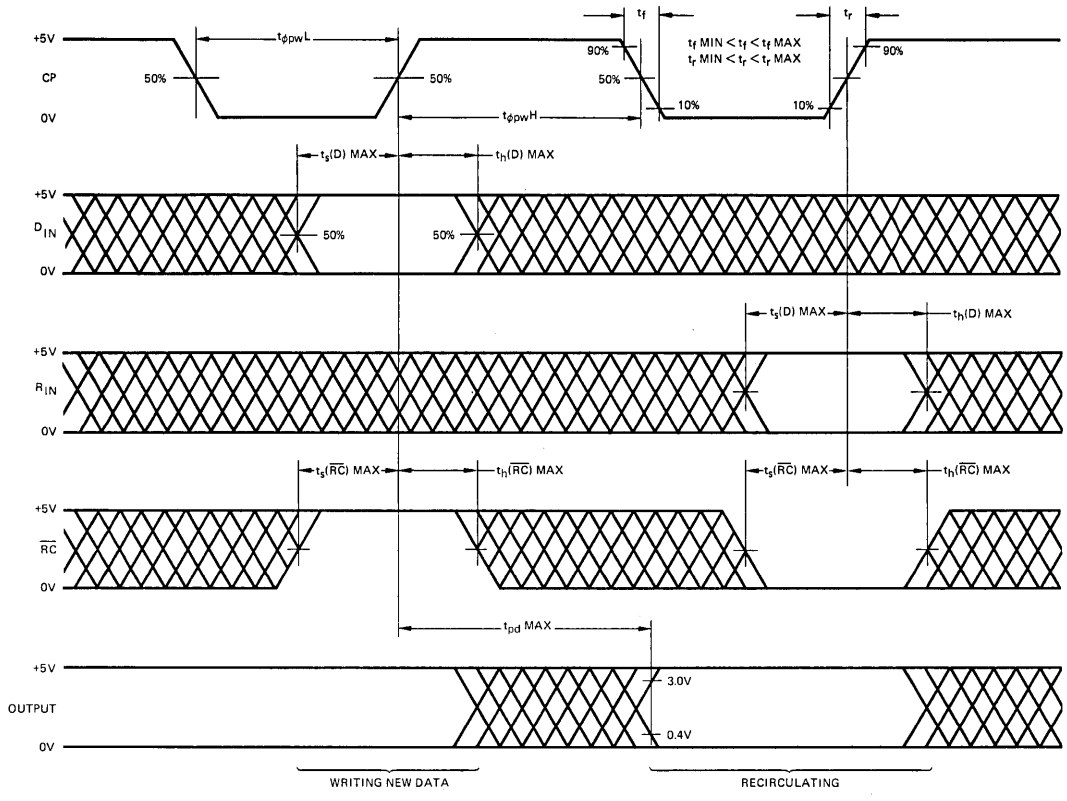
Notes: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.
2. On chip pull-up resistors are provided for the clock and data inputs; they are enabled when the appropriate V_R input is at −12V. When the V_f inputs are at V_{SS}, the resistors are disabled and the inputs exhibit normal MOS characteristics (I_{IL} and I_{IH}), the recirculate data inputs have n pull-up resistors and always exhibit MOS characteristics. All pull-up resistors are disabled on the Am1002L except the one on the clock.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Am2810 Min.	Am2810 Typ.	Am2810 Max.	Am1002P/Am1002L Min.	Am1002P/Am1002L Typ.	Am1002P/Am1002L Max.	Units
f_{max}	Maximum Clock Frequency		2.0			1.0			MHz
$t_{\phi pw}H$	Clock HIGH Time		0.2		∞	0.4		∞	μs
$t_{\phi pw}L$	Clock LOW Time		0.2		100	0.3		10	μs
t_r, t_f	Clock Rise and Fall Times		10		200	10		200	ns
t_s(D)	Set-up Time, D or R Inputs (see definitions)	$t_r = t_f$ = 50ns, V_R = −12V	100			50			ns
t_h(D)	Hold Time, D or R Inputs (see definitions)	$t_r = t_f$ = 50ns, V_R = −12V	100			200			ns
$t_s(\overline{RC})$	Set-up Time, $\overline{RC}$ Input (see definitions)		100			100			ns
$t_h(\overline{RC})$	Hold Time, $\overline{RC}$ Input (see definitions)		200			300			ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 2.9kΩ, C_L = 20pF	(Note 4)		250	(Note 4)		450	ns
t_{pr}, t_{pf}	Output Rise and Fall Times	10% to 90%			100			150	ns
C_{in}	Capacitance, Any Input (Note 3)	f = 1MHz, V_{IN} = V_{SS}		3	7		3	10	pF

Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM



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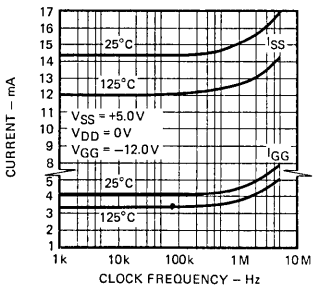
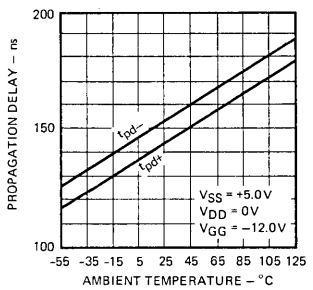
TEST CIRCUIT

Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



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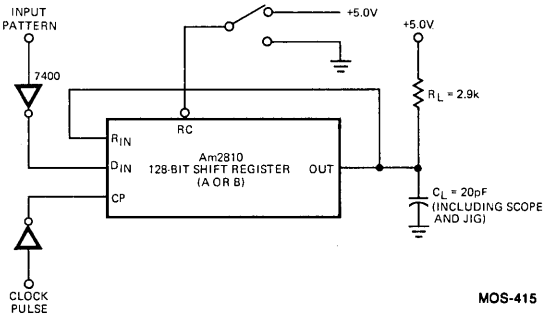

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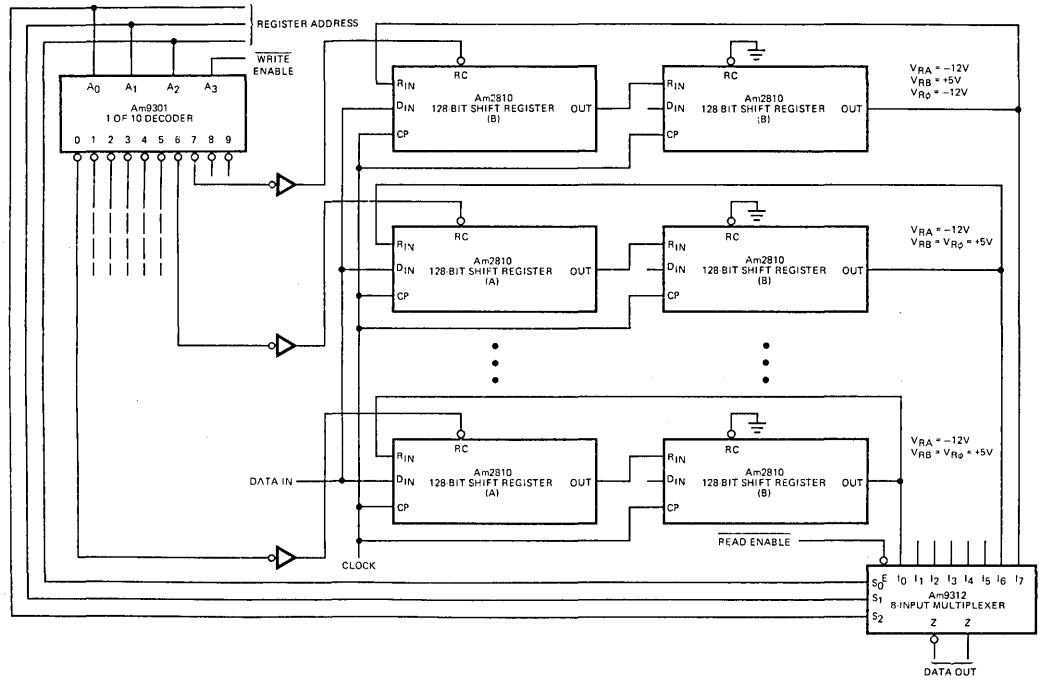
DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS



Eight Register 256-Bit Memory System

Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Note that the $V_{R\phi}$ input is connected to V_{GG} on only one device; the pull-up resistor on this device will pull the line up for all the devices. The V_{RB} inputs are all connected to V_{SS}, since only MOS compatibility is needed. The V_{RA} inputs are all connected to V_{GG} because each recirculate input needs a separate pull-up. This also increases the loading on the data input.

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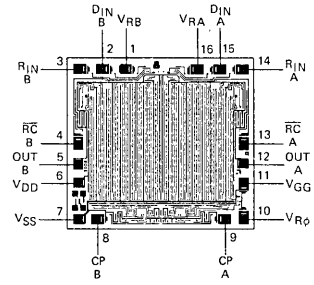
TRUTH TABLE

$\overline{RC}$	R_{IN}	D_{IN}	Data Entered
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

Metallization and Pad Layout



86 X 95 Mils