AX88772BLF / AX88772BLI
Low-Power
USB 2.0 to 10/100M Fast Ethernet Controller

Features

Document No: AX88772B/V1.07/01/21/15

- Single chip USB 2.0 to 10/100M Fast Ethernet controller
- Single chip USB 2.0 to RMII, support HomePNA and HomePlug PHY
- Single chip USB 2.0 to Reverse-RMII, supports glueless MAC-to-MAC connections

- **USB Device Interface**
  - Integrates on-chip USB 2.0 transceiver and SIE compliant to USB Spec 1.1 and 2.0
  - Supports USB Full and High Speed modes with Bus-Power or Self-Power capability
  - Supports 4 or 6 programmable endpoints on USB interface
  - Supports AutoDetach power saving. Detach from USB host when Ethernet cable is unplugged
  - High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (US Patent Approval)

- **Fast Ethernet Controller**
  - Integrates 10/100Mbps Fast Ethernet MAC/PHY
  - IEEE 802.3 10BASE-T/100BASE-TX compatible
  - IEEE 802.3 100BASE-FX compatible
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Embedded SRAM for RX/TX packet buffering
  - Supports IPv4/ IPv6 packet Checksum Offload Engine(COE) to reduce CPU loading, including IPv4 IP/TCP/UDP/ICMP/IGMP & IPv6 TCP/UDP/ICMPv6 checksum check & generation
  - Supports full duplex operation with IEEE 802.3x flow control and half duplex operation with back-pressure flow control
  - Supports 2 VLAN ID filtering, received VLAN Tag (4 bytes) can be stripped off or preserved
  - PHY loop-back diagnostic capability

- **Support Wake-on-LAN Function**
  - Supports Suspend Mode and Remote Wakeup via Link-change, Magic packet, MS wakeup frame and external wakeup pin
  - Supports Protocol Offload (ARP & NS) for Windows 7 Networking Power Management
  - Optional PHY power down during Suspend Mode

- **Versatile External Media Interface**
  - Optional RMII interface in MAC mode allows AX88772B to work with HomePNA and HomePlug PHY
  - Optional Reverse-RMII interface in PHY mode allows AX88772B to support glueless MAC-to-MAC connections

- **Advanced Power Management Features**
  - Supports dynamic power management to reduce power dissipation during idle or light traffic
  - Supports very low power Wake-on-LAN (WOL) mode when the system enters suspend mode and waits for network events to wake it up.

- Supports 256/512 bytes (93c56/93c66) of serial EEPROM (for storing USB Descriptors)
- Supports embedded Device Descriptors ROM and 512 bytes ID-SRAM (online programmable memory for USB Device Descriptors, etc) to save external EEPROM
- Supports automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM after power-on initialization
- Integrates on-chip voltage regulator and only requires a single 3.3V power supply
- Single 25MHz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Small form factor with 64-pin LQFP RoHS compliant package
- Operating commercial temperature range 0˚C to 70˚C or industriure range -40 to +85˚C

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Target Applications

PC/Internet

Consumer Electronics

Figure 1 : Target Applications

Typical System Block Diagrams

- **Hosted by USB to operate with internal Ethernet PHY only**

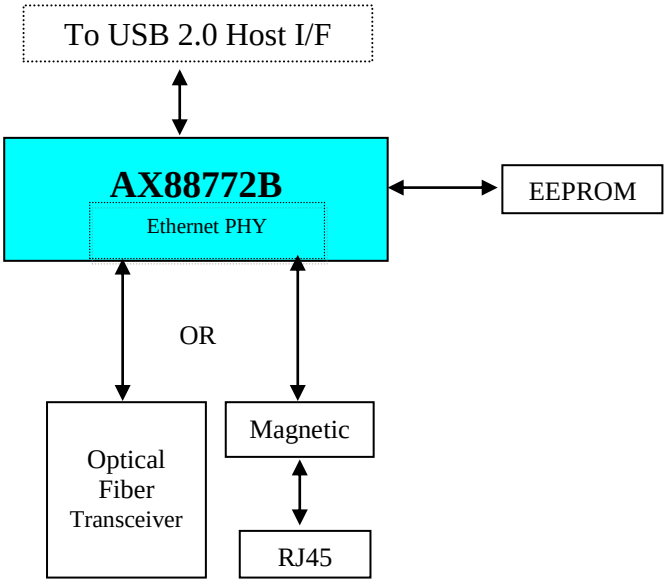

Figure 2 : USB 2.0 to LAN Adaptor (MAC mode)

- **Hosted by USB to operate with either internal Ethernet PHY or RMII (in MAC mode)**

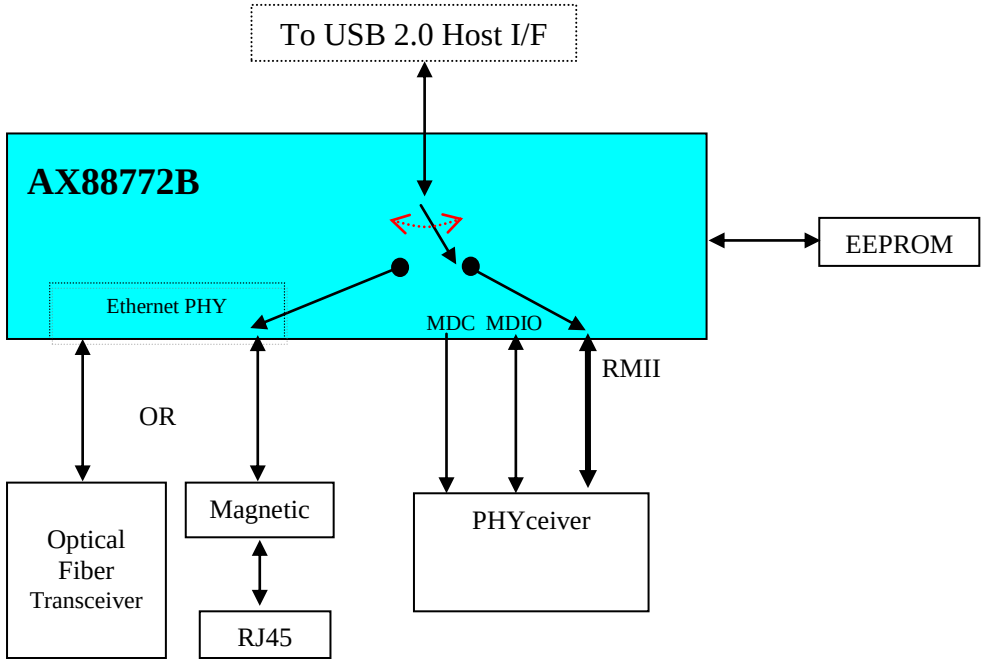

Figure 3 : USB 2.0 to Fast Ethernet and external PHYceiver Combo (MAC mode)

- **Hosted by USB to operate with either internal Ethernet PHY (in MAC mode) or Reverse-RMII (in PHY mode)**

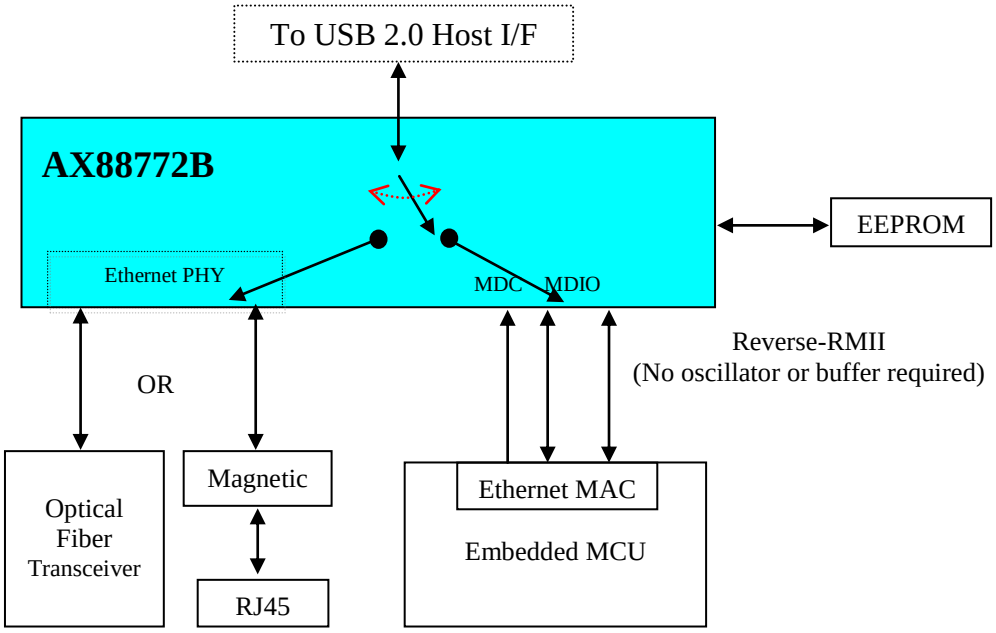

Figure 4 : Bridging Embedded MCU to USB 2.0 Host Interface (PHY mode)

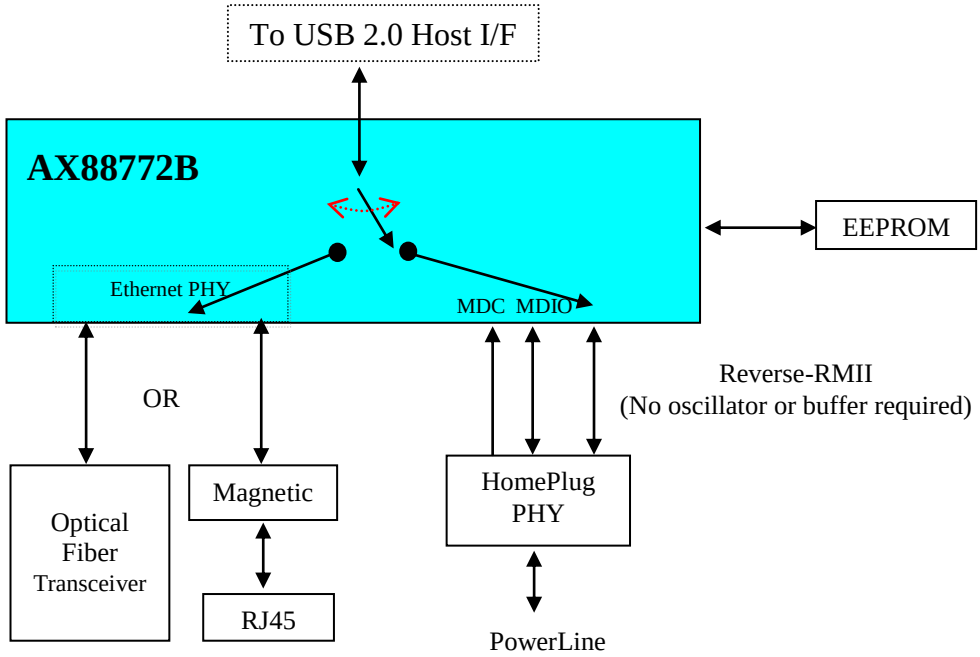

Figure 5 : USB 2.0 to HomePlug Adaptor (PHY mode)

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1 Introduction

1.1 General Description

The AX88772B Low-power USB 2.0 to 10/100M Fast Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play Fast Ethernet network connection capability for desktops, notebook PC's, Ultra-Mobile PC's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88772B features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V1.1 and V2.0. The AX88772B implements a 10/100Mbps Ethernet LAN function based on IEEE802.3, and IEEE802.3u standards with embedded SRAM for packet buffering. The AX88772B integrates an on-chip 10/100Mbps Ethernet PHY to simplify system design.

The AX88772B provides an optional Multi-Function-Bus portion A and B (MFA and MFB) for external PHY or external MAC for different application purposes. The MFA/MFB can be a reduce-media-independent interface (RMII) for implementing HomePlug, HomePNA, etc. functions. The MFA/MFB can also be a Reverse Reduced-MII (Reverse-RMII) for glueless MAC-to-MAC connections to any MCU with Ethernet MAC RMII interface. In addition, the MFA/MFB can be configured as general purpose I/O.

1.2 Block Diagram

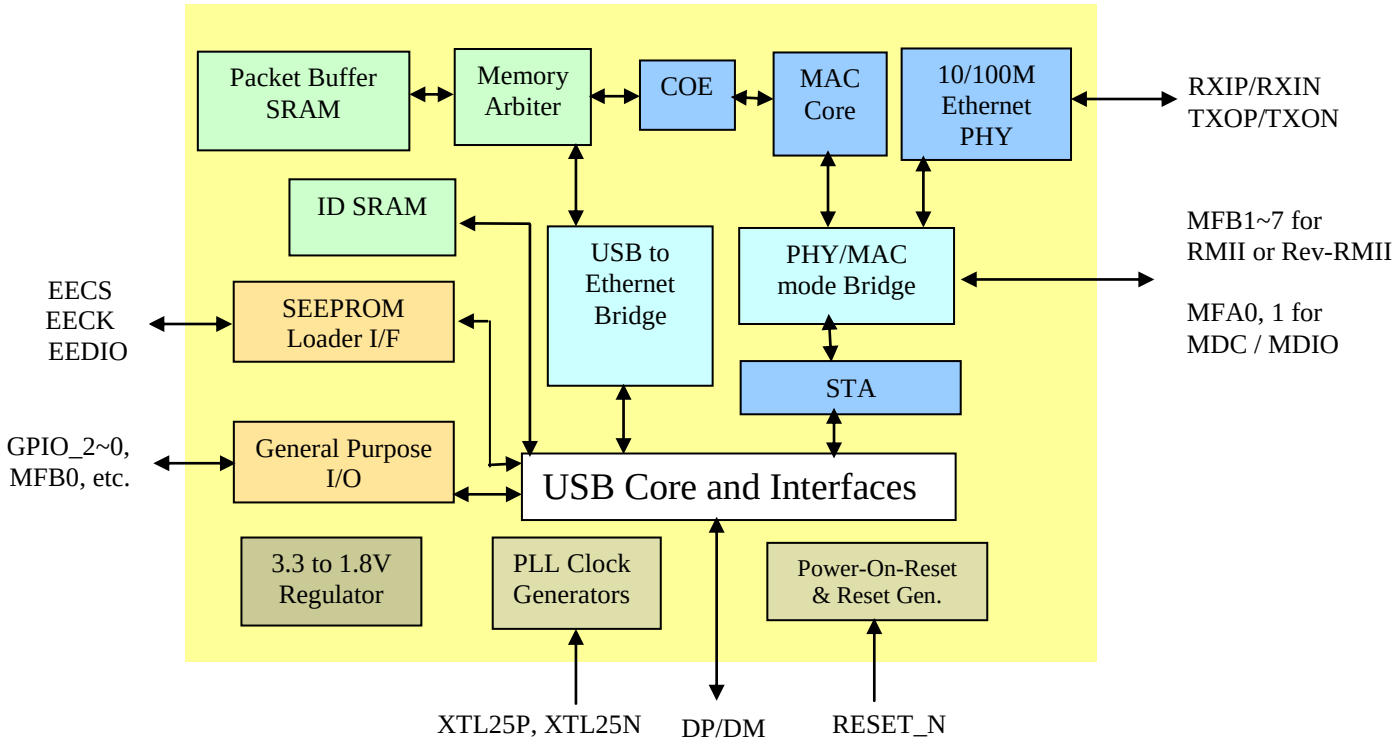


Figure 6 : Block Diagram

1.3 Pinout Diagram

- 64-pin LQFP package

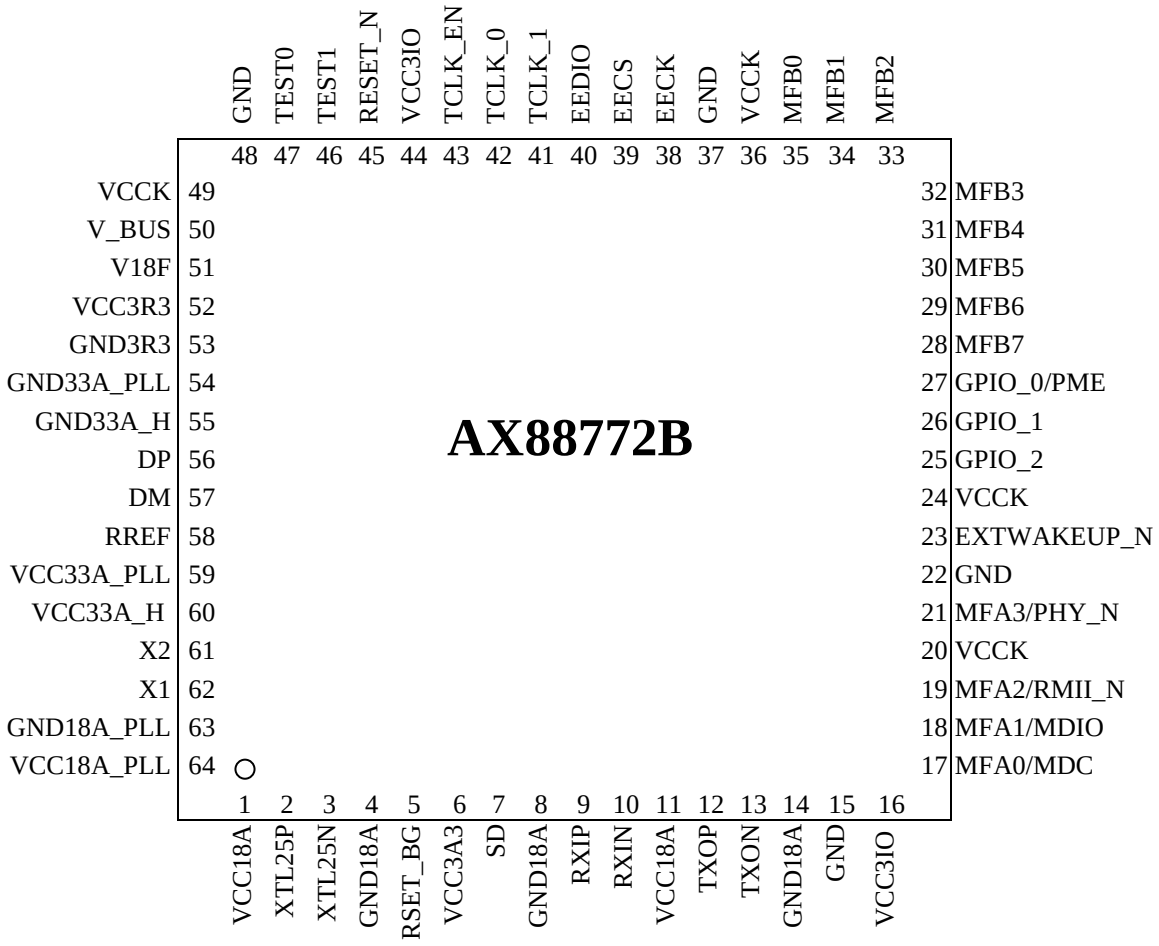


Figure 7 : Pinout Diagram

2 Signal Description

The following abbreviations apply to the following pin description table.

I18	**Input, 1.8V**	**AI**	**Analog Input**
I3	**Input, 3.3V**	**AO**	**Analog Output**
I5	**Input, 3.3V with 5V tolerant**	**AB**	**Analog Bi-directional I/O**
O3	**Output, 3.3V**	**PU**	**Internal Pull Up (75K)**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**PD**	**Internal Pull Down (75K)**
P	**Power Pin**	**S**	**Schmitt Trigger**
		T	**Tri-stateable**

Note: Every output or bi-directional I/O pin is 8mA driving strength.

2.1 Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
DP	AB	56	USB 2.0 data positive pin.
DM	AB	57	USB 2.0 data negative pin.
V_BUS	I5/PD/S	50	VBUS pin input. Please connect to USB bus power.
RREF	AI	58	For USB PHY's internal biasing. Please connect to analog GND through a resistor (12.1Kohm ±1%).
Serial EEPROM Interface			
EECK	B5/PD/T	38	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EECS	B5/PD/T	39	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	40	EEPROM Data In. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
Ethernet PHY Interface			
XTL25P	I18	2	25Mhz ± 0.005% crystal or oscillator clock input. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
XTL25N	O18	3	25Mhz crystal or oscillator clock output.
RXIP	AB	9	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	AB	10	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	AB	12	Transmit data output positive pin for both 10BASE-T and 100 BASE-TX
TXON	AB	13	Transmit data output negative pin for both 10BASE-T and 100 BASE-TX
RSET_BG	AO	5	For Ethernet PHY's internal biasing. Please connect to GND through a 12.1Kohm ±1% resistor.
Misc. Pins			
RESET_N	I5/PU/S	45	Chip reset input. Active low. This is the external reset source used to reset this chip. This input feeds to the internal power-on reset circuitry, which provides the main reset source of this chip. After completing reset, EEPROM data will be loaded automatically.
EXTWAKEUP_N	I5/PU/S	23	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 25MHz clock to be effective.
GPIO_2	B5/PD	25	General Purpose Input/ Output Pin 2.
GPIO_1	B5/PD	26	General Purpose Input/ Output Pin 1. This pin is default as input pin after power-on reset. This pin is also for Default WOL Ready Mode setting; please refer to section 2.2 Settings.

GPIO_0/PME	B5/PD	27	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wake up event detected. Please refer to section 2.2 Settings.
MFB7	B5/PU I5 I5	28	This is a multi-function pin. Please refer to section 2.2 Settings. MFB7: RMII : RXD0 Reverse_RMII : TXD0
MFB6	B5/PU I5 I5	29	This is a multi-function pin. Please refer to section 2.2 Settings. MFB6: RMII : RXD1 Reverse_RMII : TXD1
MFB5/ REF50	B5/PU B5	30	This is a multi-function pin. Please refer to section 2.2 Settings. MFB5: When RMII enable, The REF50 in/out direction is determined by EEPROM Flag [1] setting. Please refer to section 2.2 Settings.
MFB4	B5/PU O3 O3	31	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : TXD0 Reverse_RMII : RXD0
MFB3	B5/PU O3 O3	32	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : TXD1 Reverse_RMII : RXD1
MFB2	B5/PU O3 O3	33	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : TXEN Reverse_RMII : CRSDV
MFB1	B5/PU I5 I5	34	This is a multi-function pin. Please refer to section 2.2 Settings. RMII : CRSDV Reverse_RMII : TXEN
MFB0	B5/PU	35	This is a GPIO pin. Please refer to section 2.2 Settings.
MFA3/ PHY_N	O3 I5/PU	21	It is a multi-function pin. The default is USB Speed indicator. When USB bus is in Full speed, this pin will tri-state continuously. When USB bus is in High speed, this pin drives low continuously. This pin tri-state and drive low in turn (blinking) to indicate TX data transfer going on whenever the host controller sends bulk out data transfer. MFB1~7 bus is determined by setting of this input pin when MFA2 sets 0: 0: Reverse_RMII (PHY mode). 1: RMII (MAC mode). Please refer to PIN configuration of MFA and MFB in section 2.2 Settings.
MFA2/ RMII_N	O3 I5/PU	19	It is a multi-function pin. The default is Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state. MFB1~7 function is determined by setting of this input pin: 0: Reverse_RMII/RMII . 1: MFB bus as GPIO function. Please refer to PIN configuration of MFA and MFB in section 2.2 Settings.
MFA1/ MDIO	O3 B5/PU	18	It is a multi-function pin. The default is Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode. This pin can perform as MDIO when enabling Reverse_RMII/RMII.

MFA0/ MDC	O3 O3 I5/PU	17	It is a multi-function pin. The default is Full Duplex and collision detected LED indicator. This pin drives low when the Ethernet PHY is in full-duplex mode and drives high when in half duplex mode. When in half duplex mode and the Ethernet PHY detects collision, it will be driven low (or blinking). This pin can perform as MDC when enabling Reverse_RMII/RMII: RMII : Output. Reverse_RMII : Input.
SD	I	7	Fiber signal detected Twisted pair operation: Please connect to GND directly or through a resistor. Fiber operation: Please connect to the fiber transceiver signal detect output pin. Please refer to Section 9.1.7 for the detailed SD signal DC Characteristics spec.
TEST0	I5/S	47	Test pin. For normal operation, user should connect to ground.
TEST1	I5/S	46	Test pin. For normal operation, user should connect to ground.
X1	I3	62	Test pin. For normal operation, user should connect to ground.
X2	O3	61	Test pin. No connection
TCLK_EN	I5/PD/S	43	Test pin. For normal operation, user should keep this pin NC.
TCLK_0	I5/PD	42	Test pin. For normal operation, user should keep this pin NC.
TCLK_1	I5/PD	41	Test pin. For normal operation, user should keep this pin NC.
On-chip Regulator Pins			
VCC3R3	P	52	3.3V Power supply to on-chip 3.3V to 1.8V voltage regulator.
GND3R3	P	53	Ground pin of on-chip 3.3V to 1.8V voltage regulator.
V18F	P	51	1.8V voltage output of on-chip 3.3V to 1.8V voltage regulator.
Power and Ground Pins			
VCCK	P	20, 24, 36, 49	Digital Core Power. 1.8V.
VCC3IO	P	16, 44	Digital I/O Power. 3.3V.
GND	P	15, 22, 37, 48	Digital Ground.
VCC33A_H	P	60	Analog Power for USB transceiver. 3.3V.
GND33A_H	P	55	Analog Ground for USB transceiver.
VCC33A_PLL	P	59	Analog Power for USB PLL. 3.3V.
GND33A_PLL	P	54	Analog Ground for USB PLL.
VCC3A3	P	6	Analog Power for Ethernet PHY bandgap. 3.3V.
VCC18A	P	1, 11	Analog Power for Ethernet PHY and 25Mhz crystal oscillator. 1.8V.
GND18A	P	4, 8, 14	Analog Ground for Ethernet PHY and 25Mhz crystal oscillator.
VCC18A_PLL	P	64	Analog Power for USB PLL. 1.8V.
GND18A_PLL	P	63	Analog Ground for USB PLL.

Table 1 : Pinout Description

2.2 Hardware Setting For Operation Mode and Multi-Function Pins

The following hardware settings define the desired function or interface modes of operation for some multi-function pins. The logic level shown on setting pin below is loaded from the chip I/O pins during power on reset based on the setting of the pin's pulled-up (as logic '1') or pulled-down (as logic '0') resister on the schematic.

- Chip Operation Mode setting :

Pin# 19, Pin #21	Operation Modes		Remarks
1x (default)	MAC mode	Internal PHY	The Chip Operation Mode is determined by Pin# 19 (MFA2/RMII_N) and Pin #21 (MFA3/PHY_N) value of AX88772B, which is called hardware setting.
01	MAC mode	RMII	
00	PHY mode	Reverse-RMII	

- EECK pin: USB force to Full Speed mode :

EECK	Description
0	Normal operation (default).
1	USB force to Full Speed mode. External pull-up resistor must be 4.7Kohm.

- GPIO_1 pin: Determines whether this chip will go to Default WOL Ready Mode after power on reset. The WOL stands for Wake-On-LAN.

GPIO_1	Description
0	Normal operation mode (default, see Note 1).
1	Enable Default WOL Ready Mode. Notice that the external pulled-up resistor must be 4.7Kohm. For more details, please refer to APPENDIX A. Default Wake-On-LAN (WOL) Ready Mode

Note 1: This is the default with internal pulled-down resistor and doesn't need an external one.

- EEPROM Flag [12]: Defines the multi-function pin GPIO_0 / PME

GPIO_0 is a general purpose I/O normally controlled by vendor commands. Users can change this pin to operate as a PME (Power Management Event) for remote wake up purpose. Please refer to 4.1.2 Flag of bit 12 (PME_PIN).

- MFA_3 ~ MFA_0 pins: There are 4 multi-function pins for LED display purpose and as GPIO control by vendor command.

PIN Name	Default definition	Vendor Command LED_MUX	Vendor Command VMFAIO	RMII_N enable
MFA3	LED_USB indicater	Sel_LED3	MFAIO_3	-
MFA2	LED_Ethernet_LINK_Active	Sel_LED2	MFAIO_2	-
MFA1	LED_Ethernet_Speed	Sel_LED1	MFAIO_1	MDIO
MFA0	LED_Ethernet_Duplex_Collision	Sel_LED0	MFAIO_0	MDC

Table 2 ：MFA_3 ~ MFA_0 pin configuration

- PIN configuration of MFA and MFB

Pin# 19 MFA2/RMII_N	Pin #21 MFA3/PHY_N	Description		
1: MFB7~MFB0 0: RMII	1: MAC Mode 0: PHY Mode	PIN Name	Function	Pin Type
1	X	MFB0	MFBIO0	Bidirection, controlled by MFBIOEN0
1	X	MFB1	MFBIO1	Bidirection, controlled by MFBIOEN1
1	X	MFB2	MFBIO2	Bidirection, controlled by MFBIOEN2
1	X	MFB3	MFBIO3	Bidirection, controlled by MFBIOEN3
1	X	MFB4	MFBIO4	Bidirection, controlled by MFBIOEN4
1	X	MFB5	MFBIO5	Bidirection, controlled by MFBIOEN5
1	X	MFB6	MFBIO6	Bidirection, controlled by MFBIOEN6
1	X	MFB7	MFBIO7	Bidirection, controlled by MFBIOEN7
1	X	MFA0	Refer to MFA Configuration	
1	X	MFA1	Refer to MFA Configuration	
1	X	MFA2	Refer to MFA Configuration	
1	X	MFA3	Refer to MFA Configuration	
0	1	MFB0	MFBIO0	Bidirection, controlled by MFBIOEN0
0	1	MFB1	CRSDV	Input
0	1	MFB2	TXEN	Output
0	1	MFB3	TXD1	Output
0	1	MFB4	TXD0	Output
0	1	MFB5	REF50	Input/Output control by EEPROM flag[1]
0	1	MFB6	RXD1	Input
0	1	MFB7	RXD0	Input
0	1	MFA0	MDC	Output
0	1	MFA1	MDIO	I/O
0	0	MFB0	MFBIO0	Bidirection, controlled by MFBIOEN0
0	0	MFB1	TXEN	Input
0	0	MFB2	CRSDV	Output
0	0	MFB3	RXD1	Output
0	0	MFB4	RXD0	Output
0	0	MFB5	REF50	Input/Output control by EEPROM flag[1]
0	0	MFB6	TXD1	Input
0	0	MFB7	TXD0	Input
0	0	MFA0	MDC	Input
0	0	MFA1	MDIO	I/O

3 Function Description

3.1 USB Core and Interface

The USB core and interface contains a USB 2.0 transceiver, serial interface engine (SIE), USB bus protocol handshaking block, USB standard command, vendor command registers, logic for supporting bulk transfer, and an interrupt transfer, etc. The USB interface is used to communicate with a USB host controller and is compliant with USB specification V1.1 and V2.0.

3.2 10/100M Ethernet PHY

The 10/100M Fast Ethernet PHY is compliant with IEEE 802.3 and IEEE 802.3u standards. It contains an on-chip crystal oscillator, PLL-based clock multiplier, and a digital phase-locked loop for data/timing recovery. It provides over-sampling mixed-signal transmit drivers compliant with 10/100BASE-TX transmit wave shaping / slew rate control requirements. It has a robust mixed-signal loop adaptive equalizer for receiving signal recovery. It contains a baseline wander corrective block to compensate data dependent offset due to AC coupling transformers. It supports auto-negotiation and auto-MDIX functions.

3.3 MAC Core

The MAC core supports 802.3 and 802.3u MAC sub-layer functions, such as basic MAC frame receive and transmit, CRC checking and generation, filtering, forwarding, flow-control in full-duplex mode, and collision-detection and handling in half-duplex mode, etc. It provides a reduce-media-independent interface (RMII) for implementing Fast Ethernet and HomePNA functions.

The MAC core interfaces to external RMII/Reverse-RMII interfaces and the embedded 10/100M Ethernet PHY. The selection among the interfaces is done via setting Pin# 19 (MFA2/RMII_N) and Pin #21 (MFA3/PHY_N) of AX88772B package pinout during power on reset (see 2.2) and using the USB vendor command, Software Interface Selection register. Figure 8 shows the data path diagram of 10/100M Ethernet PHY and RMII/Reverse-RMII interfaces to MAC core.

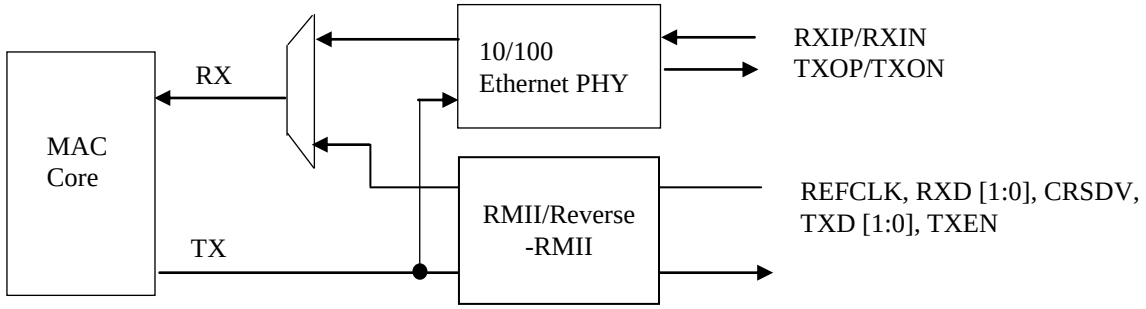


Figure 8 : Internal Data path Diagram of 10/100M Ethernet PHY and RMII/Reverse-RMII Interfaces

3.4 Checksum Offload Engine (COE)

The Checksum Offload Engine (COE) supports IPv4, IPv6, layer 4 (TCP, UDP, ICMP, ICMPv6 and IGMP) header processing functions and real time checksum calculation in hardware

The COE supports the following features in layer 3:

- IP header parsing, including IPv4 and IPv6
- IPv6 routing header type 0 supported
- IPv6 in IPv4 tunnel supported
- IPv4 header checksum check and generation (There is no checksum field in IPv6 header)
- Version error detecting on RX direction for IP packets with version != 4 or 6
- Detecting on RX direction for IP packets with error header checksum

The COE supports the following features in layer 4:

- TCP and UDP checksum check and generation for non-fragmented packet
- ICMP, ICMPv6 and IGMP message checksum check and generation for non-fragmented packet
- Packet filtering or checksum error indication on RX direction for TCP/UDP/ICMP/ICMPv6/IGMP packets with error checksum

3.5 Operation Mode

For simple USB 2.0 to Ethernet applications, user can use the AX88772B, which operates with internal Ethernet PHY.

AX88772B supports following three operation modes: (Ref. 2.2 Hardware Setting For Operation Mode And Multi-Function Pins)

1. MAC mode
2. PHY mode

Below provides a detailed description for the three operation modes:

- In MAC mode, the AX88772B Ethernet block is configured as an Ethernet MAC. From a system application standpoint, AX88772B can be used as a USB 2.0 to LAN Adaptor (see Figure 2) or a USB 2.0 to Fast Ethernet and HomePNA Combo (see Figure 3).

  In MAC mode, the AX88772B internal datapath can work with internal Ethernet PHY or RMII interface by setting Software Interface Selection register. Note that the PHY_ID for the internal Ethernet PHY and external one are defined in below Table 3. Please refer to below Figure 9, Figure 10 for RMII example.

- In PHY mode, the AX88772B Ethernet block is configured as an Ethernet PHY interface. In this case, an external microcontroller with Ethernet MAC can interface with AX88772B as if it were to interface with an Ethernet PHY chip, and AX88772B can act as a USB to Reverse-RMII bridge chip for the microcontroller to provide USB 2.0 device interface for some system applications (see Figure 4).
  Please refer to below Figure 11, Figure 12 for Reverse-RMII example.

STA PHY_ID	MAC mode	PHY mode
Embedded Ethernet PHY PHY_ID [4:0]	10h	10h
External Media Interface PHY_ID [4:0]	{Secondary PHY_ID [4:0]}	{Secondary PHY_ID [4:1], 0}

Note: The value of Secondary PHY_ID [4:0] is defined in EEPROM memory map 4.1.6

Table 3 : PHY_ID Definition Source

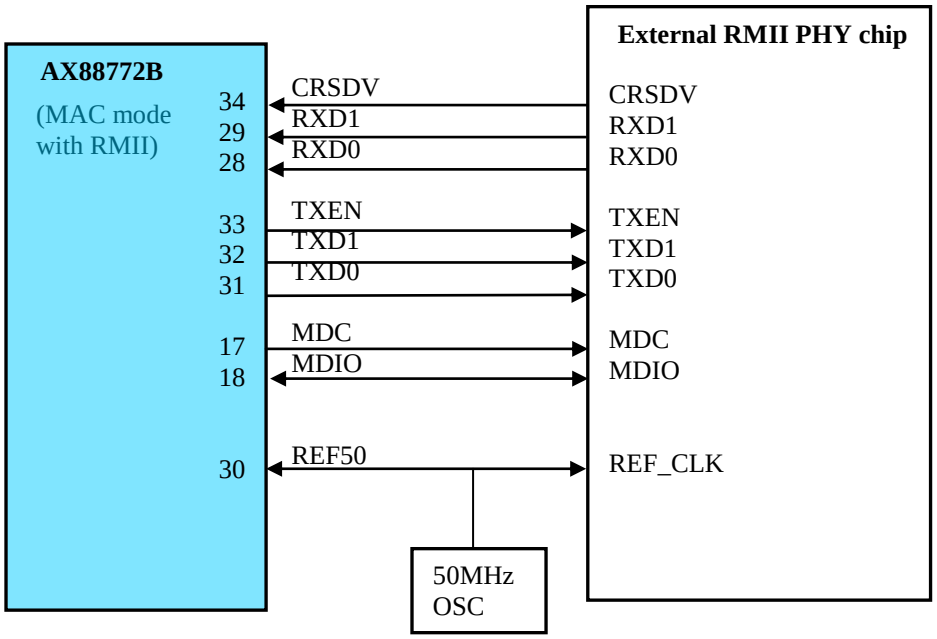


Figure 9 : RMII to External PHY chip with 50MHz OSC

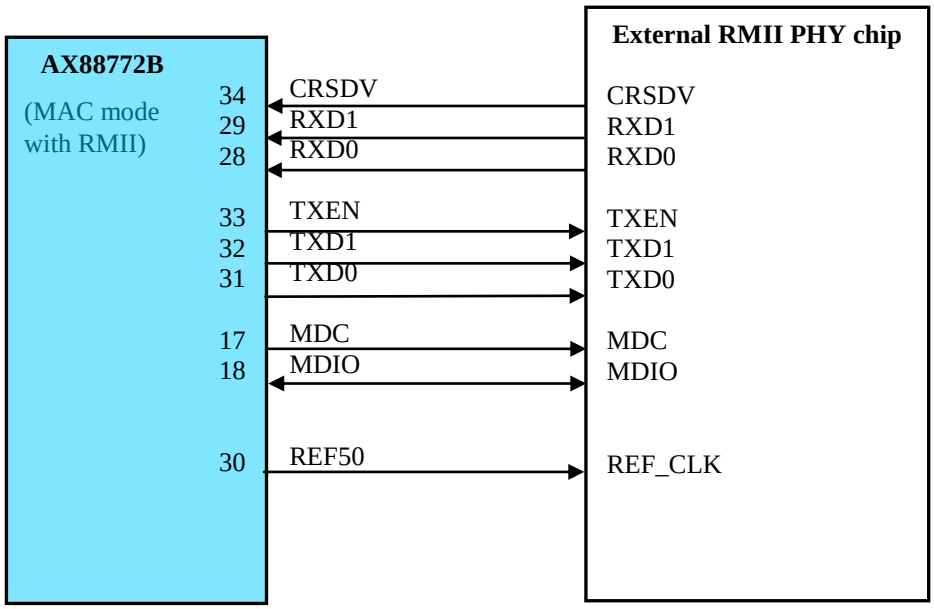


Figure 10 : RMII Interface to External PHY chip

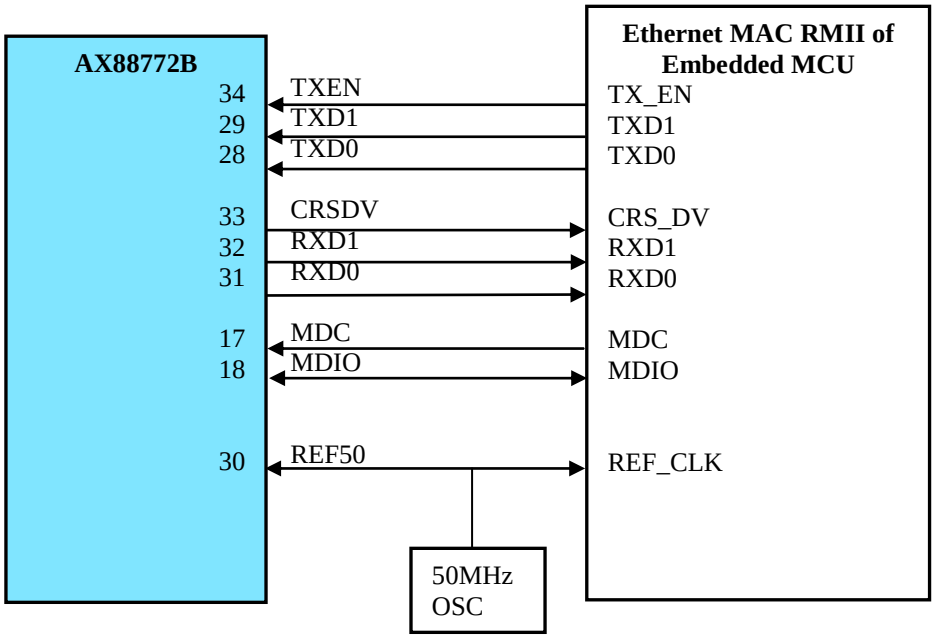


Figure 11 : Reverse-RMII to External MAC Device with 50MHz OSC

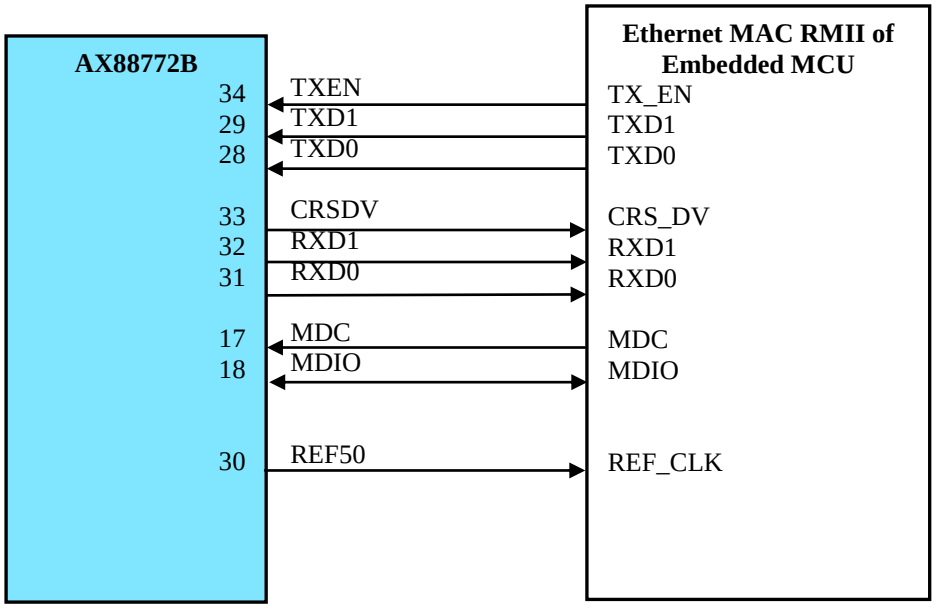


Figure 12 : Reverse-RMII Interface to External MAC Device

3.6 Station Management (STA)

The Station Management interface provides a simple, two-wire, serial interface to connect to a managed PHY device for the purpose of controlling the PHY and gathering status from the PHY. The Station Management interface allows communicating with multiple PHY devices at the same time by identifying the managed PHY with 5-bit, unique PHY_ID. The PHY ID of the embedded 10/100M Ethernet PHY is being pre-assigned to "1_0000".

The Figure 13 shows the internal control MUX of the Station Management interface when doing read in MAC operation mode, the "mdin" signal will be driven from the embedded 10/100M Ethernet PHY only if PHY ID matches with "1_0000", otherwise, it will always be driven from the external MDIO pin of the ASIC.

The Station Management unit also reports the basic PHY status when operating in PHY mode acting as a PHY role (see Figure 14). For detailed register description, please refer to the Station Management Registers in PHY mode (section 0).

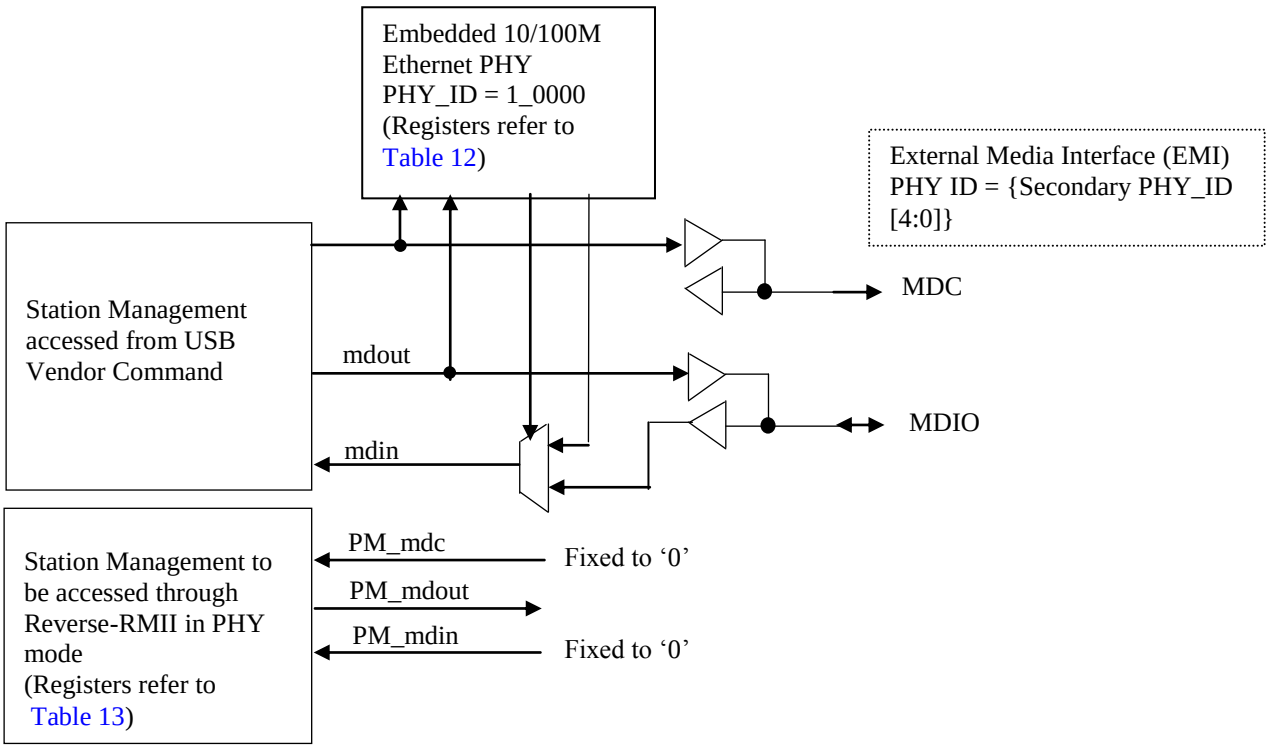


Figure 13 : Internal Control MUX of Station Management Interface in MAC mode

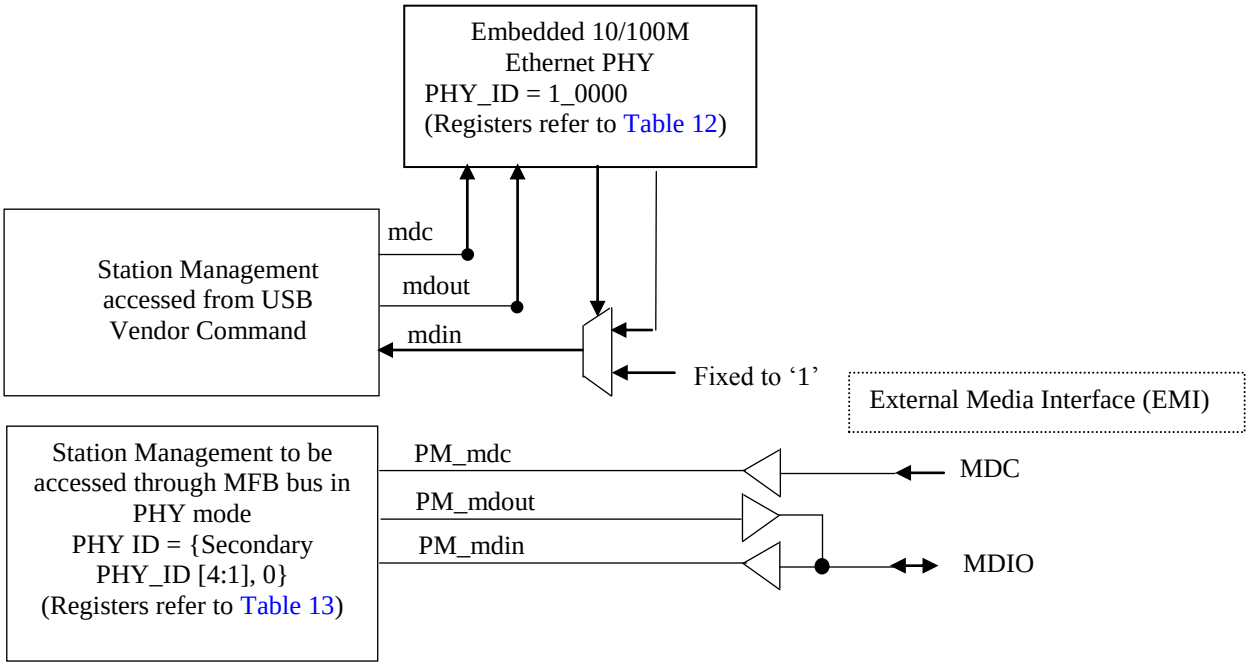


Figure 14 : Internal Control MUX of Station Management Interface in PHY mode

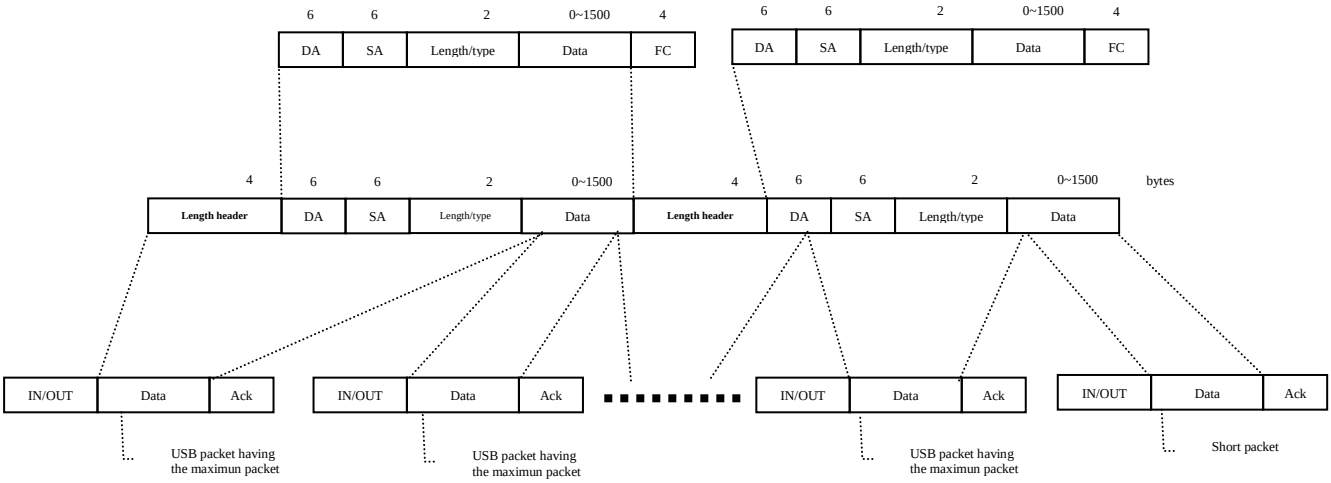
3.7 Memory Arbiter

The memory arbiter block is responsible for storing received MAC frames into on-chip SRAM (packet buffer) and then forwarding it to the USB bus upon request from the USB host via Bulk In transfer. It also monitors the packet buffer usage in full-duplex mode for triggering PAUSE frame (or in half-duplex mode to activate Backpressure jam signal) transmission out on TX direction. The memory arbiter block is also responsible for storing MAC frames received from the USB host via Bulk Out transfer and scheduling transmission out towards Ethernet network.

3.8 USB to Ethernet Bridge

The USB to Ethernet bridge block is responsible for converting Ethernet MAC frame into USB packets or vice-versa. This block supports proprietary burst transfer mechanism (US Patent Approval) to offload software burden and to offer very high packet transfer throughput over USB bus.

3.8.1 Ethernet/USB Frame Format Bridge



3.9 Serial EEPROM Loader

The serial EEPROM loader is responsible for reading configuration data automatically from the external serial EEPROM after power-on reset. If the content of EEPROM offset 0x00 (low byte of first word) is 0x00 or 0xFF, the Serial EEPROM Loader will not auto-load the EEPROM. If the content of EEPROM offset 0x18 (low byte of 18th word) is not equal to (0xFF - SUM [EEPROM offset 07H ~ 0EH]). In that case, the chip internal default value will be used to configure the chip operation setting and to respond to USB commands, etc.

3.10 General Purpose I/O

There are 3 general-purpose I/O pins (named GPIO_0/1/2), 8 multi-function pins group B (named MFB0/1/2/3/4/5/6/7) and 4 multi-function pins group A (named MFA0/1/2/3) provided by this ASIC.

3.11 Clock Generation

The AX88772B integrates internal oscillator circuits for 25Mhz, respectively, which allow the chip to operate cost effectively with just external 25Mhz crystals. There are also three PLL circuits integrated in the chip to generate precise clocks.

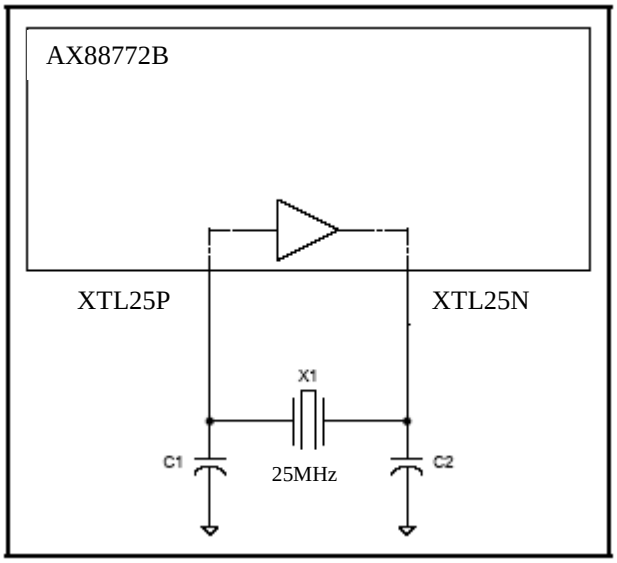
The external 25Mhz crystal or oscillator, via pins XTL25P/XTL25N, provides the reference clock to the other two internal PLL circuit to generate a free-run 100Mhz clock source for the Reverse-RMII/RMII modes of AX88772B and a 125Mhz clock source for the embedded Ethernet PHY use.

The AX88772B can provide REF50 (50Mhz output) in Reverse-RMII/RMII modes. This output clock is derived from the internal 100Mhz PLL circuit.

The external 25Mhz Crystal spec is listed in below table. For more details on crystal timing, please refer to 9.5.1 Clock Timing and AX88772B Demo board schematic reference.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25℃)		±30ppm
Frequency Stability Over Operating Temperature Range		±30ppm
Equivalent Series Resistance	ESR	70 Ohm max.
Load Capacitance	CL	20pF
Operation Temperature Range		0℃ ~ +70℃, Commerical version
		-40℃ ~ +85℃, Industrial version
Aging		±3ppm/year

Table 4 : The external 25MHz Crystal Units specifications



For the 25MHz oscillator, its feedback resistor isn't integrated into the 25MHz oscillator, so it is necessary to add feedback resistor on external circuit.

To implement the external circuits of 25MHz crystal please refer to below. One external 1Mohm resistor on 25MHz crystal oscillator is required.

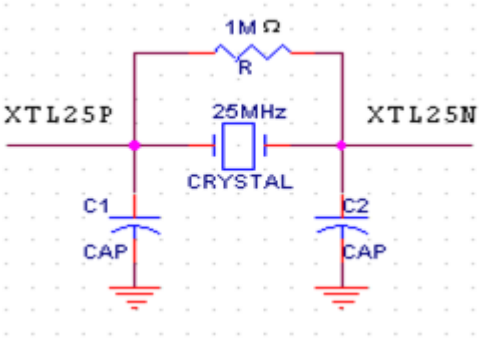


Figure 15 : One external 1M ohm resistor on 25MHz crystal oscillator is necessary

3.12 Reset Generation

The AX88772B integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset system logic after 1.8V core power ramping up to 1.2V (typical threshold). The external hardware reset input pin, RESET_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. For more details on RESET_N timing, please refer to 9.5.2 Reset Timing.

3.13 Voltage Regulator

The AX88772B contains an internal 3.3V to 1.8V low-dropout-voltage and low-standby-current voltage regulator. The internal regulator provides up to 150mA of driving current for the 1.8V core/analog power of the chip to satisfy the worst-case power consumption scenario. For more details on voltage regulator DC characteristic, please refer to 9.1.6 DC Characteristics of Voltage Regulator.

4 Serial EEPROM Memory Map

EEPROM OFFSET	HIGH BYTE		LOW BYTE	
00H	0x5A		0x15	
01H	Flag			
02H	Length of High-Speed Device Descriptor (bytes)		EEPROM Offset of High-Speed Device Descriptor	
03H	Length of High-Speed Configuration Descriptor (bytes)		EEPROM Offset of High-Speed Configuration Descriptor	
04H	Node ID 1		Node ID 0	
05H	Node ID 3		Node ID 2	
06H	Node ID 5		Node ID 4	
07H	Language ID High Byte		Language ID Low Byte	
08H	Length of Manufacture String (bytes)		EEPROM Offset of Manufacture String	
09H	Length of Product String (bytes)		EEPROM Offset of Product String	
0AH	Length of Serial Number String (bytes)		EEPROM Offset of Serial Number String	
0BH	Length of Configuration String (bytes)		EEPROM Offset of Configuration String	
0CH	Length of Interface 0 String (bytes)		EEPROM Offset of Interface 0 String	
0DH	Length of Interface 1/0 String (bytes)		EEPROM Offset of Interface 1/0 String	
0EH	Length of Interface 1/1 String (bytes)		EEPROM Offset of Interface 1/1 String	
0FH	EtherPhyMode [2:0]	PHY Register Offset 1 for Interrupt Endpoint	100	PHY Register Offset 2 for Interrupt Endpoint
10H	5'b0	Max Packet Size High Byte[10:8]	Max Packet Size Low Byte[7:0]	
11H	Secondary PHY_Type [7:5] and PHY_ID [4:0]		Primary PHY_Type [7:5] and PHY_ID [4:0]	
12H	Pause Frame Free Buffers High Water Mark		Pause Frame Free Buffers Low Water Mark	
13H	Length of Full-Speed Device Descriptor (bytes)		EEPROM Offset of Full-Speed Device Descriptor	
14H	Length of Full-Speed Configuration Descriptor (bytes)		EEPROM Offset of Full-Speed Configuration Descriptor	
15H~17H	Reserved		Reserved	
18H	Ethernet PHY Power Saving Configuration		EEPROM Checksum	

Note: To store the endpoint 5 descriptors, 93C66 (512-byte) is recommended.

Table 5 : Serial EEPROM Memory Map

- The value of EEPROM Checksum field, EEPROM offset 0x18 (low byte) = (0xFF - SUM [EEPROM offset 07H ~ 0EH])
- The value of Ethernet PHY Power Saving Configuration field (i.e. high byte of EEPROM offset 0x18) is equal to 2nd byte of Vendor Command 0x20. The AX88772B driver will read this field from high byte of EEPROM offset 0x18 and then writes it to 2nd byte of Vendor Command 0x20 at the end of driver initialization routine and during Suspend mode configuration. This field doesn't affect AX88772B before the driver writes it to Vendor Command 0x20.

Ethernet PHY Power Saving Configuration field

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
WOLLP	0	IPFPS	AutoDetach	IPCOPSC	IPCOPS	IPPSL_1	IPPSL_0

4.1 Detailed Description

The following sections provide detailed descriptions for some of the fields in serial EEPROM memory map. For other fields not covered here, please refer to the **AX88772B EEPROM User Guide** for more details.

4.1.1 Word Count for Preload (00h)

The number of words to be preloaded by the EEPROM loader = 15h.

4.1.2 Flag (01h)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PME_IND	PME_TYP	PME_POL	PME_PIN	PHY_ISO	1	TDPE	CEM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TACE	RDCE	EPOM	BOTM_EN	1	RWU	REF50_O	SP

SP: Self-Power (for USB standard command Get Status)
1: Self power (default).
0: Bus power.
REF50_O: RMII reference 50MHz clock direction
1: Sets AX88772B provides RMII reference 50MHz clock.
0: Sets AX88772B RMII reference clock source from external 50MHz clock source (default).
RWU: Remote Wakeup support.
1: Indicate that this device supports Remote Wakeup (default).
0: Not support.
BOTM_EN: Enable the bulk-type endpoint for BOTM
1: Enable (default). Please refer to 0 .
0: Disable.
EPOM: Embedded PHY copper/fiber Operation Mode
1: Sets embedded PHY in copper mode (default).
0: Sets embedded PHY in fiber mode
RDCE: RX Drop CRC Enable.
1: CRC byte is dropped on received MAC frame forwarding to host (default).
0: CRC byte is not dropped.
TACE: TX Append CRC Enable.
1: CRC byte is generated and appended by the ASIC for every transmitted MAC frame (default).
0: CRC byte is not appended.
CEM: Capture Effective Mode.
1: Capture effective mode enables (default).
0: Disabled.
TDPE: Test Debug Port Enable.
1: Enable test debug port for chip debug purpose.
0: Disable test debug port and the chip operate in normal function mode (default).
PHY_ISO: Set RMII bus to isolate mode when operating in PHY mode.
1: Set RMII bus to isolate mode (default). AX88772B can be in isolate mode when operating in PHY mode with Reverse-RMII. Following output pins are tri-stated in isolate mode.
In Reverse-RMII mode: RXD [1:0] and CRSDV, RXER, except for REF50.
0: Set RMII bus to non-isolate mode.

PME_PIN: PME / GPIO_0
1: Set GPIO_0 pin as PME (default).
0: GPIO_0 pin is controlled by vendor command.
PME_POL: PME pin active Polarity.
1: PME active high.
0: PME active low (default).
PME_TYP: PME I/O Type.
1: PME output is a Push-Pull driver.
0: PME output to function as an open-drain buffer (default).
PME_IND: PME indication.
1: A 1.363ms pulse active when detecting wake-up event.
0: A static signal active when detecting wake-up event (default).

4.1.3 Node ID (04~06h)

The Node ID 0 to 5 bytes represent the MAC address of the device, for example, if MAC address = 01-23-45-67-89-ABh, then Node ID 0 = 01, Node ID 1 = 23, Node ID 2 = 45, Node ID 3 = 67, Node ID 4 = 89, and Node ID 5 = AB.

Default values: Node ID {0, 1, 2, 3, 4, 5} = 0x000E_C687_7201.

4.1.4 PHY Register Offset for Interrupt Endpoint (0Fh)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
EtherPhyMode			PHY Register Offset 1				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100			PHY Register Offset 2				

PHY Register Offset 1: Fill in PHY's Register Offset of Primary PHY here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 5 and 6 of Interrupt Endpoint packet (default = 00101)
PHY Register Offset 2: Fill in PHY's Register Offset of Primary PHY here. Upon each Interrupt Endpoint issued, its register value will be reported in byte# 7 and 8 of Interrupt Endpoint packet (default = 00000)

EtherPhyMode: as below table (default = 000),

EtherPhyMode [2:0]	Function
000	Auto-negotiation enable with all capabilities
001	Auto-negotiation with 100BASE-TX FDX / HDX ability
010	Auto-negotiation with 10BASE-TX FDX / HDX ability
011	Reserved
100	Manual selection of 100BASE-TX FDX
101	Manual selection of 100BASE-TX HDX
110	Manual selection of 10BASE-T FDX
111	Manual selection of 10BASE-T HDX

Note:
1. EtherPhyMode is used to set the operation mode of embedded Ethernet PHY directly. For normal operation mode, set them to 000.
2. This value is latched into embedded Ethernet PHY right after it leaves reset. After that, software driver can still make change Ethernet PHY link ability through vendor command PHY Write Register to access embedded Ethernet PHY register.

4.1.5 Max Packet Size High/Low Byte (10h)

Fill the maximum RX/TX MAC frame size supported by this ASIC. The number must be even number in terms of bytes and should be less than or equal to 2048 bytes (default = 0600h).

4.1.6 Primary/Secondary PHY_Type and PHY_ID (11h)

The 3 bits PHY_Type field for both Primary and Secondary PHY is defined as follows,
000: 10/100M Ethernet PHY or 1M HomePNA PHY.
111: non-supported PHY. For example, the High Byte value of "E0h" means that secondary PHY is not supported.
Default values: Primary {PHY_Type, PHY_ID} = 10h. Secondary {PHY_Type, PHY_ID} = E0h. Note that the PHY_ID of the embedded 10/100M Ethernet PHY is being assigned to "10h".

Secondary PHY_ID always defines The PHY_ID of External Media Interface (EMI) and Secondary PHY_TYPE is not used in that case. Please refer to Table 3 for more information.

4.1.7 Pause Frame Free Buffers High Water and Low Water Mark (12H)

When operating in full-duplex mode, correct setting of this field is very important and can affect the overall packet receive throughput performance a great deal. The High Water Mark is the threshold to trigger sending Pause frame and the Low Water Mark is the threshold to stop sending Pause frame. Note that each free buffer count here represents 128 bytes of packet storage space in SRAM.

These setting values are also used in half-duplex mode to activate Backpressure to send /stop jam signal.

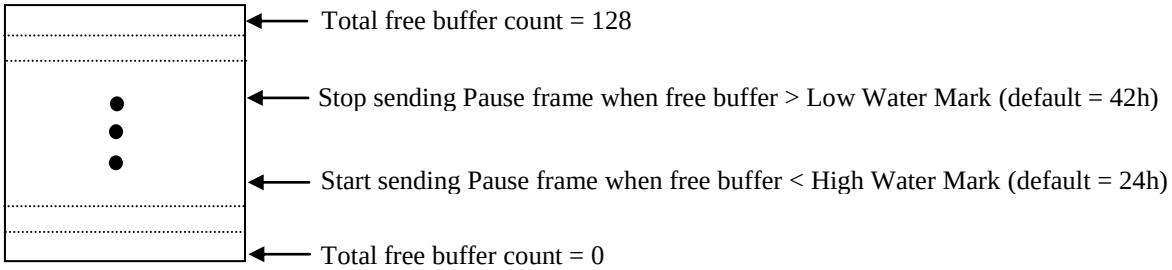


Figure 16 : Water level setting for flow control

4.1.8 Power-Up Steps

After power-on reset, AX88772B will automatically perform the following steps to the Ethernet PHYs via MDC/MDIO lines (only take effect when Chip Operation Mode is in MAC mode with external PHY on RMII interface).

1. Write to PHY_ID of 00h with PHY register offset 00h to power down all PHYs attached to station management interface.
2. Write to Primary PHY_ID with PHY register offset 00h to power down Primary PHY.
3. Write to Secondary PHY_ID with PHY register offset 00h to power down Secondary PHY.

Notice that enabling Default WOL Ready Mode (see 2.2 GPIO_1 Settings) will disable above power-up step (to prevent external Ethernet PHY on RMII interface from entering power-down mode), if external PHY is used.

4.2 Internal ROM Default Settings

AX88772B supports some default settings inside chip hardware to enable it to communicate with USB host controller during enumeration when the AX88772B EEPROM is blank (prior to being programmed) or the value of EEPROM Checksum field is wrong. The default settings inside chip facilitate users to update the EEPROM content through a Windows PC during R&D validation process or program a blank EEPROM mounted on target system PCB during manufacturing process.

Below table shows AX88772B's internal default settings being used in the case of blank EEPROM or EEPROM with wrong checksum value on board. Each of the address offset contains 16-bit data from left to right representing the low-byte and high-byte, respectively. For example, in offset address 0x01, the 'FD' is low-byte data and the '1D' is high-byte data.

Offset Address	0 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
0x00 0x08	15 00 6E 22	FD 1D 7F 12	20 12 19 0E	29 35 44 04	00 0E 44 04	C6 87 44 04	72 01 44 04	09 04 80 05
0x10 0x18	00 06 FF 08	10 E0 0E 03	42 24 30 00	47 12 30 00	50 35 30 00	FF FF 30 00	00 00 30 00	FF FF 31 00
0x20 0x28	12 01 03 01	00 02 09 02	FF FF 35 00	00 40 01 01	95 0B 04 E0	2B 77 02 09	01 00 04 00	01 02 00 05
0x30 0x38	FF FF 02 00	00 07 07 05	07 05 03 02	81 03 00 02	08 00 00 07	0B 07 05 84	05 82 02 00	02 00 02 00
0x40 0x48	07 05 00 02	05 02 FF FF	00 02 00 08	00 FF 95 0B	04 03 2B 77	30 00 01 00	FF FF 01 02	12 01 03 01
0x50 0x58	09 02 00 07	35 00 07 05	01 01 81 03	04 E0 08 00	02 09 A0 07	04 00 05 82	00 05 02 40	FF FF 00 00
0x60 0x68	07 05 05 02	03 02 40 00	40 00 00 DD	00 07 FF FF	05 84 AA AA	02 40 BB BB	00 00 22 03	07 05 41 00
0x70 0x78	53 00 2E 00	49 00 20 00	58 00 43 00	20 00 6F 00	45 00 72 00	6C 00 70 00	65 00 2E 00	63 00 12 03
0x80	41 00	58 00	38 00	38 00	37 00	37 00	32 00	42 00
0x88~FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF

Table 6 : Internal ROM Memory Map

Note:

1. The default high-byte data of offset 0x00 is 0x00.
2. The bulk out endpoint 5 enabled since bit 4 (BOTM_EN) of offset 01h is set to 1.
3. The default PID/VID is 772Bh/0B95h.
4. The default MAC address is 00-0E-C6-87-72-01, but the real MAC address is 00-00-00-00-00-00 that was auto-loaded from the AX88772B internal ROM default setting into the AX88772B Node ID register. User should manually assign a valid MAC address through the AX88772B driver parameter or by setting AX88772B Node ID register for normal network operation.
5. The default Manufacture string is "ASIX Elec. Corp.".
6. The default Product string is "AX88772B".
7. The default Serial Number is "000001".
8. The default operation mode is set to Self-Power and Remote Wakeup enabled.
9. Max Power setting to 4mA. Expressed in 2mA (for example, 0x02 indicates for 4mA)
10. The default "AutoDetach" function is disabled and set to Cable Off Power Saving Level 0.
11. The default value of EEPROM Checksum field is 0xFF.

4.2.1 Internal ROM Description

The internal ROM is a fixed value. **User can't modify it.**

Field Definition	Address Offset	Default Values	Description
Vender ID (VID)	0x24 0x4B	95 0B	ASIX's VID is 0x0B95
Product ID (PID)	0x25 0x4C	2B 77	The PID of AX88772B is 0x772B
Node ID	0x04 ~0x06	00 0E C6 87 72 01	Node ID 0 ~ 5
Power Mode/Remote Wakeup/Copper or Fiber Mode	0x01 0x2C 0x53	FD 1D E0 (high-byte only) E0 (high-byte only)	Self-Power mode, Enable the "remote wakeup" function, Copper Mode (Note 1)
Max Power under High Speed Mode	0x2D	02 (low-byte only)	4mA (Note 2)
Max Power under Full Speed Mode	0x54	02 (low-byte only)	4mA (Note 2)
Ethernet PHY Type/ID	0x11	10 E0	Primary PHY ID is 0x10 Secondary PHY is not supported
Manufacture String	0x6E~0x7E	22 03 41 00 53 00 49 00 58 00 20 00 45 00 6C 00 65 00 63 00 2E 00 20 00 43 00 6F 00 72 00 70 00 2E 00	"ASIX Elec. Corp."
Product String	0x7F~0x87	12 03 41 00 58 00 38 00 38 00 37 00 37 00 32 00 42 00	"AX88772B"
Serial Number String	0x19~0x1F	0E 03 30 00 30 00 30 00 30 00 30 00 31 00	"000001"
Ethernet PHY Power Saving Configuration	0x18	08 (high-byte only)	Disable "AutoDetach" Set to Cable Off Power Saving Level 0

Table 7 : Internal ROM Description

Note 1: Power Mode/Remote Wakeup/PME Settings

The offset 0x01 field of AX88772B EEPROM is used to configure the Power mode (i.e. Bus-power or Self-power), Remote Wakeup and PME functions. Please refer to datasheet Section 4 "Serial EEPROM Memory Map" for the detailed description of EEPROM offset 0x01.

The high byte of AX88772B EEPROM offset 0x2C and 0x53 fields are used to configure the "bmAttributes" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus Spec Rev 2.0 for the detailed description of the "bmAttributes" field of Standard Configuration Descriptor.

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
7	*bmAttributes*	1	Bitmap	Configuration characteristics D7: Reserved (set to one) D6: Self-powered D5: Remote Wakeup D4...0: Reserved (reset to zero) D7 is reserved and must be set to one for historical reasons. A device configuration that uses power from the bus and a local source reports a non-zero value in *bMaxPower* to indicate the amount of bus power required and sets D6. The actual power source at runtime may be determined using the GetStatus(DEVICE) request (see Section 9.4.5). If a device configuration supports remote wakeup, D5 is set to one.

Note 2: Max Power Setting

The low byte of AX88772B EEPROM offset 0x2D and 0x54 fields are used to configure the "bMaxPower" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus Spec Rev 2.0 for the detailed description of the "bMaxPower" field of Standard Configuration Descriptor. These fields are used to define the Maximum power consumption of the USB device drawn from the USB bus in this specific configuration when the device is fully operational. Expressed in 2mA units (for example, 0x7D indicates for 250mA).

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
8	*bMaxPower*	1	mA	Maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units (i.e., 50 = 100 mA). Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it fails operations it can no longer support. The USB System Software may determine the cause of the failure by checking the status and noting the loss of the device's power source.

4.2.2 External EEPROM Description

User can assign the specific VID/PID, Serial Number, Manufacture String, Product String, etc. user defined fields by external EEPROM. Please refer to **AX88772B EEPROM User Guide** document for more details about how to configure AX88772B EEPROM content.

5 USB Configuration Structure

5.1 USB Configuration

The AX88772B supports 1 Configuration only.

5.2 USB Interface

The AX88772B supports 1 interface.

5.3 USB Endpoints

The AX88772B supports following 4 or 6 endpoints:

- Endpoint 0: Control endpoint. It is used for configuring the device. Please refer to USB Standard Commands (6.1) and USB Vendor Commands (6.2), etc.
- Endpoint 1: Interrupt endpoint. It is used for reporting status. Please refer to Interrupt Endpoint (6.3).
- Endpoint 2: Bulk In endpoint. It is used for receiving Ethernet Packet.
- Endpoint 3: Bulk Out endpoint. It is used for transmitting Ethernet Packet.
- Endpoint 4: Reserved.
- Endpoint 5: Optional Bulk Out endpoint. It is used for transmitting BOTM frame(0).

Note that BOTM_EN bit in EEPROM Flag [4] (4.1.2) is used to enable Endpoint 5. The optional endpoint 5 is serving to specific USB host controller which allows one USB pipe only.

6 USB Commands

There are three command groups for Endpoint 0 (Control Endpoint) in AX88772B:

- The USB standard commands
- The USB vendor commands
- The USB Communication Class commands

6.1 USB Standard Commands

- The Language ID is 0x0904 for English
- PPLL means buffer length
- CC means configuration number
- I I means Interface number
- AA means Device Address

Setup Command	Data Bytes	Access Type	Description
8006_00 01 00 00 LLPP	PPLL bytes in Data stage	Read	Get Device Descriptor
8006_0002 0000_LLPP	PPLL bytes in Data stage	Read	Get Configuration Descriptor
8006_0003_0000_LLPP	PPLL bytes in Data stage	Read	Get Supported Language ID
8006_0103_0904_LLPP	PPLL bytes in Data stage	Read	Get Manufacture String
8006_0203_0904_LLPP	PPLL bytes in Data stage	Read	Get Product String
8006_0303_0904_LLPP	PPLL bytes in Data stage	Read	Get Serial Number String
8006_0403_0904_LLPP	PPLL bytes in Data stage	Read	Get Configuration String
8006_0503_0904_LLPP	PPLL bytes in Data stage	Read	Get Interface 0 String
8006_0603_0904_LLPP	PPLL bytes in Data stage	Read	Get Interface 1/0 String
8006_0703_0904_LLPP	PPLL bytes in Data stage	Read	Get Interface 1/1 String
8008_0000_0000_0100	1 bytes in Data stage	Read	Get Configuration
0009_CC00_0000_0000	No data in Data stage	Write	Set Configuration
810A_0000 _I I00_0100	1 bytes in Data stage	Read	Get Interface
010B_AS00_0000_0000	No data in Data stage	Write	Set Interface
0005_AA00_0000_0000	No data in Data stage	Write	Set Address

Table 8 : USB Standard Command Register Map

6.2 USB Vendor Commands

- AA, CC: The index of register or the content of register.
- BB, DD: The content of register

CMD No	Setup Command	Data Bytes	Access Type	Description
02	C002_AA0B_0C00_0800	8 bytes in Data stage	Read	Rx/Tx/ID-SRAM Read Register
03	4003_AA0B_0C00_0800	8 bytes in Data stage	Write	Rx/Tx/ID-SRAM Write Register
06	4006_0000_0000_0000	No data in Data stage	Write	Software Station Management Control Register
07	C007_AA00_CC00_0200	2 bytes in Data stage	Read	PHY Read Register
08	4008_AA00_CC00_0200	2 bytes in Data stage	Write	PHY Write Register
09	C009_0000_0000_0100	1 bytes in Data stage	Read	Station Management Status Register
0A	400A_0000_0000_0000	No data in Data stage	Write	Hardware Station Management Control Register
0B	C00B_AA00_0000_0200	2 bytes in Data stage	Read	SROM Read Register
0C	400C_AA00_CCDD_0000	No data in Data stage	Write	SROM Write Register
0D	400D_0000_0000_0000	No data in Data stage	Write	SROM Write Enable Register
0E	400E_0000_0000_0000	No data in Data stage	Write	SROM Write Disable Register
0F	C00F_0000_0000_0200	2 bytes in Data stage	Read	Rx Control Register
10	4010_AABB_0000_0000	No data in Data stage	Write	Rx Control Register
11	C011_0000_0000_0300	3 bytes in Data stage	Read	IPG/IPG1/IPG2 Register
12	4012_AABB_CC00_0000	No data in Data stage	Write	IPG/IPG1/IPG2 Register
13	C013_0000_0000_0600	6 bytes in Data stage	Read	Node ID Register
14	4014_0000_0000_0600	6 bytes in Data stage	Write	Node ID Register
15	C015_0000_0000_0800	8 bytes, MA0~MA7, in Data stage	Read	Multicast Filter Array Register
16	4016_0000_0000_0800	8 bytes, MA0~MA7, in Data stage	Write	Multicast Filter Array Register
17	4017_AA00_0000_0000	No data in Data stage	Write	Test Register
19	C019_0000_0000_0200	2 bytes in Data stage	Read	Ethernet/HomePNA PHY Address Register
1A	C01A_0000_0000_0200	2 bytes in Data stage	Read	Medium Status Register
1B	401B_AABB_0000_0000	No data in Data stage	Write	Medium Mode Register
1C	C01C_0000_0000_0100	1 bytes in Data stage	Read	Monitor Mode Status Register
1D	401D_AA00_0000_0000	No data in Data stage	Write	Monitor Mode Register
1E	C01E_0000_0000_0100	1 bytes in Data stage	Read	GPIOs Status Register
1F	401F_AA00_0000_0000	No data in Data stage	Write	GPIOs Register
20	4020_AABB_0000_0000	No data in Data stage	Write	Ethernet Power And Reset Control Register
21	C021_0000_0000_0100	1 bytes in Data stage	Read	Software Interface Selection Status Register
22	4022_AA00_0000_0000	No data in Data stage	Write	Software Interface Selection Register
23	C023_AA00_0000_0400	4 bytes, Wake Up Register in Data stage	Read	Wake-up Frame Array Register
24	4024_AA00_0000_0400	4 bytes, Wake Up Register in Data stage	Write	Wake-up Frame Array Register
25	C025_0000_0000_0100	1 bytes in Data stage	Read	Jam Limit Count Register
26	4026_AA00_0000_0000	No data in Data stage	Write	Jam Limit Count Register
27	C027_0000_0000_0400	4 bytes in Data stage	Read	VLAN Control Register
28	4028_AABB_CCDD_0000	No data in Data stage	Write	VLAN Control Register
2B	C02B_0000_0000_0400	4 bytes in Data stage	Read	COE RX Control Register
2C	402C_AABB_CCDD_0000	No data in Data stage	Write	COE RX Control Register
2D	C02D_0000_0000_0400	4 bytes in Data stage	Read	COE TX Control Register
2E	402E_AABB_CCDD_0000	No data in Data stage	Write	COE TX Control Register
2F	C02F_0000_0000_0400	4 bytes in Data stage	Read	COE Checksum Error Count Register
50	4050_AABB_CCDD_0000	No data in Data stage	Write	Fiber Power Save Timer Register

70	4070_AABB_CCDD_0000	No data in Data stage	Write	LED_MUX Control Register
7C	C07C_0000_0000_0100	1 bytes in Data stage	Read	VMFBIO Status Register
7D	407D_AABB_CC00_0000	No data in Data stage	Write	VMFBIO Register
7E	C07E_0000_0000_0100	1 bytes in Data stage	Read	VMFAIO Status Register
7F	407F_AABB_CC00_0000	No data in Data stage	Write	VMFAIO Register
A1	C0A1_0000_0000_0400	4 bytes in Data stage	Read	Test packet generation Control Register
A2	40A2_AABB_CCDD_0000	No data in Data stage	Write	Test packet generation Control Register
E1	C0E1_0000_0000_0200	2 bytes in Data stage	Read	Ethernet Power And Reset Control Register
F0	40F0_AA00_0000_0000	No data in Data stage	Write	Global Reset Control Register

Table 9 : USB Vendor Command Register Map

6.2.1 Detailed Register Description

6.2.1.1 Rx/Tx/ID-SRAM Read Register (02h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
Reserved				B [3:0]			
0h				C [3:0]			
DD [7:0] in Data stage							
EE [7:0] in Data stage							
FF [7:0] in Data stage							
GG [7:0] in Data stage							
HH [7:0] in Data stage							
II [7:0] in Data stage							
JJ [7:0] in Data stage							
KK [7:0] in Data stage							

{B [3:0], AA [7:0]}: The read address of RX or TX SRAM.
C [1:0]: RAM selection.
00: indicates to read from RX SRAM.
01: indicates to read from TX SRAM.
10: indicates to read from ID-SRAM.
C [3:2]: Reserved.
{DD [7:0], EE [7:0], FF [7:0], GG [7:0], HH [7:0], II [7:0], JJ [7:0], KK [7:0]}: The 64-bits of data presented in Data stage are the data to be written to RX or TX SRAM.
For the detailed ID-SRAM contrl, please refer to APPENDIX C. External EEPROM / Internal ROM / Internal ID-SRAM of Vender Descriptions selection.

6.2.1.2 Rx/Tx/ID-SRAM Write Register (03h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
Reserved				B [3:0]			
Reserved				C [3:0]			
DD [7:0] in Data stage							
EE [7:0] in Data stage							
FF [7:0] in Data stage							
GG [7:0] in Data stage							
HH [7:0] in Data stage							
II [7:0] in Data stage							
JJ [7:0] in Data stage							
KK [7:0] in Data stage							

{B [3:0], AA [7:0]}: The write address of RX or TX SRAM.
C [1:0]: RAM selection.
00: indicates to read from RX SRAM.
01: indicates to read from TX SRAM.
10: indicates to read from ID-SRAM.
C [3:2]: Reserved.
{KK [7:0], JJ [7:0], II [7:0], HH [7:0], GG [7:0], FF [7:0], EE [7:0], DD [7:0]}: The 64-bits of data presented in Data stage are the data to be written to RX or TX SRAM.
For the detailed ID-SRAM contrl, please refer to APPENDIX C. External EEPROM / Internal ROM / Internal ID-SRAM of Vender Descriptions selection.

6.2.1.3 Software Station Management Control Register (06h, write only)

When software needs to access to Ethernet PHY's internal registers, it needs to first issue this command to request the ownership of Station Management Interface. Reading Station Management Status Register can check the ownership status of the interface**.**

6.2.1.4 PHY Read Register (07h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
00h							
CC [7:0]							

AA [4:0]: The PHY ID value.
AA [7:5]: Reserved
CC [4:0]: The register address of Ethernet PHY's internal register.
CC [7:5]: Reserved

6.2.1.5 PHY Write Register (08h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
00h							
CC [7:0]							

AA [4:0]: The PHY ID value.
AA [7:5]: Reserved
CC [4:0]: The register address of Ethernet PHY's internal register.
CC [7:5]: Reserved

6.2.1.6 Station Management Status Register (09h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PM_mode	Chip_Code			Fiber_SD	PPRMF	CABOFF	Host_EN

Host_EN: Host access Enable. Software can read this register to determine the current ownership of Station Management Interface.
1: Software is allowed to access Ethernet PHY's internal registers via PHY Read Register or PHY Write Registers.
0: ASIC's hardware owns the Station Management Interface and software's access is ignored.
CABOFF: Indicate the Ethernet cable was unplugged with internal Ethernet PHY.
1: Ethernet cable was unplugged.
0: Ethernet cable was plugged.
PPRMF: Primary PHY remote fault indicates.
Fiber_SD: Fiber PHY SD detected
Chip_Code: Chip version code for software driver.
3'b010: Chip is AX88772B
PM_mode: PHY or MAC mode
1: PHY mode
0: MAC mode

6.2.1.7 Hardware Station Management Control Register (0Ah, write only)

When software is done accessing Station Management Interface, it needs to issue this command to release the ownership of the Interface back to ASIC's hardware. After issuing this command, subsequent PHY Read Register or PHY Write Register from software will be ignored. Notice that Software should issue this command every time after it finishes accessing the Station Management Interface to release the ownership back to hardware to allow periodic Interrupt Endpoint to be able to access the Ethernet PHY's registers via the Station Management Interface.

6.2.1.8 SROM Read Register (0Bh, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							

AA [7:0]: The read address of Serial EEPROM.

6.2.1.9 SROM Write Register (0Ch, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
00h							
CC [7:0]							
DD [7:0]							

AA [7:0]: The write address of Serial EEROM.
{DD [7:0], CC [7:0]}: The write data value of Serial EEROM

6.2.1.10 Write SROM Enable (0Dh, write only)

User issues this command to enable write permission to Serial EEPROM from SROM Write Register.

6.2.1.11 Write SROM Disable (0Eh, write only)

User issues this command to disable write permission to Serial EEPROM from SROM Write Register.

6.2.1.12 Rx Control Register (0Fh, read only and 10h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SO	ARP	AP	AM	AB	0	AMALL	PRO
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0			0	0	RH3M	RH2M	RH1M

AA [7:0] = {SO, ARP, AP, AM, AB, 0, AMALL, PRO}
BB [7:0] = {3'b0, 0, 0, RH3M, RH2M, RH1M}

PRO: PACKET_TYPE_PROMISCUOUS.
1: All frames received by the ASIC are forwarded up toward the host.
0: Disabled (default).
AMALL: PACKET_TYPE_ALL_MULTICAST.
1: All multicast frames received by the ASIC are forwarded up toward the host, not just the frames whose scrambling result of DA matching with multicast address list provided in Multicast Filter Array Register.
0: Disabled. This only allows multicast frames whose scrambling result of DA field matching with multicast address list provided in Multicast Filter Array Register to be forwarded up toward the host (default).
AB: PACKET_TYPE_BROADCAST.
1: All broadcast frames received by the ASIC are forwarded up toward the host (default).
0: Disabled.
AM: PACKET_TYPE_MULTICAST.
1: All multicast frames whose scrambling result of DA matching with multicast address list are forwarded up to the host (default).
0: Disabled.
ARP: Accept Runt Packet.
1: Accept Runt Packet.
0: Disabled, Reject Runt packet that byte count less then 64 bytes (default).
AP: Accept Physical Address from Multicast Filter Array.
1: Allow unicast packets to be forwarded up toward host if the lookup of scrambling result of DA is found within multicast address list.
0: Disabled, that is, unicast packets filtering are done without regarding multicast address list (default).
SO: Start Operation.
1: Ethernet MAC start operating.
0: Ethernet MAC stop operating (default).
RH1M: RX Header 1 Format selection
0: RX Header Format type 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BMC	Runt	MiiEr	CRCEr	0	RX Packet Length [10:0]										
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Sequence Number [4:0]					Packet Length bar [10:0]										

1: RX Header Format type 1 (Default)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	RX Packet Length [10:0]										
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0xF					Packet Length bar [10:0]										

RH2M: RX Header Mode 2
1: Enable RX IP header aligned double word.
0: Disable RX IP header aligned double word (default).
RH3M: RX Header Mode 3 (Checksum 2 bytes + dummy 2 bytes)
1: RX Header 3 Checksum appends.
0: Disable RX Header 3 Header appends (default).
Bit [15:11]: Please always write 0 to these bits.

Following is the truth table about unicast packet filtering condition.

DA Matching Node ID Register?	PRO bit	Broadcast or Multicast Packet?	Unicast Packet Filtered by Ethernet MAC?
No	0	No	Yes
No	1	No	No
Yes (see Note below)	0	No	No

Note: DA Matching Node ID Register including following two cases:
1. Destination Address field of incoming packets matches with Node ID Register.
2. When AP (bit 5) is set to 1and the scrambling result of DA is found within multicast address list.

Following is a truth table about broadcast packet filtering condition.

PRO bit	AB bit	Broadcast Packet?	Broadcast Packet Filtered by Ethernet MAC?
0	1	Yes	No
0	0	Yes	Yes
1	0/1	Yes	No

6.2.1.13 IPG/IPG1/IPG2 Control Register (11h, read only and 12h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPG [7:0]							
IPG1 [7:0]							
IPG2 [7:0]							

AA [6:0] = IPG [6:0].
BB [6:0] = IPG1 [6:0].
CC [6:0] = IPG2 [6:0].
IPG [6:0]: Inter Packet Gap for back-to-back transfer on TX direction in MII mode (default = 15h).
IPG1 [6:0]: IPG part1 value (default = 0Ch).
IPG2 [6:0]: IPG part1 value + part2 value (default = 12h).
AA [7]: Reserved.
BB [7]: Reserved.
CC [7]: Reserved.

6.2.1.14 Node ID Register (13h, read only and 14h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
BB [7:0]							
CC [7:0]							
DD [7:0]							
EE [7:0]							
FF [7:0]							

AA [7:0] = Node ID 0.
BB [7:0] = Node ID 1.
CC [7:0] = Node ID 2.
DD [7:0] = Node ID 3.
EE [7:0] = Node ID 4.
FF [7:0] = Node ID 5.
{FF [7:0], EE [7:0], DD [7:0], CC [7:0], BB [7:0], AA [7:0]} = Ethernet MAC address [47:0] of AX88772B.

6.2.1.15 Multicast Filter Array (15h, read only and 16h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MA 0 [7:0]							
MA 1 [7:0]							
MA 2 [7:0]							
MA 3 [7:0]							
MA 4 [7:0]							
MA 5 [7:0]							
MA 6 [7:0]							
MA 7 [7:0]							

{MA7 [7:0], MA6 [7:0], MA5 [7:0], MA4 [7:0], MA3 [7:0], MA2 [7:0], MA1 [7:0], MA0 [7:0]} = the multicast address bit map for multicast frame filtering block. For example, see below Figure 15.

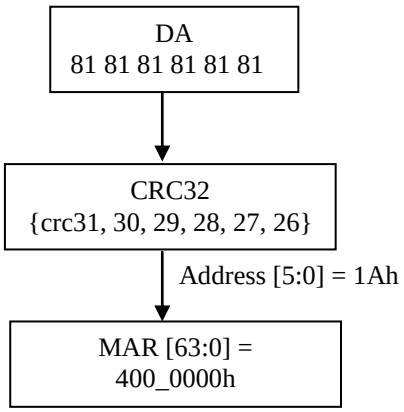


Figure 17 : Multicast Filter Example

As shown in below figure, the Multicast Filter Array (MFA) provides filtering of multicast addresses hashed through the CRC logic. All Destination Address field are fed through the 32 bits CRC generation logic. As the last bit of the Destination Address field enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 to 64 decoder to index a unique filter bit (FB0-63) in the Multicast Filter Array. If the filter bit selected is set, the multicast packet is accepted. The system designer should use a program to determine which filter bits to set in the multicast registers. All multicast filter bits that correspond to Multicast Filter Array Registers accepted by the

node are then set to one. To accept all multicast packets all of the registers are set to all ones. Note that received Pause Frames are always filtered by Ethernet MAC regardless of MFA setting.

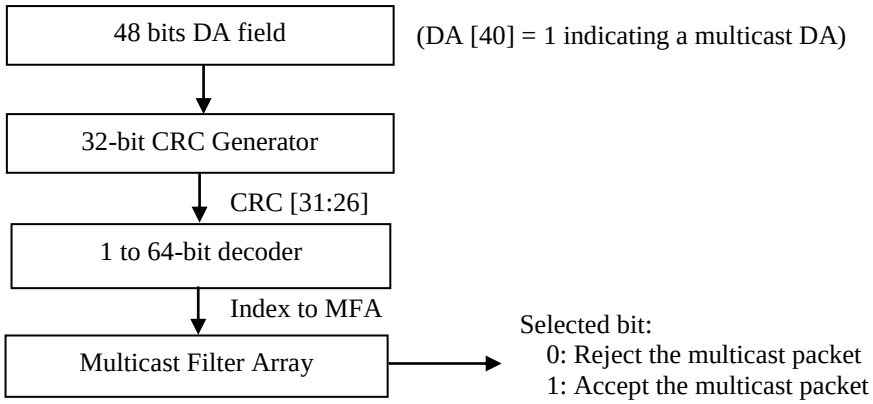


Figure 18 : Multicast Filter Array Hashing Algorithm

Example: If the accepted multicast packet's destination address Y is found to hash to the value 32 (0x20), then FB32 in MA4 should be initialized to "1". This will allow the Ethernet MAC to accept any multicast packet with the destination address Y. Although the hashing algorithm does not guarantee perfect filtering of multicast address, it will perfectly filter up to 64 logical address filters if these addresses are chosen to map into unique locations in the multicast filter. Note: The LSB bit of received packet's first byte being "1" signifies a Multicast Address.

	D7	D6	D5	D4	D3	D2	D1	D0
MA0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MA1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MA2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MA3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MA4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MA5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MA6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MA7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

Figure 19 : Multicast Filter Array Bit Mapping

Following is the truth table about multicast packet filtering condition.

PRO bit	AMALL bit	AM bit	Pass Hashing Algorithm	Multicast Packet Filtered by Ethernet MAC
0	0	0	0	Yes
0	0	0	1	Yes
0	0	1	0	Yes
0	0	1	1	No
0	1	0/1	0/1	No
1	0/1	0/1	0/1	No

Note: Passing Hashing Algorithm means that the selected bit in MFA of CRC-32 result is set to "1".

6.2.1.16 Test Register (17h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MM [7:6]							LDRND

LDRND: To load Random number into MAC's exponential back-off timer, the user writes a "1" to enable the ASIC to load a small random number into MAC's back-off timer to shorten the back-off duration in each retry after collision. This register is used for test purpose. Default value = 0.
MM [7:6]: Reserved.

6.2.1.17 Ethernet / HomePNA PHY Address Register (19h, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SecPhyType [2:0]			SecPhyID [4:0]				
PriPhyType [2:0]			PriPhyID [4:0]				

SecPhyType, SecPhyID: The Secondary PHY address loaded from serial EEPROM's offset address 11h. (The default value is E0h.)
PriPhyType, PriPhyID: The Primarily PHY address loaded from serial EEPROM's offset address 11h. (The default value is 10h.)

6.2.1.18 Medium Status Register (1Ah, read only) and Medium Mode Register (1Bh, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PF	0	TFC	RFC	0	1	FD	0
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	0	SM	SBP	Reserved	PS	RE

AA [7:0] = {PF, 0, TFC, RFC, 0, 1, FD, 0}.
BB [7:0] = {3'b0, SM, SBP, Reserved, PS, RE}.
FD: Full Duplex mode
1: Full Duplex mode (default).
0: Half Duplex mode.
RFC: RX Flow Control enables.
1: Enable receiving of pause frame on RX direction during full duplex mode (default).
0: Disabled.
TFC: TX Flow Control enables.
1: Enable transmitting pause frame on TX direction during full duplex mode (default).
0: Disabled.
PF: Check only "length/type" field for Pause Frame.
1: Enable. Pause frames are identified only based on L/T filed.
0: Disabled. Pause frames are identified based on both DA and L/T fields (default).
RE: Receive Enable.
1: Enable RX path of the ASIC.
0: Disabled (default).
PS: Port Speed in MII mode
1: 100 Mbps (default).
0: 10 Mbps.
SBP: Stop Backpressure.
1: When TFC bit = 1, setting this bit enables backpressure on TX direction "continuously" during RX buffer full condition in half duplex mode.
0: When TFC bit = 1, setting this bit enable backpressure on TX direction "intermittently" during RX buffer full condition in half duplex mode (default).

SM: Super Mac support.
1: Enable Super Mac to shorten exponential back-off time during transmission retrying.
0: Disabled (default).

6.2.1.19 Monitor Mode Status Register (1Ch, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PME_IND	PME_TYPE	PME_POL	US	RWWF	RWMP	RWLC	0

RWLC: Remote Wakeup trigger by Ethernet Link Change.
1: Enabled (default).
0: Disabled.
RWMP: Remote Wakeup trigger by Magic Packet.
1: Enabled (default).
0: Disabled.
RWWF: Remote Wakeup trigger by Wake Up Frame.
1: Enabled.
0: Disabled (default).
US: USB Speed.
1: High speed mode.
0: FS speed mode.
PME_POL: PME Polarity.
1: PME active high.
0: PME active Low (default).
PME_TYP: PME I/O Type.
1: PME output is a Push-Pull driver.
0: PME output to function as an open-drain buffer.
PME_IND: PME indication.
1: A 1.363ms pulse active when detect wake-up event.
0: A static signal active when detect wake-up event (default).

6.2.1.20 Monitor Mode Register (1Dh, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				RWWF	RWMP	RWLC	0

RWLC: Remote Wakeup trigger by Ethernet Link Change.
1: Enable (default).
0: Disable.
RWMP: Remote Wakeup trigger by Magic Packet.
1: Enable (default).
0: Disable.
RWWF: Remote Wakeup trigger by Wake Up Frame.
1: Enable
0: Disable (default).

6.2.1.21 GPIO Status Register (1Eh, read only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00		GPI_2	GPO_2_EN	GPI_1	GPO_1_EN	GPI_0	GPO_0_EN

GPO_0_EN: Current level of pin GPIO_0's output enable.
GPI_0: Input level on GPIO_0 pin when GPIO_0 is as an input pin.
GPO_1_EN: Current level of pin GPIO_1's output enable.
GPI_1: Input level on GPIO_1 pin when GPIO_1 is as an input pin.
GPO_2_EN: Current level of pin GPIO_2's output enable.
GPI_2: Input level on GPIO_2 pin when GPIO_2 is as an input pin.

6.2.1.22 GPIO Register (1Fh, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSE	Reserved	GPO_2	GPO2EN	GPO_1	GPO1EN	GPO_0	GPO0EN

GPO0EN: Pin GPIO_0 Output Enable.
1: Output is enabled (meaning GPIO_0 is used as an output pin).
0: Output is tri-stated (meaning GPIO_0 is used as an input pin) (default).
GPO_0: Pin GPIO_0 Output Value.
GPO1EN: Pin GPIO_1 Output Enable.
1: Output is enabled (meaning GPIO_1 is used as an output pin).
0: Output is tri-stated (meaning GPIO_1 is used as an input pin) (default).
GPO_1: Pin GPIO_1 Output Value.
0: (default).
GPO2EN: Pin GPIO_2 Output Enable.
1: Output is enabled (meaning GPIO_2 is used as an output pin).
0: Output is tri-stated (meaning GPIO_2 is used as an input pin) (default).
GPO_2: Pin GPIO_2 Output Value.
0: (default).
RSE: Reload Serial EEPROM.
1: Enable.
0: Disabled (default)

6.2.1.23 Ethernet PHY Power and Reset Control Register (20h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPOSC	IPPD	IPRL	BZ	0	BZ_TYP	RT	RR
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
WOLLP	0	IPFPS	AutoDetach	IPCOPSC	IPCOPS	IPPSL_1	IPPSL_0

RR: Clear frame length error for Bulk In.
1: set high to clear state.
0: set low to exit clear state (default).
RT: Clear frame length error for Bulk Out.
1: set high to enter clear state.
0: set low to exit clear state (default).
BZ_TYP: The type of BZ bit. Define BZ bit whether it can auto-clear itself.
1: Disable that BZ auto-clears itself when it force hardware return a Zero-length packet (default).
0: Auto-clears BZ when it forces hardware return a Zero-length packet.
BZ: Force Bulk In to return a Zero-length packet.
1: Software can force Bulk In to return a zero-length USB packet.
0: Normal operation mode (default).
IPRL: Internal PHY Reset control. This bit acts as reset signal of internal Ethernet PHY. AX88772B software driver can write it to control the internal Ethernet PHY. For the power-up process to PHY, please refer to APPENDIX B. Ethernet PHY Power and Reset Control.
1: Internal Ethernet PHY is in operating state.
0: Internal Ethernet PHY in reset state (default).
IPPD: Internal Ethernet PHY Power Down control. AX88772B software driver can write it to control the internal Ethernet PHY. For the power-up process to PHY, please refer to APPENDIX B. Ethernet PHY Power and Reset Control.
1: Internal Ethernet PHY power down enable (default). There are two level of power down mode. When IPPD is set to high and the IPOSC is set to low, the internal Ethernet PHY will turn off all clocks and enter deep power down mode. When IPPD is set to high and the IPOSC is also set to high, the internal Ethernet PHY will turn off most of clocks but not crystal oscillator 25MHz.
0: Internal Ethernet PHY is in operating mode.
IPOSC: Internal Ethernet PHY 25MHz crystal oscillator control. AX88772B software driver can write it to control the internal Ethernet PHY.
1: Crystal still alive if IPPD is high (default). The IPOSC must be set high at less 500ns before IPPD going to high.
0: Crystal will turn off if IPPD is high. It will disable USB function when 25MHz crystal turned off..
IPCOPS: Internal PHY Cable off power saving.
1: Internal PHY Cable off power saving active.
0: Normal operation (default).
IPPSL_0: Ethernet PHY Power Saving Level bit-0
IPPSL_1: Ethernet PHY Power Saving Level bit-1
00: Cable Off Power Saving Level 0 (default).
01: Cable Off Power Saving Level 1.
10: Reserved
11: Reserved
IPCOPSC: Internal Ethernet PHY Cable Off Power Saving Control Selecter
1: Control by Hardware handle only (default).
0: Control by Software and Switch to Hardware handle if USB suspendded.
AutoDetach: Detach from USB host when Ethernet cable unplug
1: Enable
0: Disable, Keep Device attached When Ethernet cable unplug (default).
IPFPS: Internal PHY Fiber mode Power saving
1: Enable Internal PHY Fiber mode Power Saving. Internal PHY will active Fiber Power saving when SD signal state at low level more then 5ms, it will leave Fiber power saving righ away when SD signal stated. Please reverence Vendor Command Fiber Power Save Timer Register for details.
0: Disable Internal PHY Fiber mode Power saving

WOLLP: WOL Low Power (Force PHY 10BASE)
1: Force Internal Ethernet PHY into 10BASE after entering Suspend mode. This bit only effect if both PHYs are in auto-negotiation mode with 10/100 capacities.
0: Non-force Internal Ethernet PHY (Default).

6.2.1.24 Software Interface Selection Status Register (21h, read only) and Software Interface Selection Register (22h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				Ether_mode:RO		ASEL	PSEL

PSEL: PHY Select, when ASEL = 0 (manually select the PHY to operate)
1: Select embedded 10/100M Ethernet PHY.
0: Select external one by setting MFA_2 and MFA_3 pins. (default)
ASEL: Auto Select or Manual Select the operation mode.
1: Automatic selection is based on link status of embedded 10/100M Ethernet PHY. If the embedded PHY is in link-off state, the operation mode is determined by MFA_2 and MFA_3 pins.
0: Manual selection between the internal 10/100M Ethernet PHY and the external one (default).
Ether_mode [1:0]: Operational mode.
Write to define the operation mode of External Media Interface
00: (invalid)
01: (invalid)
10: (invalid)
11: (invalid)
Read the current data path selection of Ethernet block or operation mode of External Media Interface.
00: Selected embedded Ethernet PHY
01: Selected RMII interface
10: Reserved
11: Selected Reverse-RMII

6.2.1.25 Wake-up Frame Array Register (23h, read only and 24h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AA [7:0]							
WUD0 [7:0] in Data Stage							
WUD1 [7:0] in Data Stage							
WUD2 [7:0] in Data Stage							
WUD3 [7:0] in Data Stage							

AA [7:0]: The index (from 0x0 to 0x11) of Wake-Up Frame Array Register as shown in below table.

{WUD3 [7:0], WUD2 [7:0], WUD1 [7:0], WUD0 [7:0]} = 32-bits wide register as defined in below table.

AA	**Byte3 (WUD3)**		**Byte2 (WUD2)**		**Byte1 (WUD1)**		**Byte0 (WUD0)**	
0	Byte Mask 0							
1	Byte Mask 1							
2	Byte Mask 2							
3	Byte Mask 3							
4	Byte Mask 4							
5	Byte Mask 5							
6	Byte Mask 6							
7	Byte Mask 7							
8	Wakeup Frame 1 CRC				Wakeup Frame 0 CRC			
9	Wakeup Frame 3 CRC				Wakeup Frame 2 CRC			
A	Wakeup Frame 5 CRC				Wakeup Frame 4 CRC			
B	Wakeup Frame 7 CRC				Wakeup Frame 6 CRC			
C	Offset 3		Offset 2		Offset 1		Offset 0	
D	Offset 7		Offset 6		Offset 5		Offset 4	
E	Last Byte 3		Last Byte 2		Last Byte 1		Last Byte 0	
F	Last Byte 7		Last Byte 6		Last Byte 5		Last Byte 4	
10	Command 7	Command 6	Command 5	Command 4	Command 3	Command 2	Command 1	Command 0
11	Broadcast match command		Reserved (Always zero)	Mask Wakeup Timer		DA Match Command	Cascade Command	
12	Reply TX page 3		Reply TX page 2		Reply TX page 1		Reply TX page 0	
13	Reply TX page 7		Reply TX page 6		Reply TX page 5		Reply TX page 4	
14	Partial checksum 1				Partial checksum 0			

Table 10 : Wake-up Frame Array Register (WUD3~0) Structure Definition

There are eight independent sets of wakeup frame filter supported through the above Byte Mask 0~7. Each wakeup frame filter set consists of Byte Mask, Wakeup Frame CRC, Offset, Last Byte and Command registers. Also, if a more complex pattern of Wakeup Frame is needed, user can choose to cascade two filter sets into one (or up to eight filter sets into one) through Cascade Command register and define a longer pattern for Wakeup Frame matching. Below is detailed register definition.

Byte Mask 0~7: Each set has 32 bits.
The byte mask defines which bytes in the incoming frame will be examined to determine whether or not this is a wake-up frame.

Wakeup Frame 0~7 CRC: Each has 16 bits.
Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame.

CRC-16 Polynomials = X^16 + X^15 + X^2 + 1.

If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

Offset 0~7: Each has 8 bits.
This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.

Last Byte 0~7: Each has 8 bits.
This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

Command 0~7: Each has 4 bits.
Bit 0: Individual Byte Mask enable for Byte Mask 0~7.
1: Enable.
0: Disable.
Bit 1: Destination address (DA) match enable.
1: The DA field of received packet will be compared with the MAC address of AX88772B. When receiving frame with DA matching Node ID register and the wakeup frame filter is also matched, then the packet is considered as valid wakeup frame.
0: When receiving frame with any DA value and the wakeup frame filter is matched, then the packet is considered as valid wakeup frame.
Bit 2: Multicast address match enable.
1: The DA field of received packet will be examined if it is a multicast frame and compared with the Multicast Filter Array. When receiving frame is a multicast frame, meets Multicast Filter Array, and also matches the wakeup frame filter, the packet is considered as valid wakeup frame.
0: When receiving frame with any DA value matches the wakeup frame filter, the packet is considered as valid wakeup frame.
Bit 3: Auto reply enable when suspended.
1: Enable individual auto reply function when suspended.
0: Disable.

Cascade Command: the Bit 0~6 of Wake-up Frame Array Register 0x11
Bit0:
1: Byte Mask 1 and Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 1 and Byte Mask 0 are two independent wake-up frame filters for up to 32 masked bytes each.
Bit1:

1: Byte Mask 2 and Byte Mask 1 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 2 and Byte Mask 1 are two independent wake-up frame filters for up to 32 masked bytes each.

Bit2:
1: Byte Mask 3 and Byte Mask 2 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 3 and Byte Mask 2 are two independent wake-up frame filters for up to 32 masked bytes each.

Bit3:
1: Byte Mask 4 and Byte Mask 3 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 4 and Byte Mask 3 are two independent wake-up frame filters for up to 32 masked bytes each.

Bit4:
1: Byte Mask 5 and Byte Mask 4 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 5 and Byte Mask 4 are two independent wake-up frame filters for up to 32 masked bytes each.

Bit5:
1: Byte Mask 6 and Byte Mask 5 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 6 and Byte Mask 5 are two independent wake-up frame filters for up to 32 masked bytes each

Bit6:
1: Byte Mask 7 and Byte Mask 6 are cascaded to become one wake-up frame filter that allows defining up to 64 masked bytes.
0: Byte Mask 7 and Byte Mask 6 are two independent wake-up frame filters for up to 32 masked bytes each

Note: (1) If both Bit 0 and Bit 1 set '1', Byte Mask 2 and Byte Mask 1 and Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 96 masked bytes.
(2) If both Bit 1 and Bit 2 set '1', Byte Mask 3 and Byte Mask 2 and Byte Mask 1 are cascaded to become one wake-up frame filter that allows defining up to 96 masked bytes.
(3) If Bit 3 ~ Bit 0 set '1', Byte Mask 3 ~Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 128 masked bytes.
(4) If Bit 6 ~ Bit 0 set '1', Byte Mask 7 ~Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 256 masked bytes maximum.

Bit7: Reserved.

DA Match Command: the Bit 8~9 of Wake-up Frame Array Register 0x11

Bit8:
1: DA match only enable. When receiving frame has DA matching Node ID register, then the packet is considered as valid wakeup frame.
0: DA match only disable.

Bit9:
1: Multicast address match only enable. When receiving frame is a multicast frame and meets Multicast Filter Array, the packet is considered as valid wakeup frame.
0: Multicast address match only disable.

Bit15~10: Reserved.

Mask Wakeup Timer: Mask wakeup event trigger to USB host timer. (Due to some system took a long time to enter suspend state)

Bit [3:0]: 28s, 24s, 20s, 16s, 12s, 8s, 4s, 0s

Bit [3:0]	Mask Time	Unit
0x0	0	Sec
0x1	4	Sec
0x2	8	Sec
0x3	12	Sec
0x4	16	Sec
0x5	20	Sec
0x6	24	Sec
0x7	28	Sec

Broadcast match command:

Bit [7:0]: Broadcast match enable for byte mask 7~0.

Reply TX Page point:
Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM.
Bit 6~5: Reply type.
00: Orginal packet in TX buffer.
01: Neighbor advertisement (partial checksum 0).
10: Neighbor advertisement (partial checksum 1).
11: ARP.

Partial checksum: Calculated partial checksum of neighbor advertisement packet.

6.2.1.26 Jam Limit Count Register (25h, read only and 26h write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0		Jam_Limit [5:0]					

Jam_Limit [5:0]: This is used for flow-control in half-duplex mode, which is based on force collision mechanisms to backpressure transmitting network node. During the force collision backpressure process, the Ethernet MAC will continue counting total collision count. When it has reached the Jam_Limit setting, the Ethernet MAC will stop backpressure to avoid Ethernet HUB from being partitioned (default = 3Fh) due to excessive collision on network link.
Bit 7, 6: Please always write 0 to these bits.

6.2.1.27 VLAN Control Register (27h, read only) and (28h, write only)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VID1 [7:0]							
Reserved		VSO	VFE	VID1 [11:8]			
VID2 [7:0]							
Reserved				VID2 [11:8]			

AA [7:0] = {VID1 [7:0]}.
BB [7:0] = {Reserved, VSO, VFE, VID1 [11:8]}.
CC [7:0] = {VID2 [7:0]}.
DD [7:0] = {Reserved, VID2 [11:8]}.

VID1 [11:0]: First VLAN ID for filter.
VFE: VLAN filter enable
1: Enable VLAN filter. The VLAN ID field (12 bits) received 802.1q tagged packets, as in the Figure 26 below, which will be used to compare with VID1 and VID2 setting. If it matches either VID1 or VID2, or its value is equal to all zeros, the received 802.1q tagged packets will be forwarded to the USB Host. Meanwhile, the VSO bit determines whether the VLAN Tag bytes (4 bytes) are stripped off or not during forwarding to the USB Host. Also, if the incoming packets contain no VLAN Tag bytes, they will be forwarded to the USB Host by default. If there is no match between the received 802.1q tagged packets and VID1 and VID2, the packets will be discarded. Please see below Table 12.

Received packet / VID1, VID2	Untagged	Tagged	
		VID=Zero	VID= Not zero
Zero	Forwarded	Forwarded	Discarded
Not zero	Forwarded	Forwarded	Match: Forwarded No Match: Discarded

Table 11 : VID1, VID2 setting to filter received packet

0: Disable VLAN filter. The received packets with or without 802.1q Tag bytes will always be forwarded to the USB Host (default).

VSO: VLAN Strip off

1: Strip off VLAN Tag (4 bytes) from the incoming packet.

0: Preserve VLAN Tag in the incoming packet (default).

VID2 [11:0]: Second VLAN ID for filter. Note that VID1 and VID2 function as two independent VLAN ID filters.

Note that to send the packet with VLANID Tag bytes; the software should append VLAN Tag bytes in the transmitted packets.

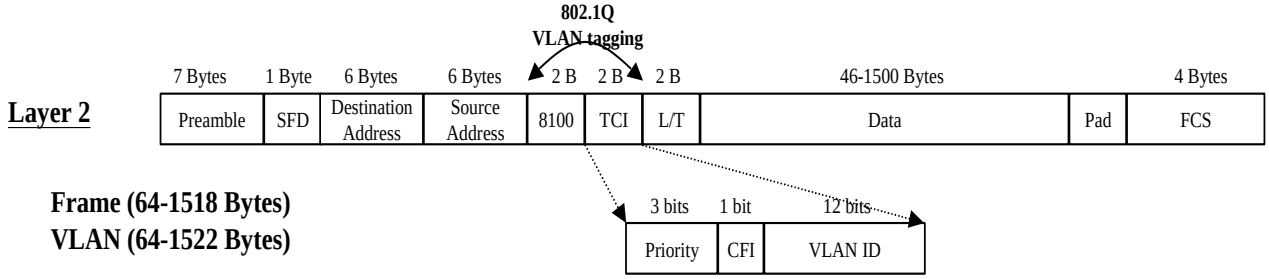


Figure 20 : 802.1q VLAN Packet Format

6.2.1.28 COE RX Control Register (CRXCR, 2Bh for read and 2Ch for write)

Bit	7	6	5	4	3	2	1	0
Name	RXICV6	RXIGMP	RXICMP	RXUDPE	RXTCPE	RXV6VE	RXIPVE	RXIPCE
Reset Value	0	0	0	0	0	0	0	0

Bit	Name	Access	Description
0	RXIPCE	R/W	Enable IPv4 checksum check. 1: Enables IP packet checksum check. 0: Disable IP packet checksum check
1	RXIPVE	R/W	Enable IP version check. 1: Enables IP packet version field check. 0: Disables IP packet version field check.
2	RXV6VE	R/W	Enable IPv6 version check. 1: Enables IPv6 packet version field check. 0: Disables IPv6 packet version field check.
3	RXTCPE	R/W	Enable TCP packet checksum check in RX path. 1: Enables the TCP packet checksum check function. 0: Disables the TCP packet checksum check function.
4	RXUDPE	R/W	Enable UDP packet checksum check in RX path. 1: Enables the UDP packet checksum check function. 0: Disables the UDP packet checksum check function.
5	RXICMP	R/W	Enable ICMP packet checksum check in RX path. 1: Enables the ICMP packet checksum check function. 0: Disables the ICMP packet checksum check function.
6	RXIGMP	R/W	Enable IGMP packet checksum check in RX path. 1: Enables the IGMP packet checksum check function. 0: Disables the IGMP packet checksum check function.
7	RXICV6	R/W	Enable ICMPv6 packet checksum check in RX path. 1: Enables the ICMPv6 packet checksum check function. 0: Disables the ICMPv6 packet checksum check function.

AA [7:0] = {RXICV6, RXIGMP, RXICMP, RXUDPE, RXTCPE, RXV6VE, RXIPVE, RXIPCE}

Bit	7	6	5	4	3	2	1	0
Name	FOPC	Reserved		RXICV6V6	RXIGMV6	RXICMV6	RXUDPV6	RXTCPV6
Reset Value	0	0	0	0	0	0		

Bit	Name	Access	Description
0	RXTCPV6	R/W	Enable TCP packet checksum check in RX path for IPv6 packet. 1: Enables the TCP packet checksum check function for IPv6 packet. 0: Disables the TCP packet checksum check function for IPv6 packet.
1	RXUDPV6	R/W	Enable UDP packet checksum check in RX path for IPv6 packet. 1: Enables the UDP packet checksum check function for IPv6 packet. 0: Disables the UDP packet checksum check function for IPv6 packet.
2	RXICMV6	R/W	Enable ICMP packet checksum check in RX path for IPv6 packet. 1: Enables the ICMP packet checksum check function for IPv6 packet. 0: Disables the ICMP packet checksum check function for IPv6 packet.
3	RXIGMV6	R/W	Enable IGMP packet checksum check in RX path for IPv6 packet. 1: Enables the IGMP packet checksum check function for IPv6 packet. 0: Disables the IGMP packet checksum check function for IPv6 packet.
4	RXICV6V6	R/W	Enable ICMPv6 packet checksum check in RX path for IPv6 packet. 1: Enables the ICMPv6 packet checksum check function for IPv6 packet. 0: Disables the ICMPv6 packet checksum check function for IPv6 packet.
6:5	Reserved	R/W	Reserved
7	FOPC	R/W	Enable Fixed Offset Partial Checksum mode. 1: Enable Fixed Offset Partial Checksum mode. If enabled this bit, COE RX part will calculate partial checksum from fixed offset 14 (bytes) to the end of packet (CRC is NOT included). Other bits should be disabled when FOPC turned ON. 0: Disable FOPC mode

BB [7:0] = {Reserved, RXICV6V6, RXIGMV6, RXICMV6, RXUDPV6, RXTCPV6}

Bit	7	6	5	4	3	2	1	0
Name	ICV6DP	IGMPDP	ICMPDP	UDPEDP	TCPEDP	V6VEDP	IPVEDP	IPCEDP
Reset Value	0	0	0	0	0	0	0	0

Bit	Name	Access	Description
0	IPCEDP	R/W	Drop received packet with IP checksum error. 1: Drop received IP packets with IP checksum error. 0: Do not drop received IP packets with IP checksum error, but indicate checksum error in RX header.
1	IPVEDP	R/W	Drop received packet with IP version error. 1: Drop received IP packets with IP version error. 0: Do not drop received IP packets with IP version error, but indicate version error in RX header.
2	V6VEDP	R/W	Drop received packet with IPv6 version error. 1: Drop received IPv6 packets with IPv6 version error. 0: Do not drop received IPv6 packets with IPv6 version error, but indicate version error in RX header.
3	TCPEDP	R/W	Drop received packet with TCP checksum error. 1: Drop received TCP packets with TCP checksum error. 0: Do not drop received TCP packets with TCP checksum error, but indicate checksum error in RX header.
4	UDPEDP	R/W	Drop received packet with UDP checksum error. 1: Drop received UDP packets with UDP checksum error. 0: Do not drop received UDP packets with UDP checksum error, but indicate checksum error in RX header.

5	ICMPDP	R/W	Drop received packet with ICMP checksum error. 1: Drop received ICMP packets with ICMP checksum error. 0: Do not drop received ICMP packets with ICMP checksum error, but indicate checksum error in RX header.
6	IGMPDP	R/W	Drop received packet with IGMP checksum error. 1: Drop received IGMP packets with IGMP checksum error. 0: Do not drop received IGMP packets with IGMP checksum error, but indicate checksum error in RX header.
7	ICV6DP	R/W	Drop received packet with ICMPv6 checksum error. 1: Drop received ICMPv6 packets with ICMPv6 checksum error. 0: Do not drop received ICMPv6 packets with ICMPv6 checksum error, but indicate checksum error in RX header.

CC [7:0] = {ICV6DP, IGMPDP, ICMPDP, UDPEDP, TCPEDP, V6VEDP, IPVEDP, IPCEDP}

Bit	7	6	5	4	3	2	1	0
Name	Reserved	ICV66DP	IG6DP	IC6DP	UDP6DP	TCP6DP	RXPPPE	RX64TE
Reset Value	0	0	0	0	0	0	0	0

Bit	Name	Access	Description
0	RX64TE	R/W	Support IPv6 in IPv4 tunnel mode. 1: COE will check L4 checksum in a IPv6 in IPv4 tunnel packet. 0: COE will not check L4 checksum in a IPv6 in IPv4 tunnel packet.
1	RXPPPE	R/W	L2 parser support PPPoE encapsulated packet in RX path. 1: COE support PPPoE encapsulated packet in RX path. 0: COE do not support PPPoE encapsulated packet in RX path.
2	TCP6DP	R/W	Drop received packet with TCP checksum error for IPv6 packet. 1: Drop received TCP packets with TCP checksum error for IPv6 packet. 0: Do not drop received TCP packets with TCP checksum error, but indicate checksum error in RX header for IPv6 packet.
3	UDP6DP	R/W	Drop received packet with UDP checksum error for IPv6 packet. 1: Drop received UDP packets with UDCP checksum error for IPv6 packet. 0: Do not drop received UDP packets with UDP checksum error, but indicate checksum error in RX header for IPv6 packet.
4	IC6DP	R/W	Drop received packet with ICMP checksum error for IPv6 packet. 1: Drop received ICMP packets with ICMP checksum error for IPv6 packet. 0: Do not drop received ICMP packets with ICMP checksum error, but indicate checksum error in RX header for IPv6 packet.
5	IG6DP	R/W	Drop received packet with IGMP checksum error for IPv6 packet. 1: Drop received IGMP packets with IGMP checksum error for IPv6 packet. 0: Do not drop received IGMP packets with IGMP checksum error, but indicate checksum error in RX header for IPv6 packet.
6	ICV66DP	R/W	Drop received packet with ICMPv6 checksum error for IPv6 packet. 1: Drop received ICMPv6P packets with ICMPv6 checksum error for IPv6 packet. 0: Do not drop received ICMPv6 packets with ICMPv6 checksum error, but indicate checksum error in RX header for IPv6 packet.
7	Reserved	R/W	Alaways write zero.

DD [7:0] = {Reserved, ICV66DP, IG6DP, IC6DP, UDP6DP, TCP6DP, RXPPPE, RX64TE}

6.2.1.29 COE TX Control Register (CTXCR, 2Dh for read and 2Eh for write)

Bit	7	6	5	4	3	2	1	0
Name	Reserved		TXICV6	TXIGMP	TXICMP	TXUDP	TXTCP	TXIP
Reset Value	0		0	0	0	0	0	0

Bit	Name	Access	Description
0	TXIP	R/W	Enable IPv4 checksum insertion function. 1: Enables IPv4 packet checksum insertion function. 0: Disables IPv4 packet checksum insertion function.
1	TXTCP	R/W	Enable TCP checksum insertion function. 1: Enables TCP packet checksum insertion function. 0: Disables TCP packet checksum insertion function.
2	TXUDP	R/W	Enable UDP checksum insertion function. 1: Enables UDP packet checksum insertion function. 0: Disables UDP packet checksum insertion function.
3	TXICMP	R/W	Enable ICMP checksum insertion function. 1: Enables ICMP packet checksum insertion function. 0: Disables ICMP packet checksum insertion function.
4	TXIGMP	R/W	Enable IGMP checksum insertion function. 1: Enables IGMP packet checksum insertion function. 0: Disables IGMP packet checksum insertion function.
5	TXICV6	R/W	Enable ICMPv6 checksum insertion function. 1: Enables ICMPv6 packet checksum insertion function. 0: Disables ICMPv6 packet checksum insertion function.
7:6	Reserved	R/W	Reserved

AA [7:0] = {Reserved, TXICV6, TXIGMP, TXICMP, TXUDP, TXTCP, TXIPV6, TXIP}

Bit	7	6	5	4	3	2	1	0
Name	Reserved			TXICV6V6	TXIGMV6	TXICMV6	TXUDPV6	TXTCPV6
Reset Value	000			0	0	0	0	0

Bit	Name	Access	Description
2	TXTCPV6	R/W	Enable TCP checksum insertion function for IPv6 packet. 1: Enables TCP packet checksum insertion function for IPv6 packet. 0: Disables TCP packet checksum insertion function for IPv6 packet.
3	TXUDPv6	R/W	Enable UDP checksum insertion function for IPv6 packet. 1: Enables UDP packet checksum insertion function for IPv6 packet. 0: Disables UDP packet checksum insertion function for IPv6 packet.
4	TXICMV6	R/W	Enable ICMP checksum insertion function for IPv6 packet. 1: Enables ICMP packet checksum insertion function for IPv6 packet. 0: Disables ICMP packet checksum insertion function for IPv6 packet.
5	TXIGMV6	R/W	Enable IGMP checksum insertion function for IPv6 packet. 1: Enables IGMP packet checksum insertion function for IPv6 packet. 0: Disables IGMP packet checksum insertion function for IPv6 packet.
6	TXICV6V6	R/W	Enable ICMPv6 checksum insertion function for IPv6 packet. 1: Enables ICMPv6 packet checksum insertion function for IPv6 packet. 0: Disables ICMPv6 packet checksum insertion function for IPv6 packet.
7	Reserved	R/W	Reserved

BB [7:0] = {Reserved, TXICV6V6, TXIGMV6, TXICMV6, TXUDPV6, TXTCPV6}

Bit	7	6	5	4	3	2	1	0
Name	Reserved						TXPPPE	TX64TE
Reset Value	6'b0						0	0

Bit	Name	Access	Description
0	TX64TE	R/W	Support IPv6 in IPv4 tunnel mode. 1: COE will insert L4 checksum in a IPv6 in IPv4 tunnel packet. 0: COE will not insert L4 checksum in a IPv6 in IPv4 tunnel packet.
1	TXPPPE	R/W	L2 parser support PPPoE encapsulated packet in TX path. 1: COE do not support PPPoE encapsulated packet in TX path. 0: COE support PPPoE encapsulated packet in TX path.
2:7	Reserved	R/W	Reserved

BB [7:0] = {Reserved, TXPPPE, TX64TE}
CC [7:0] = Reserved
DD [7:0] = Reserved

6.2.1.30 COE Checksum Error Count Register (CEDR, 2Fh for read)

Bit	7	6	5	4	3	2	1	0
Name	ICMPCEDC		UDPCEDC		TCPCEDC		IPCEDC	
Reset Value	00		00		00		00	

Bit	Name	Access	Description
1:0	IPCEDC	R	Layer 3 IPv4 checksum error detect counter. If IPv4 checksum error detected, this counter will add 1. This counter cleared after read.
3:2	TCPCEDC	R	Layer 4 TCP checksum error detect counter. If TCP checksum error detected, this counter will add 1. This counter cleared after read.
5:4	UDPCEDC	R	Layer 4 UDP checksum error detect counter. If UDP checksum error detected, this counter will add 1. This counter cleared after read.
7:6	ICMPCEDC	R	Layer 4 ICMP checksum error detect counter. If ICMP checksum error detected, this counter will add 1. This counter cleared after read.

AA [7:0] = {ICMPCEDC, UDPCEDC, TCPCEDC, IPCEDC}

Bit	7	6	5	4	3	2	1	0
Name	Reserved				ICV6CEDC		IGMPCEDC	
Reset Value	4'b0				00		00	

Bit	Name	Access	Description
1:0	IGMPCEDC	R	Layer 4 IGMP checksum error detect counter. If IGMP checksum error detected, this counter will add 1. This counter cleared after read.
3:2	ICV6CEDC	R	Layer 4 ICMPv6 checksum error detect counter. If ICMPv6 checksum error detected, this counter will add 1. This counter cleared after read.
7:4	Reserved	R/W	Reserved

BB [7:0] = {Reserved, ICV6CEDC, IGMPCEDC}

Bit	7	6	5	4	3	2	1	0
Name	L2 CRC error counter							
Reset Value	0x00							

Bit	Name	Access	Description
7:0	L2 CRC error counter	R	Layer 2 CRC error counter. Indicate the CRC error count. This counter cleared after read.

CC [7:0] = L2 CRC error counter
DD [7:0] = Reserved

6.2.1.31 Fiber Power Saving Timer Register (50h, write only)

Bit	7	6	5	4	3	2	1	0
Name	0						FART [1:0]	
Reset Value	0x01							

AA = {6'b0, FART [1:0]}

FART: Fiber PHY Auto Resume Time
00: 320ms
01: 640ms
10: 1280ms
11: 2560ms

6.2.1.32 LED_MUX control Register (70h, write only)

Bit	7	6	5	4	3	2	1	0	Reset Value
Name	Sel_LED0								0x08
	Sel_LED1								0x20
	Sel_LED2								0x40
	Sel_LED3								0x01

Select MFA_3 ~ MFA_0 LEDs output
AA [7:0] = MFA_0 output function by Sel_LED0 is defined as following
[7] Link
[6] Link & Active
[5] Speed
[4] Duplex
[3] Duplex & collision
[2] Collision
[1] Fiber Remote Fault
[0] TX Active
BB [7:0] = MFA_1 output function by Sel_LED1 defined as following
[7] Link
[6] Link & Active
[5] Speed
[4] Duplex
[3] Duplex & collision
[2] Collision
[1] RX Active
[0] TX Active

CC [7:0] = MFA_2 output function by Sel_LED2 defined as following
[7] Link
[6] Link & Active
[5] Speed
[4] Duplex
[3] Duplex & collision
[2] Collision
[1] RX Active
[0] TX Active
DD [7:0] = MFA_3 output function by Sel_LED3 defined as following
[7] X
[6] X
[5] X
[4] X
[3] Fiber Signal Detected
[2] Active
[1] USB Sspeed
[0] USB Speed & Active

6.2.1.33 VMFBIO Status Register (7Ch, read only)

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
Name	MFBI_7	MFBI _6	MFBI _5	MFBI _4	MFBI_3	MFBI _2	MFBI _1	MFBI _0	0x00

Vemdor command controls MFB0 ~ MFB3.

6.2.1.34 VMFBIO Register (7Dh, write only)

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
Name	MFBO _7	MFBO _6	MFBO _5	MFBO_4	MFBO _3	MFBO _2	MFBO _1	MFBO_0	0x00
	MFBOEN7	MFBOEN6	MFBOEN5	MFBOEN4	MFBOEN3	MFBOEN2	MFBOEN1	MFBOEN0	0x00
	0	0	0	0	0	0	0	MFBGS	0x00

Vemdor command controls MFB0 ~ MFB7.

MFBGS: MFB0~7 driving strength
0: 4mA
1: 8mA

6.2.1.35 VMFAIO Status Register (7Eh, read only)

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
Name	0	0	0	0	MFAI_3	MFAI_2	MFAI_1	MFAI_0	0x00

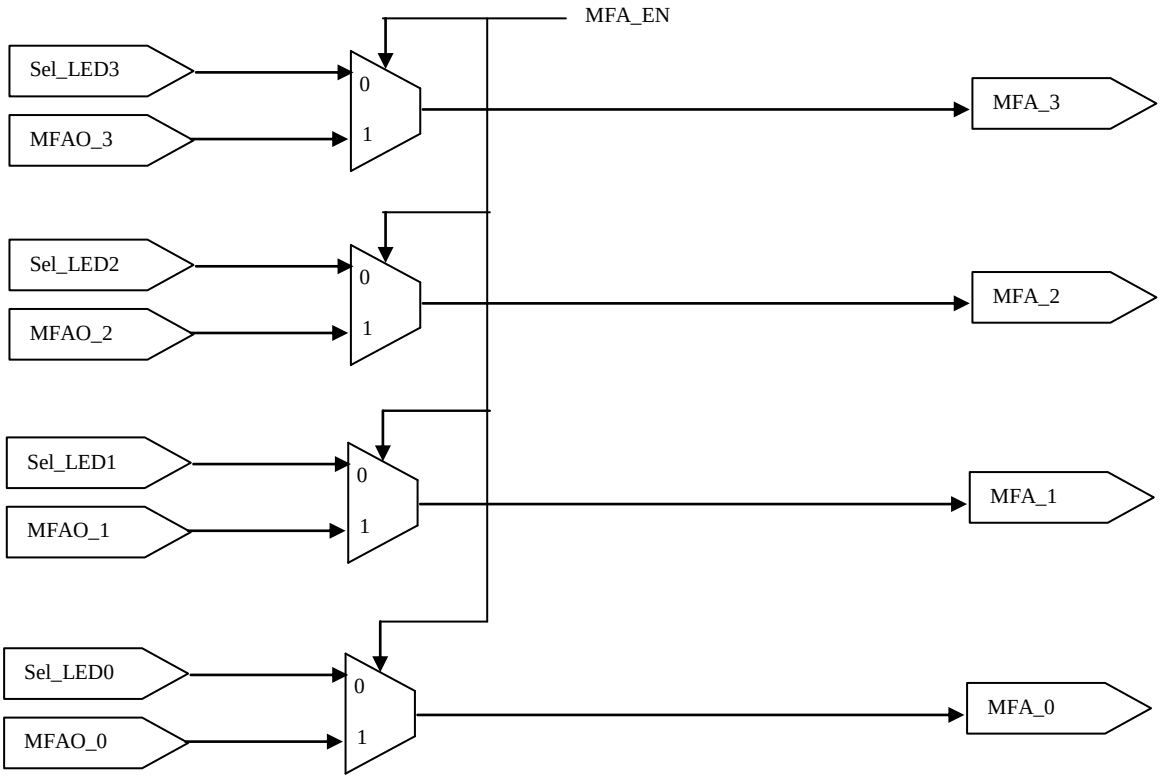
Vendor command control MFA_0 ~ MFA_3

6.2.1.36 VMFAIO Register (7Fh, write only)

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
Name	0	0	0	0	MFAO_3	MFAO_2	MFAO_1	MFAO_0	0x00
	MFA_EN	0	0	0	MFAOEN3	MFAOEN2	MFAOEN1	MFAOEN0	0x00
	0	0	0	0	0	0	0	MFAGS	0x01

Vendor command control MFA_0 ~ MFA_3

VMFAGS: MFAIO driving strength
0: 4mA
1: 8mA



6.2.1.37 Test Packet Generation Control Register (A1h, read only) and (A2h, write only)

Bit	7	6	5	4	3	2	1	0
Name	TPinterval						TPrandom	TPfix
	Data pattern or random seed							
	Test packet length low							
	4'b0				Test packet length high			
Reset Value	0x00							

The transmit test packets without padding CRC 4 bytes.

AA [7:0] = {TPinterval, TPrandom, TPfix}
TPinterval: test packet inter-frame gape
TPrandom: random data packet
TPfix: fix data packet
BB [7:0] = Data pattern or random seed. The BB[3:0] is high-nibble of data pattern and BB[7:4] is low-nibble.
CC [7:0] = Test packet length low
DD [7:0] = {4'b0, Test packet length high}
Total test packet length = {Test packet length high, Test packet length low}

Note: To enable Test Packet Generation function, please set TPrandom ='1' or Tpfix ='1'.

6.2.1.38 Ethernet Power And Reset Control Register (E1h, read only)

Please refer to Vendor command 20h for the detail data format.

6.2.1.39 Global Reset Control Register (F0h, write only)

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	0	0	0	0	0	0	0	GR
Reset Value	0x00							

AA [7:0] = {7'b0, GR}

GR: CHIP Global Reset
1: Gloobal reset active and will clear by itself
0: Normal Operation

6.3 Interrupt Endpoint

The Interrupt Endpoint contains 8 bytes of data and its frame format is defined as: A1AA_BBCC_DDEE_FFGG.

Where A1 byte in byte 1: A1 is a fixed value.

Where AA byte in byte 2:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	Fiber_SD	PPRMF

PPRMF: Primary PHY remote fault indicates.
Fiber_SD: Fiber PHY SD detected

Where BB byte in byte 3:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CABOFF	0	0	IEPSP	MDINF [8]	FLE	SPLS	PPLS

PPLS: Primary PHY Link State. The link status of internal PHY in MAC/PHY mode
1: Link is up.
0: Link is down.
SPLS: Secondary PHY Link State. It is the link status of external PHY connected with RMII. In MAC mode, it is the link status of external PHY. In PHY mode, the link status equals the inverse value of MDINF [8] in PM_Control register.
1: Link is up.
0: Link is down.
FLE: Bulk Out Ethernet Frame Length Error.
1: Proprietary Length field has parity error during Bulk Out transaction.
0: Proprietary Length field has no parity error during Bulk Out transaction.
MDINF [8]: Media Information bit [8] (default value = 1).
This bit is the same as the PHY mode register, PM_Control (10h), bit [8] value written by external Ethernet MAC device when AX88772B operates in PHY mode. User can use PM_Control register bit [8] to send some message to AX88772B software driver through Interrupt Endpoint. The typical usage is to indicate to the AX88772B software driver that the external Ethernet MAC has finished initialization and is ready to send and receive packets with AX88772B, by writing '0' to PM_Control bit [8].
IEPSP: Internal Embedded PHY speed
1: 100BASE
0: 10BASE
CABOFF: Indicate the Ethernet cable was unplugged with internal Ethernet PHY.
1: Ethernet cable was unplugged.
0: Ethernet cable was plugged.

Where CC byte in byte 4:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MDINF [7:0]							

MDINF [7:0]: Media Information bit [7:0] (default = 00h).
This byte is the same as the PHY mode register, PM_Control (10h), bit [7:0] value written by external Ethernet MAC device when AX88772B operates in PHY mode. User can use PM_Control register bit [7:0] to send some messages to AX88772B software driver through Interrupt Endpoint.

DDEE byte in byte 5 and 6: Primary PHY's register value, whose offset is given in High byte of EEPROMoffset 0Fh.
FFGG byte in byte 7 and 8: Primary PHY's register value, whose offset is given in Low byte of EEPROMoffset 0Fh.

6.4 Bulk-Out Timer and Monitor (BOTM)

BOTM controller (Bulk-Out Timer and Monitor)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte0	BOTMSignature [7:0]							
Byte1	BOTMSignature [15:8]							
Byte2	0					RMDQ	R	T
Byte3	Bulk-Out delay Timer Threshold [7:0]							
Byte4	0	Bulk-Out delay Timer Threshold [14:8]						

BOTMSignature [15:0] = {0xAAB8}

T: USB Bulk-Out delay timer Threshold
1: Enable
0: Disable
R: Check MAC to receive frame status
1: Enable
0: Disable
RMDQ: Release Manual De-Queue after Bulk-Out delay Timer Threshold timeout.
1: Enable
0: Disable
Bulk-Out delay Timer Threshold [14:0], Per Unit is 1us.

7 Embedded Ethernet PHY Register Description

In MAC mode (operating with or without internal Ethernet PHY), the embedded Ethernet PHY registers can always be accessed indirectly through the USB vendor commands, PHY Read Register and PHY Write Register.

In PHY mode, the embedded Ethernet PHY registers can still be accessed indirectly through the USB vendor commands.

Address	Register Name	Default Value	Description
00h	BMCR	3100h	Basic mode control register, basic register.
01h	BMSR	7809h	Basic mode status register, basic register.
02h	PHYIDR1	003Bh	PHY identifier register 1, extended register.
03h	PHYIDR2	1881h	PHY identifier register 2, extended register.
04h	ANAR	01E1h	Auto negotiation advertisement register, extended register.
05h	ANLPAR	0000h	Auto negotiation link partner ability register, extended register.
06h	ANER	0000h	Auto negotiation expansion register, extended register.
07h	Reserved	0000h	Reserved and currently not supported.
08h-0Fh	IEEE reserved	0000h	IEEE 802.3u reserved.

Table 12 : Embedded Ethernet PHY Register Map

7.1 PHY Register Detailed Description

The following abbreviations apply to following sections for detailed register description.

Reset value:

1: Bit set to logic one
0: Bit set to logic zero
X: No set value
Pin#: Value latched from pin # at reset time

Access type:

RO: Read only
RW: Read or write

Attribute:

SC: Self-clearing
PS: Value is permanently set
LL: Latch low
LH: Latch high

7.1.1 Basic Mode Control Register (BMCR)

Address 00h

Bit	Bit Name	Default	Description
15	Reset	0, RW / SC	Reset: 1: Software reset 0: Normal operation
14	Loopback	0, RW	Loopback: 1: Loopback enabled 0: Normal operation
13	Speed selection	1, RW	Speed selection: 1: 100 Mb/s 0: 10 Mb/s This bit must set to 1 while bit 12 (Auto-negotiation enable) is set to 1.
12	Auto-negotiation enable	1, RW	Auto-negotiation enable: 1: Auto-negotiation enabled. Bit 8 of this register is ignored and Bit 13 of this register must set to 1. 0: Auto-negotiation disabled. Bits 8 and 13 of this register determine the link speed and mode.
11	Power down	0, RW	Power down: 1: Power down 0: Normal operation
10	Isolate	(PHYAD = 00000), RW	Isolate: 1: Isolate 0: Normal operation
9	Restart auto-negotiation	0, RW / SC	Restart auto-negotiation: 1: Restart auto-negotiation 0: Normal operation
8	Duplex mode	1, RW	Duplex mode: 1: Full duplex operation 0: Normal operation
7	Collision test	0, RW	Collision test: 1: Collision test enabled 0: Normal operation
6:0	Reserved	X, RO	Reserved: Write as 0, read as “don’t care”.

7.1.2 Basic Mode Status Register (BMSR)

Address 01h

Bit	Bit Name	Default	Description
15	100BASE-T4	0, RO / PS	100BASE-T4 capable: 0: This PHY is not able to perform in 100BASE-T4 mode.
14	100BASE-TX full duplex	1, RO / PS	100BASE-TX full-duplex capable: 1: This PHY is able to perform in 100BASE-TX full-duplex mode.
13	100BASE-TX half duplex	1, RO / PS	100BASE-TX half-duplex capable: 1: This PHY is able to perform in 100BASE-TX half-duplex mode.
12	10BASE-T full duplex	1, RO / PS	10BASE-T full-duplex capable: 1: This PHY is able to perform in 10BASE-T full-duplex mode.
11	10BASE-T half duplex	1, RO / PS	10BASE-T half-duplex capable: 1: This PHY is able to perform in 10BASE-T half-duplex mode.
10:7	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
6	MF preamble suppression	0, RO / PS	Management frame preamble suppression: 0: This PHY will not accept management frames with preamble suppressed.
5	Auto-negotiation complete	0, RO	Auto-negotiation completion: 1: Auto-negotiation process completed 0: Auto-negotiation process not completed
4	Remote fault (Not supported)	0, RO / LH	Remote fault: 1: Remote fault condition detected (cleared on read or by a chip reset) 0: No remote fault condition detected
3	Auto-negotiation ability	1, RO / PS	Auto configuration ability: 1: This PHY is able to perform auto-negotiation.
2	Link status	0, RO / LL	Link status: 1: Valid link established (100Mb/s or 10Mb/s operation) 0: Link not established
1	Jabber detect	0, RO / LH	Jabber detection: 1: Jabber condition detected 0: No Jabber condition detected
0	Extended capability	1, RO / PS	Extended capability: 1: Extended register capable 0: Basic register capable only

7.1.3 PHY Identifier Register 1 (PHYIDR1)

Address 02h

Bit	Bit Name	Default	Description
15:0	OUI_MSB	0x003B, RO / PS	OUI most significant bits: Bits 3 to 18 of the OUI are mapped to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored.

7.1.4 PHY Identifier Register 2 (PHYIDR2)

Address 03h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	00_0110, RO / PS	OUI least significant bits: Bits 19 to 24 of the OUI are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	00_1000, RO / PS	Vendor model number.
3:0	MDL_REV	0001, RO / PS	Model revision number.

7.1.5 Auto Negotiation Advertisement Register (ANAR)

Address 04h

Bit	Bit Name	Default	Description
15	NP	0, RO / PS	Next page indication: 0: No next page available. The PHY does not support the next page function.
14	ACK	0, RO	Acknowledgement: 1: Link partner ability data reception acknowledged 0: Not acknowledged
13	RF	0, RW	Remote fault: 1: Fault condition detected and advertised 0: No fault detected
12:11	Reserved	X, RW	Reserved. Write as 0, read as “don’t care”.
10	Pause	0, RW	Pause: 1: Pause operation enabled for full-duplex links 0: Pause operation not enabled
9	T4	0, RO/PS	100BASE-T4 support: 0: 100BASE-T4 not supported
8	TX_FD	1, RW	100BASE-TX full-duplex support: 1: 100BASE-TX full-duplex supported by this device 0: 100BASE-TX full-duplex not supported by this device
7	TX_HD	1, RW	100BASE-TX half-duplex support: 1: 100BASE-TX half-duplex supported by this device 0: 100BASE-TX half-duplex not supported by this device
6	10_FD	1, RW	10BASE-T full-duplex support: 1: 10BASE-T full-duplex supported by this PHY 0: 10BASE-T full-duplex not supported by this PHY
5	10_HD	1, RW	10BASE-T half-duplex support: 1: 10BASE-T half-duplex supported by this PHY 0: 10BASE-T half-duplex not supported by this PHY
4:0	Selector	0_0001, RW	Protocol selection bits: These bits contain the binary encoded protocol selector supported by this PHY. [0 0001] indicates that this PHY supports IEEE 802.3u CSMA/CD.

7.1.6 Auto Negotiation Link Partner Ability Register (ANLPAR)

Address 05h

Bit	Bit Name	Default	Description
15	NP	0, RO	Next page indication: 1: Link partner next page enabled 0: Link partner not next page enabled
14	ACK	0, RO	Acknowledgement: 1: Link partner ability for reception of data word acknowledged 0: Not acknowledged
13	RF	0, RO	Remote fault: 1: Remote fault indicated by link partner 0: No remote fault indicated by link partner
12:11	Reserved	X, RO	Reserved. Write as 0, read as “don’t care”.
10	Pause	0, RO	Pause: 1: Pause operation supported by link partner 0: Pause operation not supported by link partner
9	T4	0, RO	100BASE-T4 support: 1: 100BASE-T4 supported by link partner 0: 100BASE-T4 not supported by link partner
8	TX_FD	0, RO	100BASE-TX full-duplex support: 1: 100BASE-TX full-duplex supported by link partner 0: 100BASE-TX full-duplex not supported by link partner
7	TX_HD	0, RO	100BASE-TX half-duplex support: 1: 100BASE-TX half-duplex supported by link partner 0: 100BASE-TX half-duplex not supported by link partner
6	10_FD	0, RO	10BASE-T full-duplex support: 1: 10BASE-T full-duplex supported by link partner 0: 10BASE-T full-duplex not supported by link partner
5	10_HD	0, RO	10BASE-T half-duplex support: 1: 10BASE-T half-duplex supported by link partner 0: 10BASE-T half-duplex not supported by link partner
4:0	Selector	0_0000, RO	Protocol selection bits: Link partner’s binary encoded protocol selector.

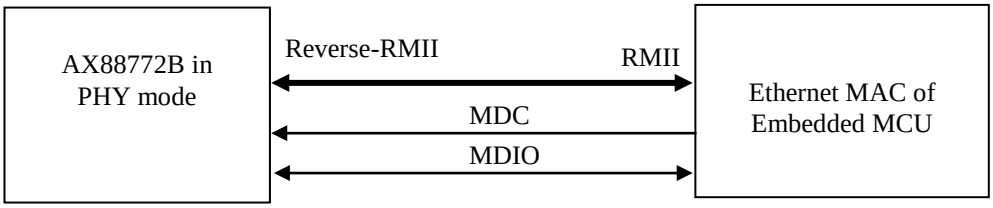
7.1.7 Auto Negotiation Expansion Register (ANER)

Address 06h

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
4	PDF	0, RO / LH	Parallel detection fault: 1: Fault detected via the parallel detection function 0: No fault detected
3	LP_NP_AB	0, RO	Link partner next page enable: 1: Link partner next page enabled 0: Link partner not next page enabled
2	NP_AB	0, RO / PS	PHY next page enable: 0: PHY not next page enabled
1	Page_RX	0, RO / LH	New page reception: 1: New page received 0: New page not received
0	LP_AN_AB	0, RO	Link partner auto-negotiation enable: 1: Auto-negotiation supported by link partner

8 Station Management Registers in PHY Mode

There are 8 registers in the station management interface of the AX88772B for the external Ethernet MAC device to access when AX88772B operates in PHY mode. The access protocol and timing format is the same as the standard management frame structure defined in the IEEE 802.3u spec. Therefore, the station management interface of AX88772B also needs a unique PHY ID to be able to receive management frame. In this case, the 5-bit PHY_ID of AX88772B station management interface is defined in the EEPROM offset 11h (Secondary PHY_ID [4:0]) and (Table 3 PHY_ID definition table).



	Management frame fields							
	PRE	ST	OP	PHY_ID	REGAD	TA	DATA	IDLE
READ	1…….1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1…….1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Figure 21 : Station Management Frame for PHY Mode

Address	Register Name	Default Value	Description
00h	PM_BMCR	3100h	(8.1.1) Basic mode control register, basic register.
01h	PM_BMSR	4029h	(8.1.2) Basic mode status register, basic register.
02h	PM_PHYIDR1	003Bh	(8.1.3) PHY identifier register 1, extended register.
03h	PM_PHYIDR2	1861h	(8.1.4) PHY identifier register 2, extended register.
04h	PM_ANAR	0501h	(8.1.5) Auto negotiation advertisement register, extended register.
05h	PM_ANLPAR	4501h	(8.1.6) Auto negotiation link partner ability register, extended register.
06h	PM_ANER	0003h	(8.1.7) Auto negotiation expansion register, extended register.
10h	PM_Control	0100h	(8.1.8) A customized STA register.

Table 13 : Station Management Register Map in PHY Mode

8.1 PHY Mode Detailed Register Description

8.1.1 PHY Mode Basic Mode Control Register (PM_BMCR)

Address 00h

Bit	Bit Name	Default	Description
15	Reset	0, RO	Reset: 1: Software reset 0: Normal operation, this bit is fixed to 0.
14	Loopback	0, RW	Loopback: 1: Loopback enabled. The AX88772B will loopback data from TXD [1:0] input back to RXD [1:0] in Reverse-RMII mode. 0: Normal operation
13	Speed selection	1, RO	Speed selection: 1: 100 Mb/s, this bit is fixed to 1. 0: 10 Mb/s
12	Auto-negotiation enable	1, RO	Auto-negotiation enable: 1: Auto-negotiation enabled, this bit is fixed to 1. 0: Auto-negotiation disabled.
11	Power down	0, RW	Power down: 1: Power down. If in Reverse-RMII mode, the CRSDV, RXD 1:0] outputs will be kept low and no toggling. The REFCLK_O keeps 50MHz clock output. 0: Normal operation
10	Isolate	PHY_ISO, RW	Isolate: (default value is loaded from EEPROM Flag [11]) 1: Isolate. The below AX88772B outputs pin will become tri-state. If in Reverse-RMII: RXD [1:0], CRSDV, except for REFCLK_O. 0: Normal operation
9	Restart auto-negotiation	0, RO	Restart auto-negotiation: 1: Restart auto-negotiation 0: Normal operation, this bit is fixed to 0.
8	Duplex mode	1, RO	Duplex mode: 1: Full duplex operation, this bit is fixed to 1. 0: Normal operation.
7	Collision test	0, RO	Collision test: 1: Collision test enabled 0: Normal operation, this bit is fixed to 0.
6:0	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.

8.1.2 PHY Mode Basic Mode Status Register (PM_BMSR)

Address 01h

Bit	Bit Name	Default	Description
15	100BASE-T4	0, RO	100BASE-T4 capable: 0: This PHY is not able to perform in 100BASE-T4 mode.
14	100BASE-TX full duplex	1, RO	100BASE-TX full-duplex capable: 1: This PHY is able to perform in 100BASE-TX full-duplex mode.
13	100BASE-TX half duplex	0, RO	100BASE-TX half-duplex capable: 0: This PHY is not able to perform in 100BASE-TX half-duplex mode.
12	10BASE-T full duplex	0, RO	10BASE-T full-duplex capable: 0: This PHY is not able to perform in 10BASE-T full-duplex mode.
11	10BASE-T half duplex	0, RO	10BASE-T half-duplex capable: 0: This PHY is not able to perform in 10BASE-T half-duplex mode.
10:7	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
6	MF preamble suppression	0, RO	Management frame preamble suppression: 0: This PHY will not accept management frames with preamble suppressed.
5	Auto-negotiation complete	1, RO	Auto-negotiation completion: 1: Auto-negotiation process completed 0: Auto-negotiation process not completed
4	Remote fault (Not supported)	0, RO	Remote fault: 1: Remote fault condition detected (cleared on read or by a chip reset) 0: No remote fault condition detected
3	Auto-negotiation ability	1, RO	Auto configuration ability: 1: This PHY is able to perform auto-negotiation.
2	Link status	0, RO	Link status: 1: Valid link established (indicate that AX88772B software initialization is finished and not in USB suspend mode) 0: Link not established (indicate that AX88772B software initialization is not finished or in USB suspend mode)
1	Jabber detect	0, RO	Jabber detection: 1: Jabber condition detected 0: No Jabber condition detected
0	Extended capability	1, RO	Extended capability: 1: Extended register capable 0: Basic register capable only

8.1.3 PHY Mode PHY Identifier Register 1 (PM_PHYIDR1)

Address 02h

Bit	Bit Name	Default	Description
15:0	OUI_MSB	0x003B, RO	OUI most significant bits: Bits 3 to 18 of the OUI are mapped to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored.

8.1.4 PHY Mode PHY Identifier Register 2 (PM_PHYIDR2)

Address 03h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	00_0110, RO	OUI least significant bits: Bits 19 to 24 of the OUI are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	00_0110, RO	Vendor model number.
3:0	MDL_REV	0001, RO	Model revision number.

8.1.5 PHY Mode Auto Negotiation Advertisement Register (PM_ANAR)

Address 04h

Bit	Bit Name	Default	Description
15	NP	0, RO	Next page indication: 0: No next page available. The PHY does not support the next page function.
14	ACK	0, RO	Acknowledgement: 1: Link partner ability data reception acknowledged 0: Not acknowledged
13	RF	0, RO	Remote fault: 1: Fault condition detected and advertised 0: No fault detected
12:11	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
10	Pause	1, RO	Pause: 1: Pause operation enabled for full-duplex links 0: Pause operation not enabled
9	T4	0, RO	100BASE-T4 support: 0: 100BASE-T4 not supported
8	TX_FD	1, RO	100BASE-TX full-duplex support: 1: 100BASE-TX full-duplex supported by this device 0: 100BASE-TX full-duplex not supported by this device
7	TX_HD	0, RO	100BASE-TX half-duplex support: 1: 100BASE-TX half-duplex supported by this device 0: 100BASE-TX half-duplex not supported by this device
6	10_FD	0, RO	10BASE-T full-duplex support: 1: 10BASE-T full-duplex supported by this PHY 0: 10BASE-T full-duplex not supported by this PHY
5	10_HD	0, RO	10BASE-T half-duplex support: 1: 10BASE-T half-duplex supported by this PHY 0: 10BASE-T half-duplex not supported by this PHY
4:0	Selector	0_0001, RO	Protocol selection bits: These bits contain the binary encoded protocol selector supported by this PHY. [0 0001] indicates that this PHY supports IEEE 802.3u CSMA/CD.

8.1.6 PHY Mode Auto Negotiation Link Partner Ability Register (PM_ANLPAR)

Address 05h

Bit	Bit Name	Default	Description
15	NP	0, RO	Next page indication: 1: Link partner next page enabled 0: Link partner not next page enabled
14	ACK	1, RO	Acknowledgement: 1: Link partner ability for reception of data word acknowledged 0: Not acknowledged
13	RF	0, RO	Remote fault: 1: Remote fault indicated by link partner 0: No remote fault indicated by link partner
12:11	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
10	Pause	1, RO	Pause: 1: Pause operation supported by link partner 0: Pause operation not supported by link partner
9	T4	0, RO	100BASE-T4 support: 1: 100BASE-T4 supported by link partner 0: 100BASE-T4 not supported by link partner
8	TX_FD	1, RO	100BASE-TX full-duplex support: 1: 100BASE-TX full-duplex supported by link partner 0: 100BASE-TX full-duplex not supported by link partner
7	TX_HD	0, RO	100BASE-TX half-duplex support: 1: 100BASE-TX half-duplex supported by link partner 0: 100BASE-TX half-duplex not supported by link partner
6	10_FD	0, RO	10BASE-T full-duplex support: 1: 10BASE-T full-duplex supported by link partner 0: 10BASE-T full-duplex not supported by link partner
5	10_HD	0, RO	10BASE-T half-duplex support: 1: 10BASE-T half-duplex supported by link partner 0: 10BASE-T half-duplex not supported by link partner
4:0	Selector	0_0001, RO	Protocol selection bits: Link partner’s binary encoded protocol selector.

8.1.7 PHY Mode Auto Negotiation Expansion Register (PM_ANER)

Address 06h

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
4	PDF	0, RO	Parallel detection fault: 1: Fault detected via the parallel detection function 0: No fault detected
3	LP_NP_AB	0, RO	Link partner next page enable: 1: Link partner next page enabled 0: Link partner not next page enabled
2	NP_AB	0, RO	PHY next page enable: 0: PHY not next page enabled
1	Page_RX	1, RO	New page reception: 1: New page received 0: New page not received
0	LP_AN_AB	1, RO	Link partner auto-negotiation enable: 1: Auto-negotiation supported by link partner

8.1.8 PHY Mode Control Register (PM_Control)

Address 10h

Bit	Bit Name	Default	Description
15		0, RO	Reserved
14	-	0, RO	Reserved
13	-	0, RO	Reserved
12	-	0, RO	Reserved
11	-	0, RO	Reserved
10	-	0, RO	Reserved
9	Reserved	0, RW	Reserved.
8	Media Information	1, RW	Media Information bit 8, MDINF [8]. This bit is reported to AX88772B software driver in MDINF [8] bit of Interrupt Endpoint as described in section 6.3. When AX88772B operates in PHY mode, the typical usage is to indicate to AX88772B software driver that the external Ethernet MAC has finished initialization and is ready to send and receive packets with AX88772B, by writing '0' to this bit. Also, any time when external Ethernet MAC can't be set online for any reasons, it can write '1' to this bit to inform AX88772B software driver. This bit can also function as a link-up remote wake event in PHY mode. In other words, after AX88772B enters into suspend mode instructed by USB Host, the external Ethernet MAC can write this bit to have a '1' to '0' transition which will be used as link-up remote wakeup trigger event to awake AX88772B and the USB Host.
7:0	Media Information	0x00, RW	Media Information bit [7:0], MDINF [7:0]. This 8 bits data is reported to AX88772B software driver in MDINF [7:0] bits of Interrupt Endpoint as described in section 6.3. When AX88772B operates in PHY mode, the external Ethernet MAC can define some command codes to send some messages to AX88772B software driver using this byte.

9 Electrical Specifications

9.1 DC Characteristics

9.1.1 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
VCCK	Digital core power supply	- 0.3 to 2.16	V
VCC18A	Analog Power. 1.8V	- 0.3 to 2.16	V
VCC3IO	Power supply of 3.3V I/O	- 0.3 to 4	V
VCC3R3	Power supply of on-chip voltage regulator	- 0.3 to 4	V
VCC3A3	Analog Power 3.3V for Ethernet PHY bandgap	- 0.3 to 3.8	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	- 0.3 to 4	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	- 0.3 to 4	V
V_{IN18}	Input voltage of 1.8V I/O	- 0.3 to 2.16	V
V_{IN3}	Input voltage of 3.3V I/O	- 0.3 to 4.0	V
	Input voltage of 3.3V I/O with 5V tolerant	- 0.3 to 5.8	V
T_{STG}	Storage temperature	- 65 to 150	℃
I_{IN}	DC input current	20	mA
I_{OUT}	Output short circuit current	20	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

9.1.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.98	V
VCC18A	Analog core power supply	1.62	1.8	1.98	V
VCC3R3	Power supply of on-chip voltage regulator	2.97	3.3	3.63	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	2.97	3.3	3.63	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	2.97	3.3	3.63	V
VCC3A3	Analog power supply for bandgap	2.97	3.3	3.63	V
V_{IN18}	Input voltage of 1.8 V I/O	0	1.8	1.98	V
V_{IN3}	Input voltage of 3.3 V I/O	0	3.3	3.63	V
	Input voltage of 3.3 V I/O with 5V tolerance	0	3.3	5.25	V
T_j	Junction operating temperature	-40	25	125	℃
T_a	Commerical ambient operating temperature in still air	0	-	70	℃
	Industrial ambient operating temperature in still air	-40	-	85	

9.1.3 Leakage Current and Capacitance

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance		-	2.2	-	pF
C_{OUT}	Output capacitance		-	2.2	-	pF
C_{BID}	Bi-directional buffer capacitance		-	2.2	-	pF

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding a pad capacitance of about 0.5pF to the package capacitance.

9.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	Iol = 8mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -8mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0	-10	±1	10	μA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	85	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

9.1.5 DC Characteristics of 3.3V with 5V Tolerance I/O Pins

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	Iol = 8mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -8mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = 5.5V or 0		±5		μA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	85	μA
I_{OZ}	Tri-state output leakage current	V_{in} = 5.5V or 0		±10		μA

9.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3R3	Power supply of on-chip voltage regulator.		3.0	3.3	3.6	V
Tj	Operating junction temperature.		0	25	125	℃
Iload	Driving current.	Normal operation	-	-	150	mA
V18F	Output voltage of on-chip voltage regulator.	VCC3R3 = 3.3V	1.71	1.8	1.89	V
Vdrop	Dropout voltage.	△V18F = -1%, Iload = 10mA	-	-	0.2	V
$\frac{\triangle V18F}{(\triangle VCC3R3 \times V18F)}$	Line regulation.	VCC3R3 = 3.3V, Iload = 10mA	-	0.2	0.4	%/V
$\frac{\triangle V18F}{(\triangle Iload \times V18F)}$	Load regulation.	VCC3R3 = 3.3V, 1mA ≦ Iload ≦ 150mA	-	0.02	0.05	%/mA
$\frac{\triangle V18F}{\triangle Tj}$	Temperature coefficient.	VCC3R3 = 3.3V,-40℃ ≦ Tj ≦ 125℃	-	0.4	-	mV/℃
Iq_25℃	Quiescent current at 25 ℃	VCC3R3 = 3.3V, Iload = 0mA, Tj = 25 ℃	-	66	96	μA
Iq_125℃	Quiescent current at 125 ℃	VCC3R3 = 3.3V, Iload = 0mA, Tj = 125 ℃	-	85	115	μA
Cout	Output external capacitor.		3.3	-	-	μF
ESR	Allowable effective series resistance of external capacitor.		0.5	-	-	Ω

9.1.7 DC Characteristics of Fiber Interface

Fiber Transmitter Specification						
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Vol	Output low voltage		1.2	1.57	1.95	V
Voh	Output high voltage		2.0	2.4	2.7	V
|Vod|	Differential output voltage		0.54	0.83	1.15	V
Vol(od)	Output low voltage (overdrive)		1.1	1.5	1.85	V
Voh(od)	Output high voltage (overdrive)		2.2	2.5	2.8	V
|Vod|(od)	Differential output voltage (overdrive)		0.65	1.02	1.4	V
Fiber Receiver Specification						
Vicm	Input commond-mode voltage range		1.67	2.0	2.33	V
|Vidth|	Input differential threshold voltage		50	-	-	mV

Fiber SD (Signal Detect) Input Voltage Specification	
SD input voltage (Visd)	**Operation mode**
Visd < 0.2V	Copper mode
1.0V < Visd < 1.8V	Fiber mode No signal detected
Visd > 2.2V	Fiber mode Signal detected

9.2 Thermal Characteristics

Description	Symbol	Rating	Units
Thermal resistance of junction to case	ΘJC	16.7	℃/W
Thermal resistance of junction to ambient	ΘJA	52.2	℃/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P}, \quad \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature T_A: ambient or environment temperature
T_C: the top center of compound surface temperature P: input power (watts)

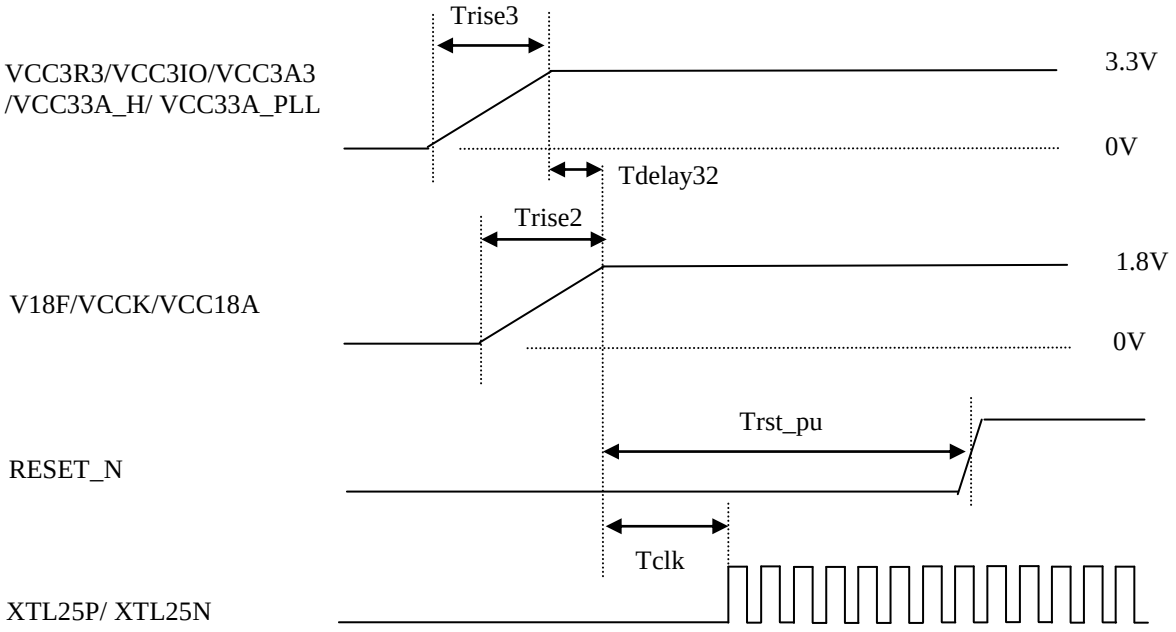
9.3 Power Consumption

Symbol	Description	Conditions	Min	Typ	Max	Unit
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 100Mbps full duplex mode and USB High speed mode	-	78.2	-	mA
IVCC33	Current Consumption of 3.3V		-	31.9	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 100Mbps full duplex mode and USB Full speed mode	-	71.4	-	mA
IVCC33	Current Consumption of 3.3V		-	25.7	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 10Mbps full duplex mode and USB High speed mode	-	21.6	-	mA
IVCC33	Current Consumption of 3.3V		-	34.3	-	mA
IVCC18	Current Consumption of 1.8V	Operating at Ethernet 10Mbps full duplex mode and USB Full speed mode	-	16.3	-	mA
IVCC33	Current Consumption of 3.3V		-	25.4	-	mA
IVCC18	Current Consumption of 1.8V	Ethernet unlink (Disable AutoDetach)	-	17.3	-	mA
IVCC33	Current Consumption of 3.3V		-	20.6	-	mA
IVCC18	Current Consumption of 1.8V	Ethernet unlink (Enable AutoDetach)		3.3		mA
IVCC33	Current Consumption of 3.3V			4.5		mA
IVCC18	Current Consumption of 1.8V	Suspend and enable Remote WakeUp and disable WOLLP (WOL Low Power) **(Refer to 6.2.1.23)**	-	63.7	-	mA
IVCC33	Current Consumption of 3.3V		-	12.8	-	mA
IVCC18	Current Consumption of 1.8V	Suspend and enable Remote WakeUp and enable WOLLP (WOL Low Power) **(Refer to 6.2.1.23)**	-	7.7	-	mA
IVCC33	Current Consumption of 3.3V		-	9.8	-	mA
IVCC18	Current Consumption of 1.8V	Suspend and disable Remote WakeUp	-	20	-	μA
IVCC33	Current Consumption of 3.3V		-	0.2	-	mA
IDEVICE	Power consumption of AX88772B full loading (chip only)	1.8V	-	78.2	-	mA
		3.3V	-	31.9	-	mA
ISYSTEM	Power consumption of AX88772B full loading (demo board)	Total of 3.3V (Including VCC3R3 regulator supplies 1.8V to VCCK and VCC18A)	-	167	-	mA

Table 14 : Power consumption

9.4 Power-up Sequence

At power-up, the AX88772B requires the VCC3R3/VCC3IO/VCC3A3/VCC33A_H/ VCC33A_PLL power supply to rise to nominal operating voltage within Trise3 and the V18F/VCCK/VCC18A power supply to rise to nominal operating voltage within Trise2.



Symbol	Description	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	0.4	-	10	ms
T_{rise2}	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
$T_{delay32}$	3.3V rise to 1.8V rise time delay		-5	-	5	ms
T_{clk}	25Mhz crystal oscillator start-up time	From VCC18A = 1.8V to first clock transition of XTALIN or XTALOUT	-	1	-	ms
T_{rst_pu}	RSTn low level interval time from power-up	From VCCK/VCC18A = 1.8V and VCC3IO = 3.3V to RSTn going high	T_{clk} + Trst *1	-	-	ms

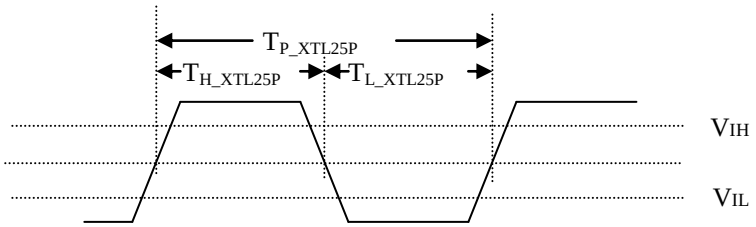
*1 : Please refer to 1.09.19.5.1 Reset Timing for the details about the Trst.

9.5 AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on C_L (Output load) =50pF.

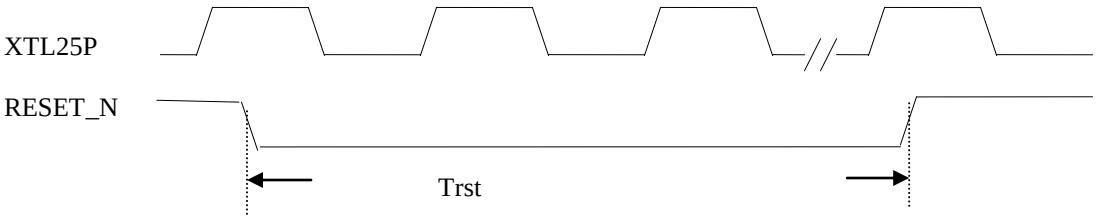
9.5.1. Clock Timing

XTL25P



Symbol	Description	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTL25P clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTL25P clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTL25P clock low time		-	20.0	-	ns

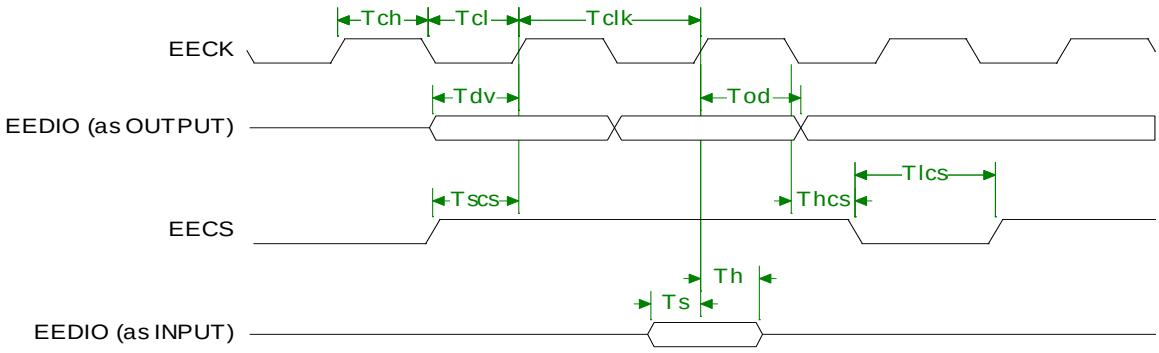
9.5.1. Reset Timing



Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTL25P is running	125	-	250000	XTL25P clock cycle (Note)

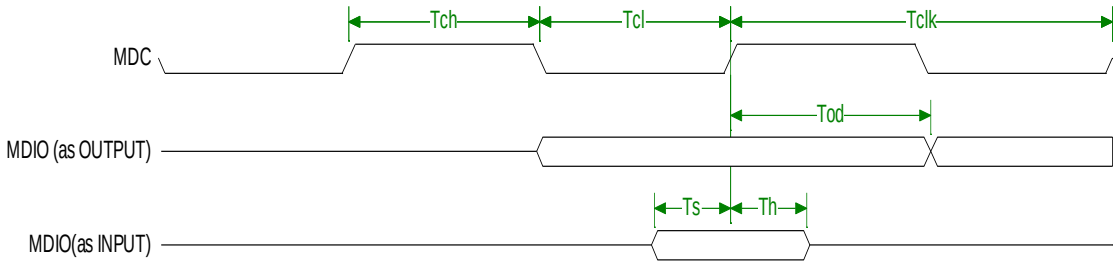
Note: If the system applications require using hardware reset pin, RESET_N, to reset AX88772B during device initialization or normal operation after VBUS pin is asserted, the above timing spec (Min=5 μs, Max=10ms) of RESET_N should be met.

9.5.2. Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	EECK clock cycle time	-	5120	-	ns
Tch	EECK clock high time	-	2560	-	ns
Tcl	EECK clock low time	-	2560	-	ns
Tdv	EEDIO output valid to EECK rising edge time	2560	-	-	ns
Tod	EECK rising edge to EEDIO output delay time	2562	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2560	-	-	ns
Thcs	EECK falling edge to EECS invalid time	7680	-	-	ns
Tlcs	Minimum EECS low time	23039	-	-	ns
Ts	EEDIO input setup time	20	-	-	ns
Th	EEDIO input hold time	0	-	-	ns

9.5.3. Station Management Timing



MAC mode with RMII: MDC=Output

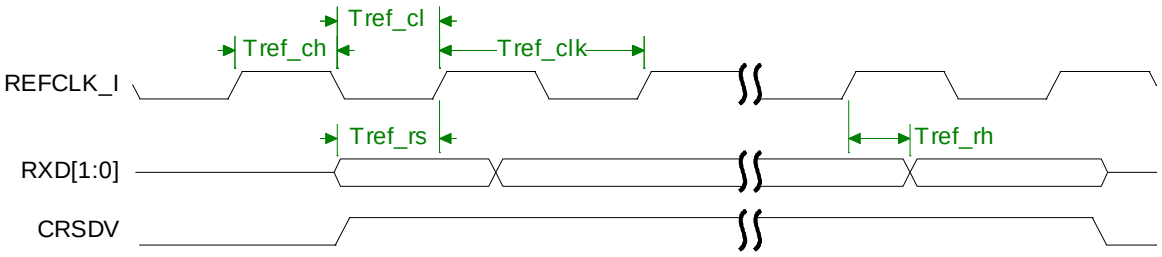
Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	640	-	ns
Tch	MDC clock high time	-	320	-	ns
Tcl	MDC clock low time	-	320	-	ns
Tod	MDC clock rising edge to MDIO output delay	0.5	-	-	Tclk
Ts	MDIO data input setup time	125	-	-	ns
Th	MDIO data input hold time	0	-	-	ns

PHY mode (Reverse-RMII): MDC=Input

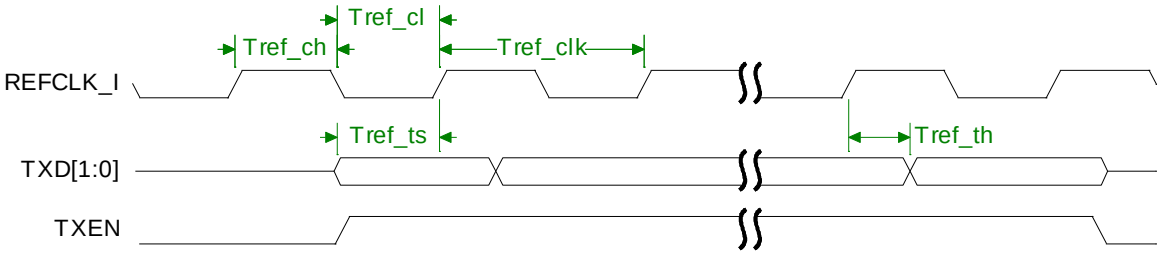
Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	320	-	ns
Tch	MDC clock high time	-	160	-	ns
Tcl	MDC clock low time	-	160	-	ns
Tod	MDC clock rising edge to MDIO output delay	0	-	300	ns
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	10	-	-	ns

Note: MDC is Pin#17, MDIO is Pin#18.

9.5.4. RMII / Reverse-RMII Timing

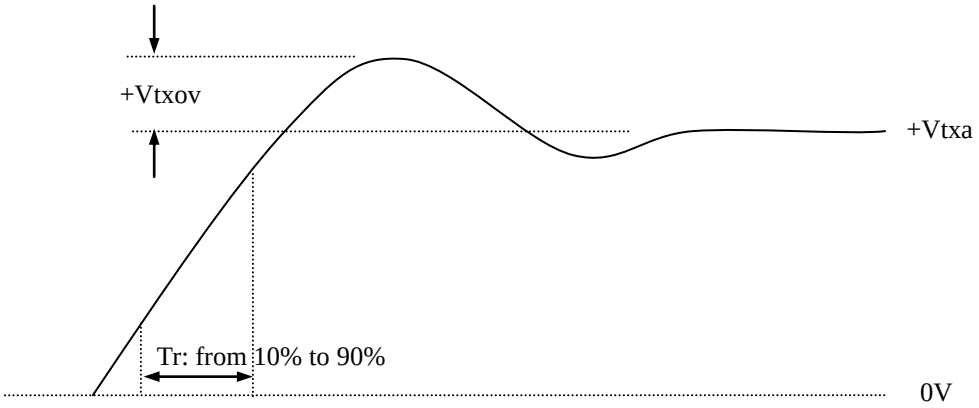


Symbol	Description	Min	Typ	Max	Unit
Tref_clk	Clock cycle time	-	20.0	-	ns
Tref_ch	Clock high time	-	10.0	-	ns
Tref_cl	Clock low time	-	10.0	-	ns
Tref_rs	RXD [1:0], CRSDV setup to rising REFCLK_I	4.0	-	-	ns
Tref_rh	RXD [1:0], CRSDV hold (delay time) from rising REFCLK_I	2.0	-	-	ns



Symbol	Description	Min	Typ	Max	Unit
Tref_ts	TXD [1:0], TXEN setup to rising REFCLK_I	4.0	-	-	ns
Tref_th	TXD [1:0], TXEN hold from rising REFCLK_I	2.0	-	-	ns

9.5.5. 10/100M Ethernet PHY Interface Timing



10/100M Ethernet PHY Transmitter Waveform and Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Peak-to-peak differential output voltage	10BASE-T mode	4.4	5	5.6	V
Vtxa *2	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2	2.1	V
Tr / Tf	Signal rise / fall time	100BASE-TX mode	3	4	5	ns
	Output jitter	100BASE-TX mode, scrambled idle signal	-	-	1.4	ns
Vtxov	Overshoot	100BASE-TX mode	-	-	5	%

10/100M Ethernet PHY Receiver Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Receiver input impedance		10	-	-	KΩ
	Differential squelch voltage	10BASE-T mode	300	400	500	mV
	Common mode input voltage		2.97	3.3	3.63	V
	Maximum error-free cable length		100	-	-	meter

9.5.6. USB Transceiver Interface Timing

VCC33A_H/ VCC33A_PLL= 3.0 ~ 3.6 V.

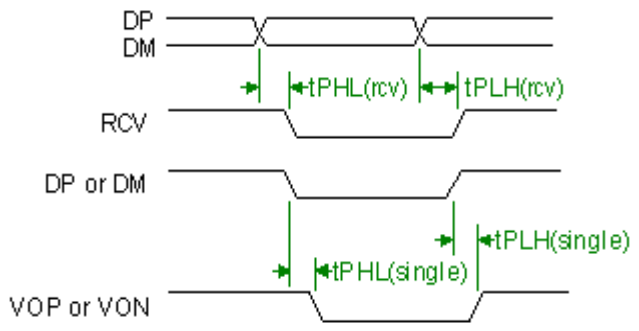
Static Characteristic for Analog I/O Pins (DP/DM):

Symbol	Description	Conditions	Min	Typ	Max	Unit
USB 2.0 Transceiver (HS)						
Input Levels (Differential Receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$ Measured at the connection as an application circuit.	300	-	-	mV
V_{HSCM}	High speed data signaling common mode voltage range		-50	-	500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected	-	-	100	mV
		No squelch detected	200	-	-	mV
Output levels (differential)						
V_{HSOI}	High speed idle level output voltage		-10	-	10	mV
V_{HSOL}	High speed low level output voltage		-10	-	10	mV
V_{HSOH}	High speed high level output voltage		-360	-	400	mV
V_{CHIRPJ}	Chirp-J output voltage		700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage		-900	-	-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	45	49.5	Ohm
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0	-	3.6	V
USB 1.1 Transceiver (FS/LS)						
Input Levels (Differential Receiver)						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$	0.2	-	-	V
V_{CM}	Differential common mode voltage		0.8	-	2.5	V
Input Levels (Single-Ended Receiver)						
V_{SE}	Single ended receiver threshold		0.8	-	2.0	V
Output levels						
V_{OL}	Low-level output voltage		0	-	0.3	V
V_{OH}	High-level output voltage		2.8	-	3.6	V

Dynamic Characteristic for Analog I/O Pins (DP/DM):

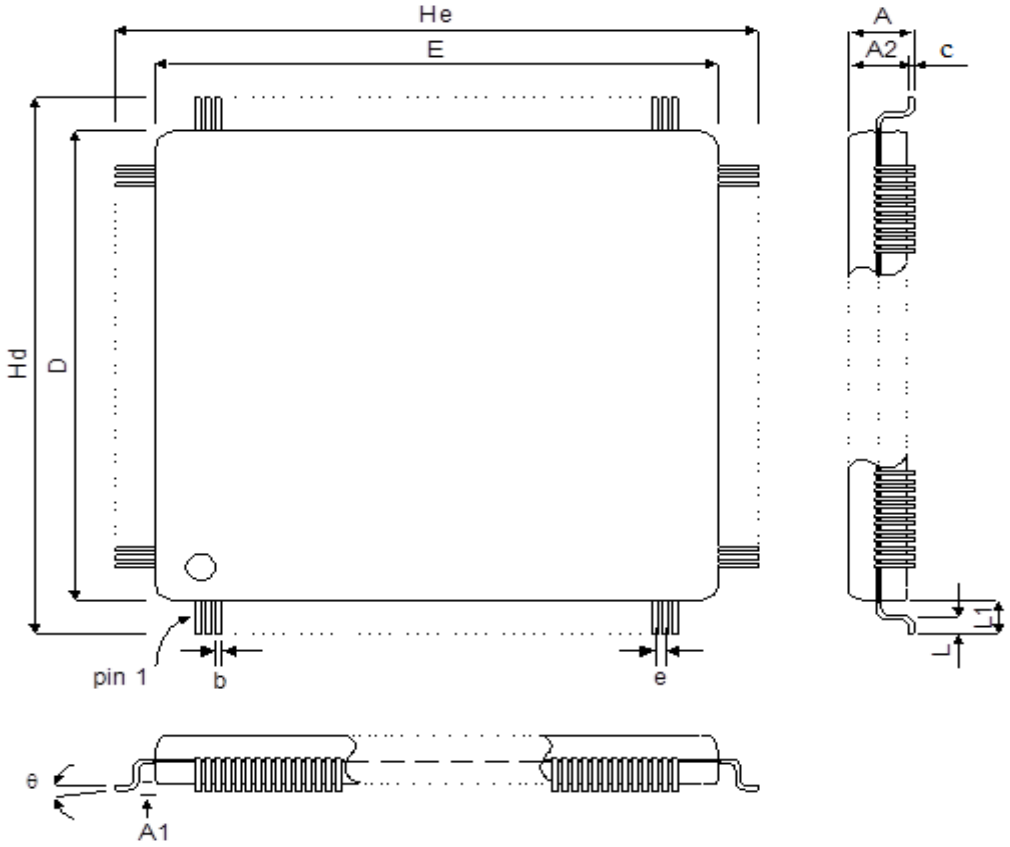
Symbol	Description	Conditions	Min	Typ	Max	Unit
Driver Characteristic						
High-Speed Mode						
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Full-Speed Mode						
t_{FR}	Rise time of DP/DM	C_L=50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time of DP/DM	C_L=50pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3	-	2.0	V
Driver Timing						
High-Speed Mode						
	Driver waveform requirement	See eye pattern of template 1	Follow template 1 described in USB rev 2.0 spec. (http://www.usb.org/developers/docs)			
Full-Speed Mode						
	VI, FSE 0, OE to DP, DN Propagation delay	For detailed description of VI, FSE 0 and OE, please refer to USB rev 1.1specification.	-	-	15	ns
Receiver Timing						
High-Speed Mode						
	Data source jitter and receiver jitter tolerance	See eye pattern of template 4	Follow template 4 described in USB rev 2.0 spec. (http://www.usb.org/developers/docs)			
Full-Speed Mode						
t_{PLH}(rcv) t_{PHL} (rcv)	Receiver propagation delay (DP; DM to RCV)	For detailed description of RCV, please refer to USB rev 1.1specification.	-	-	15 (Note)	ns
t_{PLH}(single) t_{PHL}(single)	Receiver propagation delay (DP; DM to VOP, VON)	-	-	-	15 (Note)	ns

Note: **Full-Speed Timing diagram**



10 Package Information

10.1 AX88772B 64-pin LQFP package



Symbol	Millimeter		
	Min	Typ	Max
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A	-	-	1.60
b	0.13	0.18	0.23
c	0.09	-	0.20
D		7.00	
E		7.00	
e	-	0.40	-
Hd		9.00	
He		9.00	
L	0.45	0.60	0.75
L1	-	1.00 REF	-
θ	0°	3.5°	7°

11 Ordering Information

Part Number	Description
AX88772BLF	64 PIN, LQFP Package, Commerical grade 0℃ to +70 ℃ (Green, Lead-Free)
AX88772BLI	64 PIN, LQFP Package, Industrial grade -40℃ to +85 ℃ (Green, Lead-Free)

12 Revision History

Revision	Date	Comment
V1.00	2010/04/08	Initial release.
V1.01	2010/05/04	1. Modified some descriptions in Section 4.2. 2. Modified power saving level description in Section 6.2.1.23. 3. Added Section 9.2 “Thermal Characteristics”.
V1.02	2010/06/18	1. Corrected some descriptions in Section 2.1. 2. Corrected some descriptions in Section 4.1.4. 3. Corrected a typo in Section 4.1.2. 4. Corrected some typos in Section 4.2. 5. Modified some descriptions in Section 4.2.1.
V1.03	2010/07/05	1. Corrected some typos in Section 6.2.1.19, 6.2.1.20. 2. Corrected the Storage Temperature information in Section 9.1.1. 3. Corrected the T_j and T_a information in Section 9.1.2. 4. Added more descriptions in Appendix C. 5. Updated some description in Figure 24.
V1.04	2011/08/10	1. Updated some descriptions in Section 6.2.1.37. 2. Corrected some typos in Section 8.1.4 and 9.1.2. 3. Added more descriptions in Table 13 of Section 8. 4. Added copyright legal header information.
V1.05	2013/01/18	1. Updated the T_{rise3} min. time to 0.4ms in Section 9.4. 2. Modified some descriptions in Section 6.2.1.12.
V1.06	2013/02/27	1. Modified some descriptions in Section 2.1, 3.11, 6.2.1.12, 6.2.1.25. 2. Corrected some typos in Table 9, Section 6.2.1.17. 3. Added the PHY registers reset values information in Table 12. 4. Added the “DC Characteristics of Fiber Interface” information in Section 9.1.7.
V1.07	2015/01/21	1. Added “c” and updated “A1” in Section 10.1.

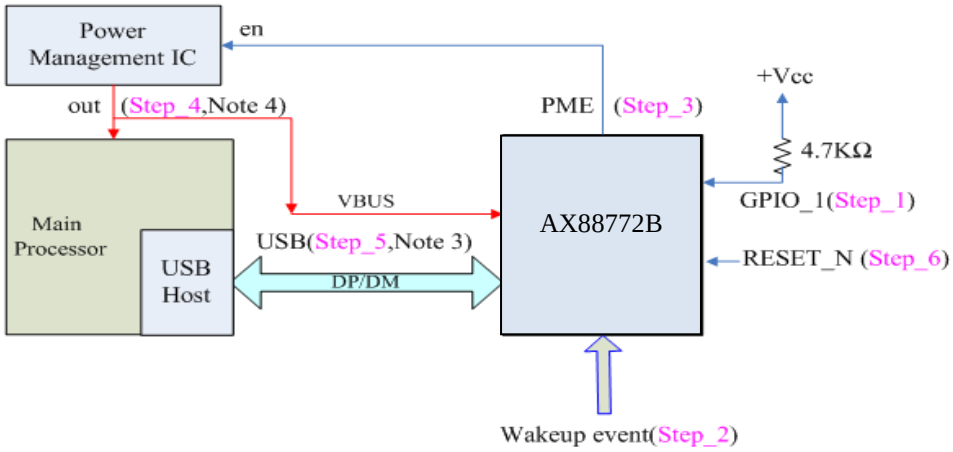
APPENDIX A. Default Wake-On-LAN (WOL) Ready Mode

This Default WOL Ready Mode application is different from normal operation where AX88772B Suspend/Resume state usually has to be configured by software driver during normal system operation. This application applies to a system that needs to use a predefined remote wakeup event to turn on the power supply of the system processor and its peripheral circuits without having any system software running in the beginning. This is quite useful when a system has been powered down already and a user needs to power on the system from a remote location.

The AX88772B can be configured to support Default WOL Ready Mode, where no system driver is required to configure its WOL related settings after power on reset. A system design usually partitions its power supply into two or more groups and the AX88772B is supplied with an independent power separated from the system processor. The power supply of AX88772B is usually available as soon as power plug is connected. The power supply of system processor remains off initially when power plug is connected and is controlled by AX88772B's PME pin, which can be activated whenever AX88772B detects a predefined wakeup event such as valid Magic Packet reception, Secondary PHY link-up, or the EXTWAKEUP_N pin trigger. To conserve power consumption, initially the USB host controller communicating with AX88772B can also be unpowered as the system processor.

The PME pin of AX88772B can control the power management IC to power up the system processor along with the USB host controller, which will perform USB transactions with AX88772B after both have been initialized. The pin polarity of PME is configured as high active when enabling Default WOL Ready Mode (see following **A.1** Note 2). Note that the AX88772B must be in self-power (via setting EEPROM Flag [0]) mode for this function.

A.1 Procedure to Enable Default WOL Ready Mode



To enable Default WOL Ready Mode, a user needs to configure GPIO_0 pin definition as PME (via setting EEPROM Flag [12]) and have GPIO_1 pulled-up with a 4.7Kohm resistor. After power on reset, AX88772B will disable most functions including USB transceiver (see Note 3) but enable Magic Packet detector logic and internal Ethernet PHY and its auto-negotiation function to be ready to receive Magic Packet. In PHY mode for AX88772B, Secondary PHY link-up can be a wakeup event (see Note 1).

When a valid Magic Packet is received, AX88772B will assert the PME pin to indicate to system processor the wakeup event. The PME pin, when being configured as static level output signal (via setting EEPROM Flag [15], see Note 2), can be used to control the power management IC to enable system power supply. After asserting the PME pin, AX88772B will also exit from the Default WOL Ready Mode and revert back to normal operation mode to start normal USB device detection, handshaking, and enumeration.

The PME pin, when being configured as static level output signal, maintains its signal level until RESET_N is asserted again. If asserting RESET_N to AX88772B with GPIO_1 pulled-up, the Default WOL Ready Mode will be re-entered. Otherwise (GPIO_1 being pulled-down), the normal operation mode (non-Default WOL Ready Mode) will be entered and the normal USB device detection, handshaking and enumeration process should take place right after RESET_N negation.

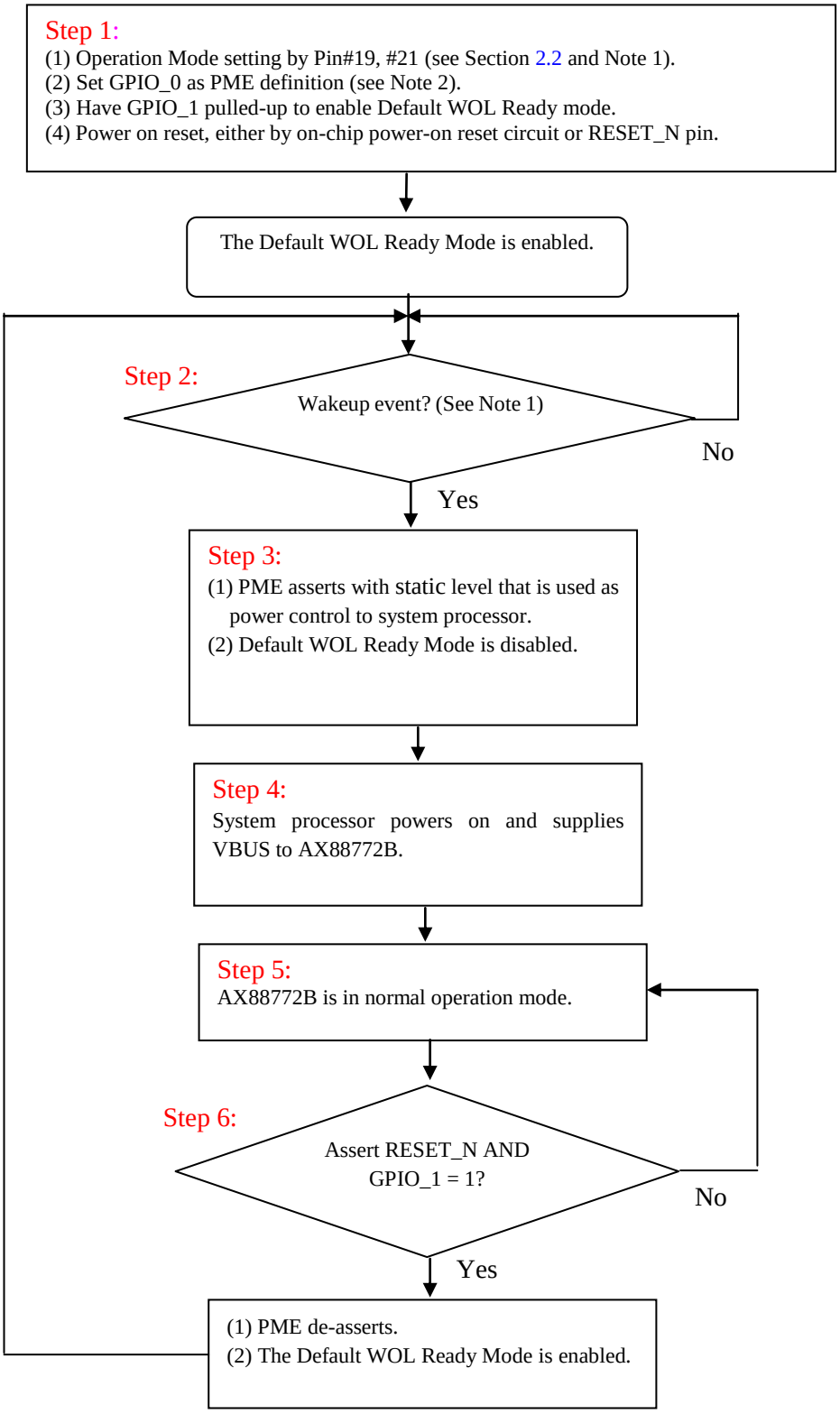
Note 1: For complete truth table of wakeup events supported, please refer to below **Remote Wakeup Truth Table** on the "GPIO_1 = 1" setting.
Note 2: Please refer to 4.1.2 Flag. The bit [15:12] of Flag (PME_IND, PME_TYP, PME_POL, PME_PIN) = 0111.
Note 3: When the Default WOL Ready Mode is enabled, the DP/DM pins ofAX88772B will be in tri-state.
Note 4: It is recommended that VBUS pin be connected to system power group directly. This way the V_BUS will become logic high when power management IC enables the system power supply.

Waken Up by	Setting						Wakeup Event						Device wakes up
	RWU bit of Flag byte in EEPROM	Set_Feature standard command	RWWF	RWMP	RWLC	GPIO_1 (*)	Host sends resume signal	Receiving a Wakeup Frame	Receiving a Magic Packet	Link status change detected On Primary PHY	Link status change detected On Secondary PHY	EXTWAKEUP_N pin	
USB Host	X	X	X	X	X	0	J → K						Yes
Device	0	0	X	X	X	0		X	X	X	X	X	No
Device	1	1	1	0	0	0		Yes					Yes
Device	1	1	0	1	0	0			Yes				Yes
Device	1	1	0	0	1	0				Yes			Yes
Device	1	1	0	0	1	0					Yes		Yes
Device	1	1	X	X	X	0						Low-pulse	Yes
Device	X	0	0	0	0	1			Yes		Yes	Low-pulse	Yes

*: About Default WOL Ready Mode, please refer to section 2.2 GPIO_1 Settings.

Table 15 : Remote Wakeup Truth Table

A.2 Flow Chart of Default WOL Ready Mode



APPENDIX B. Ethernet PHY Power and Reset Control

This section indicates some information about AX88772B Ethernet PHY Power and Reset control.

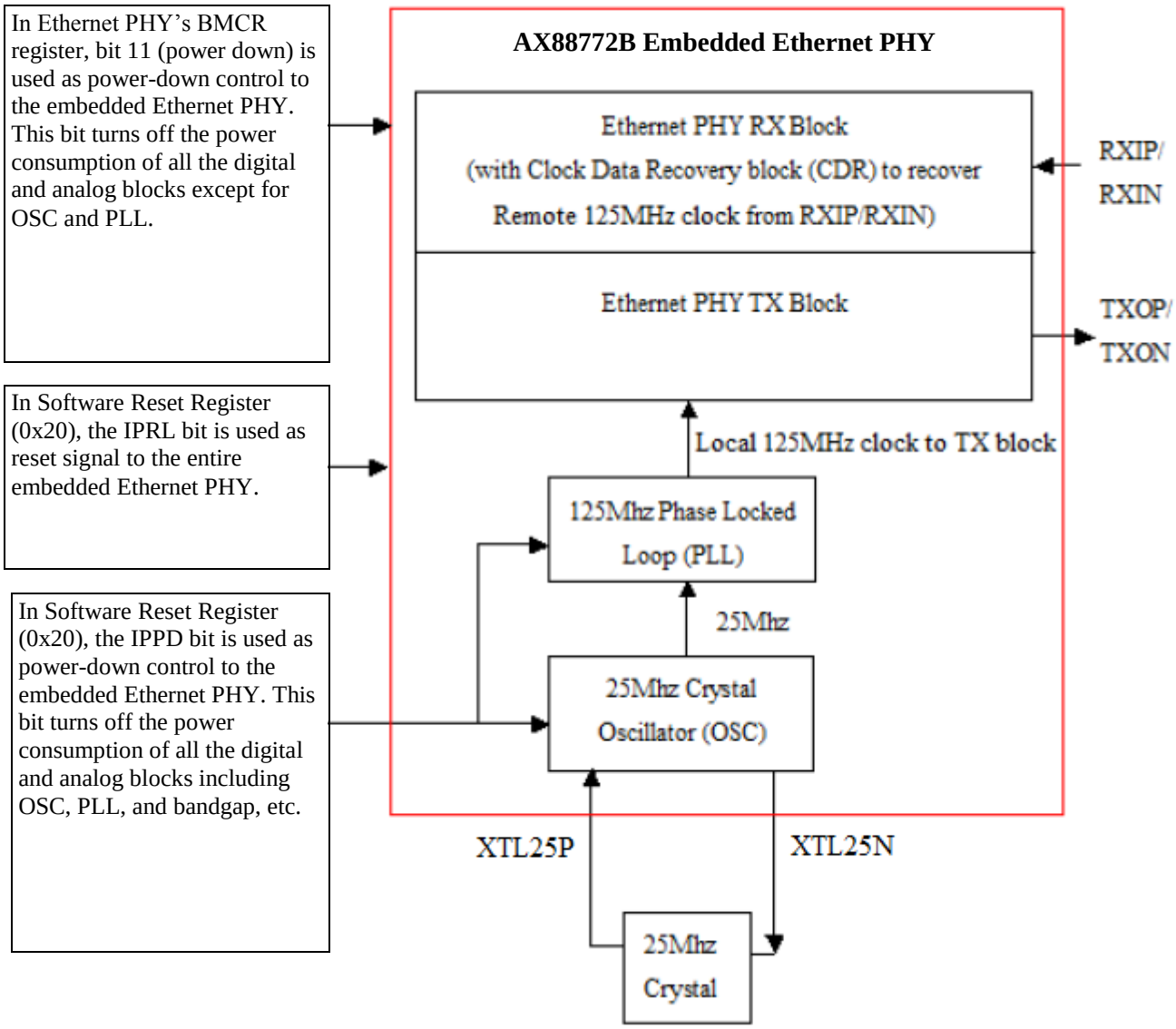
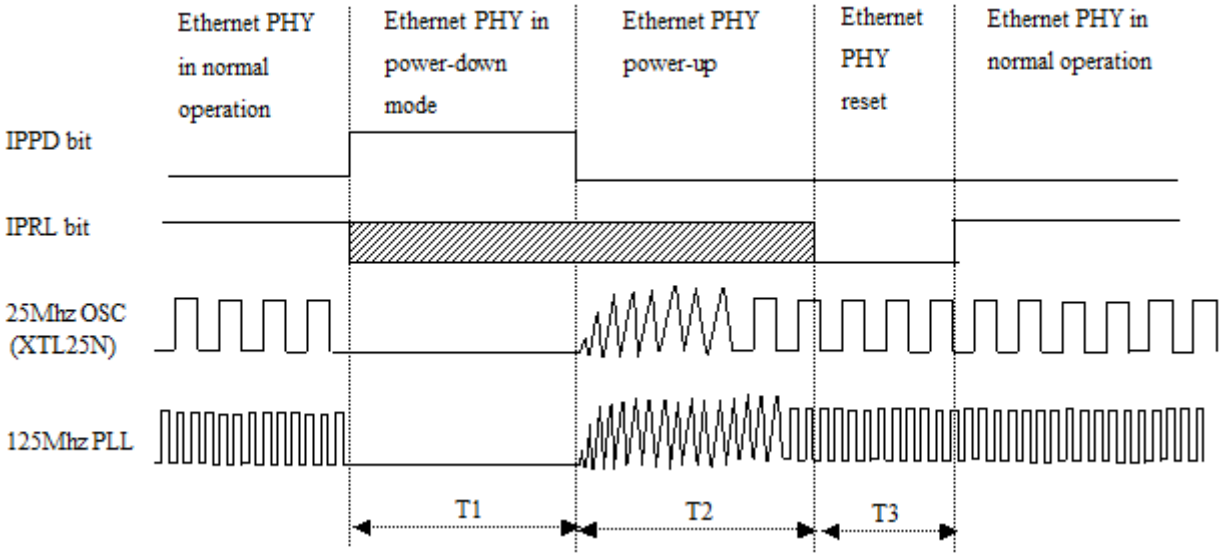


Figure 22 : Ethernet PHY Oscillator/PLL Block Diagram

The following power-up and reset signal timing issued to the Ethernet PHY of AX88772B must be met in order to initialize the Ethernet PHY properly and reliably every time after it has been put into power-down mode previously.



Symbol	Description	Min	Typ	Max
T1	Ethernet PHY in power-down mode where the internal 25Mhz OSC, 125Mhz PLL and analog bandgap of AX88772B are completely turned off for max. power saving. This is the lowest power consumption mode of the Ethernet PHY. Note: Alternatively, user can use the Ethernet PHY's BMCR register bit 11, "power down", to set the Ethernet PHY into power-down mode. When the BMCR bit 11 power-down is used, the 25Mhz OSC and 125Mhz PLL will remain toggled but the analog bandgap will be turned off. The power consumption of BMCR bit 11 power-down mode is about 15mA more than the Software Reset Register (0x20) IPPD bit power-down mode.	500ns	-	-
T2	From Ethernet PHY power-up to 25Mhz OSC and 125Mhz PLL stable time. Note: If the IPRL is low during T2, it should be kept at low for more than T2 time so that the Ethernet PHY can be reset properly right after the power-up. In other words, the successful and reliable reset to the Ethernet PHY can only be accomplished with a stable running 25Mhz OSC and 125Mhz PLL clocks.	600ms	-	-
T3	Mandatory Ethernet PHY reset time after it has just been powered up from the previous power-down mode (after >T2 time). Also, software can issue reset to the Ethernet PHY during its non-power-down mode, but the minimum reset duration defined here must be met.	500ns	-	-

Figure 23 : Ethernet PHY Power-up & Reset Timing Diagram

APPENDIX C. External EEPROM / Internal ROM / Internal ID-SRAM of Vender Descriptions selection

The AX88772B supports ASIX default device descriptors ROM and ID-SRAM to store the customized device descriptors for USB enumeration process. Therefore, the AX88772B supports two methods to replace EEPROM if AX88772B is embedded in a system board with USB Host. The following Figure 24 shows the source of vender descriptions selection policy of AX88772B.

- **EEPROM-less and selected ASIX default device descriptor ROM:**

  The Host will bring up AX88772B device by embedded internal device descriptor ROM after USB enumeration process due to none of external EEPROM, checksun error or non-programmed EEPROM.

  This method is only suitable for those applications that can work fine on the AX88772B hardware default SROM setting, and the designer should manually assign an unique MAC address for each AX88772B device. Please refer to Section 4.2 “Internal ROM Default Settings” for more details and contact ASIX's Support (support@asix.com.tw) for further support.

- **EEPROM-less and selected ID-SRAM:**

  The Host will bring up a customization of AX88772B device by programmed ID-SRAM after two procedures of USB enumeration process.

  First, the Host will find AX88772B device by embedded internal device descriptor ROM after USB enumeration process due to none of external EEPROM. The system can program customized device descriptors into internal ID-SRAM by AX88772B’s vendor command (Note AC.1) and make a global software reset (Note AC.2) after that.

  Second, based on the source of vender descriptors selection policy of AX88772B, the Host will bring up AX88772B device by ID-SRAM due to none of external EEPROM and programmed ID-SRAM.

  This method is only suitable for AX88772B self-power applications. Please refer to Figure 24 for more details and contact ASIX's Support (support@asix.com.tw) for further support.

Note AC.1 Vendor Command RX/TX/ID-SRAM Read/Write Register, 02h and 03h
Note AC.2 Vendor Command Global Reset Control Register, F0h
The ID-SRAM only cleared by power cycle or hardware reset.

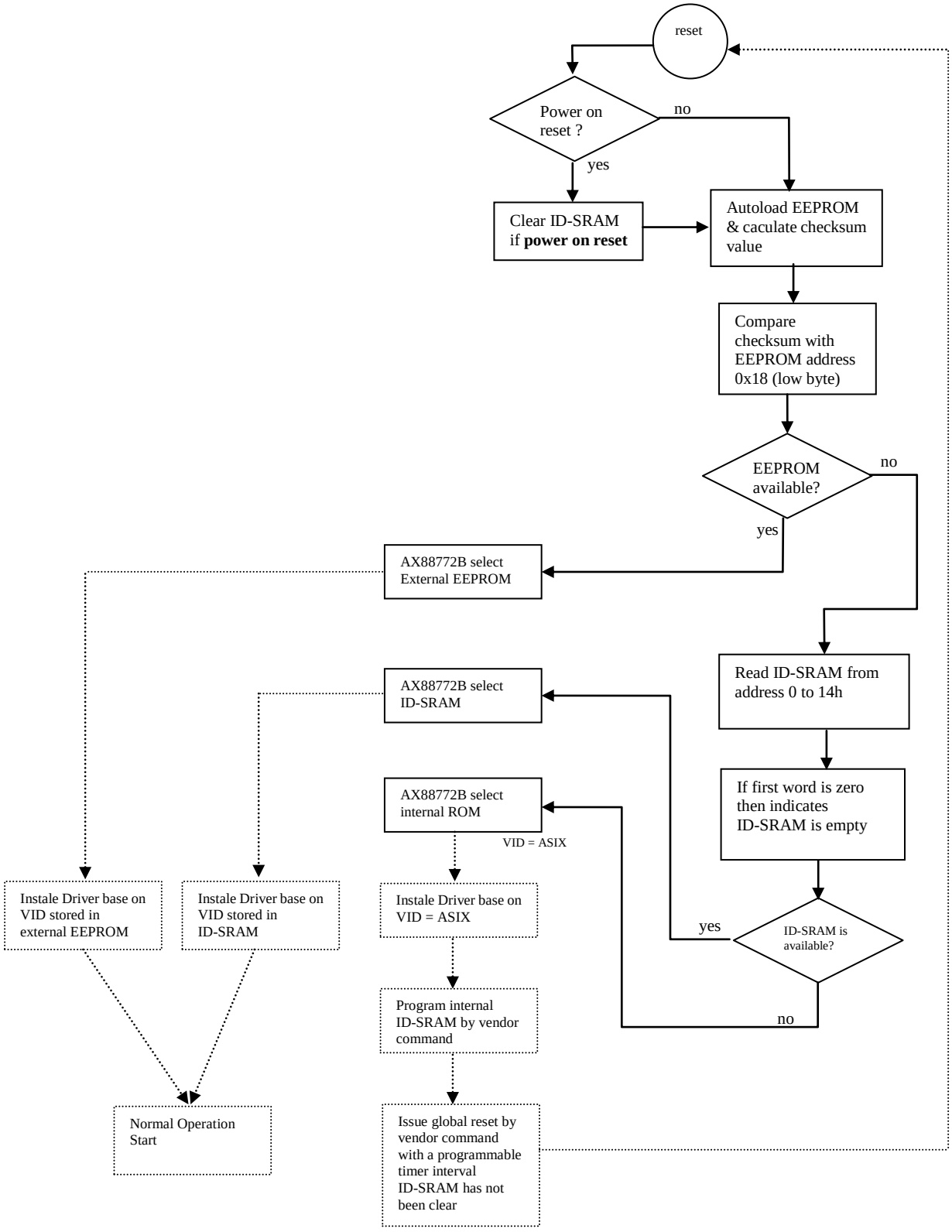


Figure 24 : External EEPROM / Internal ROM / Internal ID-SRAM of Vender Descriptions selection

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