100mA Single Inductor - Dual Output Power Supply

Features

- 2.7V to 5.5V Input Voltage
- Dual Regulated Output Using Single Inductor
- Positive Output Voltage Range:
  4.0V to 6.0V (100mV/Step)
- Negative Output Voltage Range:
  -6.0V to -4.0V (100mV/Step)
- Maximum Output Current: 100mA
- Outstanding Combined Efficiency
  η > 80% at I_{OUT} > 10 mA
  η > 85% at I_{OUT} > 40 mA
- Outstanding Transient Response & Line Regulation
- ±1.5% Output Voltage Accuracy
- Shut-Down Supply Current: 1uA
- Under-Voltage Lock-Out and Thermal Shutdown
- WLCSP 1.27mm×2.00mm×0.625mm-15B, 0.4mm Pitch Package

Applications

TFT LCD Smartphones, Tablets and NB
Dual Power Supply Application

General Description

The AW37501 is designed to support positive /negative supply for driving TFT-LCD panels mainly in smartphones and tablets. The device employs a single inductor scheme to provide a small bill-of-material and smallest PCB solution size.

It integrates a step-up DC-DC converter for preceding supply. An architecture with LDO and negative charge pump (NCP) generates dual outputs at +5.4V (default) and -5.4V (default), whose voltages can be programmed via an I^2C compatible interface.

The device offers excellent line and load regulation performances, as well as load transient. It features an outstanding efficiency that is greater than 80% when I_{OUT}>10mA and 85% when I_{OUT}>40mA. With its input voltage range of 2.7V to 5.5V, it can be powered by single-cell batteries (Li-Ion, Ni-Li, Li-Polymer).

Typical Application Circuit

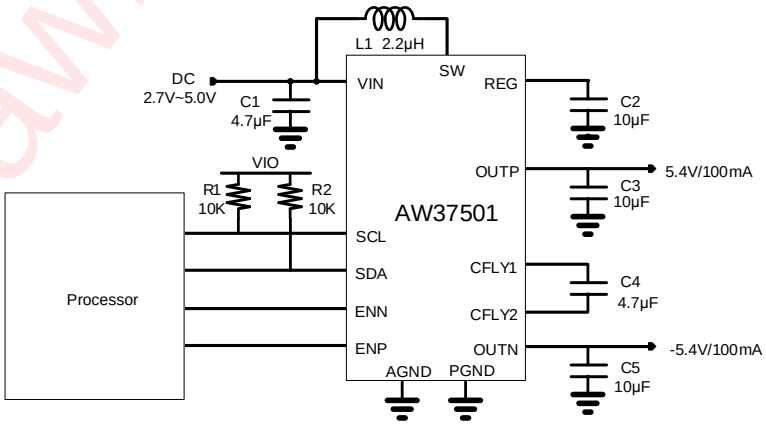
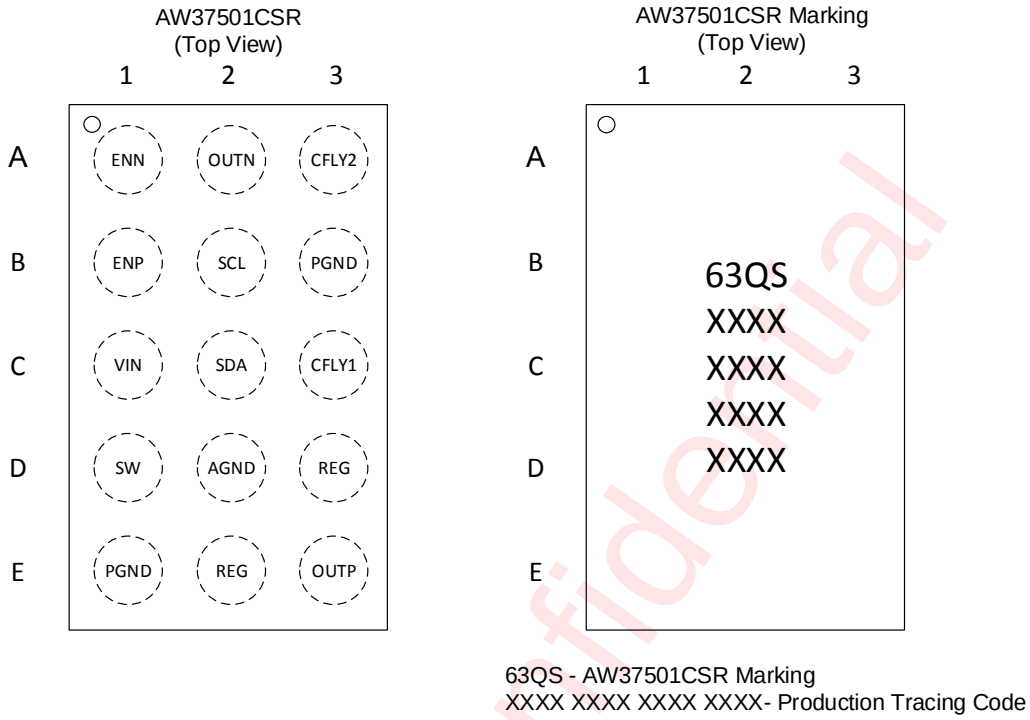


Figure 1 Typical Application Circuit of AW37501

Pin Configuration And Top Mark



63QS - AW37501CSR Marking
XXXX XXXX XXXX XXXX- Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
A1	ENN	Enable input for negative output (OUTN). A logic high enables the negative output, a logic low forces the output into shutdown.
A2	OUTN	Output pin of the negative charge pump.
A3	CFLY2	Negative charge pump flying capacitor pin.
B1	ENP	Enable Input for positive output (OUTP). A logic high enables the positive output, a logic low forces the output into shutdown.
B2	SCL	Clock input for the I^2C serial interface.
B3	PGND	Power Ground.
C1	VIN	Power Input.
C2	SDA	Data input for the I^2C serial interface.
C3	CFLY1	Negative charge pump flying capacitor pin.
D1	SW	Switch pin of the boost converter.
D2	AGND	Analog ground.
D3	REG	Boost converter output pin.
E1	PGND	Power Ground.
E2	REG	Boost converter output pin.
E3	OUTP	Output pin of the LDO.

Functional Block Diagram

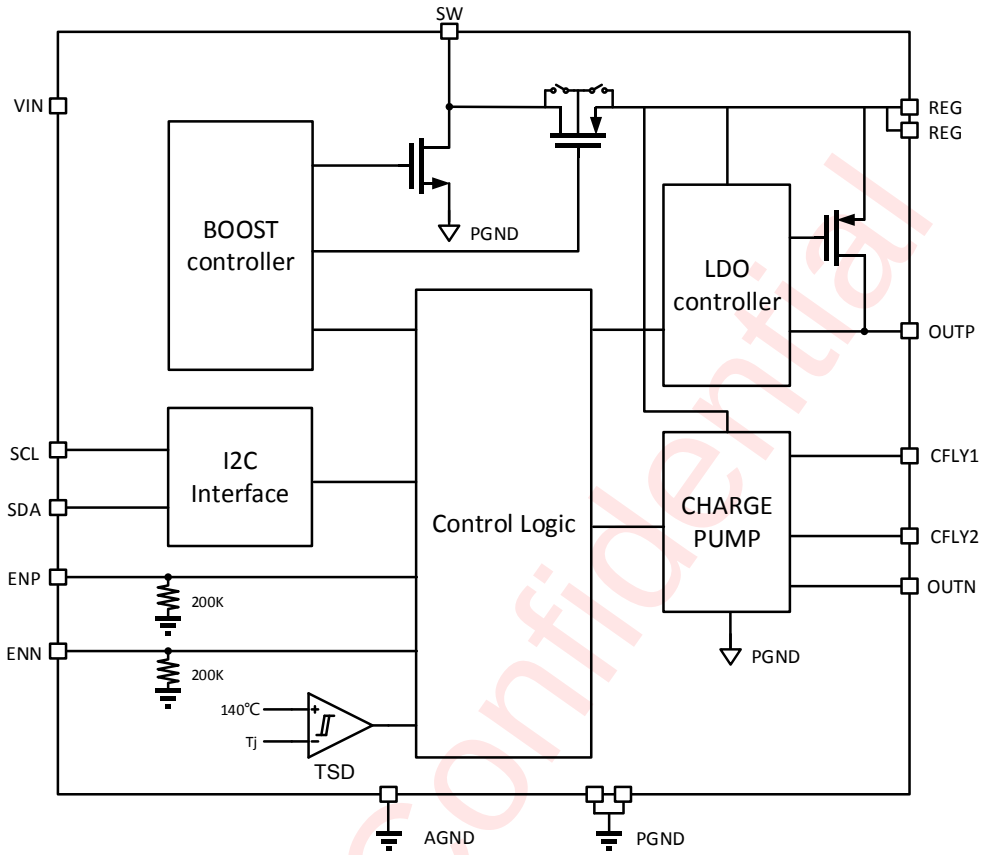


Figure 3 Functional Block Diagram

Typical Application Circuits

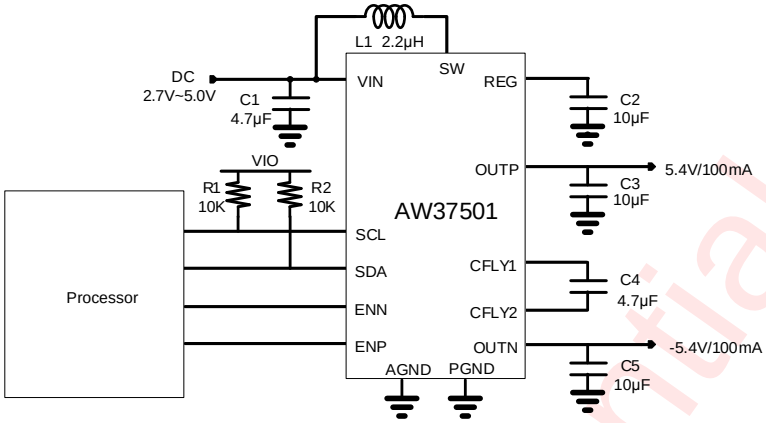


Figure 4 AW37501 Application circuit

Notice for typical application circuits:

1. All peripheral devices should be as closed as possible to the chip, C1、C2、C3、C4、C5 and L1 should be closed to VIN、REG、OUTP、CFLY1/2 and OUTN pins respectively. Besides the metal traces between them should be short and wide.
2. The inductor recommended 2.2μH is suitable for 80mA and 100mA application for better efficiency, but the value is usually 4.7μH for good current sensing and controlling function inside in 40mA mode.
3. The input capacitor C1 can be larger values; the output capacitors C2, C3 and C5 should be selected in recommended values, the larger value of C2, C3 and C5, the smaller of the ripple voltage, but the longer of starting time; the flying capacitor C4 can be larger, but overlarge value may cause large inrush current during startup.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37501CSR	-40℃～85℃	WLCSP 1.27mmX2.00mm X0.625mm-15B	63QS	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{IN}		-0.3V to 6V
Input voltage range	ENN, ENP, SDA, SCL	-0.3V to V_{IN}+0.3V
Output voltage range	SW	-0.3V to 8V
	REG, CFLY1	-0.3V to 8V
	OUTP	-0.3V to 7V
	CFLY2, OUTN	-7V to 0.3V
Junction-to-ambient thermal resistance θ_{JA}		91.5°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 2)	±2	kV
CDM(NOTE 3)	±1.5	kV
Latch-Up(NOTE 4)	+IT：200；-IT：-200	mA

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017*

NOTE3: Test method: ESDA/JEDEC JS-002-2018

NOTE4: Test method: JESD78E

Recommended Components List

Component	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
L1	Inductor		2.2		μH
C1	Input capacitor	4.7			μF
C2	REG output capacitor	4.7			μF
C4	Flying capacitor	2.2			μF
C3 & C5	OUTP and OUTN output capacitor	4.7			μF

Electrical Characteristics

V_{IN}=3.7V, ENN=ENP=V_{IN}, V_{OUTP}=5.4V, V_{OUTN}=-5.4V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT VOLTAGES and CURRENTS						
V_{IN}	VIN supply voltage range		2.7		5.0	V
V_{UVLO}	Under-voltage lockout threshold	V_{IN} rising	2.3	2.4	2.5	V
		V_{IN} falling	2.1	2.2	2.3	V
I_Q	Quiescent current	I_{OUT}=0mA	0.6	0.83	1.2	mA
I_{SD}	Shutdown down current	ENP=ENN=0V		1	2	μA
LOGIC ENN, ENP, SDA, SCL						
V_{IH}	High level input voltage	V_{IN}=2.5 V to 5.0 V	1.2			V
V_{IL}	Low level input voltage				0.4	V
V_{OL}	Low level output voltage	V_{IN}=2.5 V to 5.0 V, sinking 2mA			0.4	V
R_{EN}	Pulldown resistors	ENP and ENN pull-down resistance	0.1	0.2	0.3	MΩ
BOOST CONVERTER CHARACTERISTICS						
I_{LIM}	Boost converter valley current limit value		1.2	1.5	2.0	A
Fsw	Boost converter switching frequency		1.1	1.4	1.7	MHz
T_{SS}	Soft start-up time			0.2	1.0	ms
LDO CHARACTERISTICS						
V_{OUTP}	Positive output voltage range	In 100mV steps, no load	4.0		6.0	V
	Default output voltage	I_{OUTP}=80mA		5.4		V
	Positive output voltage accuracy	I_{OUTP}<100mA	–1.5		1.5	%
I_{OUTP}	Positive output current capability	ENP=High	200			mA
I_{OUTP_LIM}	OUTP output current limit value	REG04H[4]=0	300	370	440	mA
		REG04H[4]=1	220	270	360	mA
V_{DROP}	Dropout voltage	V_{REG}=V_{OUTP}=5.4V, I_{OUTP}=150mA	30	60	100	mV
V_{LIP}	OUTP line regulation	V_{IN}=2.7V to 5.0V, I_{OUTP}=80mA		0.024	0.08	%/V
	OUTP line variation			3	10	mV
V_{LOP}	OUTP load regulation	ΔI_{OUTP}=80mA		2	3	%/A
R_{DISP}	OUTP discharge resistor		40	60	100	Ω
NEGATIVE CHARGE PUMP CHARACTERISTICS						
V_{OUTN}	Negative output voltage range	In 100mV steps, no load	–6.0		–4.0	V
	Default Output	I_{OUTN}=80mA		-5.4		V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Negative output voltage accuracy	I_{OUTN}<100mA	–1.5		1.5	%
I_{OUTN}	Negative output current capability	REG03H[7:6]=00，40mA mode	40		60	mA
		REG03H[7:6]=01，80mA mode(default)	80		120	mA
		REG03H[7:6]=10，100mA mode	100		165	mA
F_{NCP}	Negative charge pump switching frequency		0.9	1.0	1.1	MHz
V_{LIN}	OUTN line regulation	V_{IN}=2.7V to 5.0V, I_{OUTN}=80mA		0.024	0.16	%/V
	OUTN line variation			3	20	mV
V_{LON}	OUTN load regulation	ΔI_{OUTN}=100mA		8		%/A
R_{DISN}	OUTN discharge resistor		14	20	30	Ω
PROTECTION						
T_{OTP}	Overheating shutdown temperature			140		°C
	Thermal hysteresis for T_{OTP}			20		°C

I²C INTERFACE TIMING

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock Frequency				400	kHz
$t_{DEGLITCH}$	Deglitch Time	SCL		83		ns
		SDA		115		ns
$t_{HD:STA}$	(Repeat-Start) Start Condition Hold Time		0.6			μs
t_{LOW}	Low Level Width of SCL		1.3			μs
t_{HIGH}	High Level Width of SCL		0.6			μs
$t_{SU:STA}$	(Repeat-Start) Start Condition Setup Time		0.6			μs
$t_{HD:DAT}$	Data Hold Time		0			μs
$t_{SU:DAT}$	Data Setup Time		0.1			μs
t_R	Rising Time of SDA and SCL				0.3	μs
t_F	Falling Time of SDA and SCL				0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
t_{BUF}	Time Between Start and Stop Condition		1.3			μs

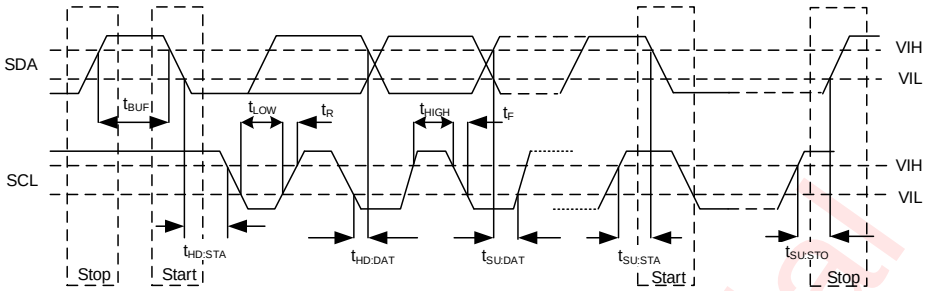


Figure 5 I²C Interface Timing

Typical Characteristics

V_{IN}=3.7V, ENN=ENP=V_{IN}, V_{OUTP}=5.4V, V_{OUTN}=-5.4V, T_A=25°C, Circuit of figure 4 unless other noted.

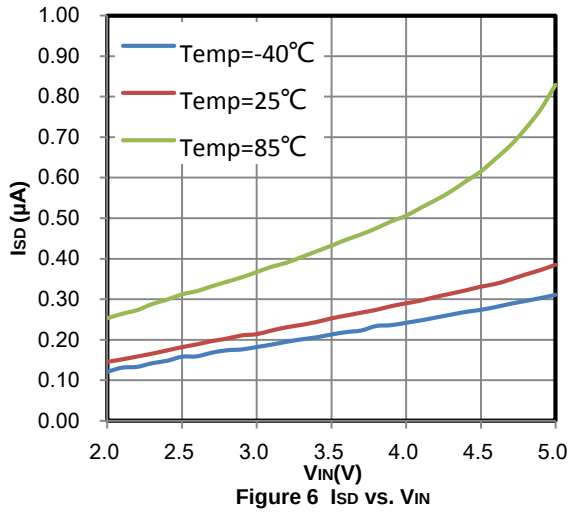


Figure 6 I_{SD} vs. V_{IN}

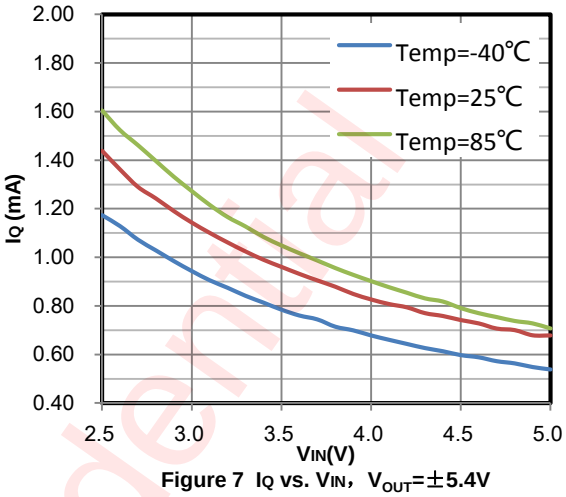


Figure 7 I_Q vs. V_{IN}, V_{OUT}=±5.4V

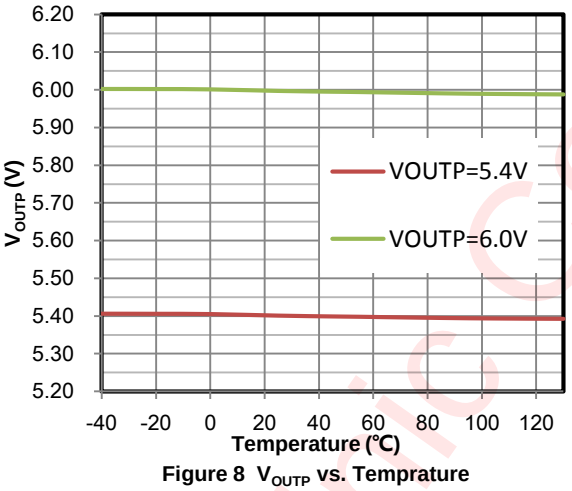


Figure 8 V_{OUTP} vs. Temprature

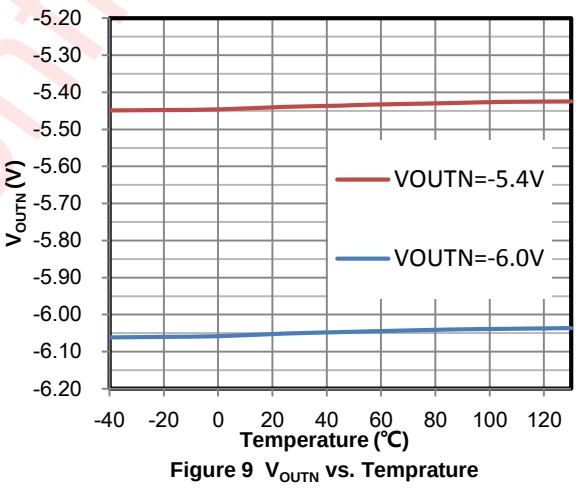


Figure 9 V_{OUTN} vs. Temprature

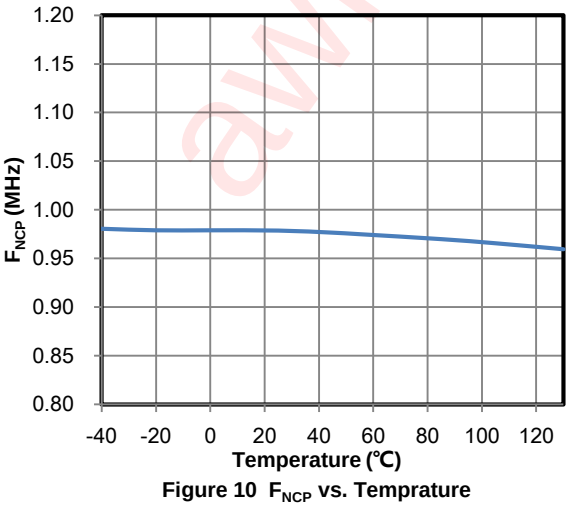


Figure 10 F_{NCP} vs. Temprature

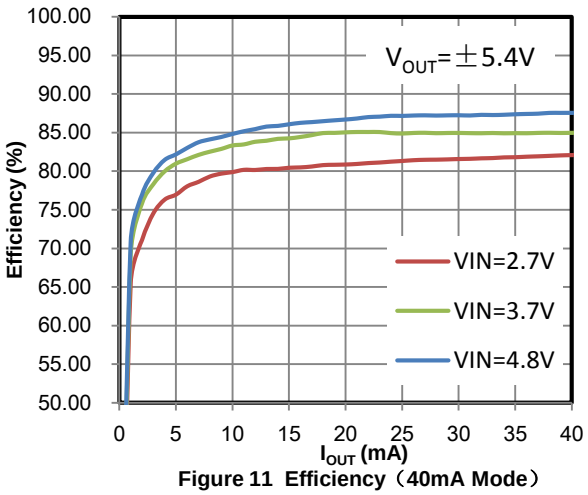


Figure 11 Efficiency（40mA Mode）

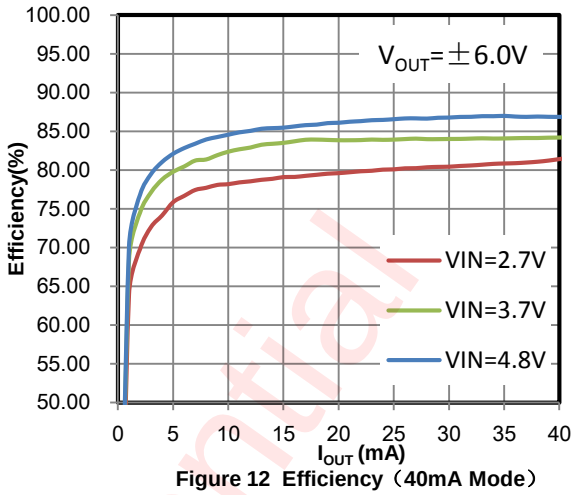


Figure 12 Efficiency（40mA Mode）

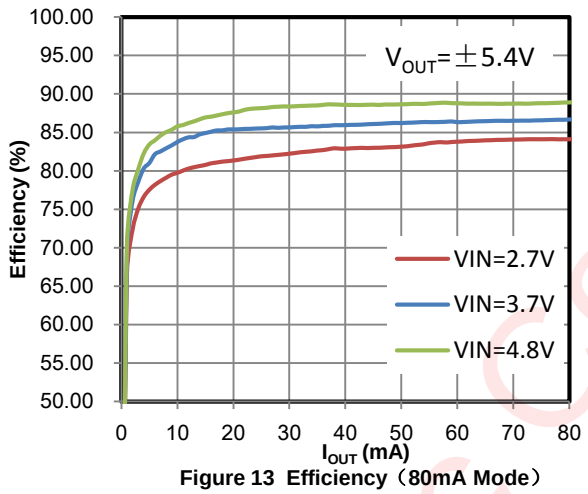


Figure 13 Efficiency（80mA Mode）

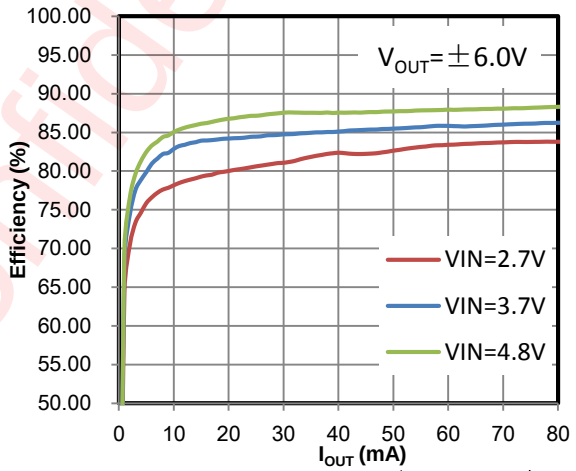


Figure 14 Efficiency（80mA Mode）

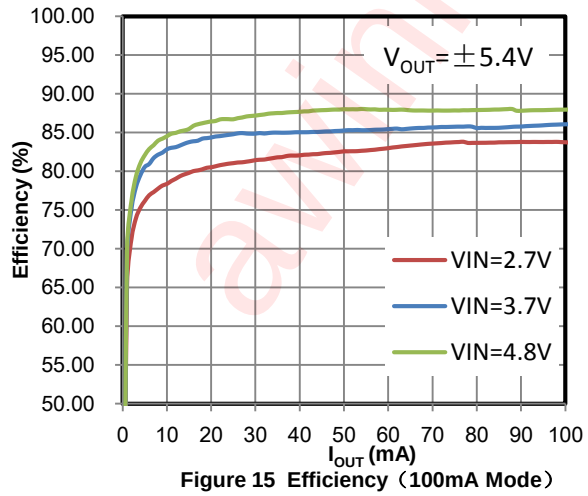


Figure 15 Efficiency（100mA Mode）

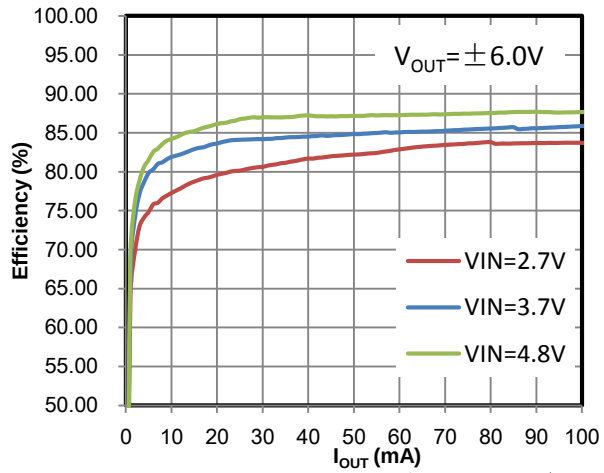


Figure 16 Efficiency（100mA Mode）

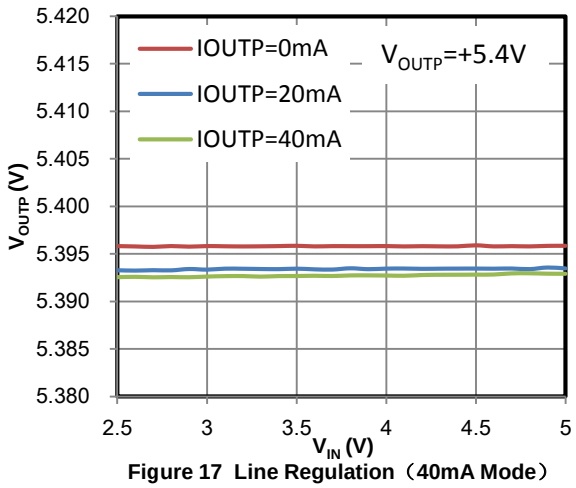


Figure 17 Line Regulation（40mA Mode）

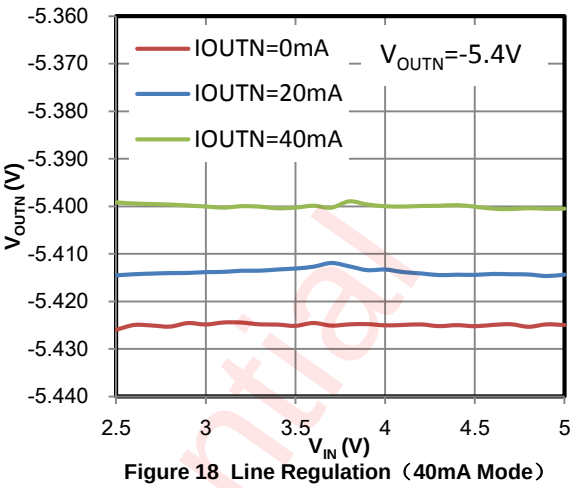


Figure 18 Line Regulation（40mA Mode）

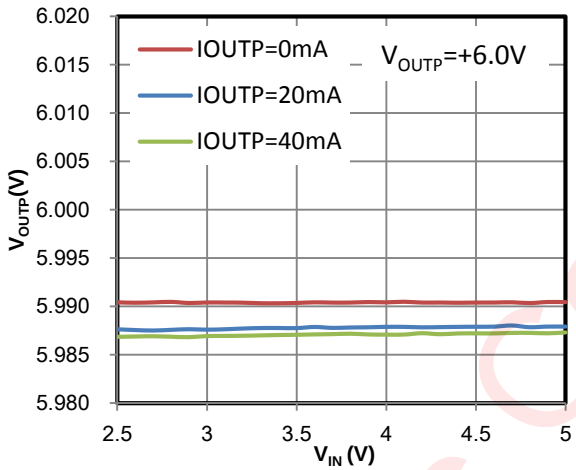


Figure 19 Line Regulation（40mA Mode）

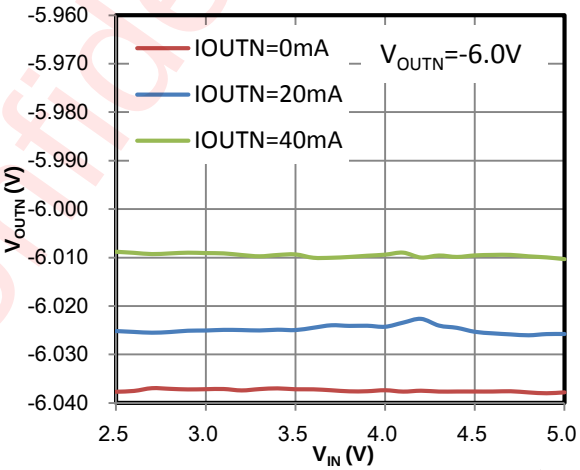


Figure 20 Line Regulation（40mA Mode）

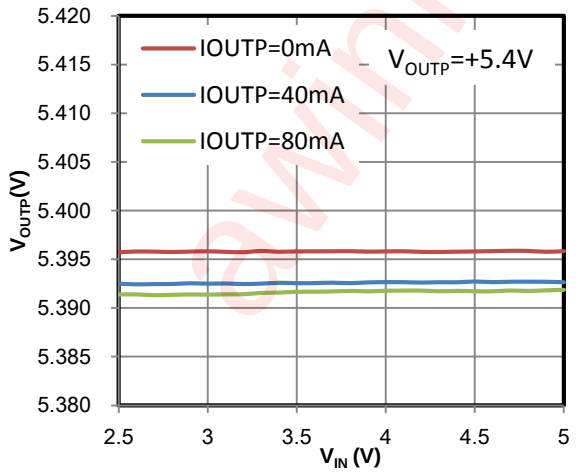


Figure 21 Line Regulation（80mA Mode）

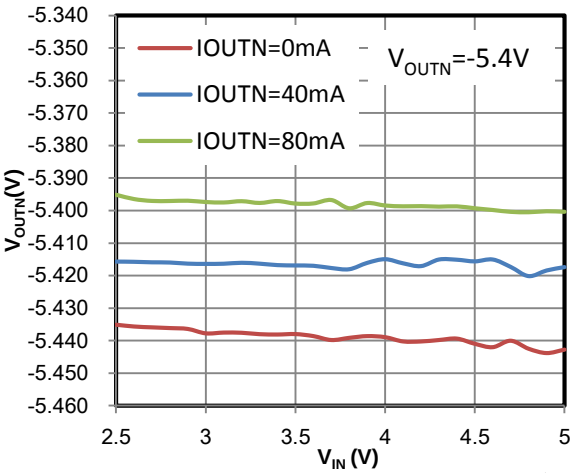


Figure 22 Line Regulation（80mA Mode）

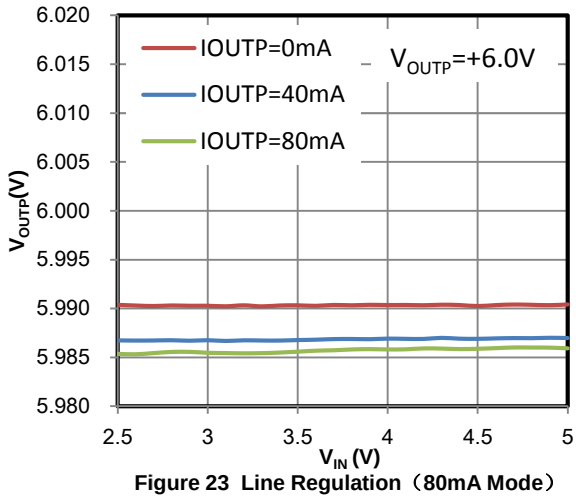


Figure 23 Line Regulation（80mA Mode）

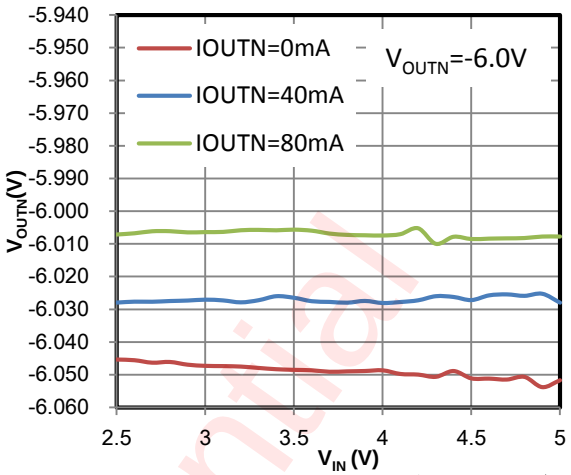


Figure 24 Line Regulation（80mA Mode）

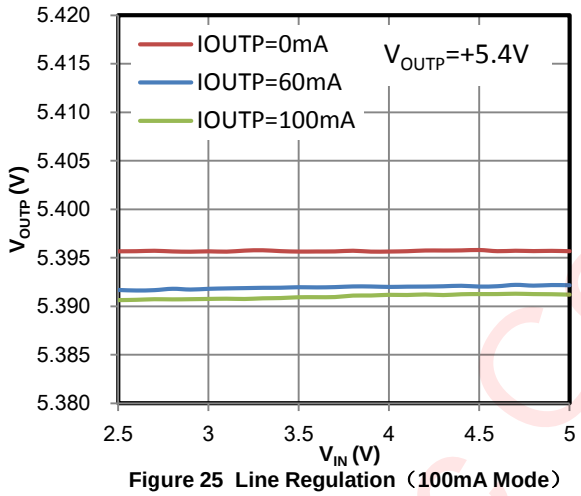


Figure 25 Line Regulation（100mA Mode）

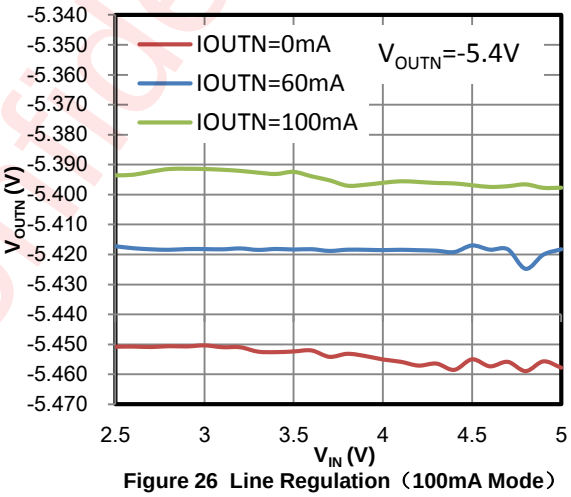


Figure 26 Line Regulation（100mA Mode）

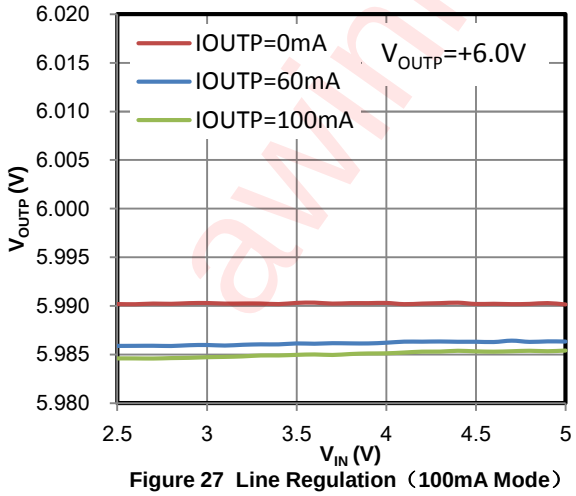


Figure 27 Line Regulation（100mA Mode）

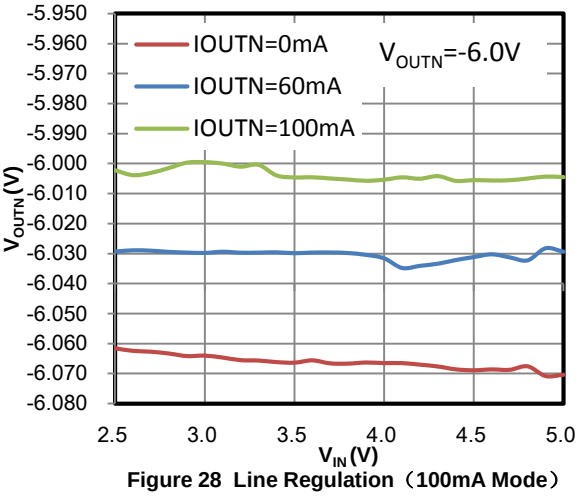


Figure 28 Line Regulation（100mA Mode）

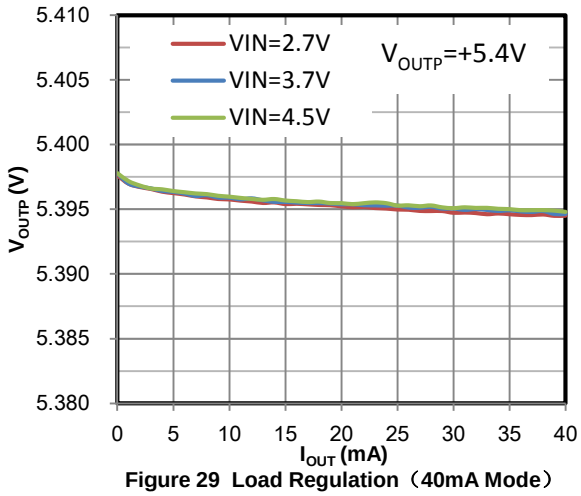


Figure 29 Load Regulation（40mA Mode）

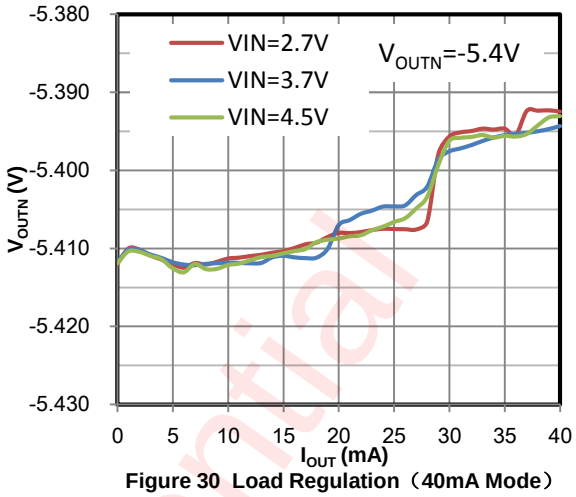


Figure 30 Load Regulation（40mA Mode）

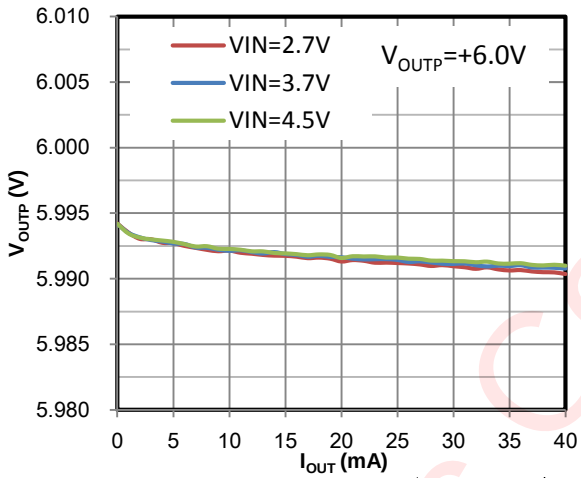


Figure 31 Load Regulation（40mA Mode）

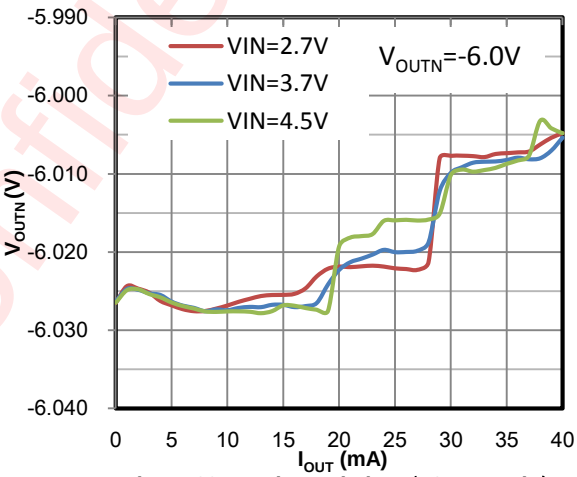


Figure 32 Load Regulation（40mA Mode）

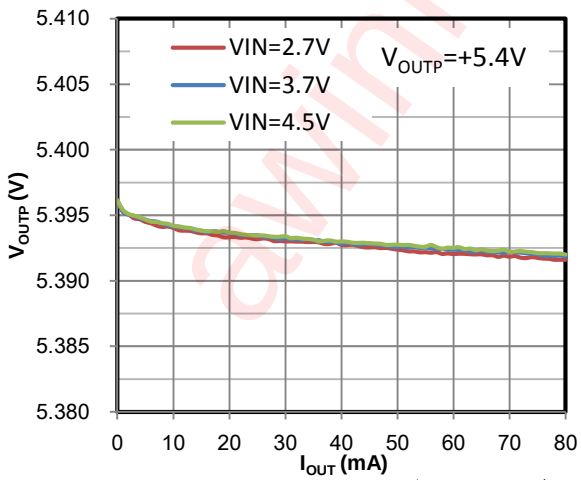


Figure 33 Load Regulation（80mA Mode）

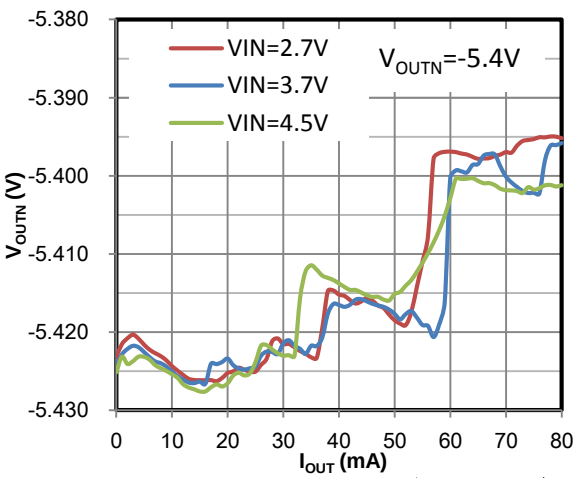


Figure 34 Load Regulation（80mA Mode）

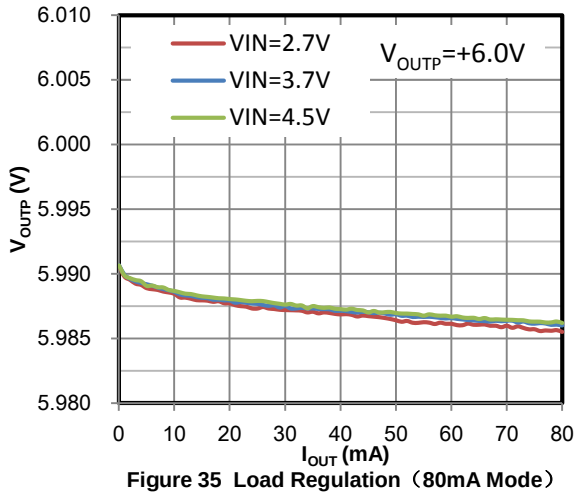


Figure 35 Load Regulation（80mA Mode）

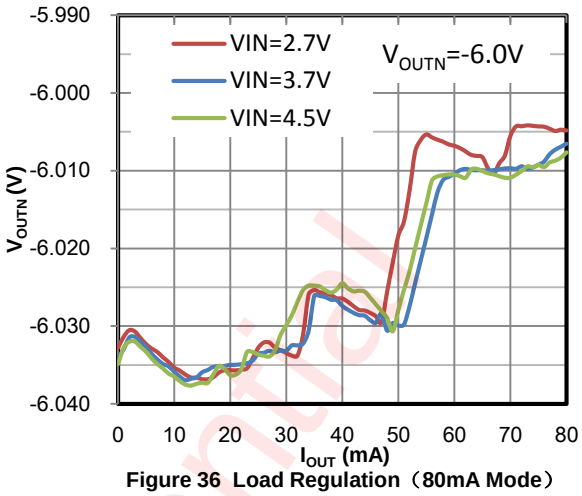


Figure 36 Load Regulation（80mA Mode）

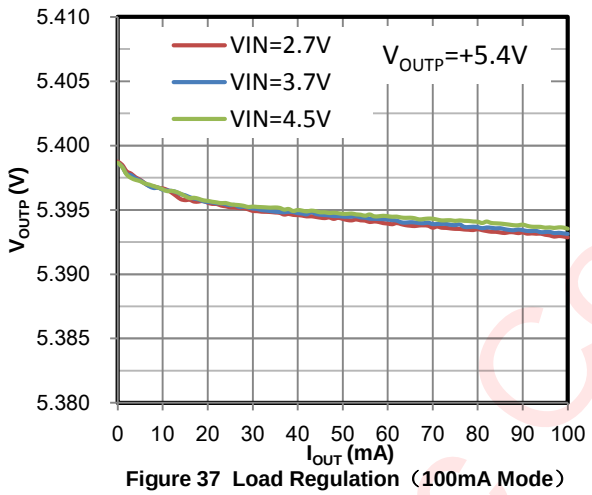


Figure 37 Load Regulation（100mA Mode）

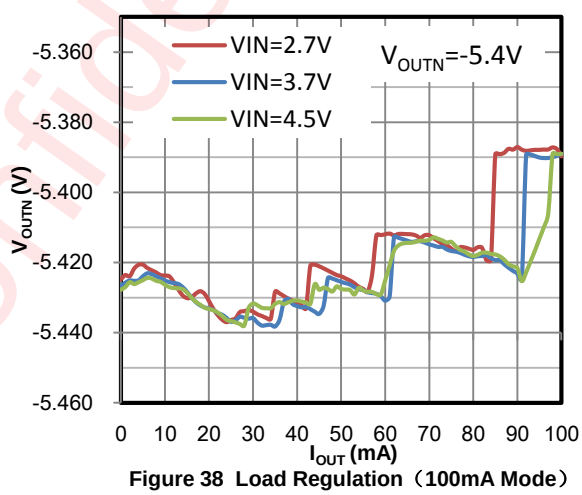


Figure 38 Load Regulation（100mA Mode）

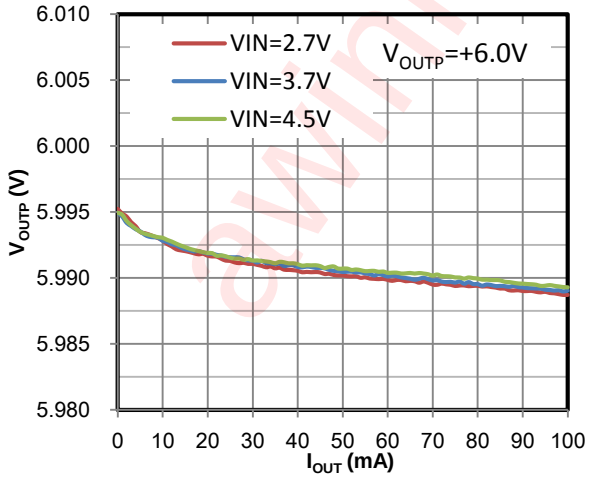


Figure 39 Load Regulation（100mA Mode）

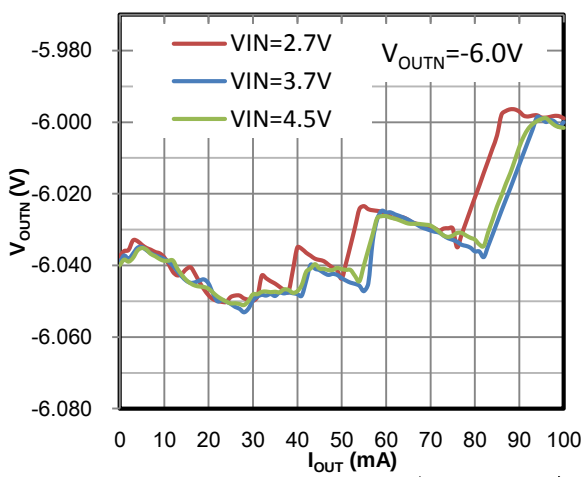


Figure 40 Load Regulation（100mA Mode）

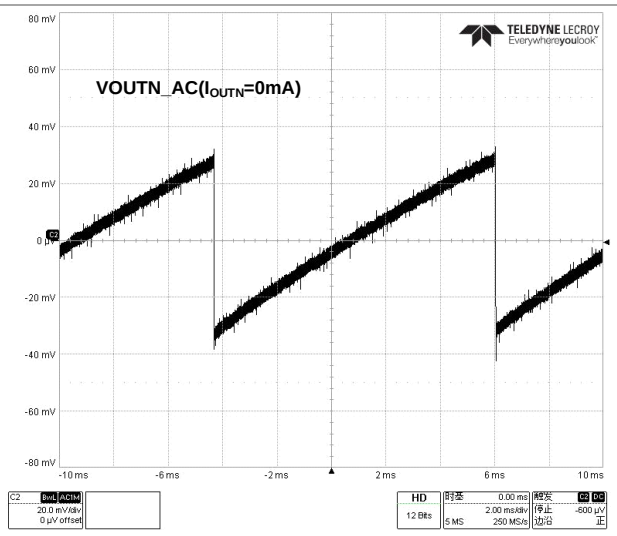


Figure 41 V_{OUTN} Output Voltage Ripple（80mA Mode）

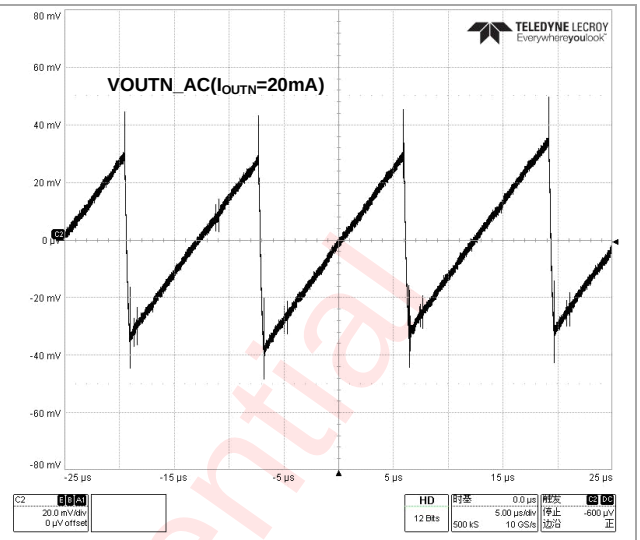


Figure 42 V_{OUTN} Output Voltage Ripple（80mA Mode）

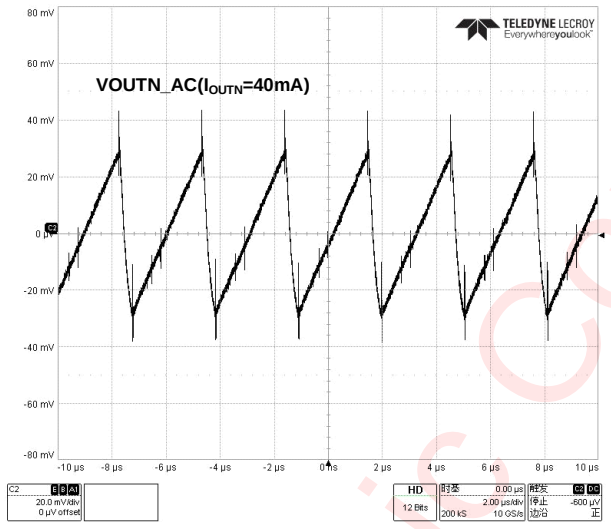


Figure 43 V_{OUTN} Output Voltage Ripple(80mA Mode)

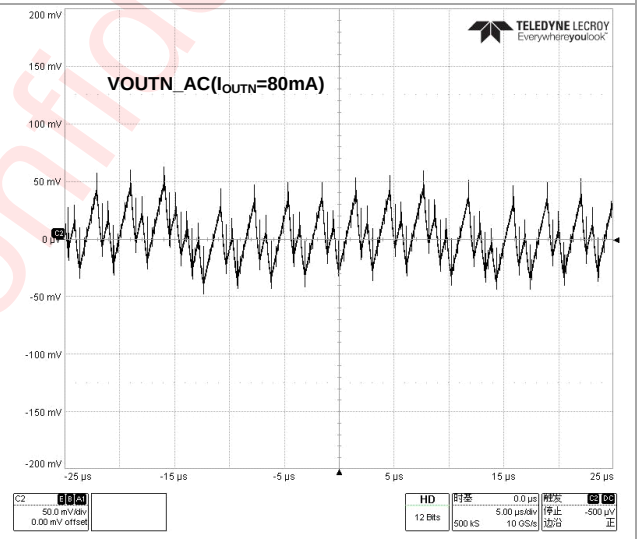


Figure 44 V_{OUTN} Output Voltage Ripple(80mA Mode)

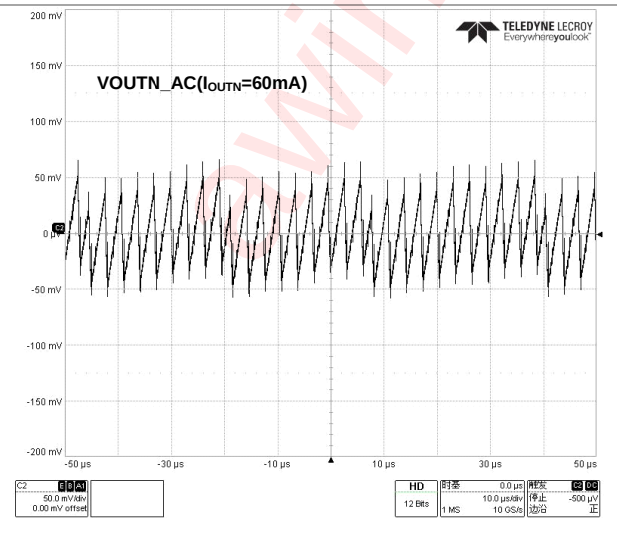


Figure 45 V_{OUTN} Output Voltage Ripple(100mA Mode)

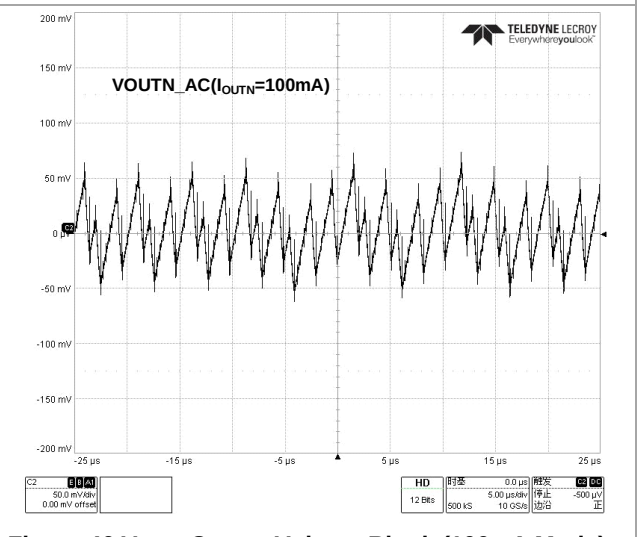


Figure 46 V_{OUTN} Output Voltage Ripple(100mA Mode)

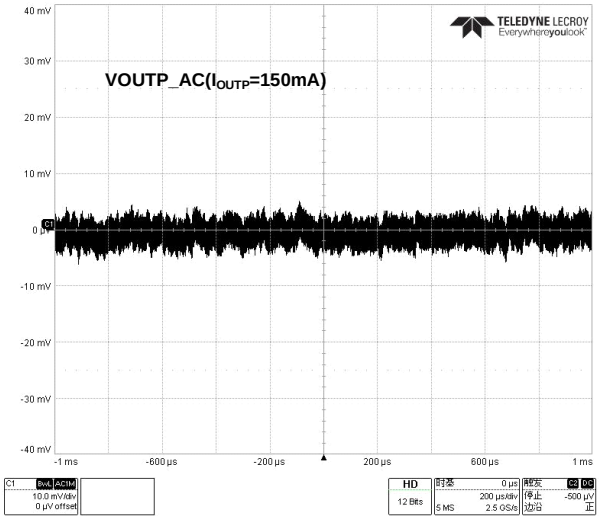


Figure 47 V_{OUTP} Output Voltage Ripple

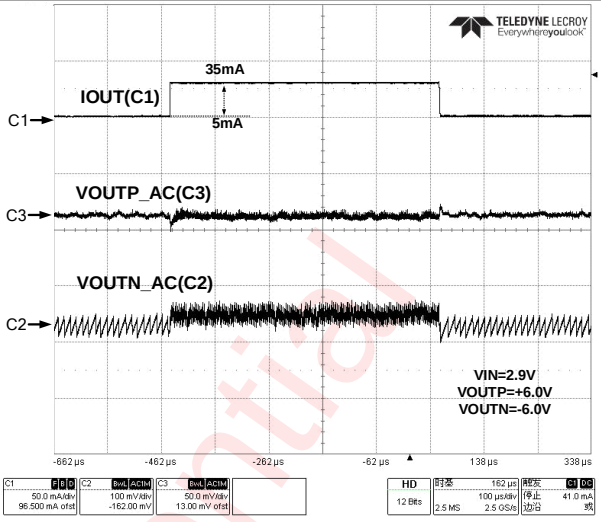


Figure 48 Load Transient（40mA Mode）

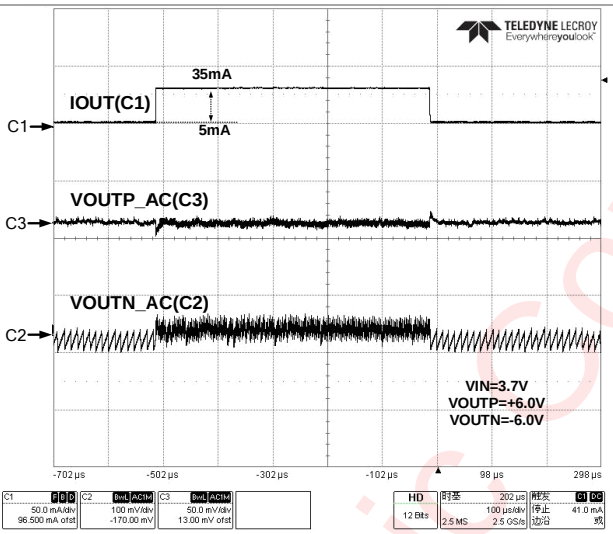


Figure 49 Load Transient（40mA Mode）

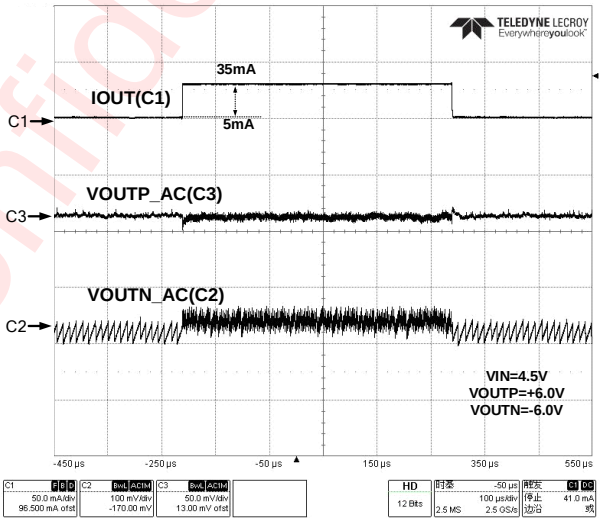


Figure 50 Load Transient（40mA Mode）

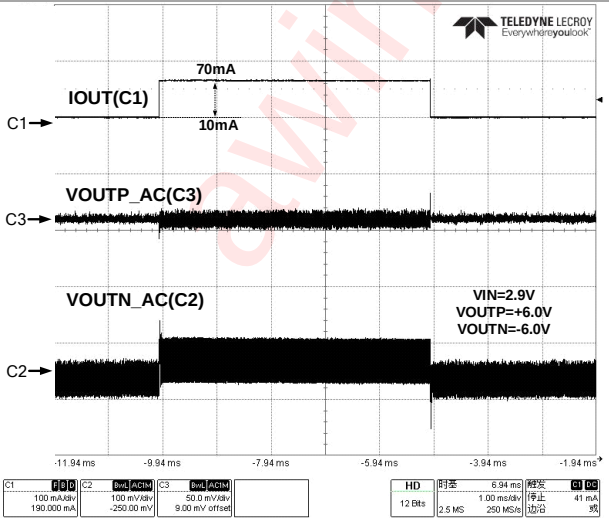


Figure 51 Load Transient（80mA Mode）

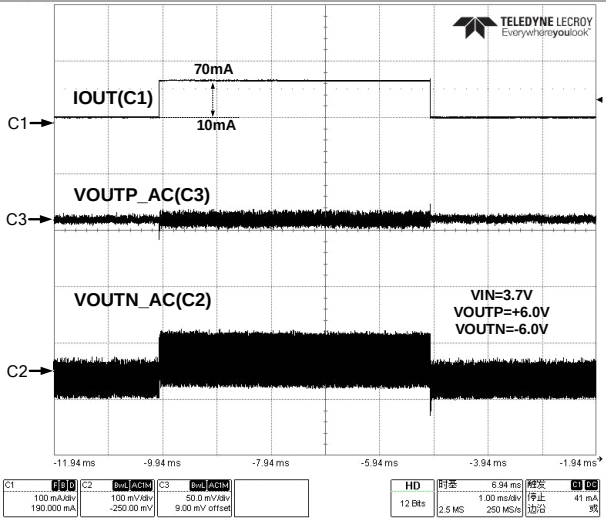


Figure 52 Load Transient（80mA Mode）

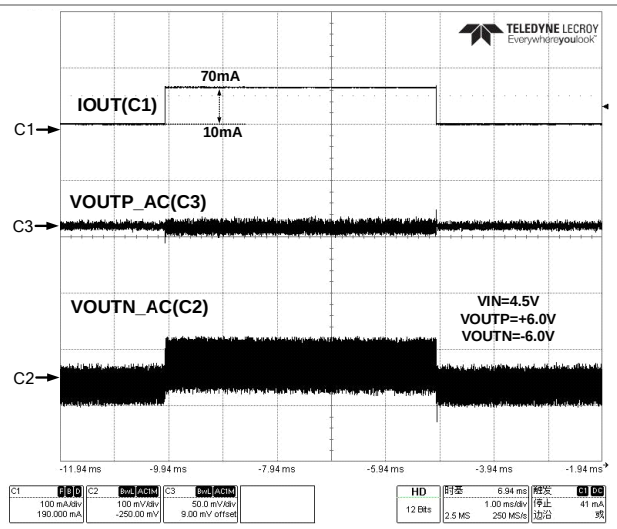


Figure 53 Load Transient（80mA Mode）

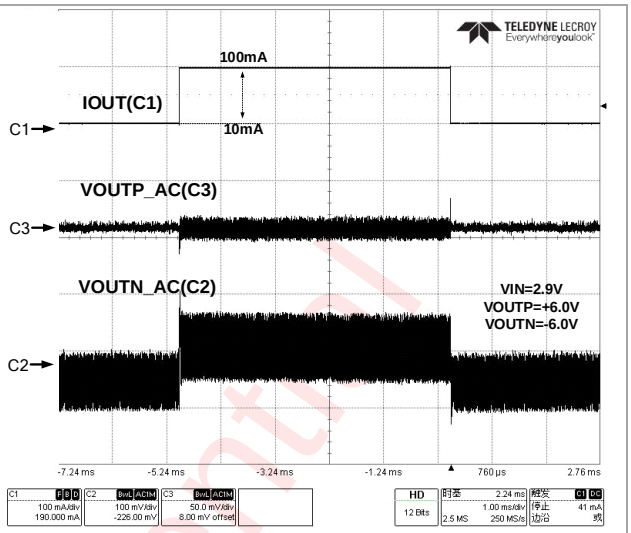


Figure 54 Load Transient（100mA Mode）

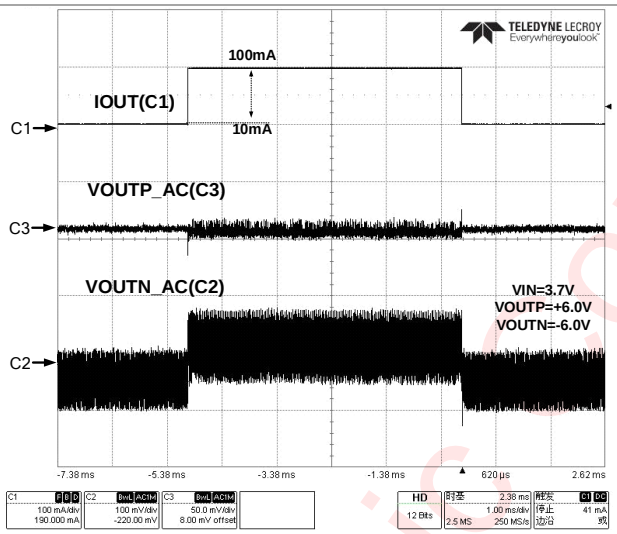


Figure 55 Load Transient（100mA Mode）

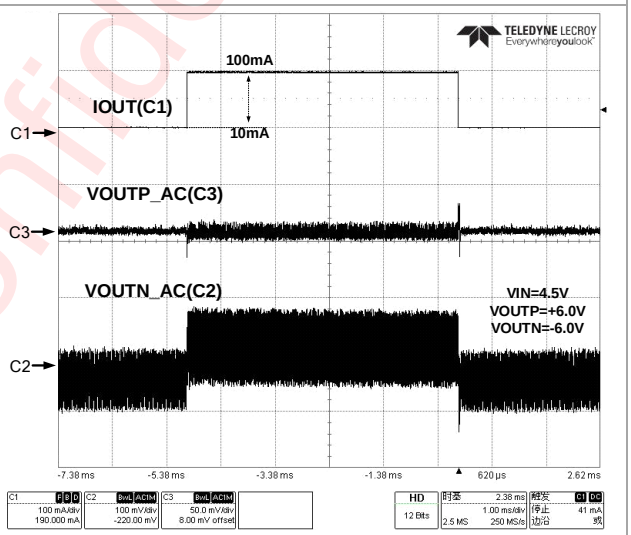


Figure 56 Load Transient(100mA Mode)

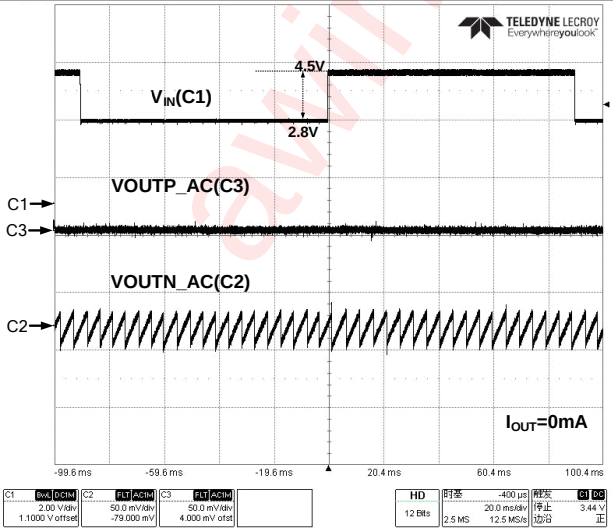


Figure 57 Line Transient (40mA Mode)

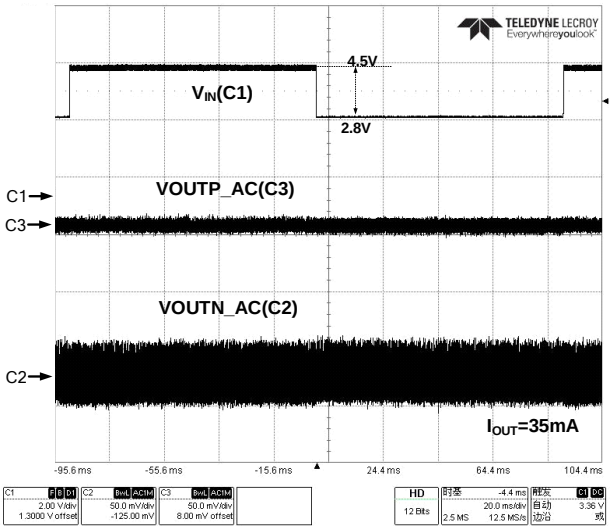


Figure 58 Line Transient (40mA Mode)

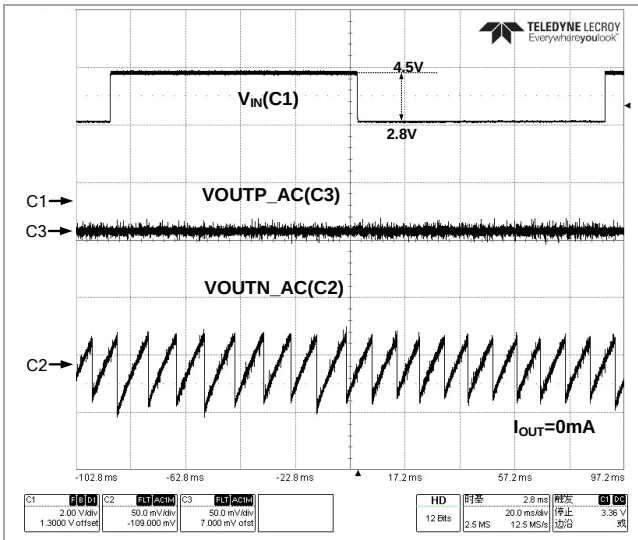


Figure 59 Line Transient (80mA Mode)

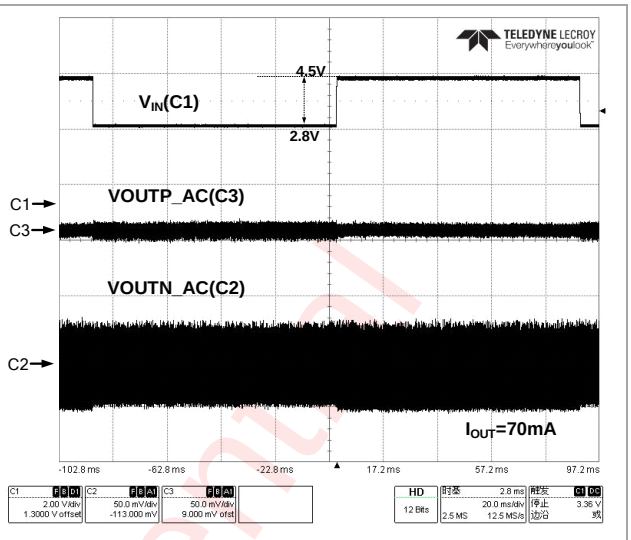


Figure 60 Line Transient (80mA Mode)

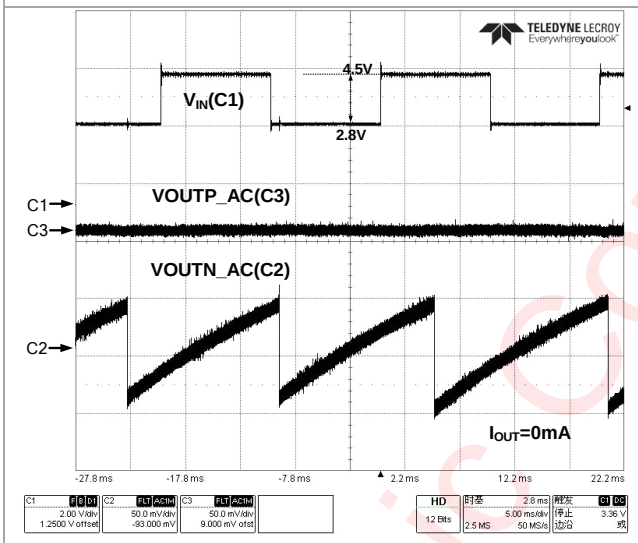


Figure 61 Line Transient (100mA Mode)

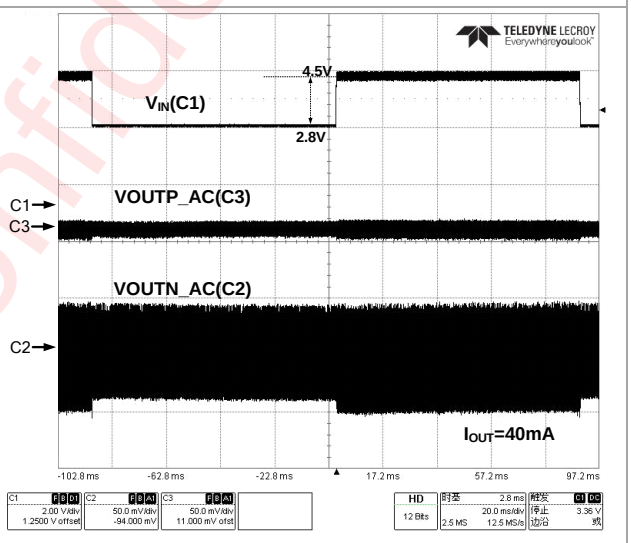


Figure 62 Line Transient (100mA Mode)

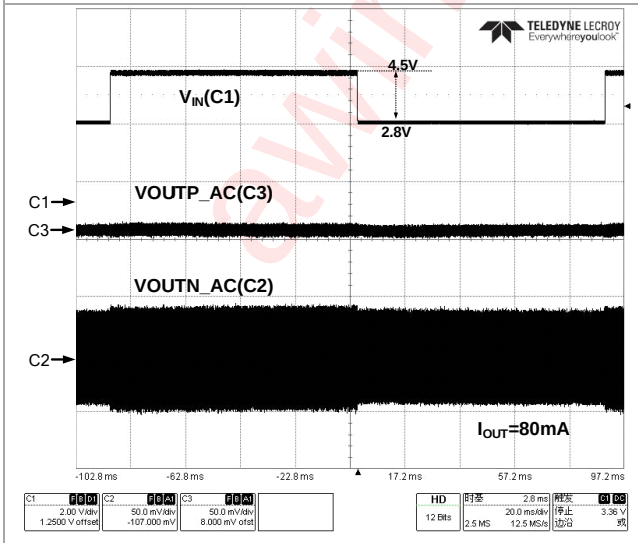


Figure 63 Line Transient (100mA Mode)

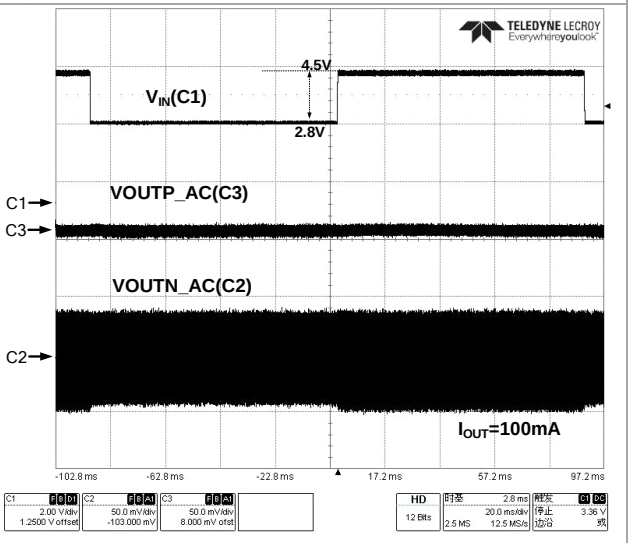


Figure 64 Line Transient (100mA Mode)

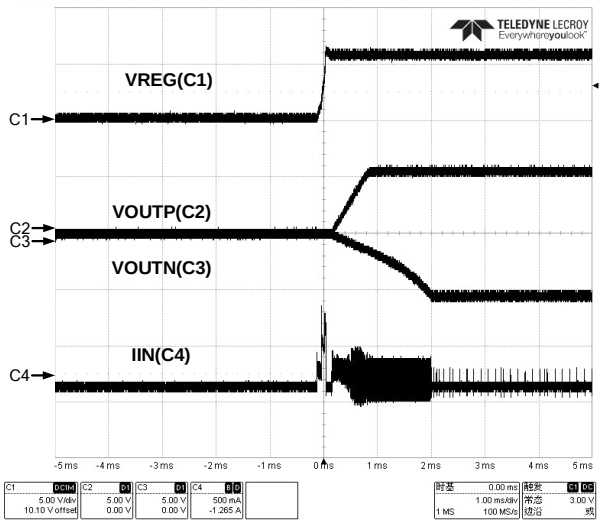


Figure 65 Inrush Current (Simultaneous)

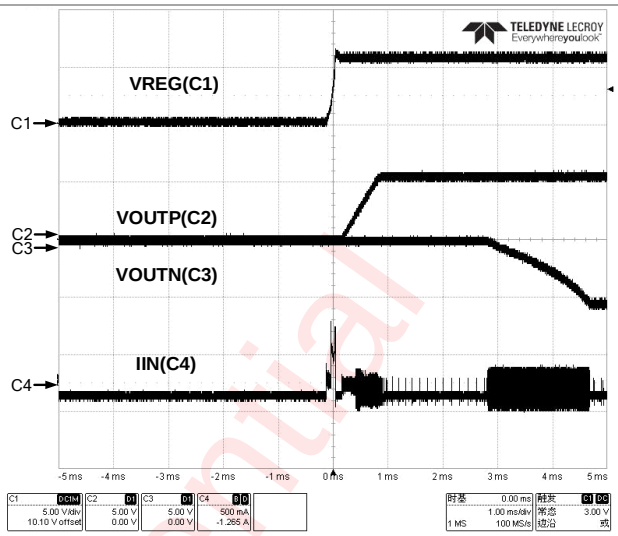


Figure 66 Inrush Current (Sequential)

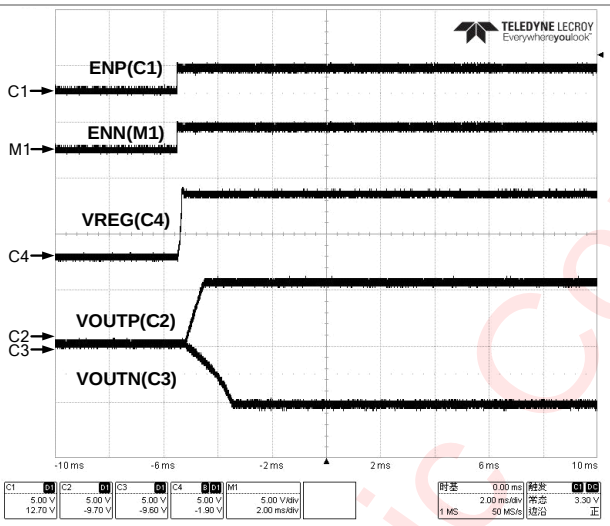


Figure 67 Power Up Sequencing (Simultaneous)

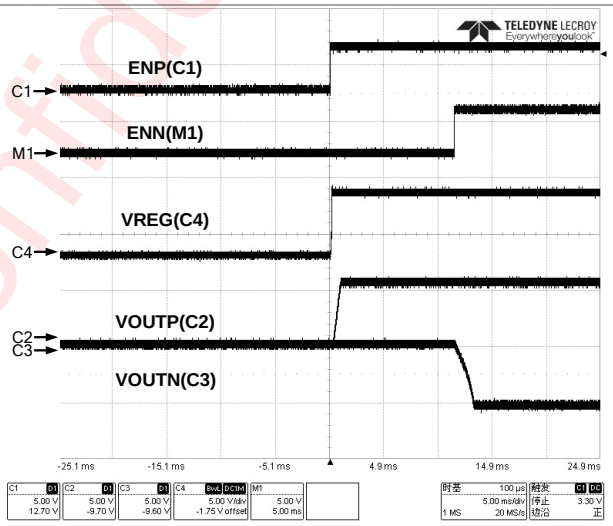


Figure 68 Power Up Sequencing (Sequential)

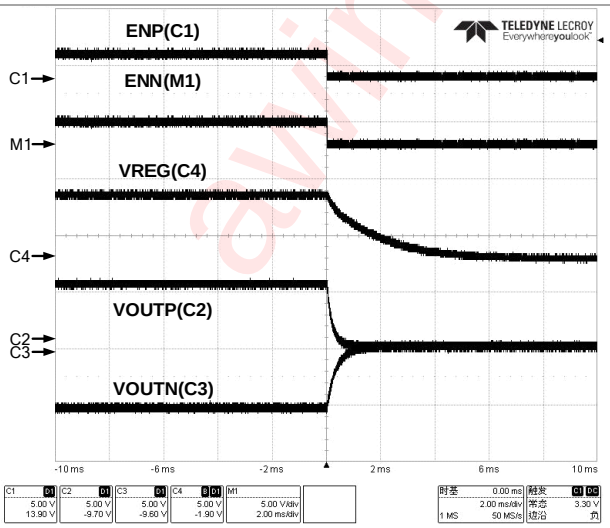


Figure 69 Power Down Sequencing (Simultaneous)

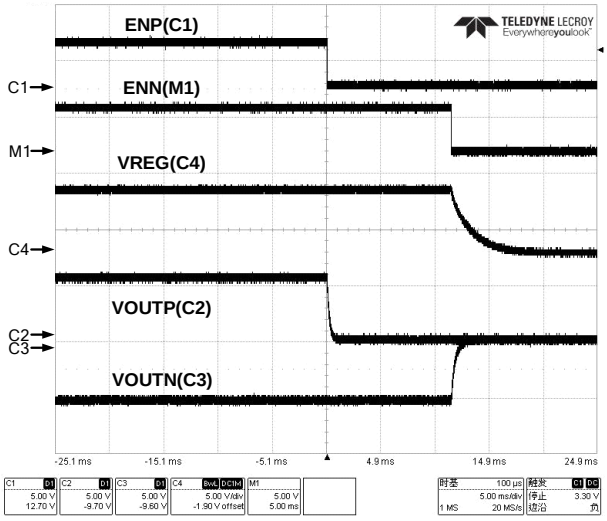


Figure 70 Power Down Sequencing (Sequential)

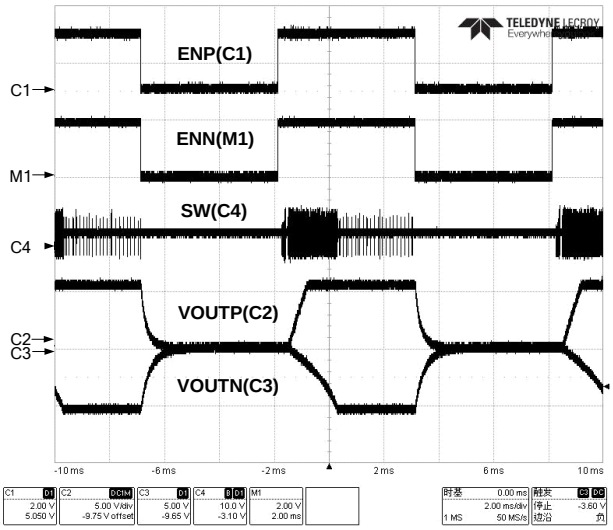


Figure 71 Power Up/Down With Active Discharge

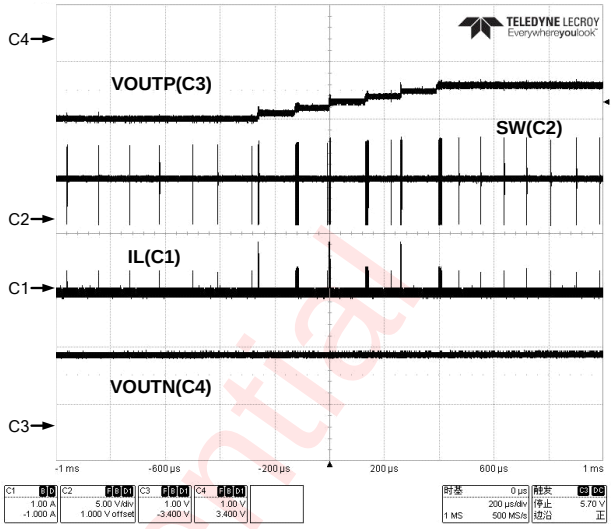


Figure 72 Ramp Up (V_{OUTP})

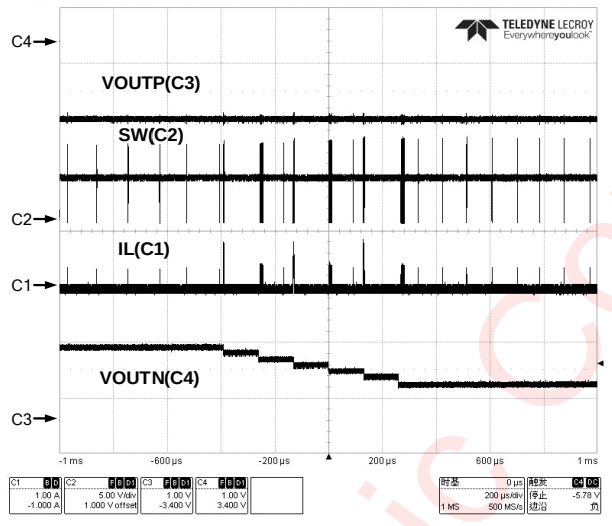


Figure 73 Ramp Up (V_{OUTN})

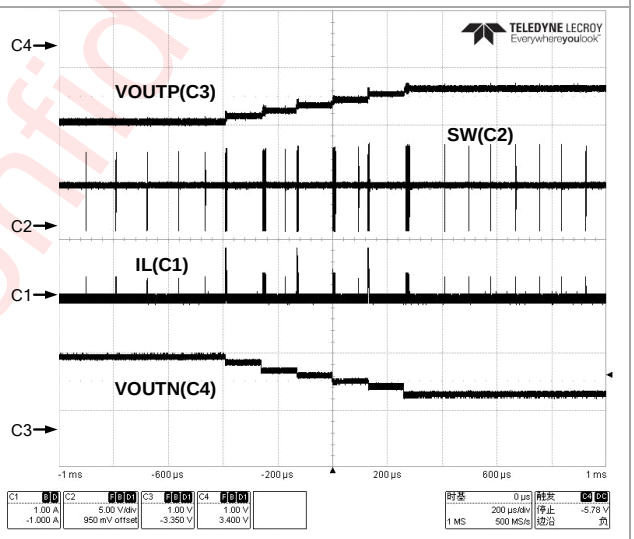


Figure 74 Ramp Up (V_{OUTP} And V_{OUTN})

Detailed Functional Description

AW37501 is designed to generate both positive and negative bias voltages for TFT-LCD panels or other general dual power supply applications. It consists a highly integrated synchronous boost converter with input voltage range from 2.7V to 5.5V. An internal LDO drops down the output voltage of the boost converter (V_{REG}), delivering the positive supply from +4.0V to +6.0V (100mV/step). A charge pump inverts and regulates the output voltage of the boost converter (V_{REG}), providing the negative supply from -4.0V to -6.0V (100mV/step). The operating mode can be selected among 40mA, 80mA and 100mA in order to achieve the necessary current capability and to get the best efficiency performance based on the application.

Enabling and Disabling the Device

ENP and ENN separately control positive output(V_{OUTP}) and negative output (V_{OUTN}) enable or disable. When V_{IN} is above the UVLO threshold, ENP or ENN goes to a logic-high, the boost converter will start up firstly and then the positive or negative voltage output. The boost converter is turned off when both ENP and ENN are low or V_{IN} falls below the UVLO stop threshold. Both ENP pin and ENN pin have an internal 200kΩ pull-down resistance to ground.

Power-Up and Soft-Start

When V_{IN} is above UVLO threshold and ENN or ENP is pulled to high voltage, the boost converter is enabled. To avoid drawing high inrush current from a battery or high impedance power source during startup, the boost converter employs an internal soft-start feature.

During boost's soft start, inductance current is limited in two ways. When V_{REG} < 1.2V, the low side power transistor of boost is turned on for fixed on time and switching period, and the inductance current is DCM state; when V_{REG} > 1.2V, boost works in the low valley current limiting state; when V_{REG} reaches the target voltage, the boost converter has reached its power good, which means that boost output is established, soft start is finished, and LDO and charge pump are allowed to work after 60μs delay.

The LDO starts operating as soon as the ENP signal is pulled HIGH, when the boost converter has reached its power good threshold. The LDO integrates a soft-start that slowly ramps up its output voltage V_{OUTP} regardless of the output capacitor and the target voltage, as long as the LDO current limit is not reached. the typical ramp-up time is 500μs.

The charge pump starts operating as soon as the ENN signal is pulled HIGH, when the boost converter has reached its power good threshold. The charge pump integrates a soft-start that slowly ramps up its output voltage V_{OUTN} regardless of the output capacitor and the target voltage, the charge pump current is limited and the limit current can be configured by REG03H[7:6].

The LDO and charge pump can be turn on via configuring REG03H[4:3] and REG21H, the REG21H is the written protect register of REG03H[4:3]. The detail function of REG03H[4:3] is descripted as below：

Power Control

REG03H[4]: ENN = Enable OUTN output.
REG03H[3]: ENP = Enable OUTP output.
Note: Turning ON either the OUTP or OUTN output will also turn-on the boost converter for the REG voltage.

Power-Down and Discharge

The BOOST, LDO and NCP stop operating when V_{IN} goes down below the UVLO threshold (usually 2.2V) or when both ENP and ENN are pulled low. The LDO stops operating when only ENP is pulled down while boost and NCP can still work, the same as NCP when ENN is pulled down. Both OUTP and OUTN can be actively discharged to GND by setting controlling bits DISP and DISN of REG03H with an approximately 60Ω and 20Ω discharging resistor respectively. If programmed to be active, when the enable signals go low or V_{IN} falls below UVLO, the discharge will occur during power down.

Programmable OUTP and OUTN Voltage

The OUTP positive output voltage is generated from the LDO supplied from a synchronous Boost converter, and OUTP is set at a default value of 5.4V. The boost converter also drives an inverting charge pump to generate OUTN negative output voltage which is set at a default value of -5.4V. The dual output voltages can be respectively programmed via a I^2C interface, and the available voltage ranges are from +4V to +6V for OUTP and from -4V to -6V for OUTN with 100mV per step.

BOOST Converter Output Voltage and Efficiency Improvement

The output voltage of boost is adjusted automatically based on the output voltages of LDO and charge pump. In order to achieve good efficiency and overall ripple effect, select the higher between V_{OUTP} and $|V_{OUTN}|$, and accumulate according to the current gear configuration. 200mV will be increased if 40mA or 80mA mode is configured; 300mV will be increased if 100mA mode is configured.

In 40mA or 80mA mode,

$$V_{REG} = \max (V_{OUTP}, |V_{OUTN}|) + 200\ mV$$

In 100mA mode,

$$V_{REG} = \max (V_{OUTP}, |V_{OUTN}|) + 300\ mV$$

In order to improve the efficiency, when boost works in DCM state, once the inductance current reaches 0A, it will enter the skip cycle mode and stop switching. When the output voltage is lower than the output regulation value, the switching will be restore again for realizing the constant voltage output. This mechanism can achieve the power saving effect under light load.

Under Voltage Lockout (UVLO)

To avoid the mistaken operation of the IC at low input voltage, an under voltage lockout is designed which shuts down the device at voltage lower than the typical UVLO threshold of 2.2V. A hysteresis of 200mV is added so that the device cannot be enabled again until the input voltage goes up to 2.4V. This hysteresis voltage avoids unusual shutdown due to broad line transients when the battery gets suddenly heavily loaded. The serial interface I^2C is still functional in the UVLO stop condition and the I^2C registers' contents is only reset under POR, which is lower than UVLO stop condition.

Overvoltage Protection

The output voltage of the boost converter (V_{REG}) is monitored with an overvoltage protection comparator, as soon as the OVP threshold of 7.3V is reached, the device stops switching. The device starts operation again once the output voltage falls 0.12V below the overvoltage threshold.

Over Current Protection

The AW37501 features a valley current limit sensing scheme to prevent from the BOOST is over loading. Current limit detection occurs during on-time of the synchronous rectifier cycle by cycle. When the inductor current is above the current limit within the whole switching cycle time, the off-time is increased to allow the inductor current to decrease to its threshold before the next on-time begins. When the current limit is reached, the output voltage V_{REG} will decreases if the load further increases. If V_{REG} is approximately below 1.2V during unexpected short circuit event, the boost converter works in discontinuous conduction mode to decrease the current from the battery. Once the short circuit event is released, the boost restarts.

The device also has an internal current limit circuit to help protect the LDO. During transient high-load current events, the OUTP sources a limited current of 370mA or 270mA, which is largely independent of the voltage at OUTP and can be configured via REG04H[4]. But if the output voltage of OUTP drops to 60% of the target value and over loading continues 32ms, this chip will shut down.

OUTN Output Current Limit

The OUTN built-in output current limit prevents the charge pump from over loading and OUTN short condition. The current limit threshold is decided by current mode set by REG03H[7:6].

Current mode	Current limit threshold
40mA mode	>40mA
80mA mode	>80mA
100mA mode	>100mA

Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. When the junction temperature exceeds 140℃, IC shuts down. When the junction temperature falls below the thermal recovery temperature, approximately 120℃, the device restarts by using the soft-start sequence.

General I²C Operation

The device supports the I²C serial bus and data transmission protocol. It operates as a slave on the I²C bus. The maximum clock frequency specified by the I²C standard is 400kHz. Connect to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ when I²C frequency is 400kHz. Different high level from 1.2V to 5V of this I²C interface is supported.

Device Address

AW37501 7-bit slave address (A7~A1) is 0111110 binary(0x3EH). After the START condition, the I²C master sends the 7-bit chip address followed by an eighth (A0) read or write bit (R/W). R/W= 0 indicates a WRITE function and R/W = 1 indicates a READ function.

Table 5. Device Address

A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	1	1	0	R/W

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

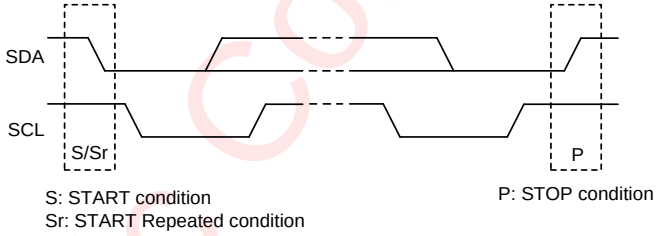


Figure 75 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

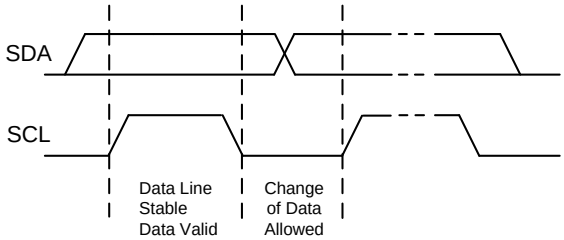


Figure 76 Data Validation Diagram

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

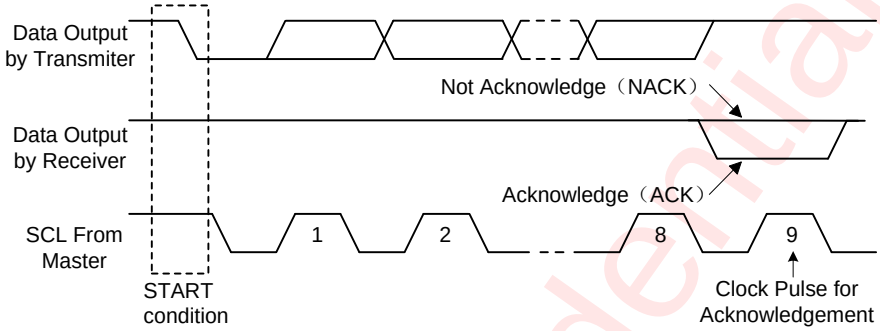


Figure 77 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal
h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g)
i) Master generates STOP condition to indicate write cycle end

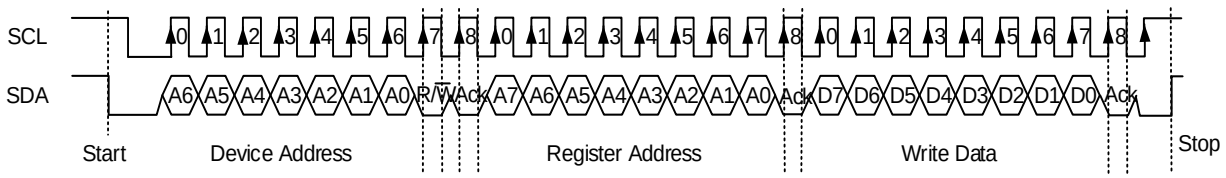


Figure 78 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

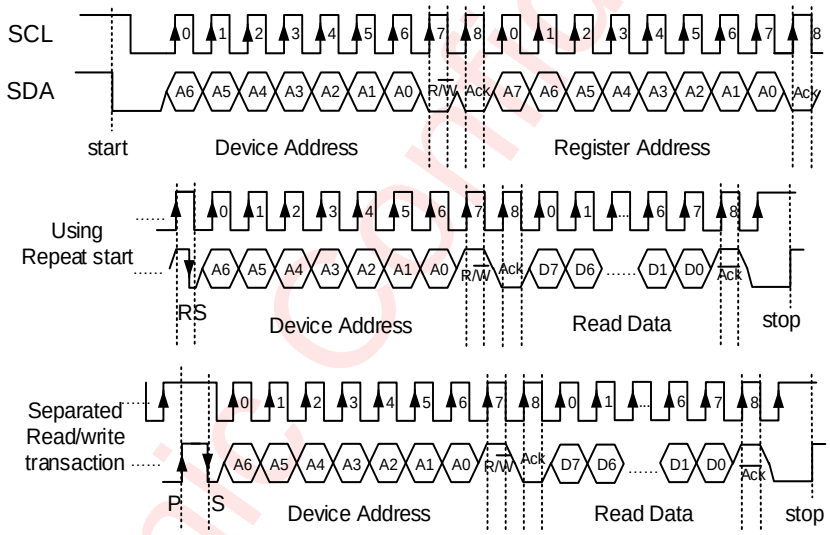


Figure 79 I²C Read Byte Cycle

Register Configuration

Register MAP

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	**VOUTP**	R/W	RSVD[2:0]			VOUTP[4:0]					0x0E
0x01	**VOUTN**	R/W	RSVD[2:0]			VOUTN[4:0]					0x0E
0x03	**APPS**	R/W	APPS[1:0]		RESET	ENN	ENP	RSVD	DISP	DISN	0x43
0x04	**CTRL**	R/W	RSVD[2:0]			ILMTLDO	RSVD		VENDOR[1:0]		0x01
0x21	**WPRTEN**	R/W	Written protect functional Register								0x00

R/W = Read/Write.

Register Detailed Description

VOUTP：VOUTP Configure Register(Address 00H)

Bit	Symbol	R/W	Description				Default
7:5	RSVD[2:0]	R	Reserved.				0x0E
4:0	VOUTP[4:0]	RW	Output voltage of LDO				
			VOUTP[4:0]	VOUTP(V)	VOUTP[4:0]	VOUTP(V)	
			00000	4.0	01011	5.1	
			00001	4.1	01100	5.2	
			00010	4.2	01101	5.3	
			00011	4.3	01110	**5.4(default)**	
			00100	4.4	01111	5.5	
			00101	4.5	10000	5.6	
			00110	4.6	10001	5.7	
			00111	4.7	10010	5.8	
			01000	4.8	10011	5.9	
			01001	4.9	10100	6.0	
			01010	5.0			

VOUTN：VOUTN Configure Register(Address 01H)

Bit	Symbol	R/W	Description				Default
7:5	RSVD[2:0]	R	Reserved.				0x0E
4:0	VOUTN[4:0]	RW	Output voltage of charge pump				
			VOUTN[4:0]	VOUTN(V)	VOUTN[4:0]	VOUTN(V)	
			00000	-4.0	01011	-5.1	
			00001	-4.1	01100	-5.2	
			00010	-4.2	01101	-5.3	
			00011	-4.3	01110	**-5.4(default)**	
			00100	-4.4	01111	-5.5	
			00101	-4.5	10000	-5.6	
			00110	-4.6	10001	-5.7	
			00111	-4.7	10010	-5.8	
			01000	-4.8	10011	-5.9	
			01001	-4.9	10100	-6.0	
			01010	-5.0			

APPS：Applications Configure Register(Address 03H)

Bit	Symbol	R/W	Description	Default
7 6	APPS[1:0]	R/W	Current mode application. 00: 40mA mode; **01: 80mA mode(default)**. 10: 100mA mode; 11: 100mA mode.	0x43
5	RESET	R/W	Soft reset bit. 0: keep; Write 1: reset.	
4	ENN	R/W	Enable charge pump output. It must be written after writing the register 0x21H=4CH; **0: disable (default)**; 1: enable.	
3	ENP	R/W	Enable LDO output. It must be written after writing the register 0x21H=4CH; **0: disable (default)**; 1: enable.	
2	RSVD	R/W	Reserved.	
1	DISP	R/W	LDO actively discharge enable. 0:disable; **1:enable (default)**.	
0	DISN	R/W	Charge pump actively discharge enable. 0:disable; **1:enable (default)**.	

CTRL：Control State Configure Register(Address 04H)

Bit	Symbol	R/W	Description	Default
7:5	RSVD[2:0]	R	Reserved.	0x01
4	ILMTLDO	R/W	LDO output current limit value configure: **0: 370mA(default)**; 1: 270mA.	
3:2	RSVD[1:0]	R	Reserved.	
1:0	VENDOR[1:0]	R	Vendor ID, read only. **01: AWINIC Vendor Number(default)**. 00,10,11: others.	

WPRTEN：Written Protect Functional Register(Address 21H)

Bit	Symbol	R/W	Description	Default
7:0	WPRTEN	W/R	Write protect functional register of APPS[4:2]: Write 4CH open written protect function, and read, return 01H; Write other codes to disable writing register of APPS[4:2], and return 00H when read;	0x00

Application Information

The AW37501 employs a single inductor scheme to support positive /negative supply at current up to 100mA. Below are some peripheral selection guidelines.

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirement. A simple approach is to estimate the converter efficiency, by taking the efficiency number from the provided efficiency curves at the application's maximum load or to use a worst case assumption for the expected efficiency.

1. Duty cycle:

$$D = 1 - \frac{V_{IN\_min} \times \eta}{V_{REG}} \quad (1)$$

2. Inductor ripple current:

$$\Delta I_L = \frac{V_{IN\_min} \times D}{f_{SW} \times L} \quad (2)$$

3. Maximum output current:

$$I_{OUT\_max} = \left(I_{LIM\_min} + \frac{\Delta I_L}{2}\right)(1-D) \quad (3)$$

4. Peak switch current of the application:

$$I_{SWPEAK} = \frac{I_{OUT}}{1-D} + \frac{\Delta I_L}{2} \quad (4)$$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 85% as an estimation)

f_{SW} = Boost converter switching frequency

L = Selected inductor value for the boost converter

I_{SWPEAK} = Boost converter switch current at the desired output current (must be < [I_{LIM_min} + ΔI_L])

ΔI_L = Inductor peak-to-peak ripple current

V_{REG} = max (V_{OUTP}, V_{OUTN}) + 200mV (in 40mA mode or 80 mA mode) or + 300mV (in 100mA mode)

I_{OUT} = I_{OUT_VOUTP} + |I_{OUT_VOUTN}|, (I_{OUT_max} being the maximum current delivered on each rail)

The peak switch current is the current that the integrated switch and the inductor have to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

The AW37501 integrates a charge pump to support negative supply. The charge pump uses only two external capacitors C4 and C5 as shown in the Figure 1. The output characteristics of this charge pump can be approximated by an ideal voltage source in series with a resistor. The voltage source equals -V_{REG}. The output resistance R_{out} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C4 and C5. A good approximation is:

$$R_{OUT} = 2 \times R_{SW} + \frac{1}{F_{OSC} \times C_4} + 4ESR_{C4} + ESR_{C5} \quad (5)$$

Where R_{SW} is the ON resistance of the internal MOS switches. High value, low ESR capacitors reduce the output resistance. The littler of the distance from C_4 to CFLY1/2 in the PCB layout can also reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the $2/(F_{OSC}*C_4)$ term. Once this term is trivial compared with R_{SW} and ESRs, further increase to oscillator frequency and capacitance become ineffective. Furthermore larger oscillator frequency can increase quiescent current. The peak to peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C5:

$$V_{ripple} = \frac{I_{OUTN}}{F_{OSC} \times C_5} + 2 \times I_{OUTN} \times ESR_{C5} \quad (6)$$

Again, using a low ESR capacitor results in lower ripple.

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop from V_{RGE} to $-V_{OUTN}$ is the load current times the output resistance, and the charge pump efficiency is shown by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{(I_{OUTN})^2 R_L}{(I_{OUTN})^2 R_L + (I_{OUTN})^2 R_{OUT} + I_{Q(NCP)}} \quad (7)$$

where

$I_{Q(NCP)}$ is the quiescent power loss of the charge pump

$(I_{OUTN})^2 R_{OUT}$ is the conversion loss associated with the switch on resistance, the two external capacitors and their ESRs.

Inductor Selection

Saturation current: the inductor must handle the maximum peak current {$I_{L\_SAT} > I_{SWPEAK}$, or $I_{L\_SAT} > [I_{LIM\_min} + \Delta I_L]$ as conservation approach}.

DC Resistance: the lower the DCR, the lower the losses. Inductor value: in order to keep the ratio $I_{OUT}/\Delta I_L$ low enough for proper sensing operation purpose, it is recommended to use a 4.7μH inductor for 40mA mode (a 2.2μH might however be used, but the efficiency might be lower than with 4.7μH at light loads depending on the inductor characteristics).

L(μH)	Supplier	Component Code	ELA Size	I_{SAT}(A)	DCR TYP(mΩ)
2.2	Toko	1269AS-H-2R2N=P2	1008	2.4	130
2.2	Chilisin	MHCD252012A-2R2M-A8S	2520	2	102
4.7	Toko	1269AS-H-4R7N=P2	1008	1.6	250
4.7	Sunlord	WPN252010HS4R7MT	2520	1.3	276

Capacitor Selection

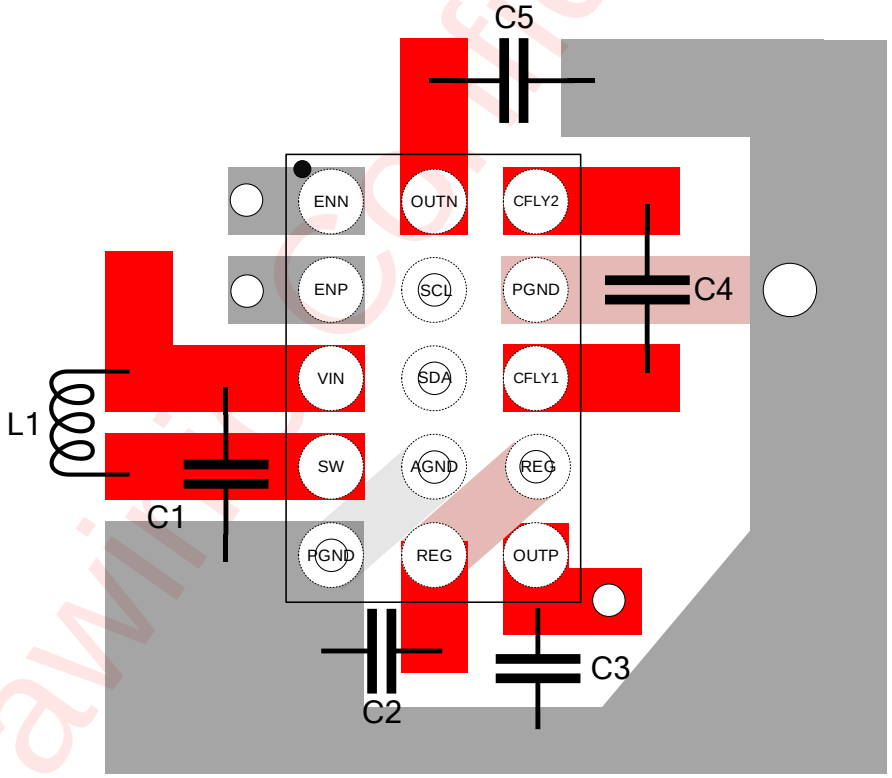
For best input voltage filtering low ESR ceramic capacitors are recommended for input capacitors. The AW37501 has an analog input pin VIN. A 4.7μF minimum bypass capacitor is required as closed as possible from VIN to GND. For better input voltage filtering, this value can be increased or two capacitors can be used. For output capacitors, higher capacitors values can be used to improve the load transient response and reduce output voltage ripple. For the best output voltage filtering, low ESR ceramic capacitors are recommended. A minimum of 4.7μF ceramic output capacitors is required. The NCP needs an external flying capacitor. The minimum value is 2.2μF. For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on REG pin.

Capacitor(μF)	Supplier	Component Code	ELA Size	Voltage Rating(V)	Comments
2.2	Murata	GRM188R61C225KAAD	0603	16	C_{FLY}
4.7	Murata	GRM188R61C475KAAJ	0603	16	C_{IN}, C_{OUTN}, C_{FLY}, C_{OUTP}, C_{REG}
10	Murata	GRM219R61C106KA73	0603	16	C_{OUTN}, C_{OUTP}, C_{REG}

PCB Layout Consideration

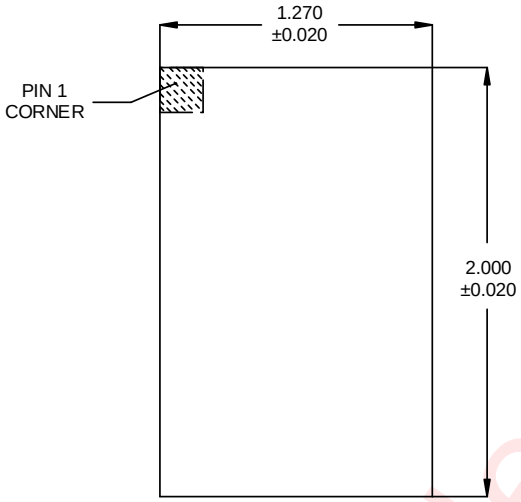
AW37501 is a single inductor and dual outputs power supple, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All peripheral components should be placed as close to the chip as possible. C1、C2、C3、C4、C5 and L1 should be close to VIN、REG、OUTP、CFLY1/2 and OUTN pins respectively. Avoid to connect device and chip pins with two different layers of copper, use the same layer of copper instead.
2. VIN and SW are the large current input of the chip, please routed according to 2.5A rule, and the advised width is 100mil.
3. The connection lines between the planes of C1、C2、C3、C4、C5 and respective chip pins should be as short and wide as possible, to reduce noise and ripple.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient via below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.
5. To achieve optimal large-current performance, the power path shown in red as the figure below must be widen.

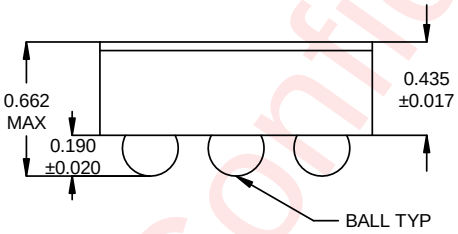


Via to signal layer on internal or bottom layer.

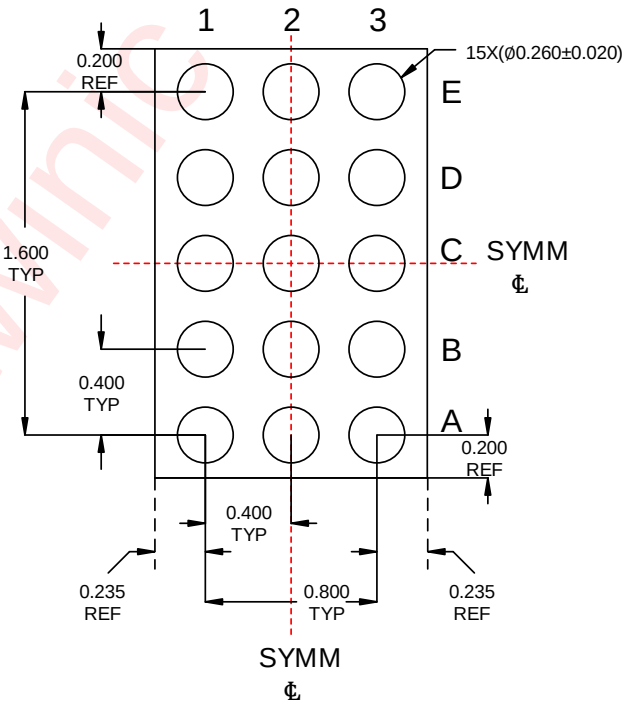
Package Description



Top View



Side View

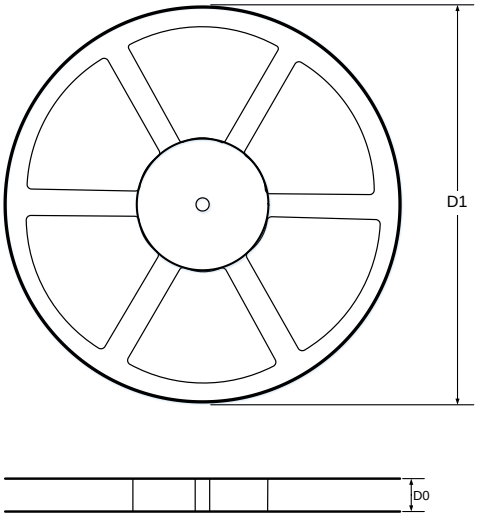


Bottom View

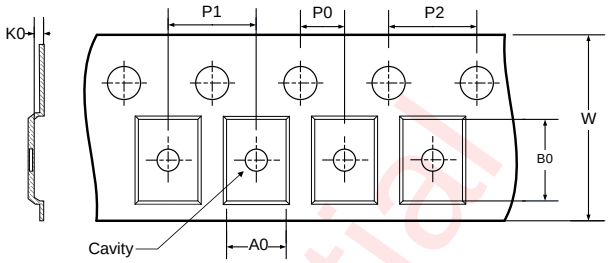
Unit: mm

Tape And Reel Information

REEL DIMENSIONS

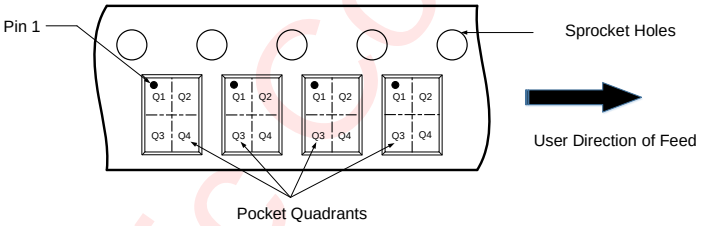


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

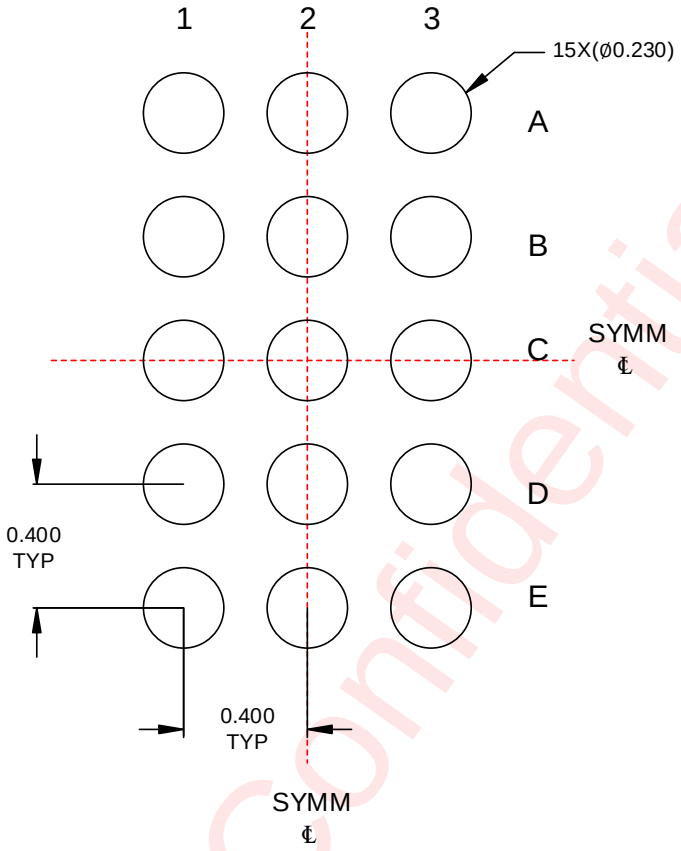
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

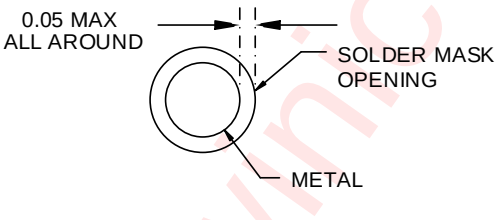


All Dimensions are nominal

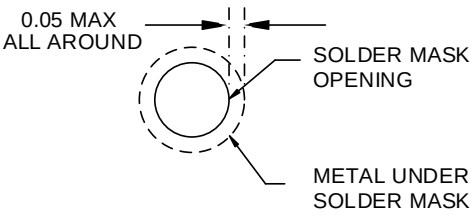
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.40	2.10	0.76	2.00	4.00	4.00	8.00	Q1

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

UNIT: mm

Revision History

Version	Date	Change Record
V1.0	Sep. 2020	Official released
V1.1	Apr. 2021	1. Changed V_{OUTP} and V_{OUTN} default output condition: amend I_{OUT}=40mA to I_{OUT}=80mA (Page 6) 2. Added V_{OUTP} line variation and V_{OUTN} line variation to Electrical Characteristics table (Page 6 and Page 7) 3. Modified the line regulation of V_{OUTP} and V_{OUTN} (Page 6 and Page 7) 4. Revised figure 71 (Page 20) 5. Fixed some formatting and syntax errors
V1.2	Jun. 2021	1. Add the range of parameters in Electrical Characteristics (Page 6 and Page 7) 2. Add Application Information (Page 29 and Page 30)
V1.3	Oct. 2021	1. Changed the input voltage rang “2.7V to 5.0V” to “2.7V to 5.5V” 2. Added V_{IH}, V_{IL} and V_{OL} parameters of SDA and SCL ports in EC table 3. Deleted the ENSTB description in register 0x03[2], and change it to RSVD 4. Fixed the molecular numerical error for the second item of formula (5).

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

