3-Channel LED Drivers with Auto Charging Indicator

FEATURES

- 3-channel constant current LED drivers
  - 4-level IMAX selections: 5/10/15/30mA
  - 16-level current setting for each LED，4096 mixed-color available
  - 256-level exponential PWM dimming
- Automatic breathing light
  - Three independent pattern controllers
  - Individual and sync control selectable
- Support charging indication under low battery voltage condition
  - Directly start up blinking on LED1 via pulling pin CHRG up to high
  - Blink period 2s, max output current 6mA
- LED current accuracy: ±3%
- LED matching accuracy: ±3%
- Low dropout voltage: 50mV
- 400kHz I²C interface (address: 0x64)
- Shutdown control by pulling down pin SCL
- UVLO and OTP protection
- Single power supply, 2.5V~5.5V
- 1.5mm×1.5mm×0.45mm DFN-8L package

GENERAL DESCRIPTION

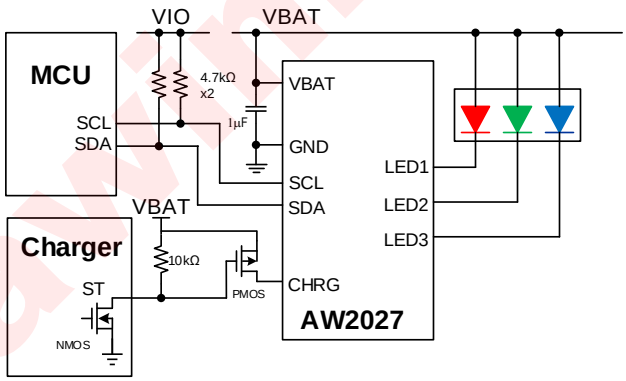
AW2027 is a three-channel constant current LED driver with auto charging indication function. The maximum output current is 4-level selectable (5mA/ 10mA/15mA/30mA). The driving current of each LED has 16 levels configurable so as to achieve 4096 color mixing. The 256-level exponential PWM creates fine and smooth dimming effect even in low brightness.

AW2027 can provide auto charging indication under the condition of low battery voltage. When the voltage of battery is too low, and the I²C interface halts, the internal pattern controller will be activated by pulling pin CHRG to high, and pin LED1 will output blinking lighting with period of 2s and max 6mA current.

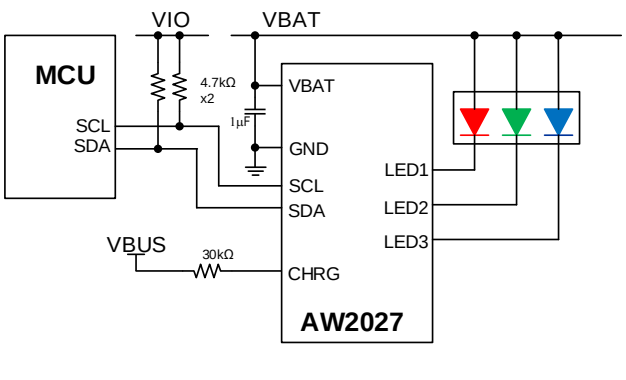
AW2027 contains three independent pattern controllers. Three LEDs can be controlled to work synchronously or individually according to different applications.

AW2027 is available in a 1.5mm×1.5mm×0.45mm DFN-8L package.

TYPICAL APPLICATION CIRCUIT



Charging Status Indication Application



Adapter Plug-in Indication Application

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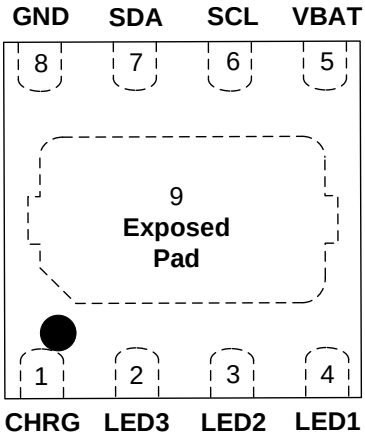
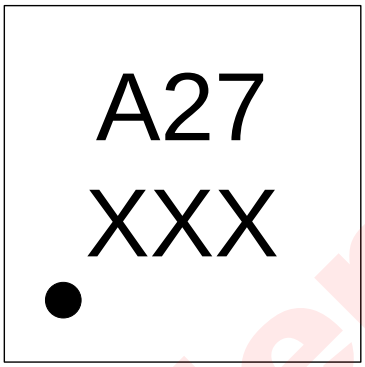
PIN CONFIGURATION AND TOP MARK

AW2027 TOP VIEW



AW2027 MARKING

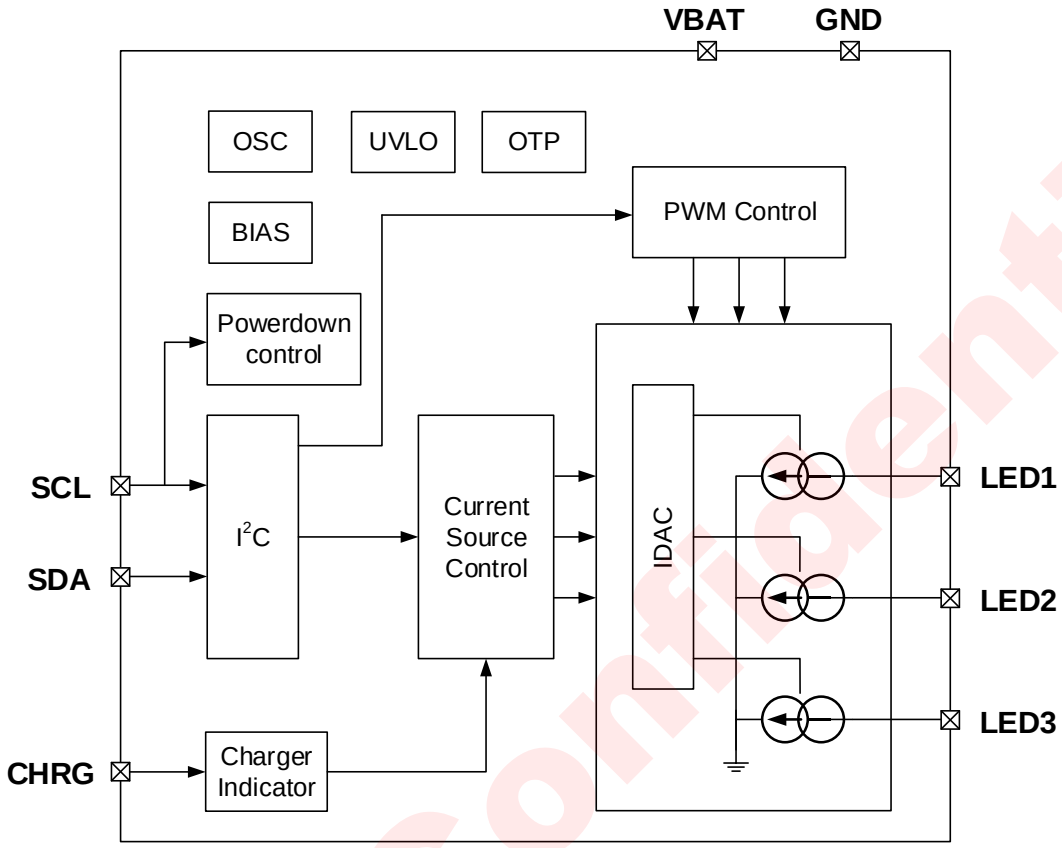


A27 ---- AW2027
XXX ---- Manufacture date code

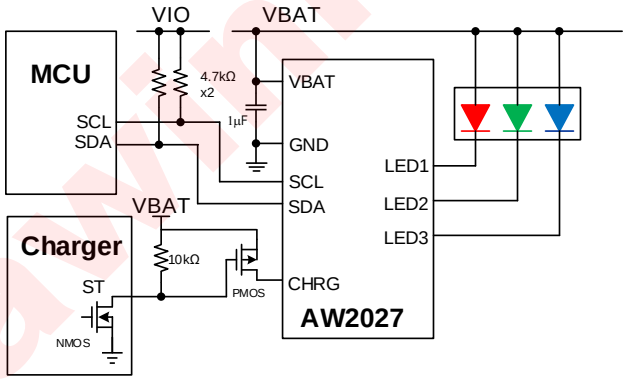
PIN DEFINITION

No.	NAME	DESCRIPTION
1	CHRG	Charge indicator input, active high.
2	LED3	LED3 cathode driver, anode connected to VBAT
3	LED2	LED2 cathode driver, anode connected to VBAT
4	LED1	LED1 cathode driver, anode connected to VBAT
5	VBAT	Power supply (2.5V~ 5.5V)
6	SCL	Serial clock Input for I^2C Interface
7	SDA	Serial data I/O for I^2C Interface
8	GND	Ground
9	Exposed Pad	Exposed Pad must be soldered to the PCB board and connected to GND.

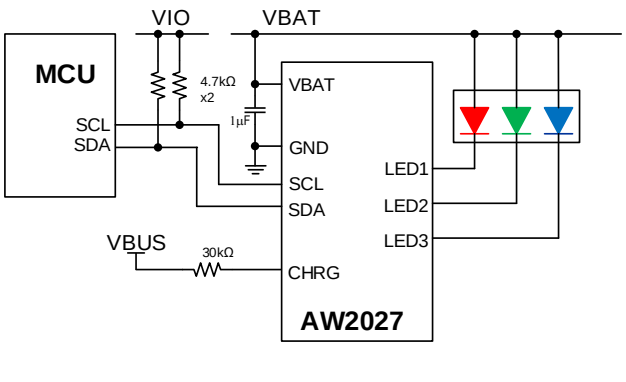
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUITS



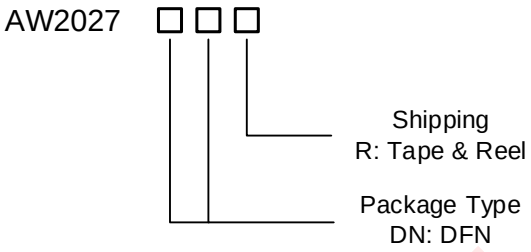
Charging Status Indication Application



Adapter Plug-in Indication Application

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW2027DNR	-40℃～85℃	1.5mm×1.5mm×0.45mm DFN-8L	A27 XXX	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

PARAMETERS		RANGE
Supply voltage range V_{BAT}		-0.3V to 6.0V
Input voltage range	SCL, SDA,	-0.3V to 6.0V
	CHRG	-0.3V to 6.0V
	LED1~LED3	-0.3V to 6.0V
Output voltage range	SDA	-0.3V to 6.0V
Junction-to-ambient thermal resistance θ_{JA}		121.6℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-55℃ to 125℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 2)		
HBM		±2000V
MM		±200V
CDM		±2000V
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		350mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

ELECTRICAL CHARACTERISTICS

V_{BAT}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
Power Supply						
V_{BAT}	Input operation voltage		2.5		5.5	V
$I_{SHUTDOWN}$	Current in shutdown mode	SCL/ SDA =0V (over 130ms)			2	μA
$I_{STANDBY}$	Current in standby mode	SCL/SDA=1.8V			10	μA
I_{ACTIVE}	Quiescent current in active mode	register CHIPEN=1 all LEDs off			100	μA
V_{POR}	Power-on-reset voltage			1.25		V
V_{UVLO}	UVLO threshold	GCR2.UVTH[1:0]=00		2		V
T_{OTP}	Over temperature threshold			140		℃
T_{HYS}	Over temperature hysteresis			20		℃
F_{OSC}	Oscillator frequency		-5%	1.024	+5%	MHz
LED Driver						
I_{ACC}	Current accuracy	I_{LED}=15mA	-3%		+3%	%
I_{MATCH}	Matching accuracy	I_{LED}=15mA	-3%		+3%	%
V_{DROP}	Dropout voltage	I_{LED}=15mA		50	100	mV
F_{PWM}	PWM frequency	LCTR.FREQ=0	-5%	250	+5%	Hz
Digital Logical Interface						
V_{IL}	Logic input low level	SDA,SCL			0.4	V
		CHRG			0.4	
V_{IH}	Logic input high level	SDA,SCL	1.3			V
		CHRG	V_{BAT} -0.2			
I_{IL}	Low level input current	SDA,SCL		5		nA

I_{IH}	High level input current	SDA,SCL		5		nA
V_{OL}	Logic output low level	SDA, I_{OUT}=3mA			0.4	V
I_L	Output leakage current	SDA open drain			1	nA

I²C INTERFACE TIMING

Parameter Name			Min	Typ.	Max	Units
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

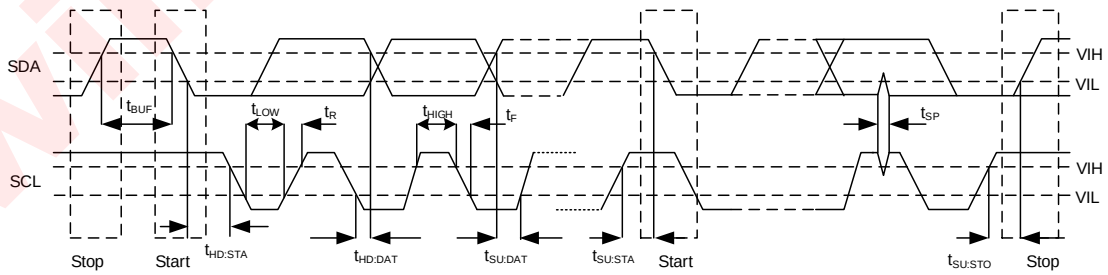


Figure 1 Timing of I²C Interface Signals

FUNCTIONAL DESCRIPTION

POWER ON RESET

When the supply voltage on pin VBAT drops below the predefined voltage V_{POR} (1.25V), the device enters shutdown mode, and generate a reset signal to perform a power-on reset operation, which will reset all control circuits and configuration registers.

The status bit STATUS.PUIS (register: 0x02 bit4) will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of STATUS register. Usually the STATUS.PUIS bit can be used to check whether an unexpected power-on event has taken place.

OPERATING MODE

In AW2027, pin SCL provides power down control. There are three work modes available: Shutdown, Standby and Active mode.

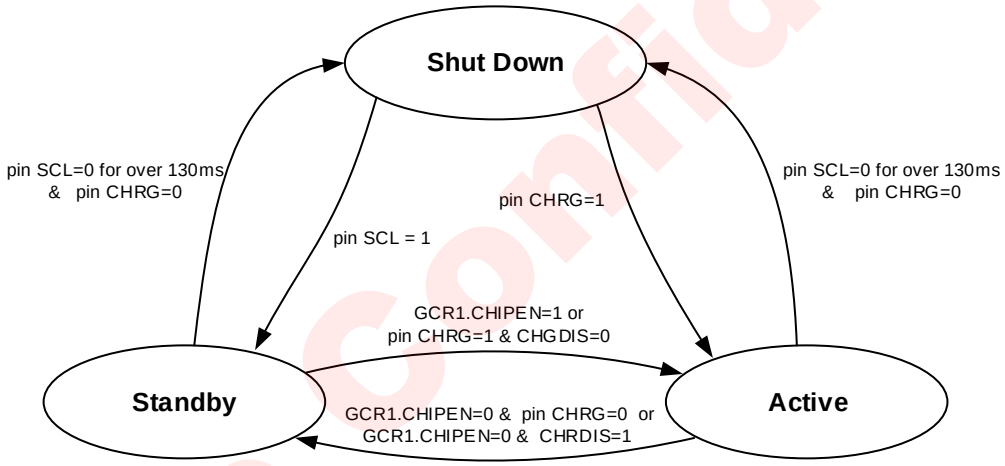


Figure 2 AW2027 operating modes transition

SHUTDOWN MODE

AW2027 enters into the shutdown mode when CHRG is low and SCL level is pulled low for over 130ms.

In shutdown mode, AW2027 will reset all internal circuits and configuration registers, all internal blocks are switched off except the power-on-reset circuit and the SCL level detect circuit, and the current consumption is very low (< 2μA).

STANDBY MODE

AW2027 enters into standby mode when SCL level is pulled high from shutdown mode or when pin CHRG is low and GCR1.CHIPEN become 0 in active mode.

In standby mode, only part of internal circuit work. The I^2C interface is accessible, but only registers RSTR and GCR1 can be written, the internal OSC keep closed and there is not internal clock. The current consumption is

less than 10μA.

ACTIVE MODE

When bit CHIPEN of GCR1 register is set to 1 in standby mode or CHRG is pulled high in shutdown mode, the device enters into active mode.

In active mode, the internal OSC works to provide clock signal. User can configure the device to produce the specified breath lighting effects in pattern mode or turn any LED on or off directly.

SOFTWARE RESET

Writing 0x55 to register RSTR (register: 0x00) via I²C interface will reset the device, including all functional circuits and configuration registers.

UNDER VOLTAGE LOCK OUT (UVLO)

The voltage on pin VBAT is monitored internally by the AW2027. When voltage of VBAT drops below predefined threshold by bit GCR2.UVTH (2.0v typically), the UVLOIS flag bit in STATUS register is set to “1”. After a read, the flag register can be cleared.

When UVLO condition is met, the bit CHIPEN in register GCR1 will be cleared, and the device return to standby state. If VBAT rises above the threshold and GCR1.CHIPEN bit is set to “1”, the device will enter into active mode again.

If the UVDIS bit in register GCR2 is set to “1”, the internal UVLO monitor is disabled. The default value of the UVDIS bit is “0”.

If the DUVP bit in register GCR2 is set to “1”, the UVLO protection function is closed, the device keeps working even though UVLO state is detected. The default value of the DUVP bit is “0”.

OVER TEMPERATURE PROTECTION

When the device reaches 140℃, the over-temperature protection be activated, and the OTPIS flag bit in register STATUS is set to “1”, and after a read, the flag register can be cleared.

When OTP condition is met, the bit CHIPEN in register GCR1 will be cleared, and the device will be forced to standby state. Once the temperature of the device drops below 120℃, and GCR1.CHIPEN bit is set to “1”, the device will enter into active mode again.

If the OTDIS bit in register GCR2 is set to “1”, the OTP function is disabled. The default value of the OTDIS bit is “0”.

If the DOTP bit in register GCR2 is set to “1”, the OTP protection function is closed, the device keeps working even though over-temperature condition is detected. The default value of the DOTP bit is “0”.

I²C INTERFACE

The AW2027 supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz, and operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. Different I²C interface

voltage of 1.8V ~ 3.3V are all supported.

DEVICE ADDRESS

The I²C device address (7-bit) of AW2027 is 0x64, followed by the R/W bit (Read=1/Write=0).

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

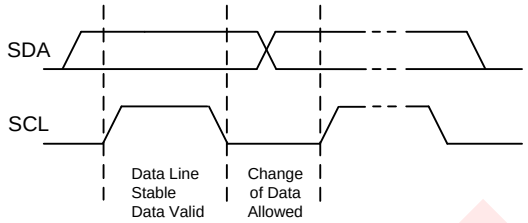


Figure 3 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

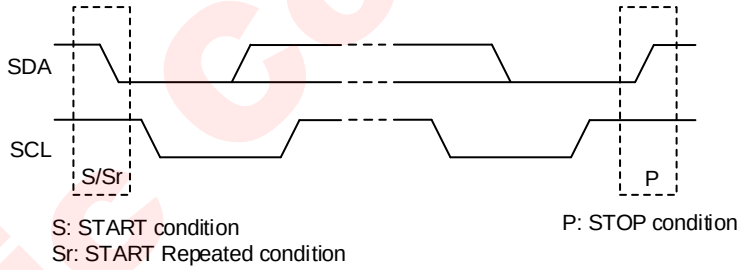


Figure 4 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

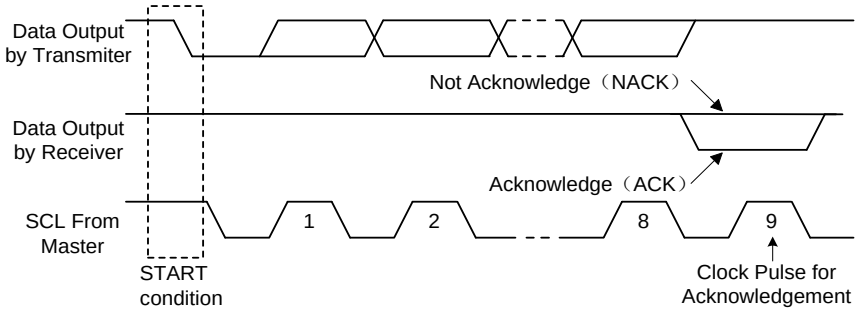


Figure 5 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f, g)

i) Master generates STOP condition to indicate write cycle end

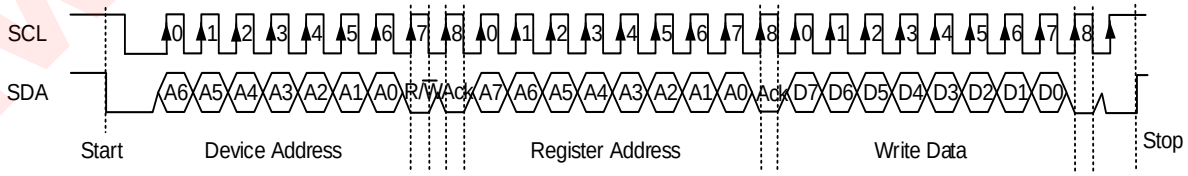


Figure 6 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

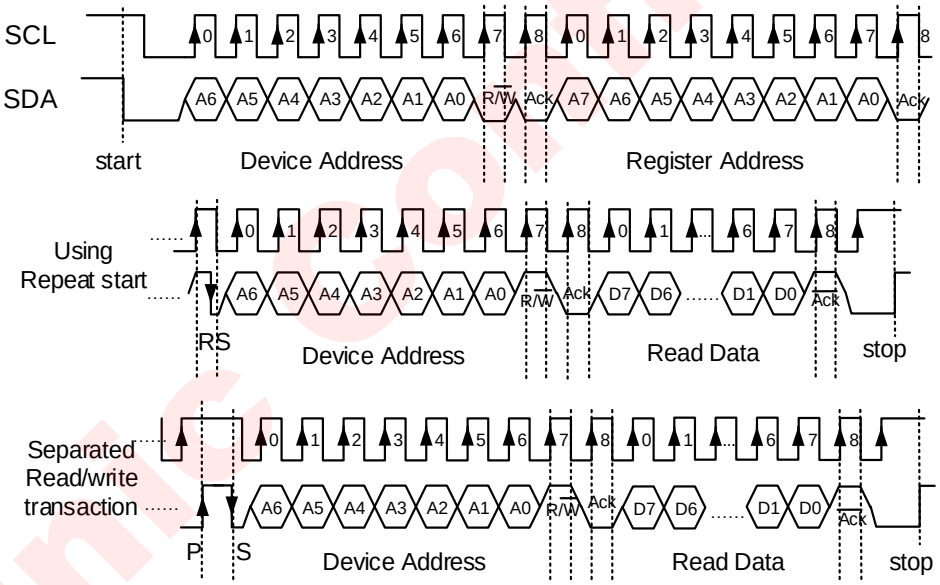


Figure 7 I²C Read Byte Cycle

LED DRIVER

AW2027 has 3 LEDs drivers to drive one RGB LED or three single-color LEDs. Each LED is driven by constant current source with duty cycle controlled by PWM. Both current and PWM level can be configured via I²C interface.

LED CURRENT

Globally, the maximum output current for three LEDs is 4-level selectable among 5mA, 10mA, 15mA and 30mA via register GCR2.IMAX (address 0x04). In general, GCR2.IMAX is used to set the max brightness of LED

output.

For each LED, there is 16 current levels configurable via 4-bit register groups LCFGx.CUR (x=1~3). So totally 4096 (16x16x16) kinds of color can be generated by setting different R/G/B current combination.

PWM DIMMING CONTROL

The LED output current source is gated by exponent 256-level PWM signal to create better dimming effect. The registers PWMx (address 0x34, 0x35, 0x36) define 8-bit PWM level for each LED.

When register PWMx being modified or working in PATTERN mode, the smooth transition effect is available by continuously adjusting PWM duty. The slope of ramp up/down, are separately set via configuring the bit4~bit7 in pattern registers LEDxT0/1 (x=1~3).

The ramping curve can be configured to be linear and exponential by setting bit3 (EXP) in register LCTR (address 0x30).

LED CONTROL

All LEDs in AW2027 can be independently turned on or off via setting bit LEx (x=1~3) of register LCTR
- LCTR.LEx=0, LEDx is switched off.
- LCTR.LEx=1, LEDx is switched on.

PATTERN MODE

When register bit LCFGx.MD (address 0x31, 0x32, 0x33, x=1~3) is set to “1”, the corresponding LEDx operates in pattern mode.

In this mode, the LEDx is controlled by internal pattern controller to produce breathing lighting effect with user-defined timing parameter. In AW2027, each LED has an independent pattern controller with respective pattern parameter configuration register, and work independently.

The waveform of a breathing pattern is shown in the diagram below. The parameter T0~T4 define 4 key primary time in a complete breathing period. T0 is the delay time before pattern starting, T1~T4 composite a breathing cycle, which denote the rise-time, on-time, fall-time and off- time respectively.

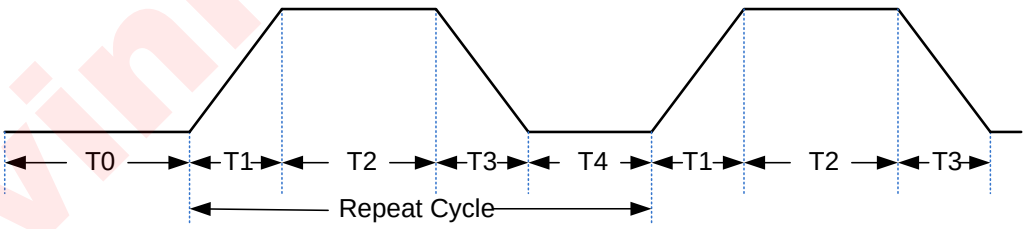


Figure 8 LED breath timing in pattern mode

The repeat times of pattern is configured by bit0~3 (REPEAT) in register LEDxT2. A pattern can repeat for 1 to 15 times if LEDxT2.REPEAT is not “0000”, or loop continuously if LEDxT2.REPEAT is “0000”

After defined times of pattern repeat is finished, the status bit STATUS.LISx (x=1~3, address 0x02) will be set to “1” automatically, which only can be cleared after reading register STATUS via I^2C.

In pattern mode, each channel can be configured independently. The breath effect will start once LEDxT2 is written. If user wants to sync the three channel start at the same time, please follow the following steps:

a) Set LCTR to 00h

b) Set LCFGx.MD to “0”

c) Configure LEDxT0,LEDxT1, LEDxT2 for parameters T0~T4, repeat time .

d) Set LCFGx.MD to “1”

e) Set LCTR to 07h

MANUAL CONTROL MODE

When control bit LCFGx.MD (address 0x31, 0x32, 0x33 bit4) is set to 0, the corresponding LEDx is work in manual control mode.

In manual control mode, the pattern controller is disable and the LED is directly controlled by setting current/ PWM level register via I²C interface.

Even in manual control mode, smooth dimming is supported. If LCFGx.FO and/or LCFGx.FI (address 0x31, 0x32 0x33, bit6/bit5) is set to 1, automatic fade-out and/or fade-out is enabled. If a new value is set on register PWMx when LCFGx.FO and/or LCFGx.FI is set, the brightness of LED output ramp up/down smoothly, with its transition time defined by parameter T1,T3 sourced from corresponding pattern configuration registers (LEDxT0 and LEDxT1).

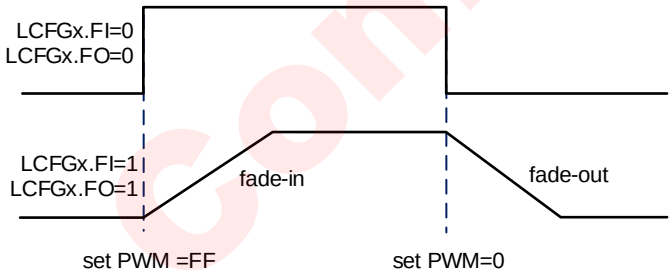


Figure 9 Manual Control Mode

SYNC CONTROL MODE

In order to simplify configuration and control in the case of all LEDs synchronously dimming, especially in application of RGB LED, the AW2027 can be configured to work on sync control mode.

When LCFG1.SYNC is set to 1, the device works in sync control mode. In this mode, user can control all LEDs to turn on, turn off, or output breathing lighting synchronously by controlling LED1 only.

In sync control mode, the output currents of all LEDs are still defined via register LCFGx.CUR individually, but their PWM levels of LED2,LED3 are both sourced from LED1, the setting of register PWM2,PWM3 are ignored. The control bit LCFG1.MD defines operating mode globally for all LEDs. If LCFG1.MD is 0, manual mode is selected for all LEDs, user can set all LEDs on or off by simply setting register PWM1, and fade-in or fade-out effect are selected by bit LCFG1.FI and LCFG1.FO. If register LCFG1.MD is set 1, all LEDs work in pattern mode, user only need to configured and control the pattern of LED1.

AUTO CHARGING INDICATION

In application of mobile phone, when battery voltage is too low and the PMU cannot work, the LED driver cannot be controlled by application processor via I²C interface. In this case, extra LED control circuit is necessary to be built in for charging status indication.

AW2027 provides the auto charging indication function for low battery voltage application. When the external USB power is inserts to phone, the pin CHRG is pulled high, AW2027 will enter active state automatically. The predefined blink lighting will output only on pin LED1, the LED2 and LED3 keep off status. The blinking waveform is showed in figure below. The maximum current is 6mA, blinking period is about 2.08s. Once the CHRG pin goes low, the device comes back to shutdown state again and stops LED1 output.

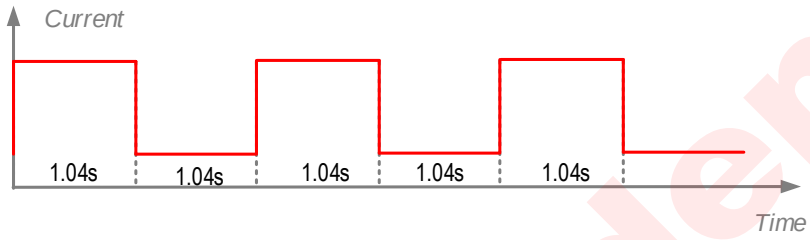


Figure 10 Blinking waveform on LED1 for auto charging indication

The auto charging indication function should be closed by configured register GCR1.CHGDIS (address 0x01, bit1) to 1 when the processor is able to configure AW2027 via I²C interface, then the lighting effects will have no relation with the CHRG status.

When special charger IC is used and pin CHRG is recommend to be connected to status pin of charger IC, the pin LED1 of AW2027can indicate the real battery charging status.

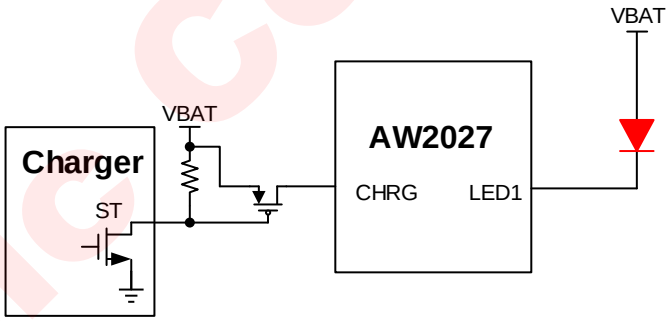


Figure 11 Real Charging Status Indication in special charger IC application

When no charger IC is applied, and battery charging is managed by PMU, no real charging status signal can be adapted, so the LED1 status can only indicate whether the USB power is plugged in or not.

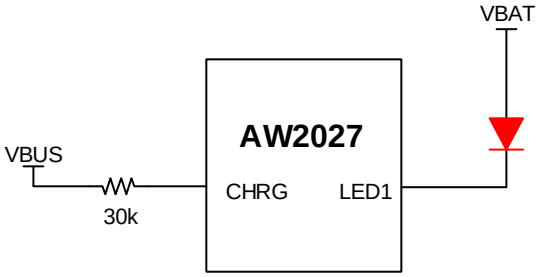


Figure 12 USB power Insertion status Indication in PMU-controlled charging application

REGISTER DESCRIPTION

REGISTER LIST

Addr	Name	W/R	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	RSTR	WR	0	0	0	0	1	0	0	1
01h	GCR1	WR	-	-	-	-	-	-	CHGDIS	CHIPEN
02h	STATUS	R	PS3	PS2	PS1	PUIS	UVLOIS	OTPIS	-	-
03h	PATST	R	0	0	0	0	0	ST3	ST2	ST1
04h	GCR2	WR	DUVP	DOTP	UVDIS	OTDIS	UVTH		IMAX	
30h	LCTR	WR	-	-	FREQ	P255	EXP	LE3	LE2	LE1
31h	LCFG1	WR	SYNC	FO	FI	MD	CUR			
32h	LCFG2	WR	-	FO	FI	MD	CUR			
33h	LCFG3	WR	-	FO	FI	MD	CUR			
34h	PWM1	WR	PWM							
35h	PWM2	WR	PWM							
36h	PWM3	WR	PWM							
37h	LED1T0	WR	T1				T2			
38h	LED1T1	WR	T3				T4			
39h	LED1T2	WR	T0				REPEAT			
3Ah	LED2T0	WR	T1				T2			
3Bh	LED2T1	WR	T3				T4			
3Ch	LED2T2	WR	T0				REPEAT			
3Dh	LED3T0	WR	T1				T2			
3Eh	LED3T1	WR	T3				T4			
3Fh	LED3T2	WR	T0				REPEAT			

DETAILED REGISTER DESCRIPTION

RSTR, Chip ID and Software Reset Register

Address: 0x00, R/W, default: 0x09

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Symbol	Description
7:0	RSTR	Read: Chip ID, 0x09 Write: write 0x55 to RSTR, reset internal logic and register

GCR1, Global Control Register

Address: 0x01, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	CHGDIS	CHIPEN

Bit	Symbol	Description

7-2	-	Reserved
1	CHGDIS	Disable Auto Charge Indication Function 0: enable auto charge indication (default) 1: disable auto charge indication
0	CHIPEN	Device operating Enable 0: disable, the device is in standby state (default) 1: enable, the device enters active state

STATUS, Chip Status Register

Address: 0x02, Read only, Cleared after Read

7	6	5	4	3	2	1	0
PS3	PS2	PS1	PUIS	UVLOIS	OTPIS	-	-

Bit	Symbol	Description
7:5	PSx	LEDx Pattern Complete Indication 0: pattern is running or not start 1: pattern completed
4	PUIS	Power Up Interrupt Status 0: No power-up reset has taken place 1: Power-up reset has taken place
3	UVLOIS	UVLO Detection Status 0: no UVLO detected 1: UVLO detected
2	OTIS	Over-temperature Detection Status 0: no Over-Temperature detected 1: Over-Temperature detected
1-0	-	Reserved

PATST, Pattern Status Register

Address: 0x03, Read only, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	ST3	ST2	ST1

Bit	Symbol	Description
7:3	-	Reserved
2	ST3	LED3 Pattern Status 0: Pattern is not running 1: Pattern is running
1	ST2	LED2 Pattern Status 0: Pattern is not running 1: Pattern is running
0	ST1	LED1 Pattern Status 0: Pattern is not running

1: Pattern is running

GCR2, LED Maximum Current Register

Address: 0x04, R/W, default: 0x00

7	6	5	4	3	2	1	0
DUVP	DOTP	UVDIS	OTDIS	UVTH		IMAX	

Bit	Symbol	Description
7	DUVP	Disable UVLO Protection function 0: enable UVLO protection, reset CHIPEN when UVLOIS=1 (default) 1: disable UVLO protection
6	DOTP	Disable Over-Temperature-Protection function 0: enable OTP protection, reset CHIPEN when OTPIS=1 (default) 1: disable OTP protection
5	UVDIS	Disable UVLO Detection Function 0: enable UVLO detection (default) 1:disable UVLO detection
4	OTDIS	Disable Over-Temperature Detection Function 0: enable Over-temperature detection (default) 1: disable Over-Temperature detection
3:2	UVTH	UVLO Detection Threshold Selection 00：2.0v (default) 01：2.1v 10：2.2v 11：2.2v
1:0	IMAX	Global Max Output Current Select IMAX 00: Imax=15mA （default） 01: Imax=30mA 10: Imax=5mA 11: Imax=10mA

LCTR, LED Control Register

Address: 0x30, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	FREQ	P255	EXP	LE3	LE2	LE1

Bit	Symbol	Description
5	FREQ	PWM Carrier Frequency Selection 0:250Hz (default) 1:125Hz
4	-	Reserved
3	EXP	PWM Transition mode Selection 0: Exponential transition (default) 1: Linear transition
2	LE3	LED3 Enable

0: LED3 module stop work and LED3 out disable (default)
1: LED3 output is enabled

2 LE2 LED2 Enable
0: LED2 module stop work and LED2 out disable (default)
1: LED2 output is enabled

0 LE1 LED1 Enable
0: LED1 module stop work and LED1 out disable (default)
1: LED1 output is enabled

LCFG1, LED1 Mode Configuration Register

LCFG1: Address: 0x31, R/W, default: 0x00

7	6	5	4	3	2	1	0
SYNC	FO	FI	MD	CUR			

Bit	Symbol	Description
7	SYNC	Sync Mode Enable 0: Independently control mode (default) 1: Sync control mode
6	FO	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable (default) 1: PWM fade-out is enable, the dimming time defined by T3
5	FI	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable (default) 1: PWM fade-in is enable, the dimming time defined by T1
4	MD	LED1 Operating Mode Select. 0: Manual mode (default) 1: Pattern mode
3:0	CUR	LED1 output Current Setting. LED1 output current Io = Imax*CUR/15 (mA) when PWM1 is 255, default value is 0.

LCFG2, LED2 Mode Configuration Register

LCFG1: Address: 0x32, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	FO	FI	MD	CUR			

Bit	Symbol	Description
6	FO	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable (default) 1: PWM fade-out is enable, the dimming time defined by T3
5	FI	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable (default) 1: PWM fade-in is enable, the dimming time defined by T1
4	MD	LED2 Operating Mode Select.

0: Manual mode (default)
1: Pattern mode

3:0	CUR	LED2 output Current Setting. LED2 output current Io = Imax*CUR/15 (mA) when PWM2 is 255, default value is 0.

LCFG3, LED3 Mode Configuration Register

LCFG2: Address: 0x33, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	FO	FI	MD	CUR			

Bit	Symbol	Description
6	FO	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable (default) 1: PWM fade-out is enable, the dimming time defined by T3
5	FI	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable (default) 1: PWM fade-in is enable, the dimming time defined by T1
4	MD	LED3 Operating Mode Select. 0: Manual mode (default) 1: Pattern mode
3:0	CUR	LED3 output Current Setting. LED3 output current Io = Imax*CUR/15 (mA) when PWM3 is 255, default value is 0.

PWM1/PWM2/PWM3 , PWM Dimming Level Register

PWM1: Address: 0x34, R/W, default:0x00
PWM2: Address: 0x35, R/W, default:0x00
PWM3: Address: 0x36, R/W, default:0x00

7	6	5	4	3	2	1	0
PWM							

Bit	Symbol	Description
7:0	PWM	PWM level for LEDx (x=1~3), default value is 0.

LEDxT0, T1 & T2 Configuration Register

LED1T0: Address: 0x37, R/W, default: 0x00
LED2T0: Address: 0x3A, R/W, default: 0x00
LED3T0: Address: 0x3D, R/W, default: 0x00

7	6	5	4	3	2	1	0
T1				T2			

Bit	Symbol	Description
7:4	T1	T1 (Rise-time) selection

0000:	0.00s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

3:0 T2 T2 (On-time) selection

0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

LEDxT1, T3 & T4 Configuration Register

LED1T1: Address: 0x38, R/W, default: 0x00
LED2T1: Address: 0x3B, R/W, default: 0x00
LED3T1: Address: 0x3E, R/W, default: 0x00

7	6	5	4	3	2	1	0
T3				T4			

Bit	Symbol	Description

7:4 T3 T3 (Fall-time) selection

0000:	0.00s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

3:0 T4 T4 (Off-time) selection

0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s

0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

LEDxT2, T0 & Repeat Times Configuration Register

LED1T2: Address: 0x39, R/W, default: 0x00
LED2T2: Address: 0x3C, R/W, default: 0x00
LED3T2: Address: 0x3F, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	T0			REPEAT			

Bit	Symbol	Description
7:4	T0	T0 (delay time of pattern startup) selection

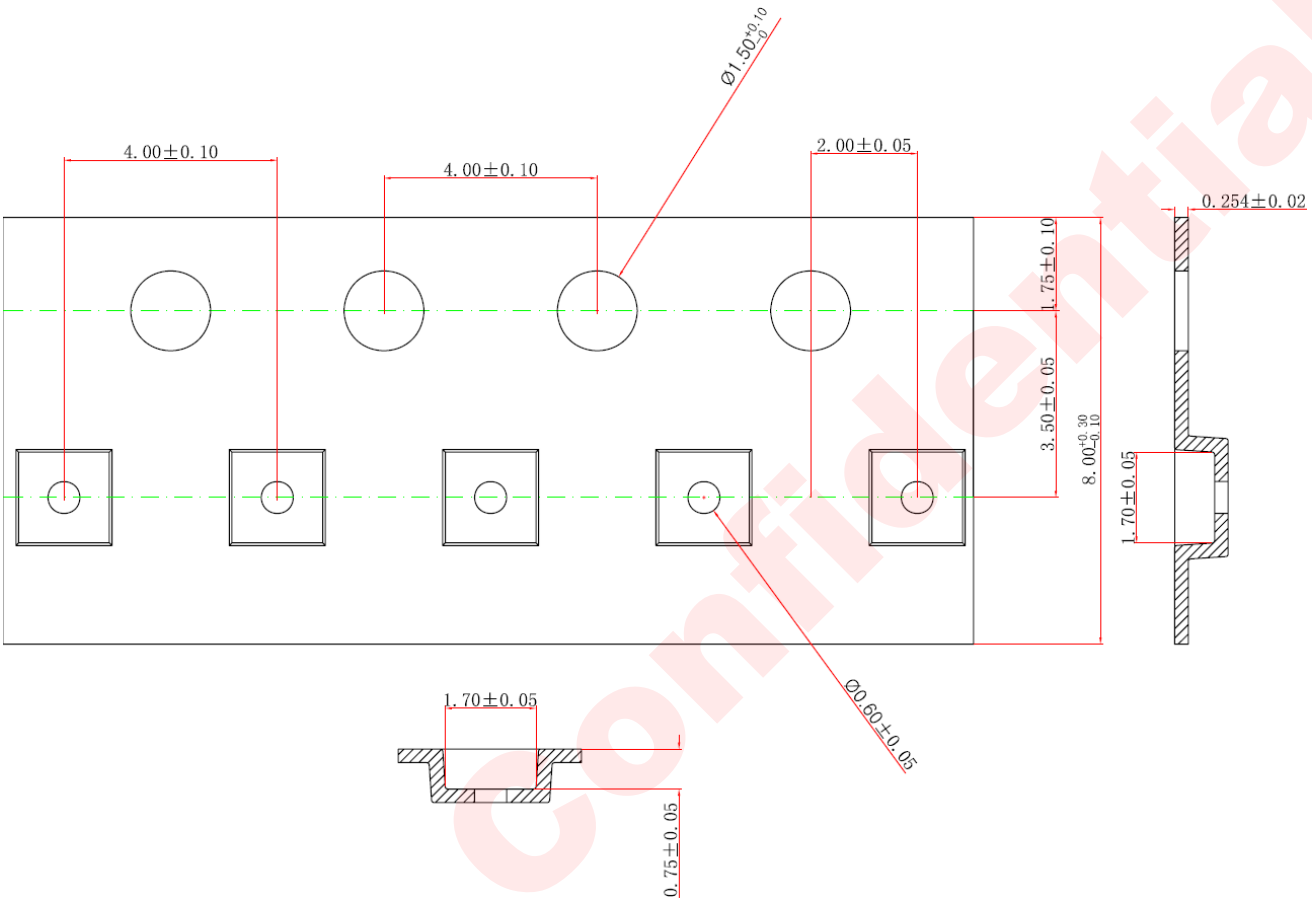
0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

3:0 REPEAT Pattern Repeat Time

0000: don't stop
0001: pattern run 1 time
0010: pattern run 2 times
……
1111: pattern run 15 times

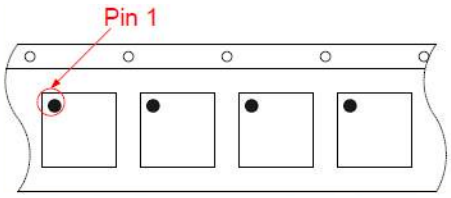
TAPE AND REEL INFORMATION

CARRIER TAPE

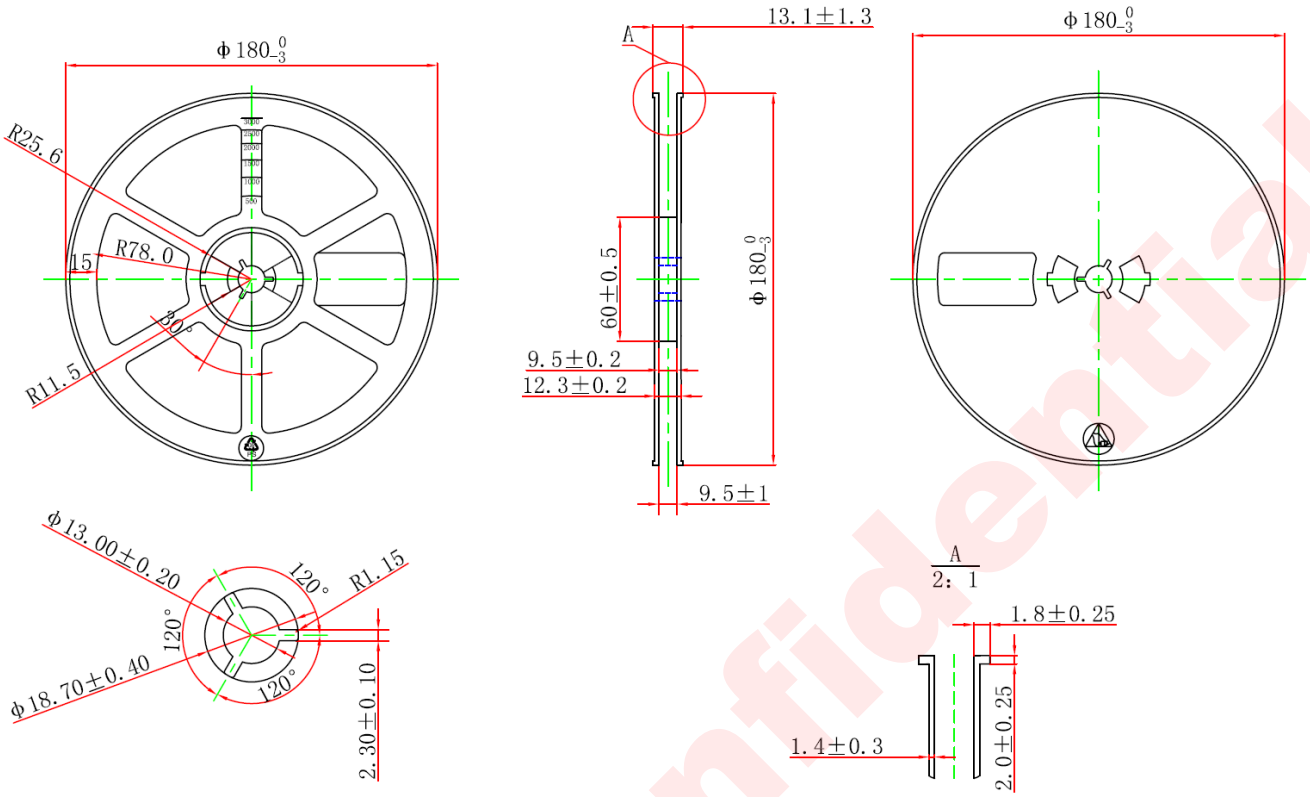


NOTE: ALL DIMS IN mm.

PIN 1



REEL

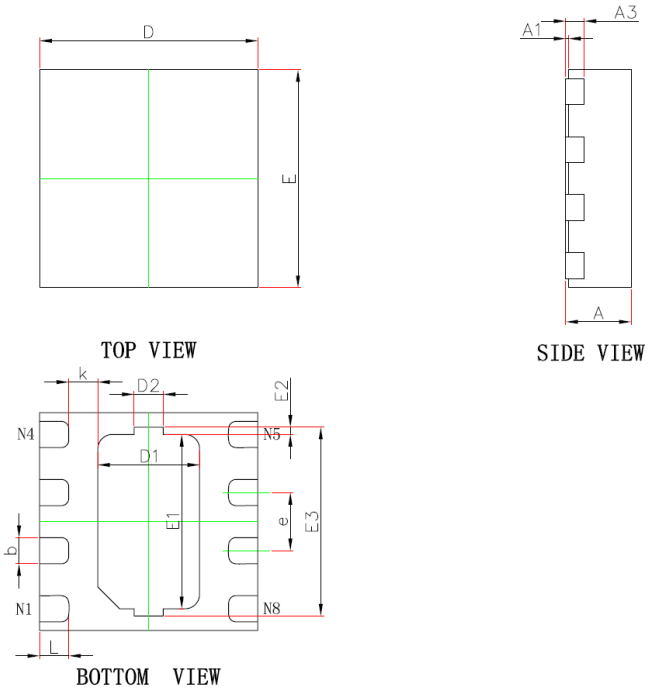


NOTE:

1、 ALL DIMS IN mm;

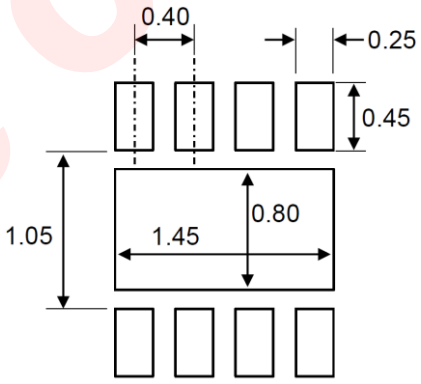
2、 General Tolerance ±0.25mm.

PACKAGE DESCRIPTION



SYMBOL	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.400	0.500	0.016	0.200
A1	0.000	0.050	0.000	0.002
A3	0.127REF.		0.005REF.	
D	1.450	1.550	0.057	0.061
E	1.450	1.550	0.057	0.061
D1	0.650	0.750	0.026	0.030
D2	0.200REF.		0.008REF.	
E1	1.150	1.250	0.045	0.049
E2	0.050REF.		0.002REF.	
E3	1.250	1.350	0.049	0.053
k	0.200REF.		0.008REF.	
b	0.150	0.250	0.006	0.010
e	0.400BSC.		0.016BSC.	
L	0.150	0.250	0.006	0.010

LAND PATTERN EXAMPLE



* Dimensions are in millimeters.

REFLOW

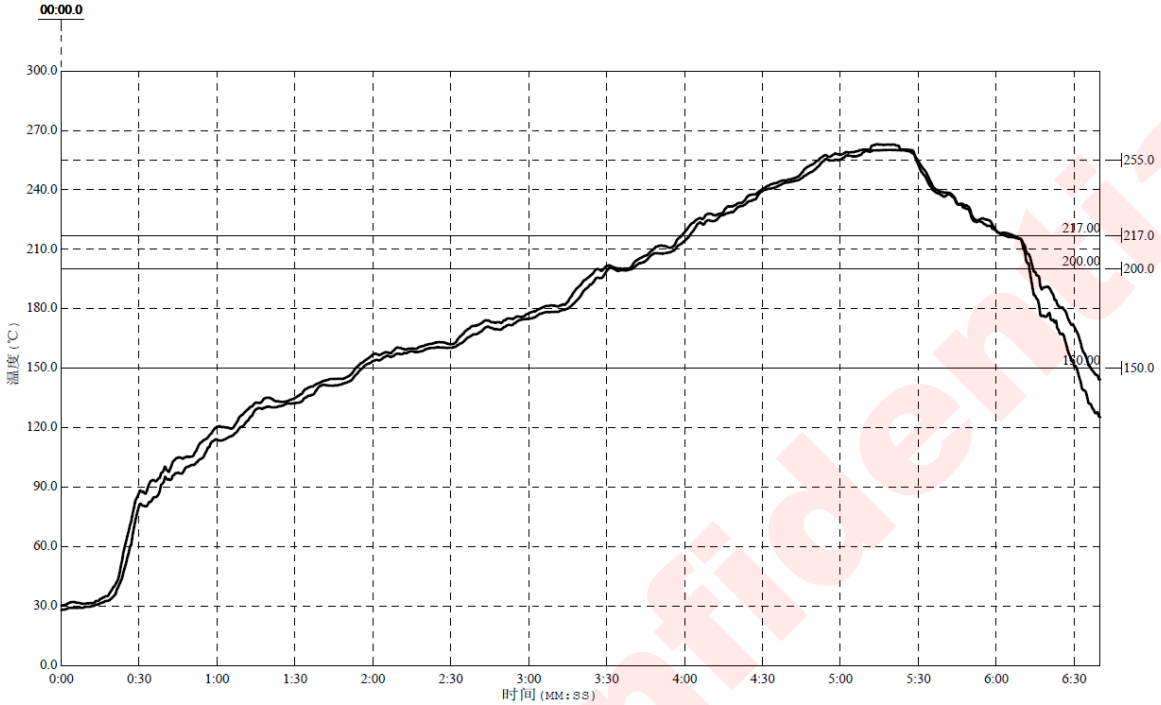


Figure 17 Package Reflow Oven Thermal Profile

Reflow Note	Spec
Average ramp-up rate (217℃ to Peak)	Max. 3℃/sec
Time of Preheat temp.(from 150℃ to 200℃)	60-120sec
Time to be maintained above 217℃	60-150sec
Peak Temperature	>260℃
Time within 5℃ of actual peak temp	20-40sec.
Ramp-down rate	Max. 6℃/sec
Time from 25℃ to peak temp	Max. 8min.

REVISION HISTORY

Vision	Date	Change Record
V1.0	May 2017	Initial release
V1.1	Sep 2017	1.Update part of functional descriptions 2.Amend the default value description of register GCR2.IMAX
V1.2	Nov 2017	Modify the typical application circuit --page 1,3 Add the Exposed Pad descriptions --page 2 Modify F_{PWM}=250Hz --page 5

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