



AVED MEMORY PRODUCTS

Where Quality & Memory Merge

AVEF30F080U04SJ08-XX

4MB FLASH SIMM, based on Hyundai Hy29F080T-90 (Uniform Sector Flash Memory)

DESCRIPTION

AVED Memory Products AVEF30F080U04SJ08-XX is a 5.0V flash memory SIMM, composed of four CMOS 8Mbit wide uniform sector devices, each organized as 1M X 8bits, mounted on a substrate along with decoupling capacitors. The module is an 80-pin, JEDEC standard SIMM, organized into 1 bank of 1M X 32 bits, mechanically compatible to many commercial sockets for any memory application.

FEATURES

- Single 5V power supply
- Fast Access Time: 70, 90, 120ns(max)
- Compatible with JEDEC Std (E²PROM) programmers
- Flexible sector architectures
- Embedded Erase™ algorithm facilitates full chip erase or any combination of design sectors
- Embedded Program™ algorithm facilitates write and verification control at specified addresses
- Ready/Busy# detection
- Data# Polling and Toggle Bit capability for detection of program or erase cycle completion
- Erase Suspend/Erase Resume operation
- Low Power consumption

AVEF30F080U04SJ08-XX = Tin Contact Plating

PIN NAMES

A0 – A19	Address Inputs
DQ0 - DQ31	Data In/Out
RESET#	Hardware Reset Pin (optional)
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
Vcc	5V±10% or ±5% for High Performance
Vss	Device Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

MODULE	PD1	PD2	PD3	PD4
4MB	NC	NC	NC	Vss
SPEED	PD5	PD6	PD7	
70ns	Vss	Vss	NC	
90ns	NC	NC	Vss	
120ns	Vss	NC	Vss	

PIN CONFIGURATIONS

Pin	Name	Pin	Name
1	VSS	41	A11
2	VCC	42	A10
3	NC	43	A9
4	OE#	44	A8
5	WE0#	45	A7
6	WE1#	46	A6
7	RESET# (optional)	47	A5
8	DQ16	48	A4
9	DQ17	49	A3
10	DQ18	50	A2
11	DQ19	51	A1
12	DQ20	52	A0
13	DQ21	53	WE3#
14	DQ22	54	VSS
15	DQ23	55	DQ15
16	DQ24	56	DQ14
17	DQ25	57	DQ13
18	DQ26	58	DQ12
19	DQ27	59	DQ11
20	DQ28	60	DQ10
21	*CE3#	61	DQ9
22	*CE2#	62	DQ8
23	*CE1#	63	DQ7
24	CE0#	64	DQ6
25	VSS	65	DQ5
26	DQ29	66	DQ4
27	DQ30	67	DQ3
28	DQ31	68	DQ2
29	WE2#	69	DQ1
30	NC	70	DQ0
31	NC	71	NC
32	NC	72	VCC
33	A19	73	PD1
34	A18	74	PD2
35	A17	75	PD3
36	A16	76	PD4
37	A15	77	PD5
38	A14	78	PD6
39	A13	79	PD7
40	A12	80	VSS

*These pins are not used in this module



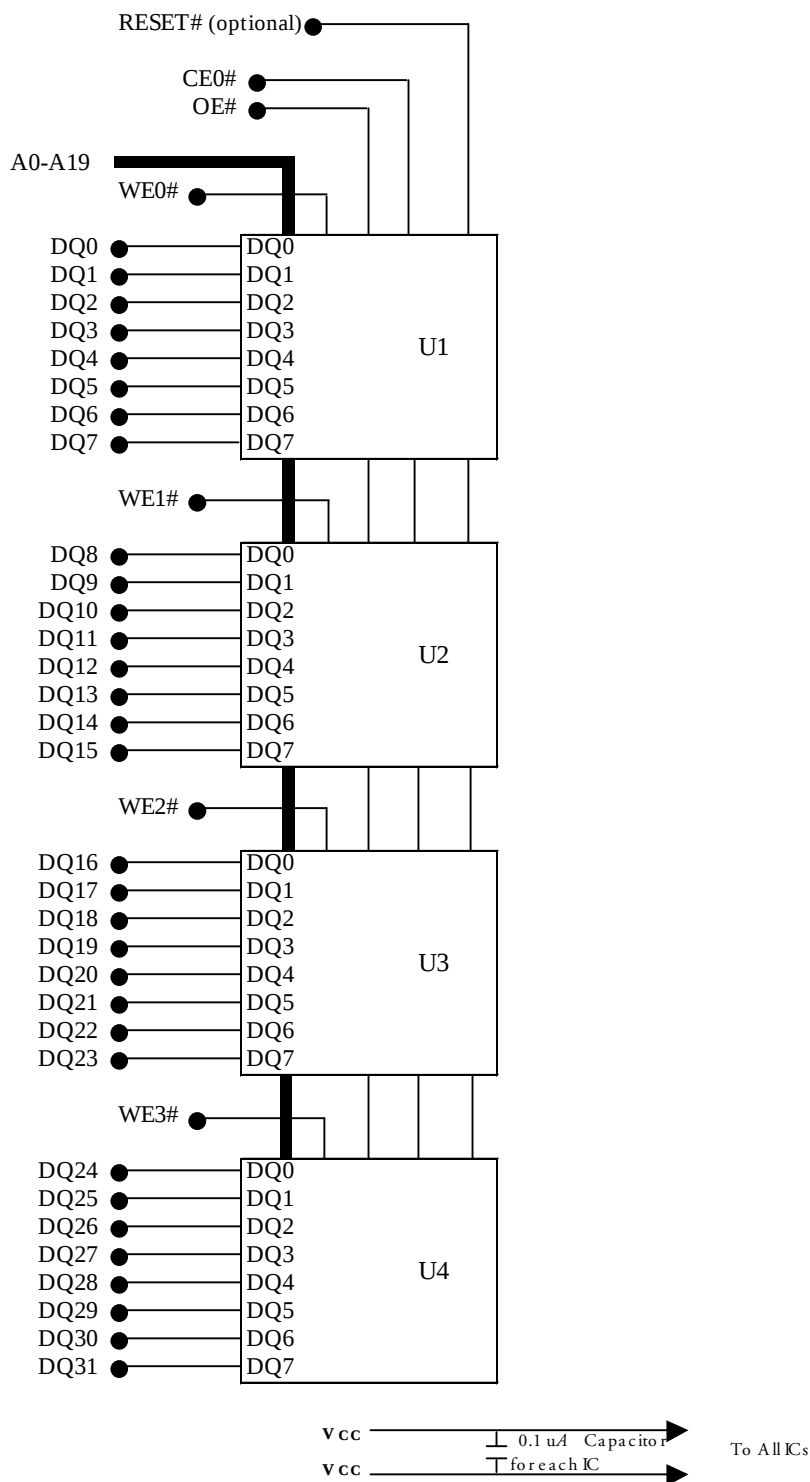
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BLOCK DIAGRAM




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ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages -65°C to +125°C

Ambient Temperature

with Power Applied -55°C to +125°C

Voltage with Respect to Ground

V_{cc} (Note 1) -2.0V to + 7.0V

A9 and OE# (Note 2) -2.0V to + 12.5V

All other pins (Note 1) -2.0V to 7.0V

Output Short Circuit Current (Note 3) 200mA

OPERATING RANGES

Commerical (C) Devices

Ambient Temperature (TC) 0°C to + 70°C

Industrial (I) Devices

Ambient Temperature(TC) -40°C to + 85°C

Extended (E) Devices

Ambient Temperature (TA) -55°C to + 125°C

V_{cc} Supply Voltages

V_{cc} for ±5% devices +4.75V to + 5.25V

V_{cc} for ±10% devices +4.5V to + 5.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{ss} to -2.0V for periods of up to 20ns. Maximum DC voltage on output or I/O pins is V_{cc} +0.5V. During voltage transitions, outputs may overshoot to V_{cc} +2.0 for periods of up to 20ns.
2. Minimum DC input voltage on A9 and OE# pins is -0.5V. During voltage transitions, A9 and OE# pins may overshoot V_{ss} to -2.0V for periods of up to 20ns. Maximum DC input voltage on pin A9 and OE# is 12.5V, which may overshoot to +13.5V for periods up to 20ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

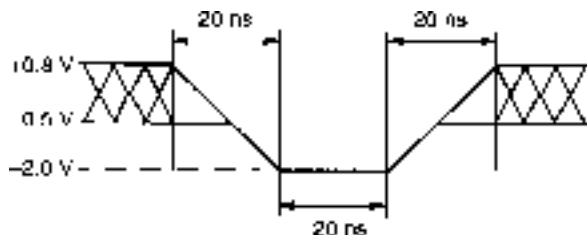


Figure 1. Maximum Negative Overshoot Waveform

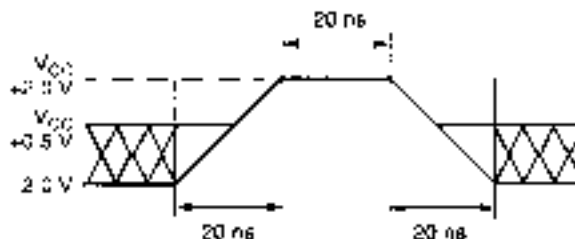


Figure 2. Maximum Positive Overshoot Waveform


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DC CHARACTERISTICS (CMOS Compatible)

Sym	Description	Test Conditions	Min	Typ	Max	Unit
ILI	Input Load Current	V _{IN} = V _{SS} to V _{CC} V _{CC} = V _{CC} (max)			± 4.0	μA
ILIT	A9 Input Load Current	V _{CC} = V _{CC} (max) A9 = 12.5V			50	μA
ILO	Output Leakage Current	V _{OUT} = V _{SS} to V _{CC} V _{CC} = V _{CC} (max)			± 4.0	μA
ICC1	VCC Read Current (Note 1)	CE# = V _{IL} , OE# = V _{IH}		100	160	mA
ICC2	VCC Write Current (Notes 2,3)	CE# = V _{IL} , OE# = V _{IH}		120	160	mA
ICC3	VCC Standby Current (CE# Controlled) (Note 4)	V _{CC} = V _{CC} (max), CE# = V _{CC} ± 0.5V,		4	20	μA
V _{IL}	Input Low Voltage		-0.5		0.8	V
V _{IH}	Input High Voltage		0.7 x V _{CC}		V _{CC} + 0.3	V
V _{ID}	Voltage for Autoselect and Sector Protect	V _{CC} = 5.0V	11.5		12.5	V
V _{OL}	Output Low Voltage	I _{OL} = 12.0mA, V _{CC} = V _{CC} (min)			0.45	V
V _{OH1}	Output High Voltage	I _{OH} = -2.5mA, V _{CC} = V _{CC} (min)	0.85 V _{CC}			V
V _{OH2}		I _{OH} = -100μA, V _{CC} = V _{CC} (min)	V _{CC} - 0.4			V
V _{LK0}	Low VCC Lock-Out Voltage		3.2		4.2	V

Notes:

1. The I_{CC} current listed is typically less than 1mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Erase or Embedded Program algorithm is in progress.
3. Not 100% tested.
4. I_{CC3} and I_{CC4} = 20uA at extended temperature(>+85°C).


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AC CHARACTERISTICS

Read-Only Operations

JEDEC	Std.	Description		-75	- 90	-120	Unit
tAVAV	tRC	Read Cycle Time (Note1)	Min	70	90	120	ns
tAVQV	tACC	Address to Output Delay (CE#, OE# = VIL)	Max	70	90	120	ns
tELQV	tCE	Chip Enable to Output Delay (OE# = VIL)	Max	70	90	120	ns
tGLQV	tOE	Output Enable to Output Delay	Max	40	40	50	ns
	tOE _H	Output Enable Hold Time (Note1)	Read	Min	0	0	ns
		Toggle and Data# Polling	Min	10	10	10	ns
tEHQZ	tDF	Chip Enable to Output High Z	Max	20	20	30	ns
tGHQZ	tDF	Output Enable to Output High Z	Max	20	20	30	ns
tAXQX	tOH	Output Hold Time From Addresses CE# or OE#, Whichever Occurs First	Min	0	0	0	ns

Notes:

1. Not 100% tested.

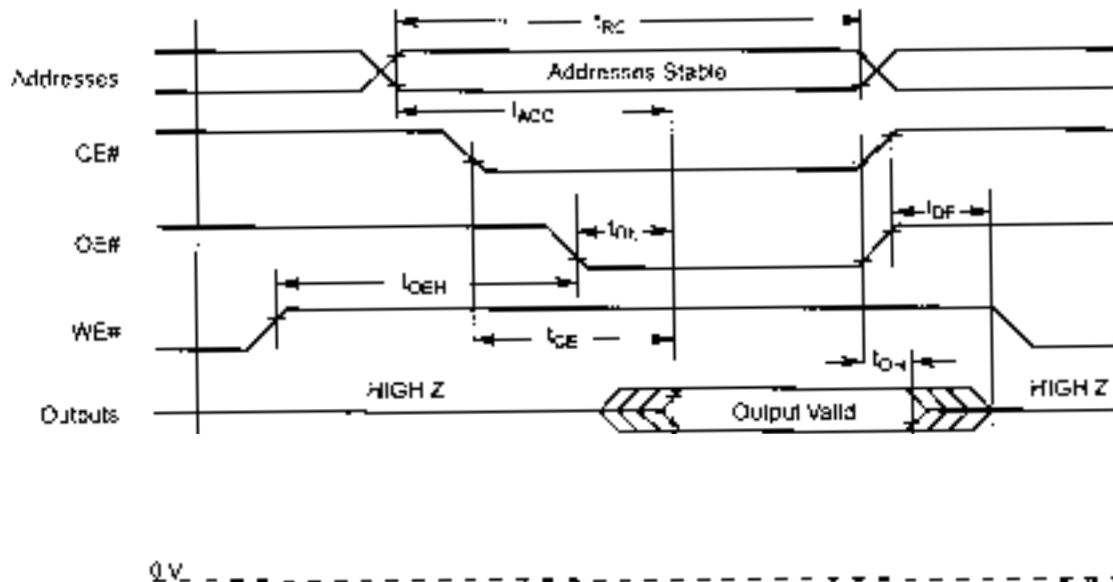


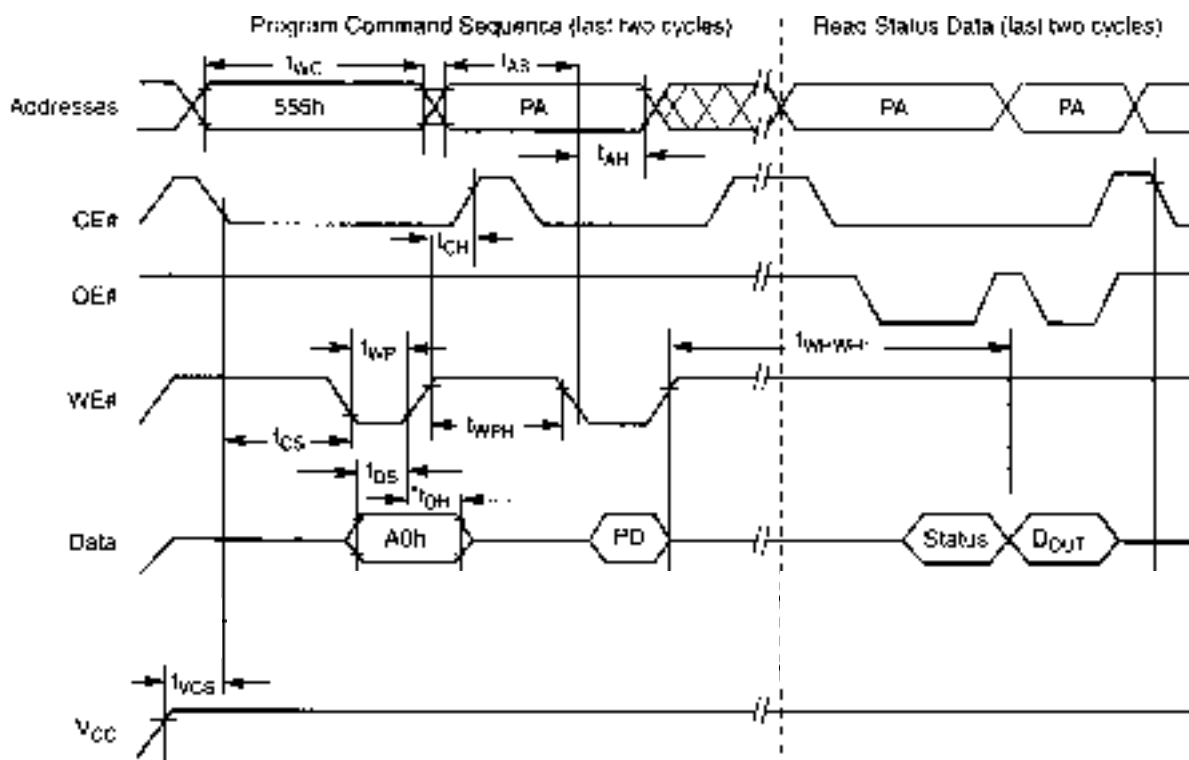
Figure 3. Read Operations Timings


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AC CHARACTERISTICS
Erase/Program Operations

JEDEC	Std	Description		-75	-90	-120	Unit
tAVAV	tWC	Write Cycle Time (Note 1)	Min	70	90	120	ns
tAVWL	tAS	Address Setup Time	Min		0		ns
tWLAX	tAH	Address Hold Time	Min	40	45	50	ns
tDVWH	tDS	Data Setup Time	Min	40	45	50	ns
tWHDX	tDH	Data Hold Time	Min	0			ns
	tOES	Output Enable Setup Time	Min	0			ns
tGHWL	tGHWL	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0			ns
tELWL	tCS	CE# Setup Time	Min	0			ns
tWHEH	tCH	CE# Hold Time	Min	0			ns
tWLWH	tWP	Write Pulse Width	Min	40	45	50	ns
tWHWL	tWPH	Write Pulse Width High	Min	20			ns
	tVCS	VCC Setup Time (Note 1)	Min	50			µs

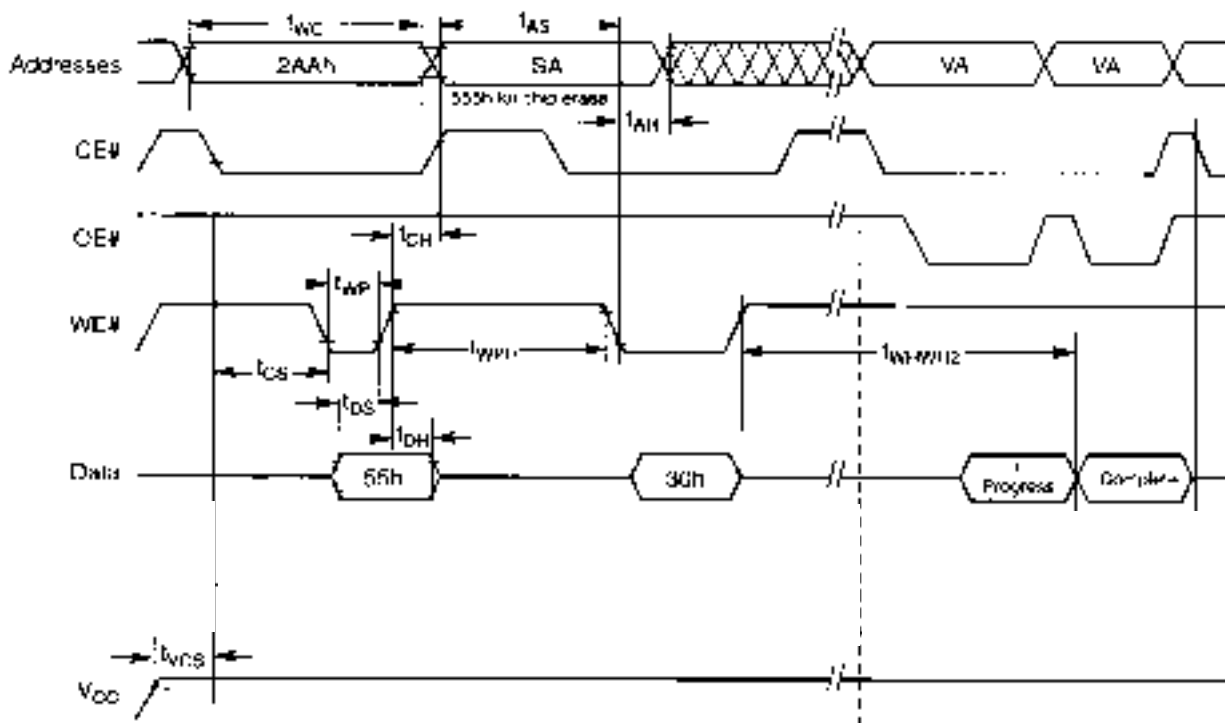
Notes:

1. Not 100% tested.


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AC CHARACTERISTICS


Note: PA = program address, PD = program data, D_{OUT} is the true data at the program address.

Figure 4. Program Operation Timings

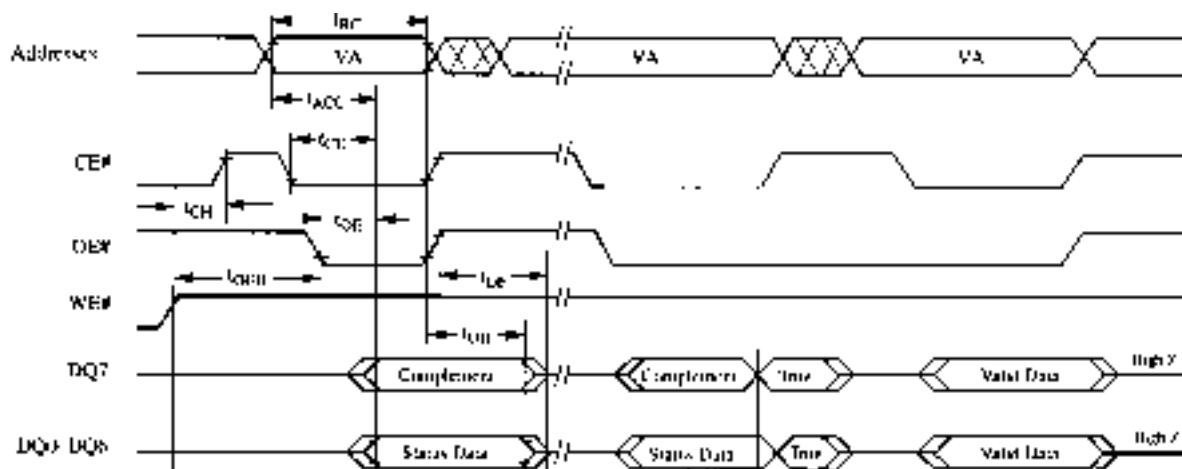

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AC CHARACTERISTICS

Note:

SA – Sector Address. VA – Valid Address for reading status data

Figure 5. Chip/Sector Erase Operation Timings


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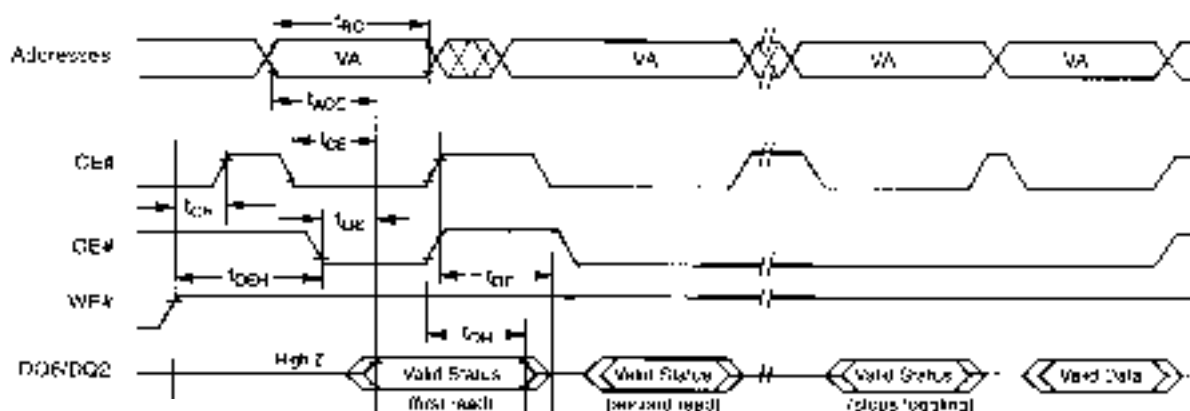
AC CHARACTERISTICS



Note:

VA = Valid address. Illustration shows first status cycle after command sequence, 1st status read cycle, and array data read cycle.

Figure 6. Data# Polling Timings (During Embedded Algorithms)



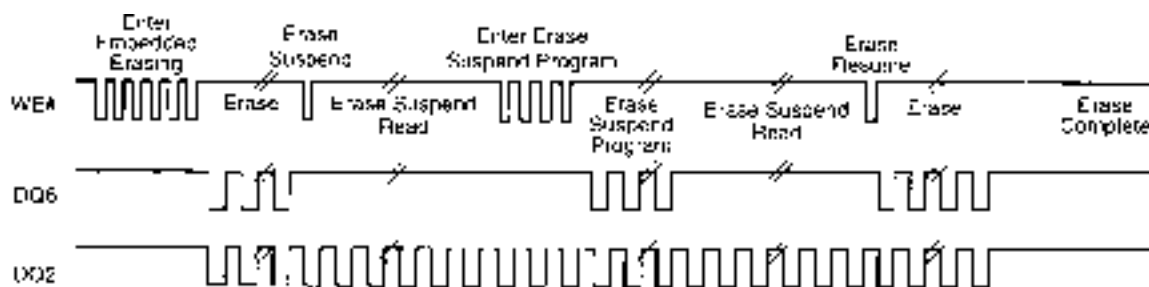
Note:

VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 7. Toggle Bit Timings (During Embedded Algorithms)


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AC CHARACTERISTICS


Note:

The system may use OE# or CE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within the erase-suspended sector.

Figure 8. DQ2 vs. DQ6

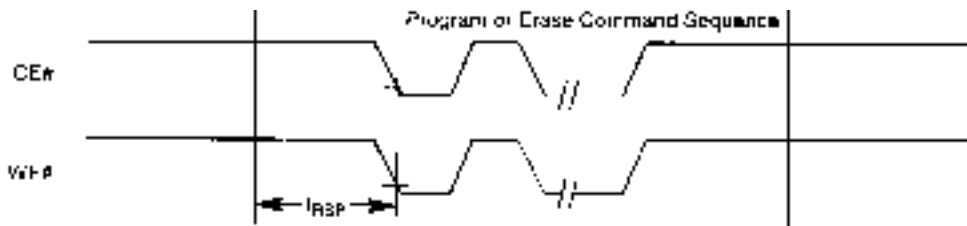


Figure 9. Temporary Sector Group Unprotect Timings


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AC CHARACTERISTICS

Erase and Program Operations Alternate CE# Controlled Writes

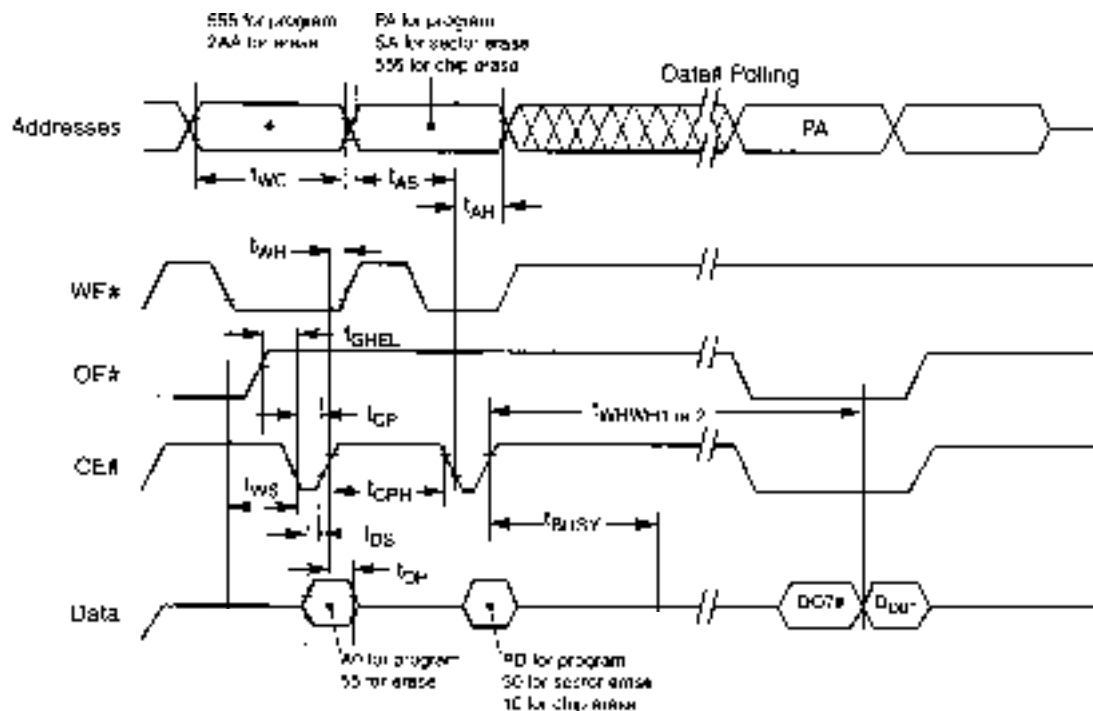
JEDEC	Std	Description		-75	-90	-120	Unit
tAVAV	tWC	Write Cycle Time (Note 1)	Min	70	90	120	ns
tAVEL	tAS	Address Setup Time	Min		0		ns
tELAX	tAH	Address Hold Time	Min	40	45	50	ns
tDVEH	tDS	Data Setup Time	Min	40	45	50	ns
tEHDx	tDH	Address Hold Time	Min		0		ns
tGHEL	tGHEL	Read Recover Time Before Write	Min		0		ns
tWLEL	tWS	CE# Setup Time	Min		0		ns
tEHWH	tWH	CE# Hold Time	Min		0		ns
tELEH	tCP	Write Pulse Width	Min	40	45	50	ns
tEHEL	tCPH	Write Pulse Width High	Min		20		ns

Notes:

1. Not 100% tested.


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AC CHARACTERISTICS



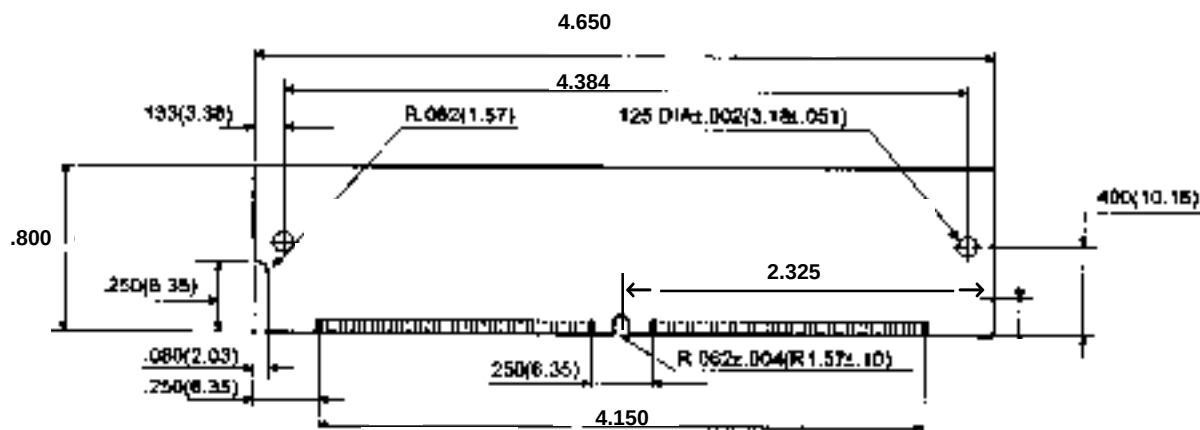
Notes:

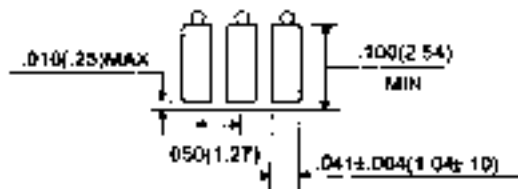
- 1 PA - Program Address. PD - Program Data. SA - Sector Address, DQ7# - Complement of Data Input, DOUT = Array Data.
- 2 Figure indicates the last two bus cycles of the command sequence

Figure 10. Alternate CE# Controlled Write Operation Timings


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PACKAGE DIMENSIONS

Units: Inches(millimeters)


 Tolerances: $\pm .005(.13)$ unless otherwise specified

Solder Plating Lead


AVED Memory Products reserves the right to change products and specifications without notice.