Integrated Circuit Systems, Inc.

AV9154A-39

Preliminary Product Preview

Low Cost 16-Pin Frequency Generator

General Description

The **ICS9154A-39** is a 0.8mm technology low-cost frequency generator designed for general purpose PC and disk drive applications. However, because the **ICS9154A-39** uses 0.8mm technology and the latest phase-locked loop architecture, it offers significant performance advantages that enable the device to be used in high performance systems when clock jitter is a key design issue.

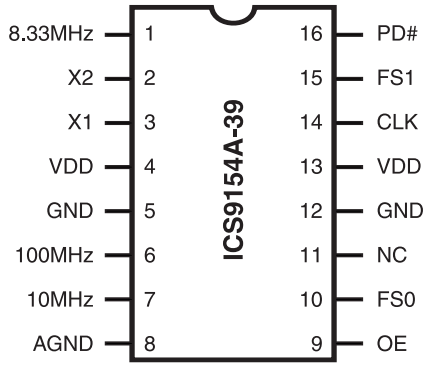
The **ICS9154A-39** guarantees a 45/55 duty cycle over all frequencies. In addition, a worst case jitter of ±250ps is achieved.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the cpu speed. The **ICS9154A-39** makes a gradual transition between frequencies.

Features

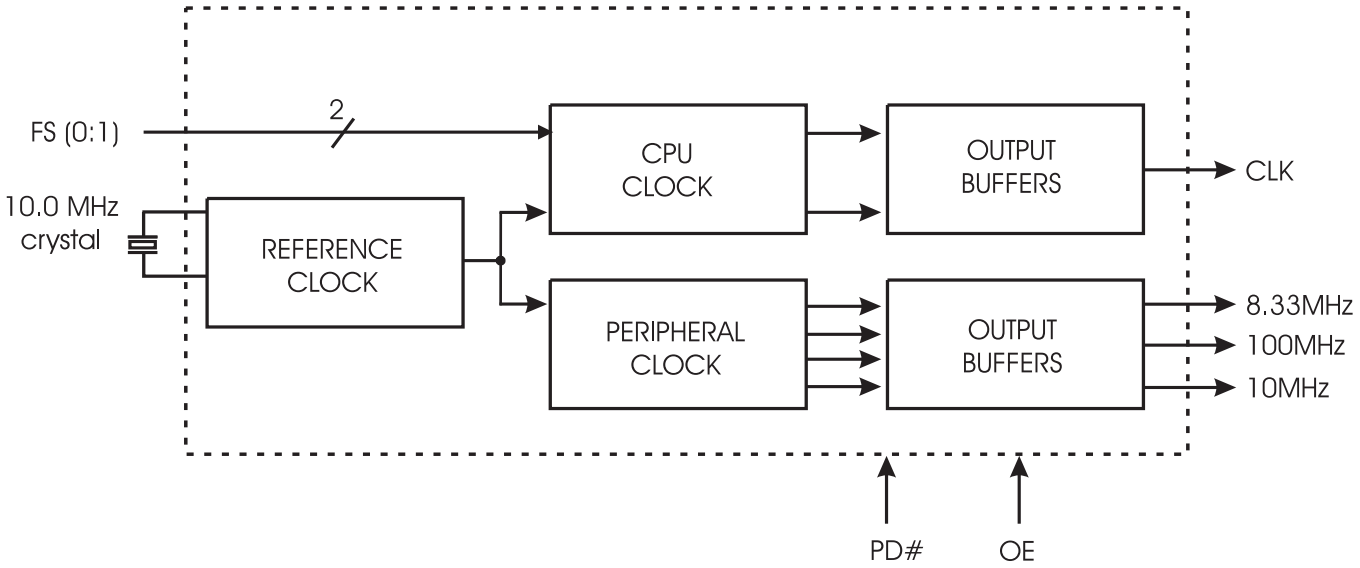
- All loop filter components internal
- 5V operation
- 16-pin 150-mil SOIC
- Power-down control of CPU clock and Fixed Clock when PD# goes low
- Output enable control of all output pins

Pin Configuration



16-Pin SOIC

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	8.33 MHz	OUT	8.33 MHz output clock.*
2	X2	OUT	Crystal Out.
3	X1	IN	Crystal In, nominally 10.0 MHz.
4	VDD	PWR	Digital power (+5V).
5	GND	PWR	Digital ground.
6	100 MHz	OUT	100 MHz clock output.*
7	10 MHz	OUT	10 MHz keyboard clock output.*
8	AGND	PWR	Analog ground.
9	OE	IN	Tristates outputs when low.
10	FS0	IN	Frequency select 0 for CPU clock.
11	NC	-	No connect (Do not connect to this pin.).
12	GND	PWR	Digital ground.
13	VDD	PWR	Digital power (+5V).
14	CPUCLK	OUT	CPU clock output.
15	FS1	IN	Frequency select 1 for CPU clock.
16	PD#	IN	Power-down, shuts off internal clocks and forces outputs to low logic level when input pulled logic low.

Note: The following input pins are pulled-up to VDD internal: 9, 10, 15 and 16.

Functionality

FS1	FS0	CLK(MHz)
0	0	40.0
0	1	30.0
1	0	37.0
1	1	25.0

These frequencies assume an input frequency of 10.0 Mhz.

Absolute Maximum Ratings

VDD referenced to GND 7V
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Operating temperature under bias. . . . . 0°C to +70°C
Power dissipation . . . . . 0.5 Watts
Storage temperature . . . . . -40°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V	-35	-16.0		µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5		5	µA
Output Low Voltage	V_{OL}	I_{OL}=10mA		0.15	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA	2.4	3.7		V
Output Low Current[1]	I_{OL}	V_{OL}=0.8	15	32		mA
Output High Current[1]	I_{OH}	V_{OH}=2.0V		-48	-30	mA
Supply Current	I_{DD}	Unloaded, 40 MHz		25	50	mA
Output Frequency Change over Supply and Temperature[1]	F_D	With respect to typical frequency		0.002	0.01	%
Input Capacitance[1]	C_I	Except X1, X2			10	pF
Load Capacitance[1]	C_L	Pins X1, X2		20		pF

Notes:
1. Parameter is guaranteed by design and characterization, not subject to production testing.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C

AC Characteristics						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Clock Rise Time[1]	tICr				20	ns
Input Clock Fall Time[1]	tICf				20	ns
Output Rise time[1]	tr	15pF load, 0.8 to 2.0V	-	0.8	2	ns
Rise time[1]	tr	15pF load, 20% to 80% VDD	-	1.4	3	ns
Output Fall time[1]	tf	15pF load, 2.0 to 0.8V	-	0.7	2	ns
Fall time[1]	tf	15pF load, 80% to 20% VDD	-	0.8	2	ns
Duty cycle[1]	dt	15pF load @ 1.4V	45		55	%
Duty cycle, reference clocks[1]	dt	15pF load @ 1.4V	40		60	%
Jitter, one sigma, 32 MHz-100 MHz clocks[1]	tjls			80	120	ps
Jitter, one sigma, 16 MHz-30 MHz clocks[1]	tjls			100	150	ps
Jitter, one sigma, clocks below 16 MHz[1]	tjls			400	500	ps
Jitter, absolute, 32 MHz-100 MHz clocks[1]	tjab		-250		250	ps
Jitter, absolute, 16-30 MHz clock[1]	tjab		-700		700	ps
Jitter, absolute, clocks below 16 MHz[1]	tjab		-2		2	ns
Input Frequency[1]	fin			10.0		MHz
Power-up Time[1]	tPO	to 100 MHz		10	20	ms
Frequency Transition Time[1]	tft	from 25.0 to 40.0 MHz			8	ms

Notes: 1. Parameter is guaranteed by design and characterization, not subject to production testing.

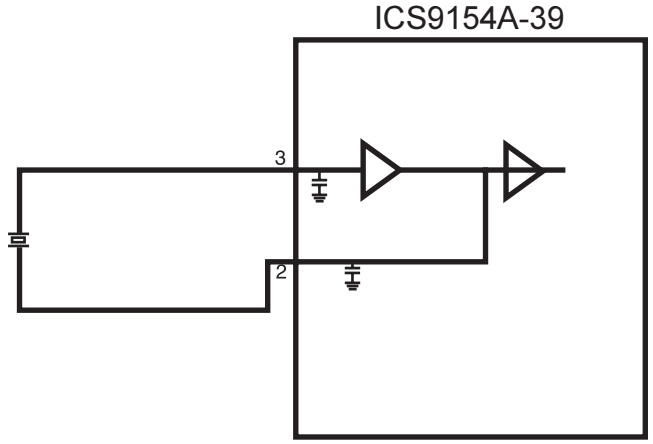
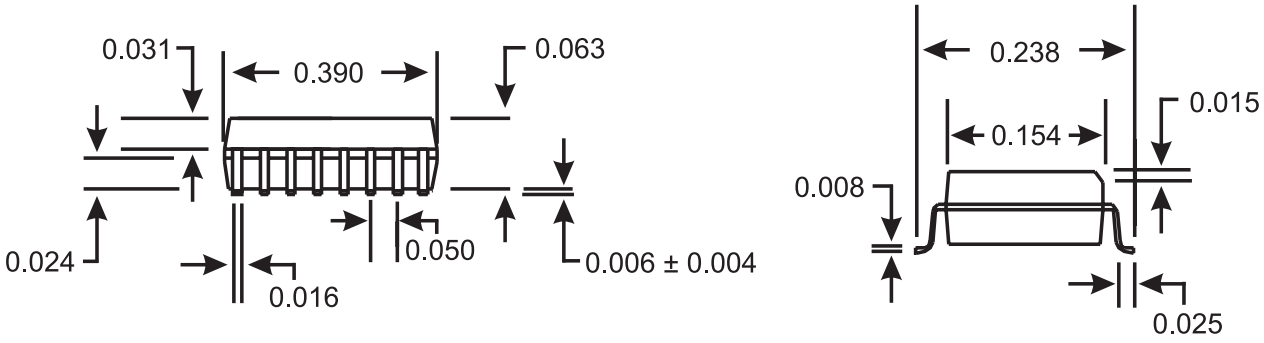


Figure 1: Typical Crystal Circuitry

Note: Crystal load capacitors are internal to the ICS9154A-39 device and no external components are required.



16-Pin SOIC Package

Ordering Information

AV9154A-39CS16

Example:

XXX XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device