International
IOR Rectifier

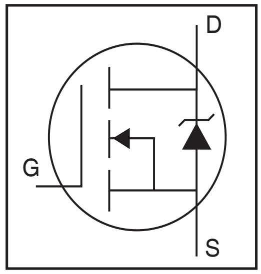
AUTOMOTIVE GRADE

AUIRFB8405

HEXFET® Power MOSFET

Features

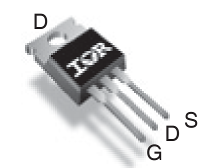
- Advanced Process Technology
- New Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		40V
$R_{DS(on)}$	typ.	2.1mΩ
	max.	2.5mΩ
I_D (Silicon Limited)		185A①
I_D (Package Limited)		120A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.



TO-220AB
AUIRFB8405

G	D	S
Gate	Drain	Source

Applications

- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- DC-DC Applications

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFB8405	TO-220	Tube	50	AUIRFB8405

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	185①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	131①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	120	
I_{DM}	Pulsed Drain Current ②	904	
P_D @T_C = 25°C	Maximum Power Dissipation	163	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf· in (1.1N· m)	

HEXFET® is a registered trademark of International Rectifier.
*Qualification standards can be found at http://www.irf.com/

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	181	mJ
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑩	247	
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 24a, 24b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧⑨	–––	0.92	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	62	

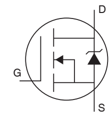
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.026	–––	V/°C	Reference to 25°C, I_D = 1.0mA②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	2.1	2.5	mΩ	V_{GS} = 10V, I_D = 100A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	V_{DS} = V_{GS}, I_D = 100μA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		–––	–––	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	–––	2.3	–––	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	100	–––	–––	S	V_{DS} = 10V, I_D = 100A
Q_g	Total Gate Charge	–––	107	161	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	–––	29	–––		V_{DS} =20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	39	–––		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	–––	68	–––		I_D = 100A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	–––	14	–––	ns	V_{DD} = 26V
t_r	Rise Time	–––	128	–––		I_D = 100A
$t_{d(off)}$	Turn-Off Delay Time	–––	55	–––		R_G = 2.7Ω
t_f	Fall Time	–––	77	–––		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	–––	5193	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	754	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	519	–––		f = 1.0 MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	–––	878	–––		V_{GS} = 0V, V_{DS} = 0V to 32V ⑦, See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	–––	1225	–––		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	185①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	–––	–––	904	A	
V_{SD}	Diode Forward Voltage	–––	0.9	1.3	V	$T_J = 25°C$, $I_S = 100A$, $V_{GS} = 0V$ ⑤
dv/dt	Peak Diode Recovery ④	–––	1.7	–––	V/ns	$T_J = 175°C$, $I_S = 100A$, $V_{DS} = 40V$
t_{rr}	Reverse Recovery Time	–––	44	–––	ns	$T_J = 25°C$ $V_R = 34V$,
		–––	45	–––	ns	$T_J = 125°C$ $I_F = 100A$
Q_{rr}	Reverse Recovery Charge	–––	44	–––	nC	$T_J = 25°C$ di/dt = 100A/μs ⑤
		–––	46	–––	nC	$T_J = 125°C$
I_{RRM}	Reverse Recovery Current	–––	1.9	–––	A	$T_J = 25°C$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting $T_J = 25°C$, L = 0.036mH, $R_G = 50\Omega$, $I_{AS} = 100A$, $V_{GS} = 10V$. Part not recommended for use above this value.

④ $I_{SD} \le 100A$, di/dt $\le$ 1295A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 175°C$.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

⑨ $R_{\theta JC}$ value shown is at time zero.

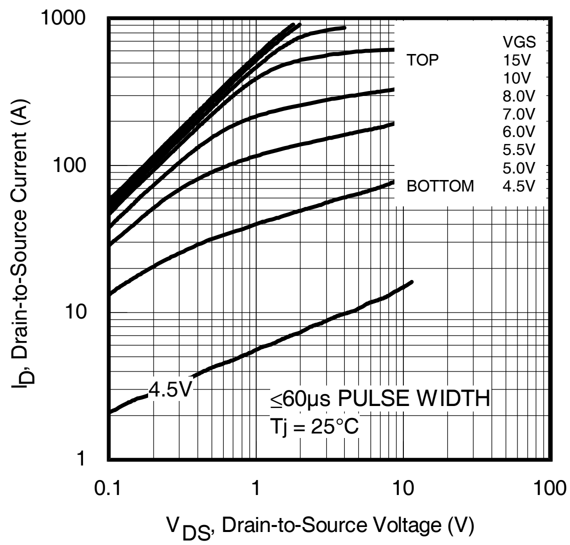


Fig 1. Typical Output Characteristics

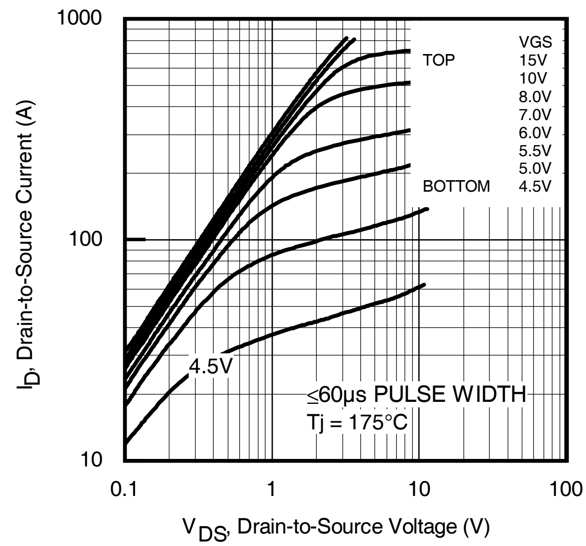


Fig 2. Typical Output Characteristics

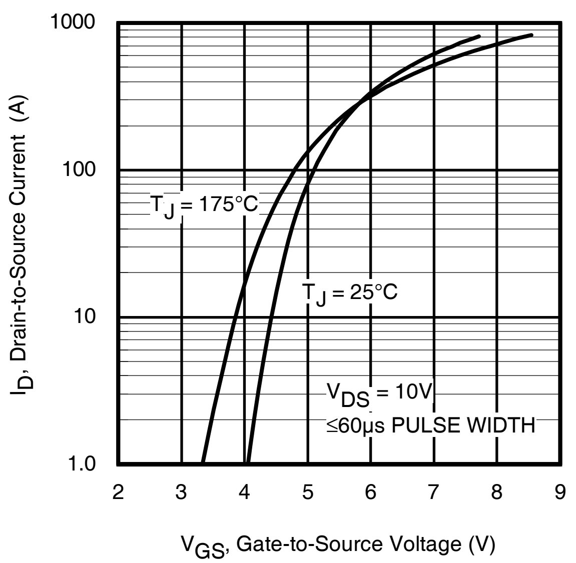


Fig 3. Typical Transfer Characteristics

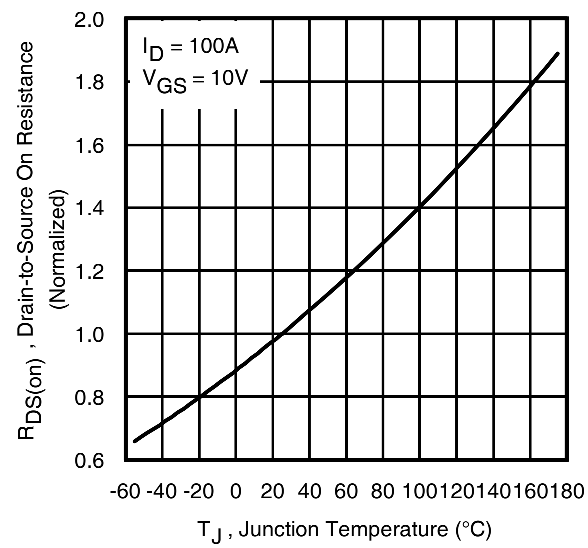


Fig 4. Normalized On-Resistance vs. Temperature

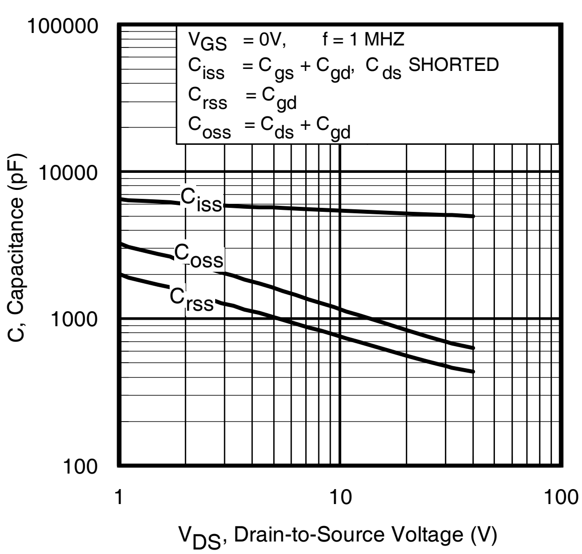


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

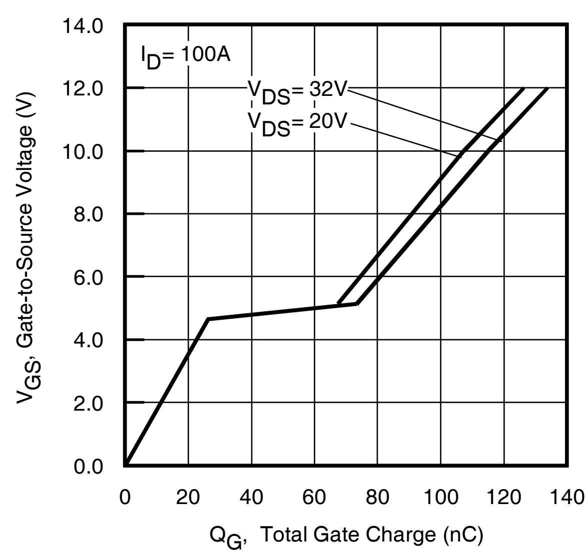


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

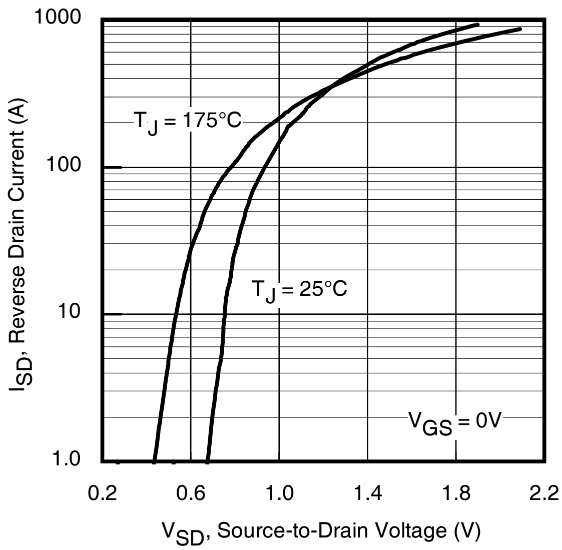


Fig 7. Typical Source-Drain Diode Forward Voltage

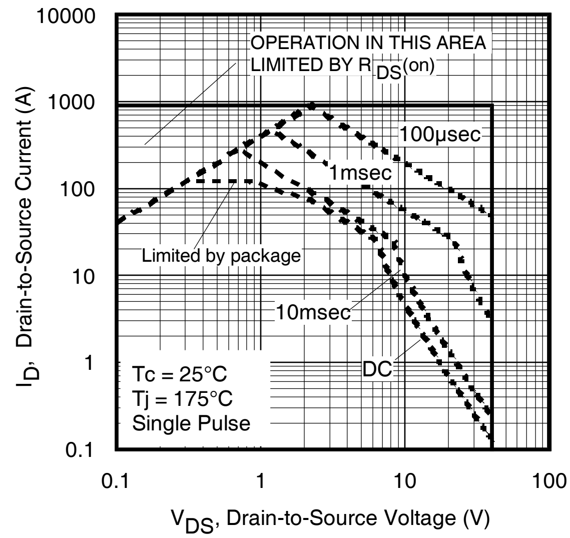


Fig 8. Maximum Safe Operating Area

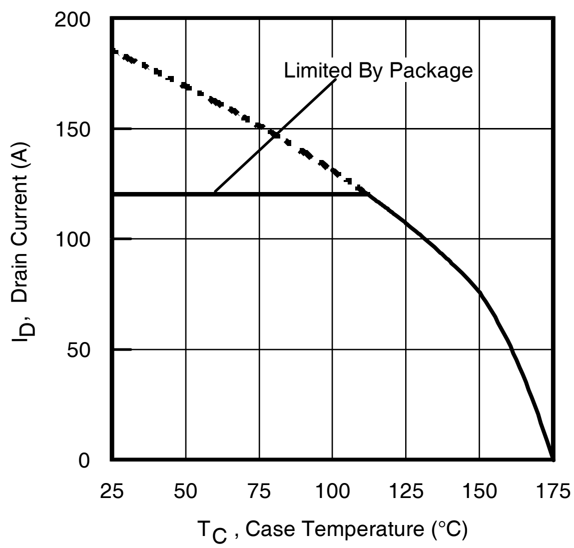


Fig 9. Maximum Drain Current vs. Case Temperature

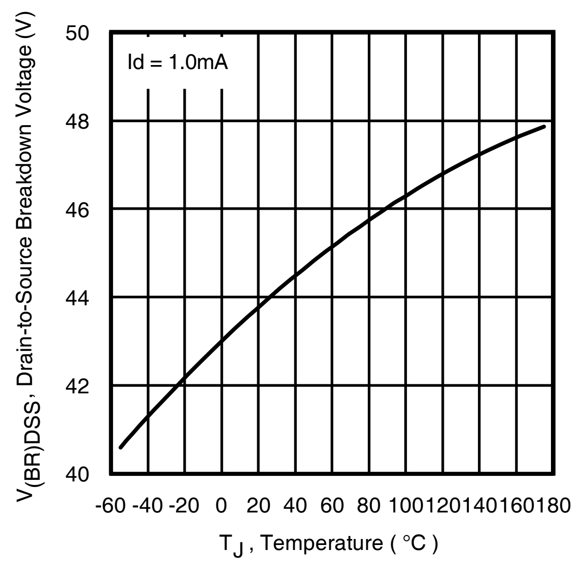


Fig 10. Drain-to-Source Breakdown Voltage

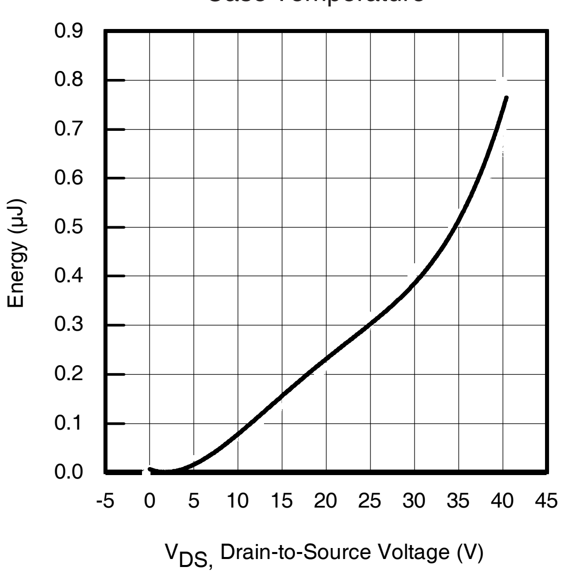


Fig 11. Typical C_{OSS} Stored Energy

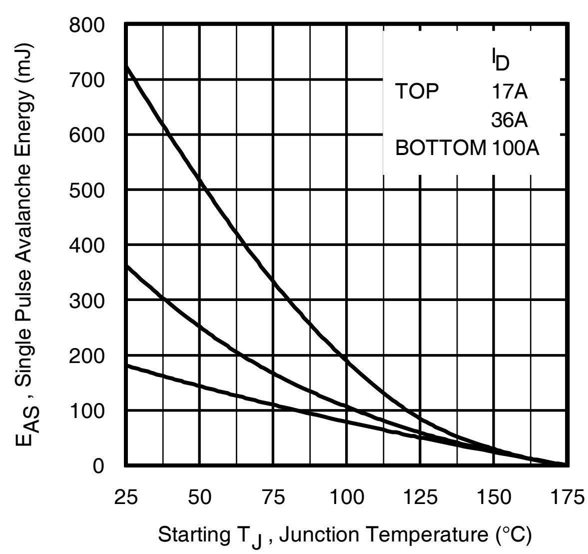


Fig 12. Maximum Avalanche Energy vs. DrainCurrent

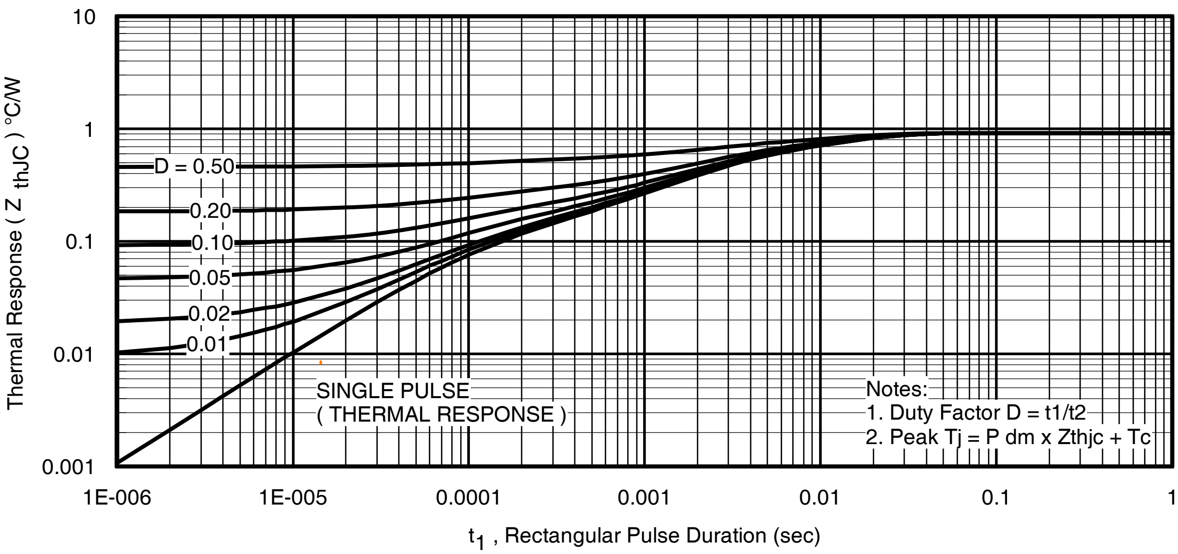


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

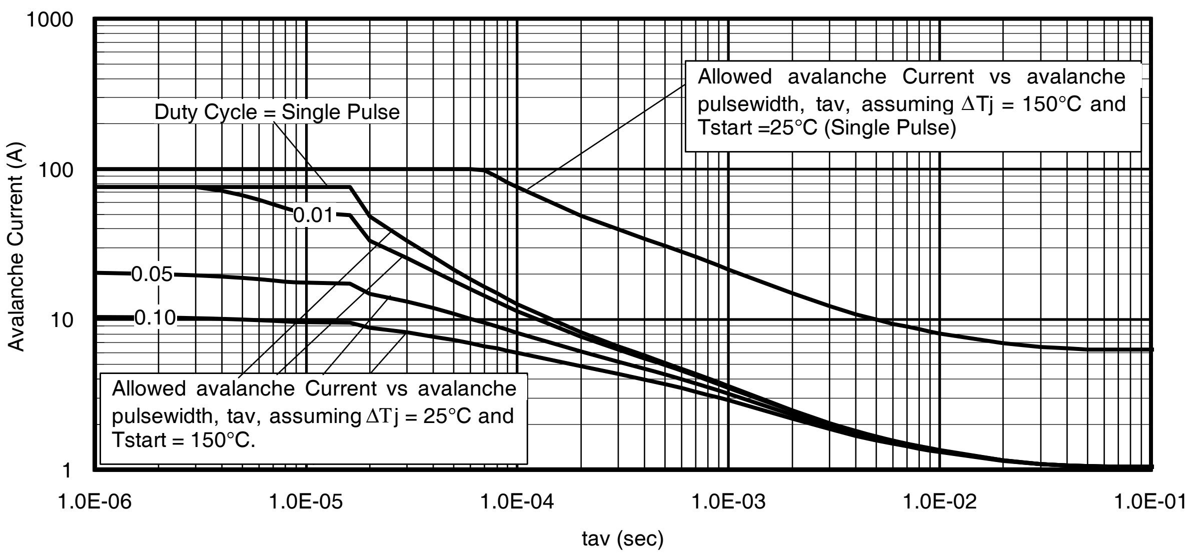


Fig 14. Typical Avalanche Current vs.Pulsewidth

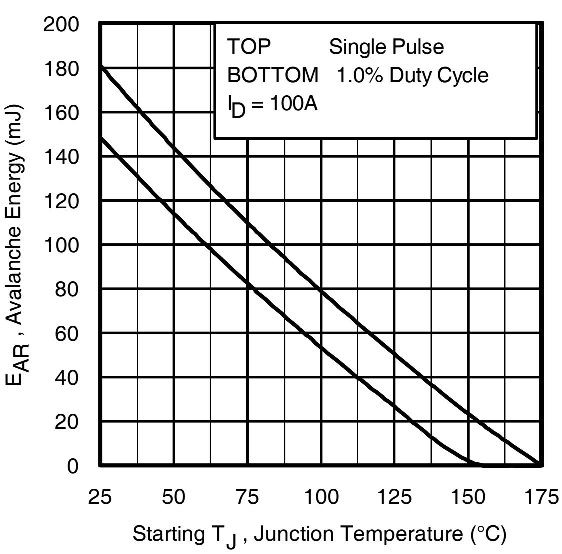


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24a, 24b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

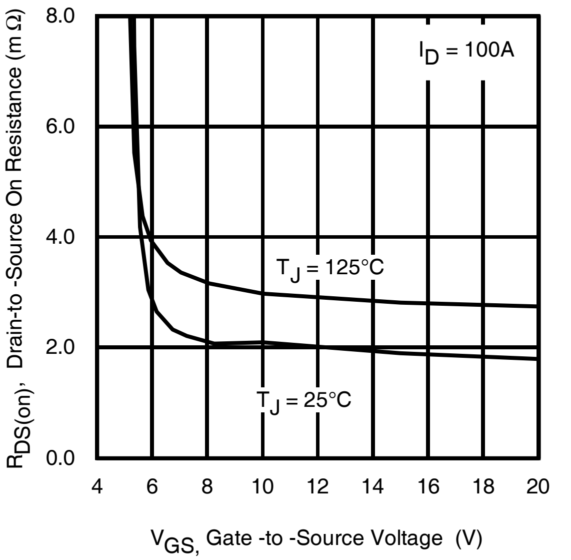


Fig 16. On-Resistance vs. Gate Voltage

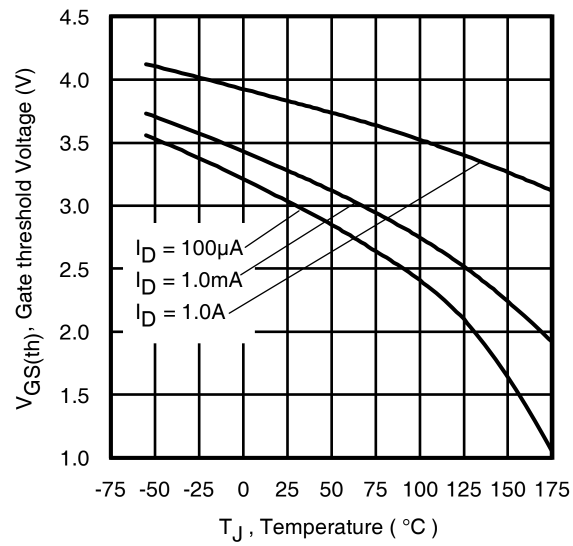


Fig 17. Threshold Voltage vs. Temperature

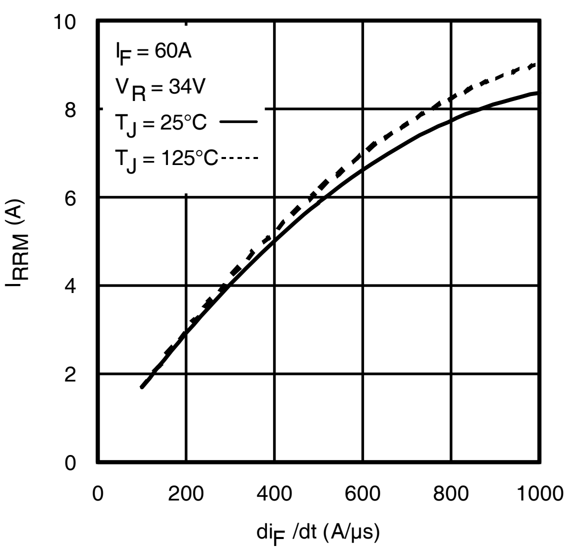


Fig. 18 - Typical Recovery Current vs. di_f/dt

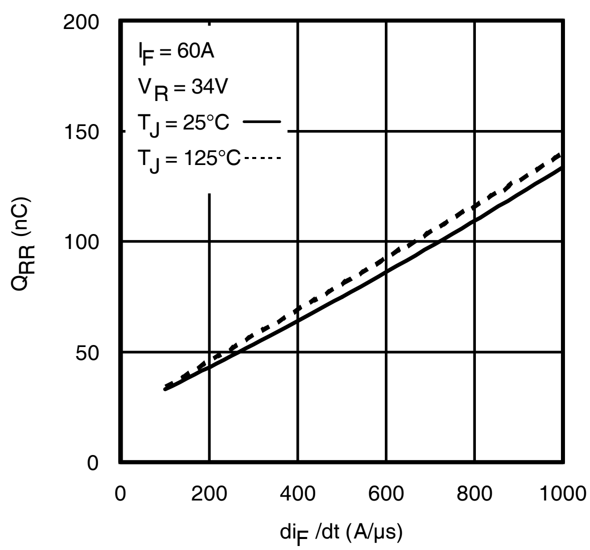


Fig. 19 - Typical Stored Charge vs. di_f/dt

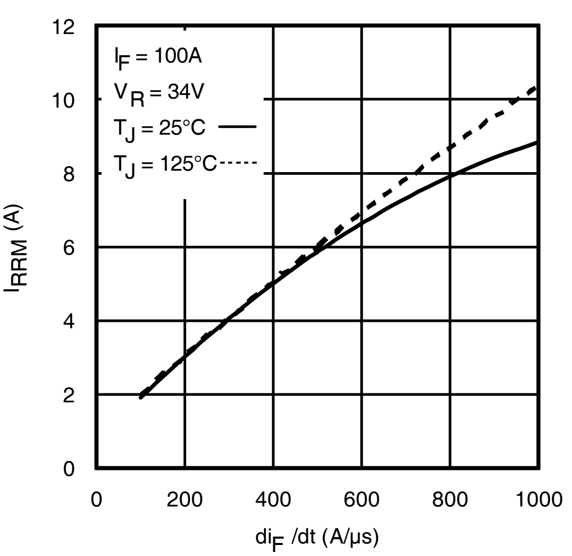


Fig. 20 - Typical Recovery Current vs. di_f/dt

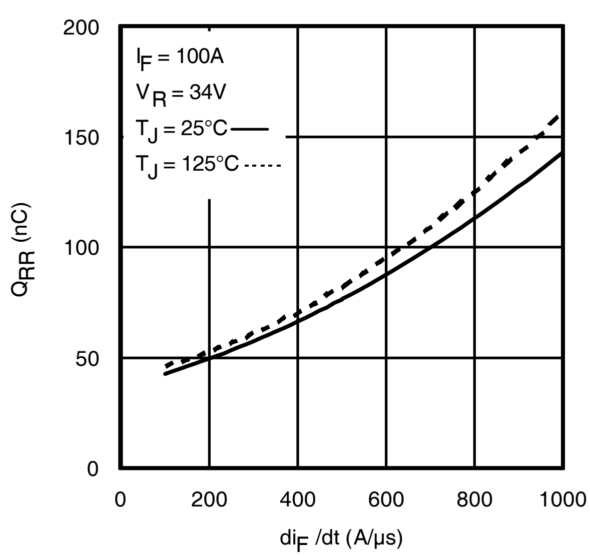


Fig. 21 - Typical Stored Charge vs. di_f/dt

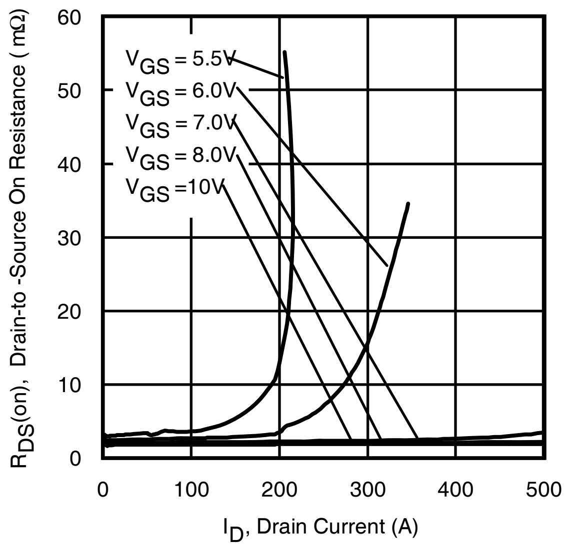


Fig 22. Typical On-Resistance vs. Drain Current

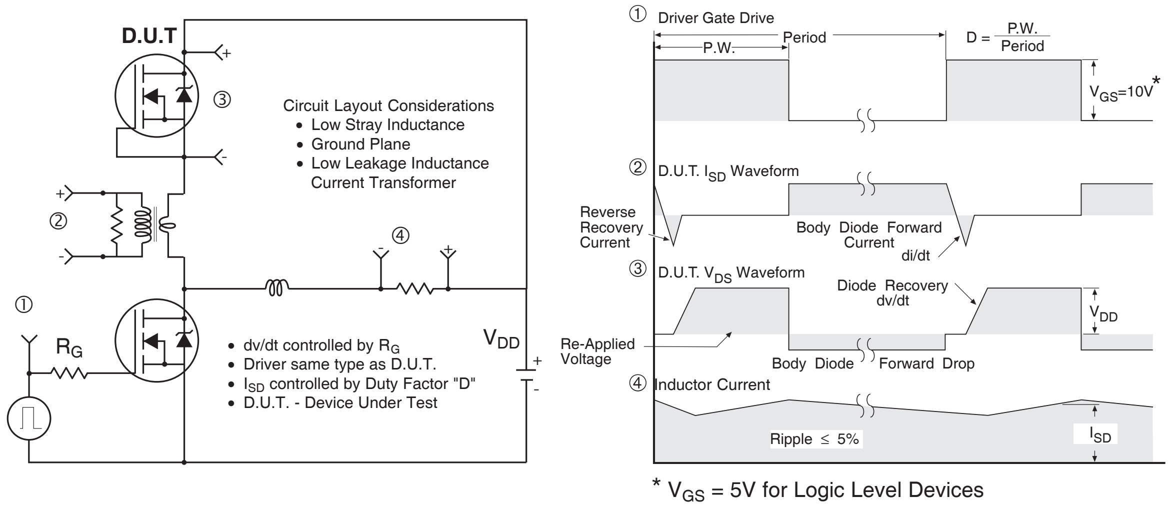


Fig 23. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

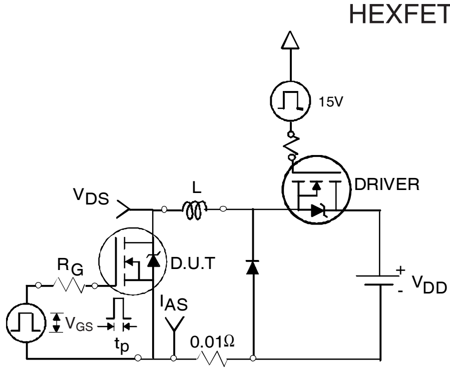


Fig 24a. Unclamped Inductive Test Circuit

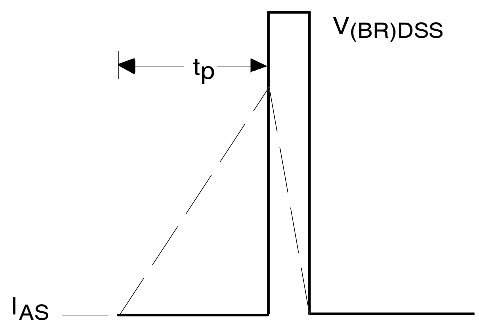


Fig 24b. Unclamped Inductive Waveforms

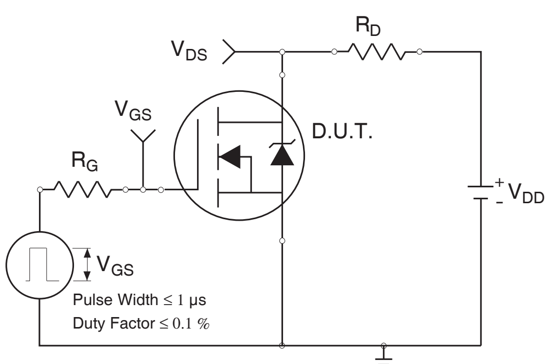


Fig 25a. Switching Time Test Circuit

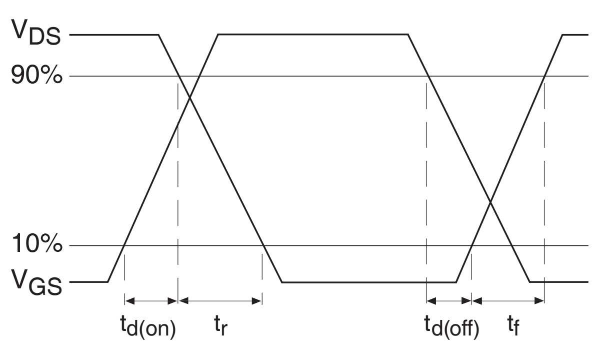


Fig 25b. Switching Time Waveforms

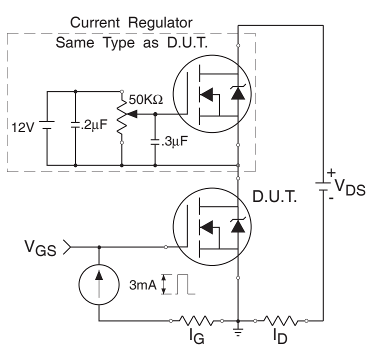


Fig 26a. Gate Charge Test Circuit

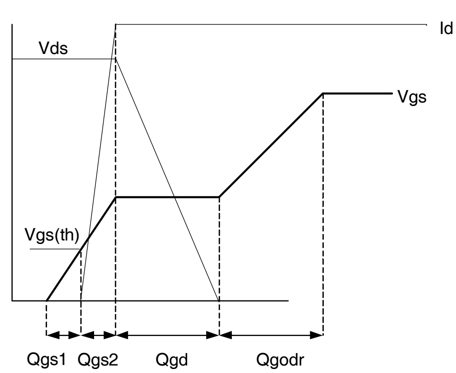
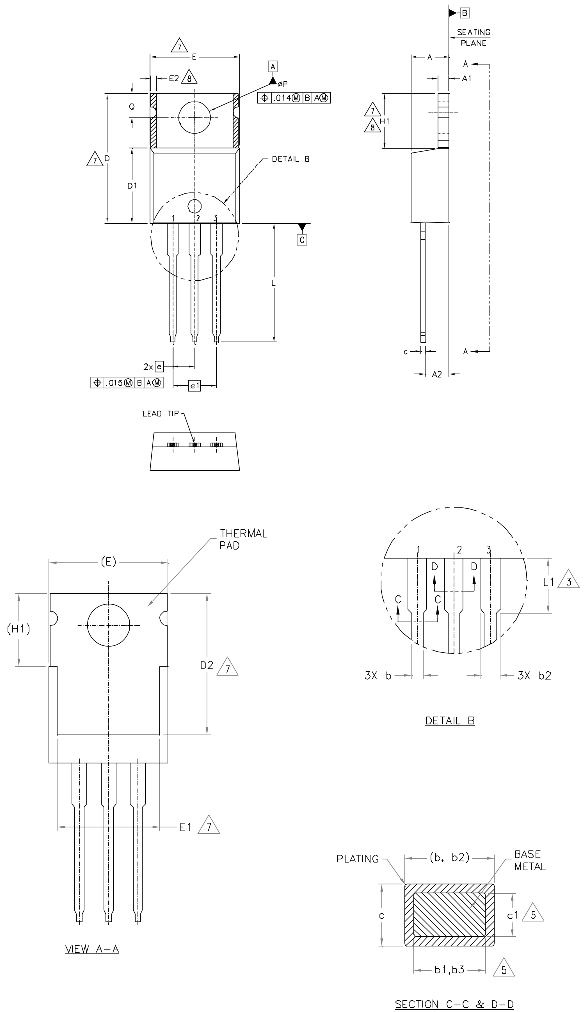


Fig 26b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO–220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE

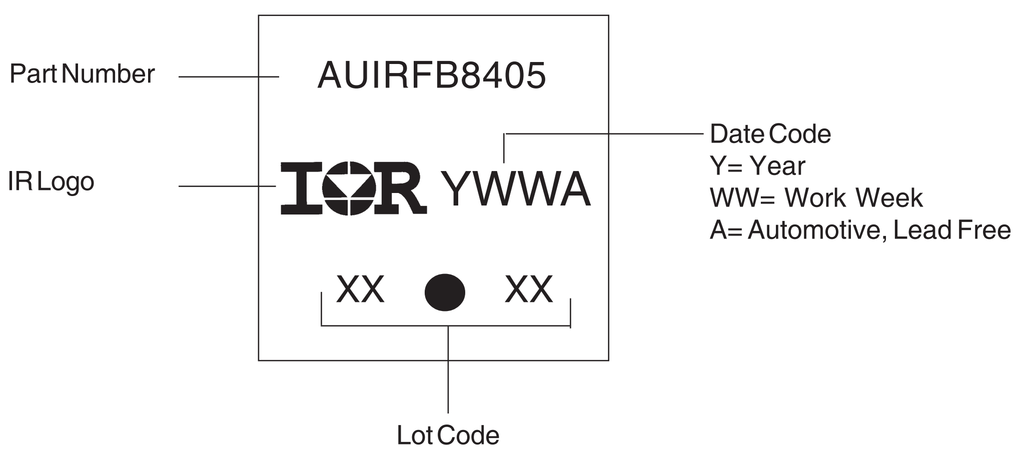
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE
2.– CATHODE
3.– ANODE

TO-220AB Part Marking Information



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
		TO-220	N/A
ESD	Machine Model	Class M3 (+/- 400V)†† AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V)†† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)†† AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Highest passing voltage.

IMPORTANT NOTICE

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