



AU9228

USB KVM Controller

Technical Reference Manual



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1. Introduction

1.1 Description

AU9228 is a highly integrated single chip USB KVM controller offering users the possibility of sharing keyboard, mouse and monitor among up to four PCs. Not like traditional PS2 KVM devices, AU9228 uses USB as its upstream and downstream interface to support its driver-free and plug-n-play features, which allow users to easily install and use the KVM.

Typical application of AU9228 is under an environment, in which only one set of monitor, keyboard and mouse is available. Applying such kind of devices in a computing environment will not only result in a centralized control, but also reduce the power and space consumption.

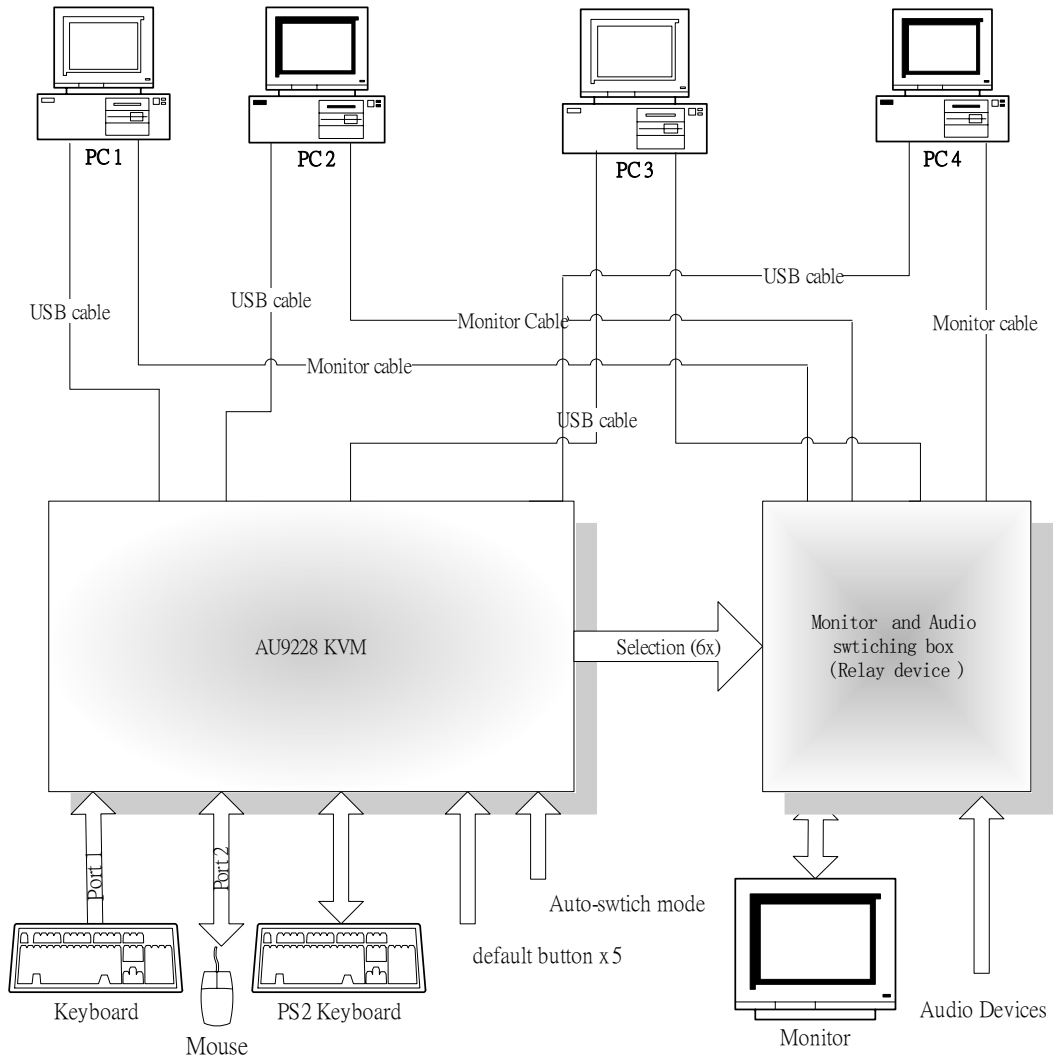
1.2 Features

- Fully USB v1.1 specification compliant
- Support USB bus power and device self power
- Support up to 4 PCs via 4 USB upstream ports
- Support USB downstream port 1 for USB keyboard
- Support USB downstream port 2 for USB mouse
- Support PS2 keyboard
- Support both “panel button” and “hot key” to switch among PCs
- Support “auto-scan” mode for users to monitor PCs easily
- Support audio beep when system switches
- Support upstream port selected LED indicators for each PC respectively
- Support phantom keyboard to let user does not need to configure BIOS to turn on “No halt on error”
- Support 4 different sets of key sequence to switch among PCs (Please see the key definition in the following)
- Recalls “Caps Lock”, “Num Lock” and “Scroll Lock” keys’ status for each PC automatically
- Output the monitor selection signals to the external video-switching circuits
- Support 8-bit MCU interface to provide control from external MCU
- Support serial MCU interface to provide control from external MCU
- No need to install device driver under Windows, Macintosh, Linux, FreeBSD and Sun system

2. Application Block Diagram

Typical application is in a computing environment where it demands a centralized control and space & energy saving is critical.

Figure 2.1 Block Diagram



3. Pin Assignment

The AU9228 is delivered in 64pin LQFP form factor. Documented below is a figure shows signal names of each pin and a table in the following page describes each pin in more details.

Figure 3.1 Pin Assignment Diagram

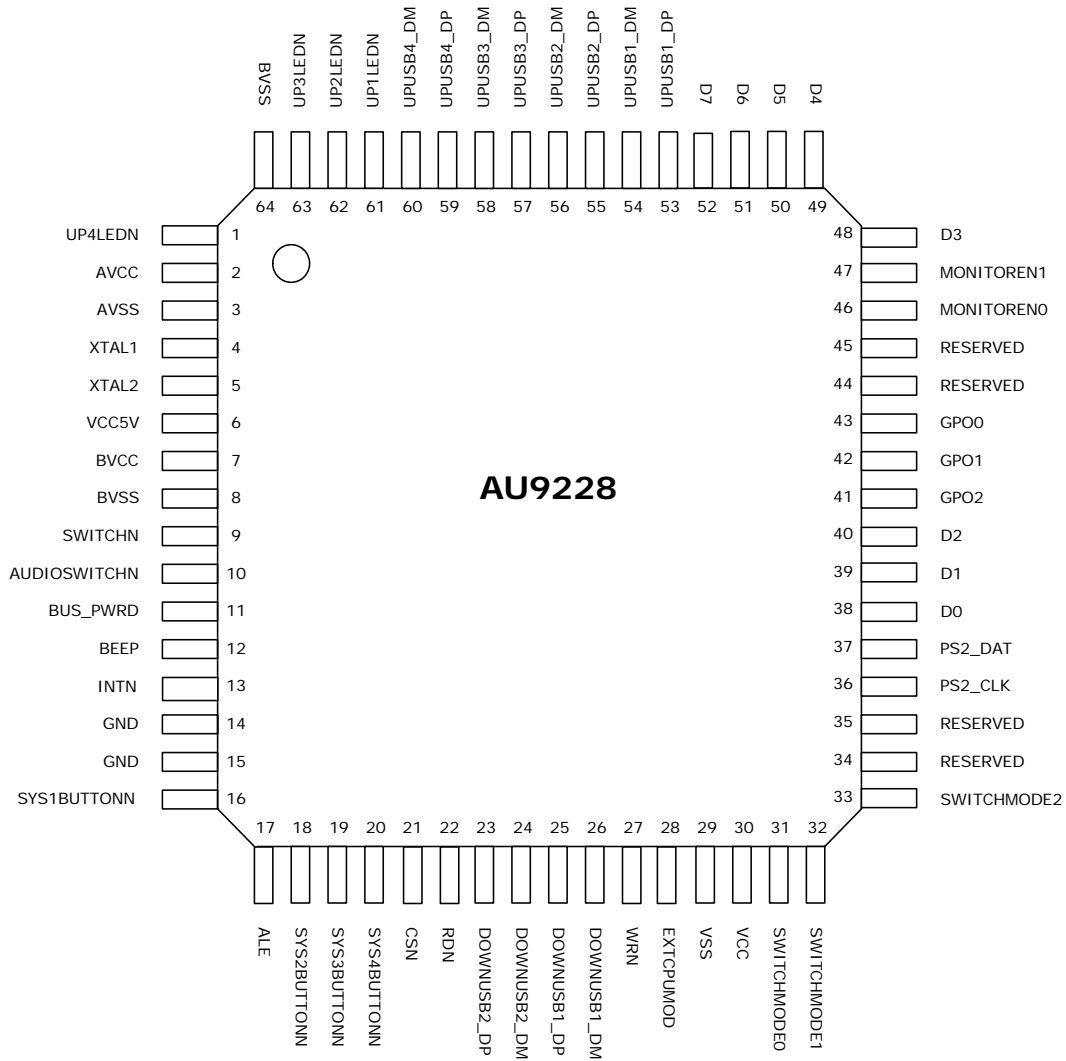


Table 3.1 Pin Descriptions

| Pin # | Pin Name | I/O | Description |
|-------|--------------|-----|---|
| 1 | UP4LEDN | O | System 4 LED indicator (0:ON; 1:OFF) |
| 2 | AVCC | PWR | 3.3V analog input power |
| 3 | AVSS | PWR | Analog ground |
| 4 | XTAL1 | I | 12 MHz crystal input |
| 5 | XTAL2 | O | 12 MHz crystal output |
| 6 | VCC5V | PWR | 5.0V input power from USB port |
| 7 | BVCC | PWR | 3.3V output power from internal regulator |
| 8 | BVSS | PWR | Ground pin of internal regulator |
| 9 | SWITCHN | I | Button with internal pull-up for switching to next system (0: Enable; 1: Normal) |
| 10 | AUDIOSWITCHN | I | Audio ON/OFF switch with internal pull-up (1: OFF; 0: ON) |
| 11 | BUS_PWRD | I | Bus power selection (1: Device Self Power; 0: Bus Power) |
| 12 | BEEP | O | Audio output (4 KHz frequency) when system switches |
| 13 | INTN | O | Interrupt signal output to external MCU when SWITCHMODE2='1' and EXTCPUMOD='1' (falling-edge triggered) |
| 14 | GND | | Ground |
| 15 | GND | | Ground |
| 16 | SYS1BUTTONN | I | Panel button with internal pull-up for enabling system 1 (0: Enable; 1: Normal) |
| 17 | ALE | I | When not using external parallel MCU, it should be pulled down. Address latch enable when SWITCHMODE2='1' and EXTCPUMOD='1' (1: AD bus is address; 0: AD bus is data) |
| 18 | SYS2BUTTONN | I | Panel button with internal pull-up for enabling system 2 (0: Enable; 1: Normal) |
| 19 | SYS3BUTTONN | I | Panel button with internal pull-up for enabling system 3 (0: Enable; 1: Normal) |
| 20 | SYS4BUTTONN | I | Panel button with internal pull-up for enabling system 4 (0: Enable; 1: Normal) |
| 21 | CSN | I | Chip enable for the MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1' (0: Enable) |
| 22 | RDN | I | Read strobe for the MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1' (0: Enable) |
| 23 | DOWNUSB2_DP | I/O | DownPort2 DP |

| Pin # | Pin Name | I/O | Description |
|-------|-------------|-----|--|
| 24 | DOWNUSB2_DM | I/O | DownPort2 DM |
| 25 | DOWNUSB1_DP | I/O | DownPort1 DP |
| 26 | DOWNUSB1_DM | I/O | DownPort1 DM |
| 27 | WRN | I | Read strobe for the MCU interface when SWITCHMODE2='1' and EXTCPUMOD ='1' (0: Enable; 1: Normal) |
| 28 | EXTCPUMOD | I | External MCU mode selection (1: Parallel; 0: Serial). Serial is the default mode. |
| 29 | VSS | PWR | Digital ground |
| 30 | VCC | PWR | 3.3V digital input power |
| 31 | SWITCHMODE0 | I | Switch mode selection (SW0, SW1) for internal hotkey mode when SWITCHMODE2='0' and D2='0', it's defined as: (0, 0): [Scroll][Scroll] mode (default) (0, 1): [Caps Lock][Caps Lock] mode (1, 0): [Num Lock][Num Lock] mode (1, 1): [Ctrl][Shift] mode (left-hand side) |
| 32 | SWITCHMODE1 | I | |
| 33 | SWITCHMODE2 | I | Enable external MCU mode (1: Enable; 0: Disable). Disable is the default setting. |
| 34 | RESERVED | | Reserved |
| 35 | RESERVED | | Reserved |
| 36 | PS2_CLK | I/O | PS2 clock signal (external pull-up required) |
| 37 | PS2_DAT | I/O | PS2 data signal (external pull-up required) |
| 38 | D0 | I/O | Bit 0 with internal pull-up in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1'. It also provides alternative functions: I2C bus SDA signal (slave mode) when SWITCHMODE2='1' and EXTCPUMOD='0' I2C bus SDA signal (master mode) when SWITCHMODE2='0' and D2='1' |
| 39 | D1 | I/O | Bit 1 with internal pull-up in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1'. It also provides alternative functions: I2C bus SCL signal (slave mode) when SWITCHMODE2='1' and EXTCPUMOD='0' I2C bus SCL signal (master mode) when SWITCHMODE2='0' and D2='1' |
| 40 | D2 | I/O | Bit 2 with internal pull-down in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1'. It also provides alternative functions: I2C bus address 0 (slave mode) when SWITCHMODE2='1' and EXTCPUMOD='0' I2C bus master mode enable bit when SWITCHMODE2='0' |

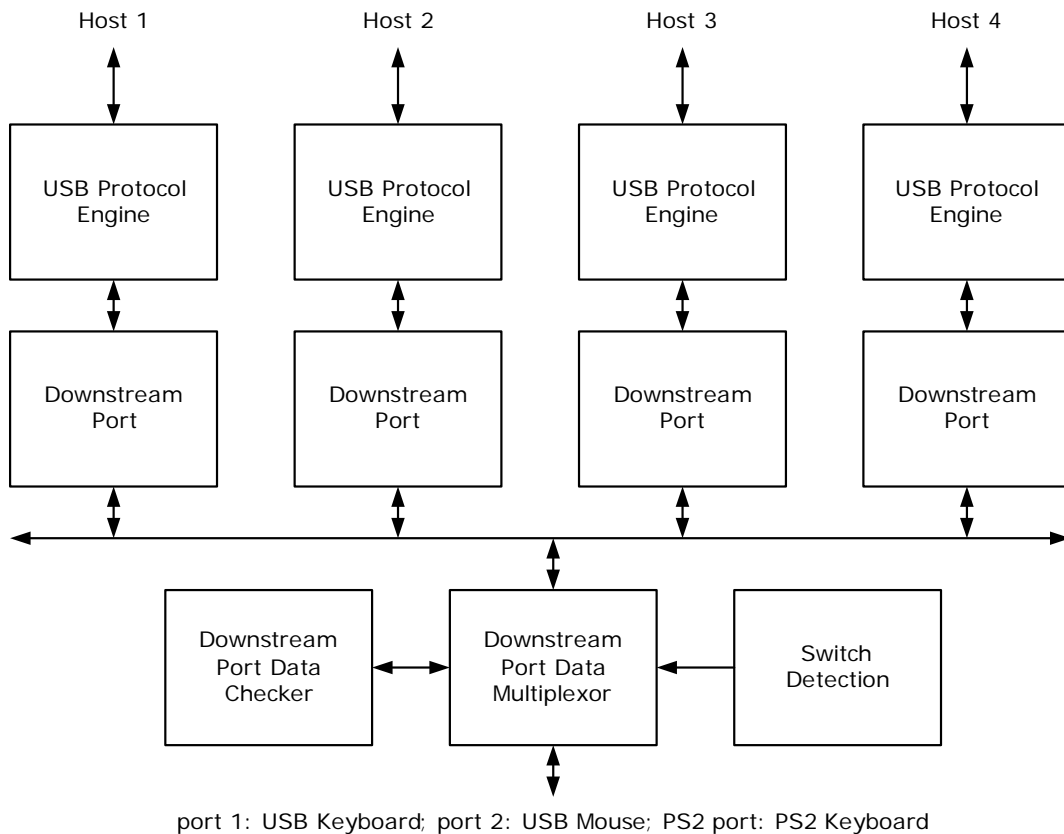
| Pin # | Pin Name | I/O | Description |
|-------|------------|-----|--|
| 41 | GPO2 | O | General purpose output pin 2 |
| 42 | GPO1 | O | General purpose output pin 1 |
| 43 | GPO0 | O | General purpose output pin 0 |
| 44 | RESERVED | | Reserved |
| 45 | RESERVED | | Reserved |
| 46 | MONITOREN0 | O | Monitor selection (MON0, MON1): (0, 0) : monitor 1 select (1, 0) : monitor 2 select (0, 1) : monitor 3 select (1, 1) : monitor 4 select |
| 47 | MONITOREN1 | O | |
| 48 | D3 | I/O | Bit 3 with internal pull-down in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1'. It also provides alternative function: I2C bus address 1 (slave mode) when SWITCHMODE2='1' and EXTCPUMOD='0' |
| 49 | D4 | I/O | Bit 4 with internal pull-down in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1'. It also provides alternative function: I2C bus address 2 (slave mode) when SWITCHMODE2='1' and EXTCPUMOD='0' |
| 50 | D5 | I/O | Bit 5 with internal pull-down in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1' |
| 51 | D6 | I/O | Bit 6 with internal pull-down in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1' |
| 52 | D7 | I/O | Bit 5 with internal pull-down in address/data bus of MCU interface when SWITCHMODE2='1' and EXTCPUMOD='1' |
| 53 | UPUSB1_DP | I/O | Upstream port 1 DP |
| 54 | UPUSB1_DM | I/O | Upstream port 1 DM |
| 55 | UPUSB2_DP | I/O | Upstream port 2 DP |
| 56 | UPUSB2_DM | I/O | Upstream port 2 DM |
| 57 | UPUSB3_DP | I/O | Upstream port 3 DP |
| 58 | UPUSB3_DM | I/O | Upstream port 3 DM |
| 59 | UPUSB4_DP | I/O | Upstream port 4 DP |
| 60 | UPUSB4_DM | I/O | Upstream port 4 DM |
| 61 | UP1LEDN | O | System 1 LED indicator (0:ON; 1:OFF) |
| 62 | UP2LEDN | O | System 2 LED indicator (0:ON; 1:OFF) |

| Pin # | Pin Name | I/O | Description |
|-------|----------|-----|--------------------------------------|
| 63 | UP3LEDN | O | System 3 LED indicator (0:ON; 1:OFF) |
| 64 | BVSS | PWR | Ground pin of internal regulator |

4. System Architecture and Reference Design

4.1 AU9228 Block Diagram

Figure 4.1 AU9228 Block Diagram



5. Hot Key Definition

AU9228 supports 4 sets of “Hot Key” to help users to switch PC, rapidly and easily, via hot key sequence defined using keypads on the left hand side of a keyboard.

5.1 [Scroll] ++ [Scroll] mode

| Hot Key Definition | |
|---|---|
| [Scroll] ++ [Scroll] + 1 (note1) | Switch to PC1 |
| [Scroll] ++ [Scroll] + 2 | Switch to PC2 |
| [Scroll] ++ [Scroll] + 3 | Switch to PC3 |
| [Scroll] ++ [Scroll] + 4 | Switch to PC4 |
| [Scroll] ++ [Scroll] + → or ↓ | Switch to Next PC |
| [Scroll] ++ [Scroll] + ← or ↑ | Switch to Previous PC |
| [Scroll] ++ [Scroll] + B | Beeper ON/OFF (note2) |
| [Scroll] ++ [Scroll] + S | Auto-scan mode every 10 second. ([ESC] switch to regular key code) |
| [Scroll] ++ [Scroll] + S + n | Set Auto-scan rate (note3). ([ESC] switch to regular key code) |
| [Scroll]++[Scroll]+F1~F8 | Customer define key (note4). |
| [Scroll]++[Scroll]+[Caps] | Switch to [Caps]++[Caps] hot key mode |
| [Scroll]++[Scroll]+[Num] | Switch to [Num]++[Num] hot key mode |
| [Scroll]++[Scroll]+[Ctrl] | Switch to [Ctrl]+[Shift] hot key mode |

5.2 [Caps] ++ [Caps] mode

| Hot Key Definition | |
|-------------------------|---|
| [Caps]++[Caps]+1 | Switch to PC1 |
| [Caps]++[Caps]+2 | Switch to PC2 |
| [Caps] ++ [Caps] + 3 | Switch to PC3 |
| [Caps] ++ [Caps] + 4 | Switch to PC4 |
| [Caps]++[Caps]+ → or ↓ | Switch to Next PC |
| [Caps]++[Caps]+← or ↑ | Switch to Previous PC |
| [Caps]++[Caps]+B | Beeper ON/OFF (note2) |
| [Caps]++[Caps]+S | Auto-scan mode every 10 second. ([ESC] switch to regular key code) |
| [Caps]++[Caps]+S + n | Set Auto-scan rate (note3). ([ESC] switch to regular key code) |
| [Caps]++[Caps]+F1~F8 | Customer define key (note4) |
| [Caps]++[Caps]+[Scroll] | Switch to [Scroll]++[Scroll] hot key mode |
| [Caps]++[Caps]+[Num] | Switch to [Num]++[Num] hot key mode |
| [Caps]++[Caps]+[Ctrl] | Switch to [Ctrl]+[Shift] hot key mode |

5.3 [Num] ++ [Num] Mode

| Hot Key Definition | |
|-----------------------|---|
| [Num]++[Num]+1 | Switch to PC1 |
| [Num]++[Num]+2 | Switch to PC2 |
| [Num] ++ [Num] + 3 | Switch to PC3 |
| [Num] ++ [Num] + 4 | Switch to PC4 |
| [Num]++[Num]+→ or ↓ | Switch to Next PC |
| [Num]++[Num]+← or ↑ | Switch to Previous PC |
| [Num]++[Num]+B | Beeper ON/OFF (note2) |
| [Num]++[Num]+S | Auto-scan mode every 10 second. ([ESC] switch to regular key code) |
| [Num]++[Num]+S + n | Set Auto-scan rate (note3). ([ESC] switch to regular key code) |
| [Num]++[Num]+F1~F8 | Customer define key (note4) |
| [Num]++[Num]+[Scroll] | Switch to [Scroll]++[Scroll] hot key mode |
| [Num]++[Num]+[Caps] | Switch to [Caps]++[Caps] hot key mode |
| [Num]++[Num]+[Ctrl] | Switch to [Ctrl]+[Shift] hot key mode |

5.4 [Ctrl] + [Shift] mode (left-hand side)

| Hot Key Definition | |
|-------------------------|---|
| [Ctrl]++[Ctrl] | Switch to next live PC |
| [Ctrl + Shift + 1] | Switch to PC1 |
| [Ctrl + Shift + 2] | Switch to PC2 |
| [Ctrl + Shift + 3] | Switch to PC3 |
| [Ctrl + Shift + 4] | Switch to PC4 |
| [Ctrl + Shift + → or ↓] | Switch to Next PC |
| [Ctrl + Shift + ← or ↑] | Switch to Previous PC |
| [Ctrl + Shift + B] | Beeper ON/OFF (note2) |
| [Ctrl + Shift + S] | Auto-scan mode every 10 second. ([ESC] switch to regular key code) |
| [Ctrl + Shift + S + n] | Set Auto-scan rate (note3). ([ESC] switch to regular key code) |
| [Ctrl + Shift + F1~F8] | Customer define key (note4) |
| [Ctrl + Shift + Scroll] | Switch to [Scroll]++[Scroll] hot key mode |
| [Ctrl + Shift + Caps] | Switch to [Caps]++[Caps] hot key mode |
| [Ctrl + Shift + Num] | Switch to [Num]++[Num] hot key mode |

Note 1: “++” means press key rapidly, “[Scroll]++[Scroll]+1” means press “Scroll” twice rapidly and then press “1”. If system receives “Scroll ++ Scroll” command only, system will reset the buffer when it does not receive any input comes after within a defined interval of time (say, 5 seconds).

Note 2: Audible feedback when beeper is ON and keep the device in silent mode when beeper is OFF.

Note 3: n = number from 1 to 9, each represents 5 seconds' interval latency to 60 seconds correspondingly.

| Auto-scan rate set | |
|--------------------|--------|
| 【N】 number | Second |
| 1 | 5 |
| 2 | 10 |
| 3 | 15 |
| 4 | 20 |
| 5 | 25 |
| 6 | 30 |
| 7 | 35 |
| 8 | 40 |
| 9 | 60 |

Note 4:

| | GPO 2 | GPO 1 | GPO 0 |
|------------------|-------|-------|-------|
| Function key +F1 | 0 | 0 | 0 |
| Function key +F2 | 0 | 0 | 1 |
| Function key +F3 | 0 | 1 | 0 |
| Function key +F4 | 0 | 1 | 1 |
| Function key +F5 | 1 | 0 | 0 |
| Function key +F6 | 1 | 0 | 1 |
| Function key +F7 | 1 | 1 | 0 |
| Function key +F8 | 1 | 1 | 1 |

6. Electrical Characteristics

6.1 Recommended Operating Conditions

Table 6.1 Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|------------------|-----------------------|------|-----|-----------------|-------|
| V _{CC} | Power Supply | 4.75 | 5 | 5.25 | V |
| V _{IN} | Input Voltage | 0 | | V _{CC} | V |
| T _{ORP} | Operating Temperature | 0 | | 85 | OC |
| T _{STG} | Storage Temperature | -40 | | 125 | OC |

6.2 General DC Characteristics

Table 6.2 General DC Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------|-----------------------------------|-------------------------|-----|-----|-----|-------|
| I _{IL} | Input low current | no pull-up or pull-down | -1 | | 1 | μA |
| I _{IH} | Input high current | no pull-up or pull-down | -1 | | 1 | μA |
| O _Z | Tri-state leakage current | | -10 | | 10 | μA |
| C _{IN} | Input capacitance | | | 5 | | ρF |
| C _{OUT} | Output capacitance | | | 5 | | ρF |
| C _{BID} | Bi-directional buffer capacitance | | | 5 | | ρF |

6.3 DC Electrical Characteristics of 3.3V I/O Cells

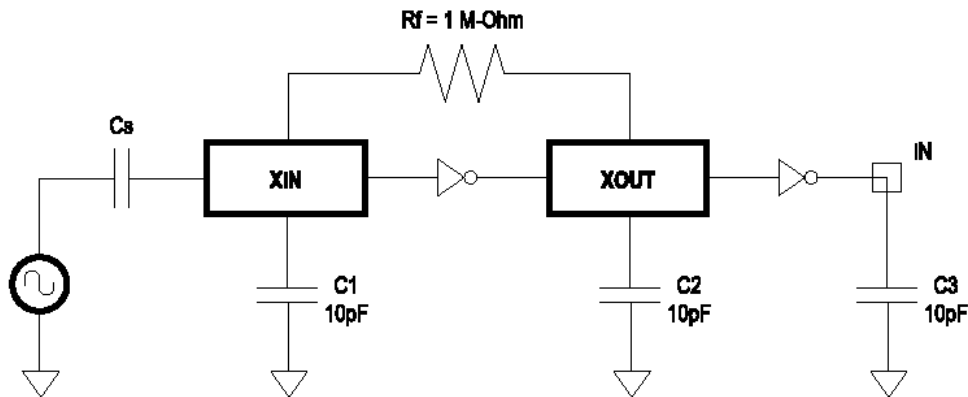
Table 6.3 DC Electrical Characteristics of 3.3V I/O Cells

| SYMBOL | PARAMETER | CONDITIONS | Limits | | | UNIT |
|-----------------|-------------------------------|-------------------|--------|----------|-----|------|
| | | | MIN | TYP | MAX | |
| V _{IL} | Input Low Voltage | CMOS | | | 0.9 | V |
| V _{IH} | Input High Voltage | CMOS | 2.3 | | | V |
| V _{OL} | Output low voltage | IOL=4mA, 16mA | | | 0.4 | V |
| V _{OH} | Output high voltage | IOH=4mA, 16mA | 2.4 | | | V |
| R _I | Input Pull-up/down resistance | Vil=0V or Vih=VCC | | 10k/200k | | KΩ |

6.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, C_s , is much larger than C_1 and C_2 .

Figure 6.1 Crystal Oscillator Circuit Setup for Characterization



6.5 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

- Zap Interval : 1 second
- Number of Zaps : 3 positive and 3 negative at room temperature
- Criteria : I-V Curve Tracing

Table 6.4 ESD Data

| Model | Model | S/S | TARGET | Results |
|-------|---------------|-----|--------|---------|
| HBM | Vdd, Vss, I/C | 15 | 2000V | TBD |
| MM | Vdd, Vss, I/C | 15 | 200V | TBD |

6.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.

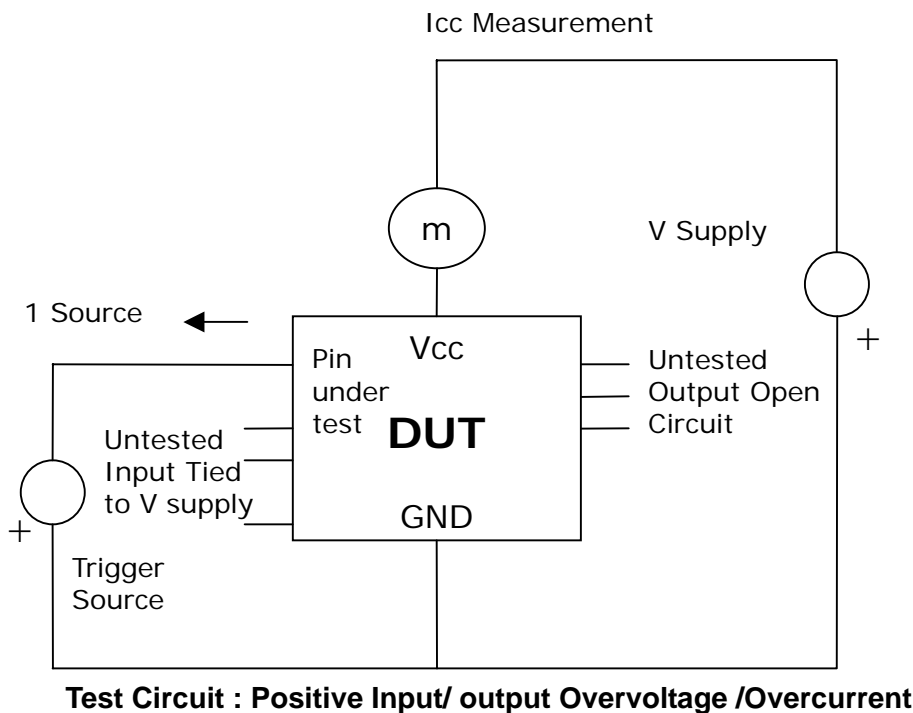
Testing was started at 5.0 V (Positive) or 0 V (Negative), and the DUT was biased for 0.5 seconds.

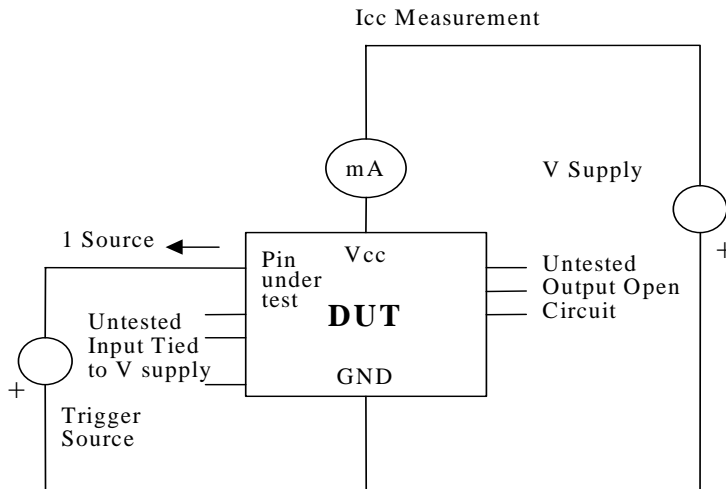
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA, Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.

This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

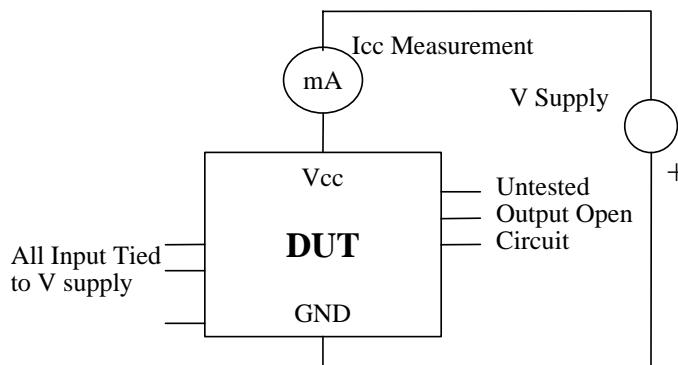
Notes:

1. DUT: Device Under Test.
2. PUT: Pin Under Test.





Test Circuit: Negative Input/Output Overvoltage/Overcurrent



Supply voltage Test

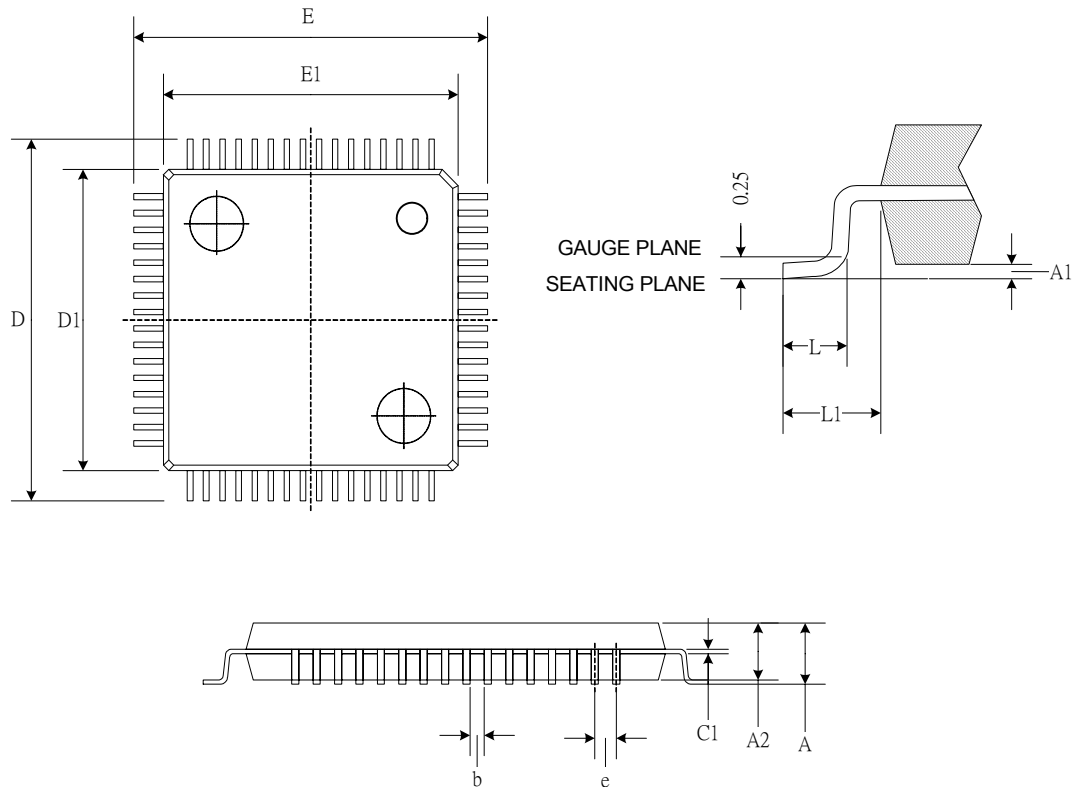
Figure 6.2 Latch-Up Test Circuits

| Model | Model | Voltage (v)/ Current (mA) | S/S | Results |
|---------|-------|---------------------------|-----|---------|
| Voltage | + | 11.0 | 5 | TBD |
| | - | 11.0 | | |
| Current | + | 200 | 5 | TBD |
| | - | 200 | | |
| Vdd-Vxx | | 9.0 | 5 | TBD |

Table 6.5 Latch-Up Data

7. Mechanical Information

Figure 7.1 Mechanical Information Diagram



| SYMBOLS | MIN. | MAX. |
|---------|-----------|------|
| A | -- | 1.60 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.17 | 0.27 |
| c1 | 0.09 | 0.16 |
| D | 12.00 BSC | |
| D1 | 10.00 BSC | |
| E | 12.00 BSC | |
| E1 | 10.00 BSC | |
| e | 0.50 BSC | |
| L | 0.45 | 0.75 |
| L1 | 1.00 REF | |

1. JEDEC OUTLINE: MS-026 BCD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

| | |
|-------------|-------------------------------------|
| SIE | Serial Interface Engine |
| UTMI | USB Transceiver Macrocell Interface |

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.