Features

- **Single-chip Synthesizer + Effects, Features include**
  - **High-quality Wavetable Synthesis, Serial MIDI In & Out, MPU-401 (UART)**
  - **Effects: Reverb + Chorus, on MIDI and/or Audio In**
  - **Up to 64-voice Polyphony**
  - **Surround on Two or Four Speakers with Intensity/Delay Control**
  - **Four-band Parametric Equalizer**
  - **Audio-in Processing through Reverb, Chorus, Equalizer, Surround**
- **Low Chip Count in Applications**
  - **ATSAM2133B Synthesizer, ROM/Flash, DAC**
  - **Built-in (32K x 16) Effects RAM**
- **Low-power**
  - **40 mA Typical Operating Current, <1 µA Power-down**
  - **2.5V and 3.3V Supply**
  - **Built-in Power Switch**
- **16-bit Samples, 44.1 KHz Sampling Rate, 24 dB Digital Filter per Voice**
- **Available Wavetable Firmwares and Sample Sets**
  - **CleanWave8® Low-cost General MIDI 1-MB Firmware + Sample Set**
  - **CleanWave32® Top-quality 4-MB Firmware + Sample Set**
  - **Other Sample Sets Available under special conditions**
- **Built-in ROM Debugger, Flash Programmer through Dedicated Pins**
  - **Fast Product-to-market**
- **Small Footprint**
  - **12 x 12 mm, 0.4 mm Pitch, 100-lead TQFP Package**
  - **10 x 10 mm, 0.8 mm Pitch 100-ball CBGA Package**
- **Typical Applications**
  - **Portable Telephones**
  - **Computer Karaoke, Portable Karaoke Systems**
  - **Keyboards, Portable Keyboard Instruments**

Description

The ATSAM2133B is a low-cost derivative of the ATSAM97xx series. It retains the same high-quality synthesis with up to 64-voice polyphony. The ATSAM2133B maximum wavetable memory is 16 MB and the parallel communication is via a standard MPU-401. The integrated 32K x 16 RAM allows for high-quality effects without additional components.

The highly integrated architecture of the ATSAM2133B combines a specialized high-performance RISC-based digital signal processor (Synthesis/DSP) and a general-purpose 16-bit CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the MPU port, the on-chip MIDI UART, and the Codec control interface, with minimum intervention from the control processor.

Sound Synthesis

ATSAM2133B Low-power Synthesizer with Effects and Built-in RAM

Rev. 2694A–DRMSD–05/03

Typical Applications

Figure 1. Portable Telephone

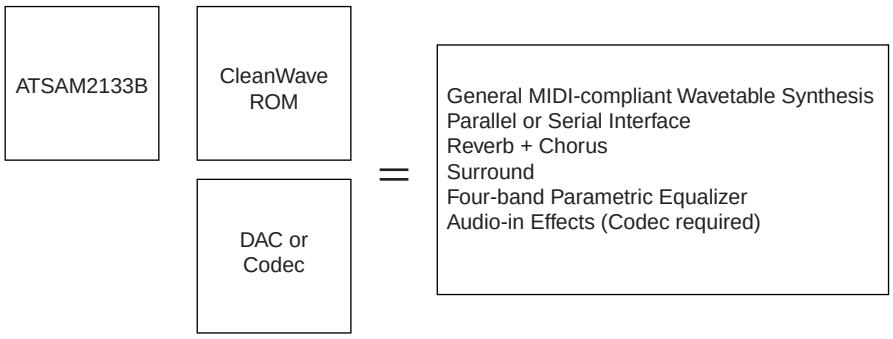


Figure 2. Low-cost Karaoke, Hand-held Karaoke

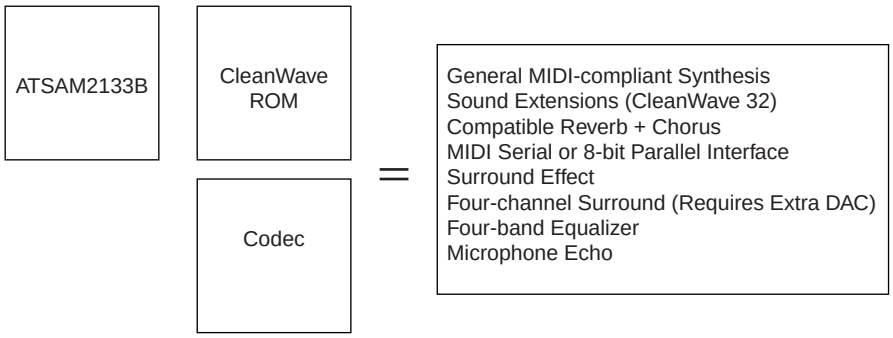
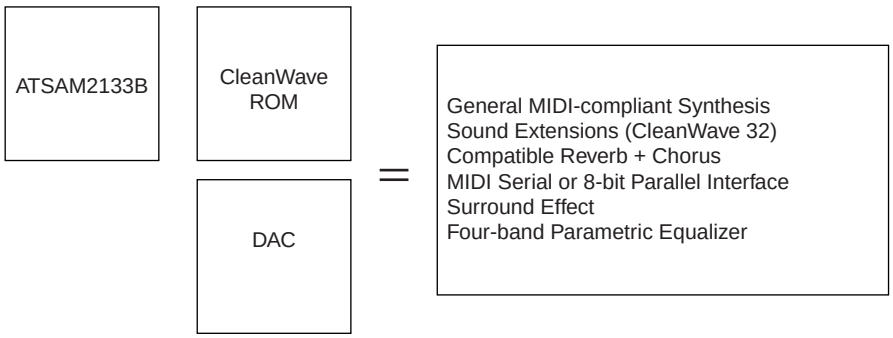
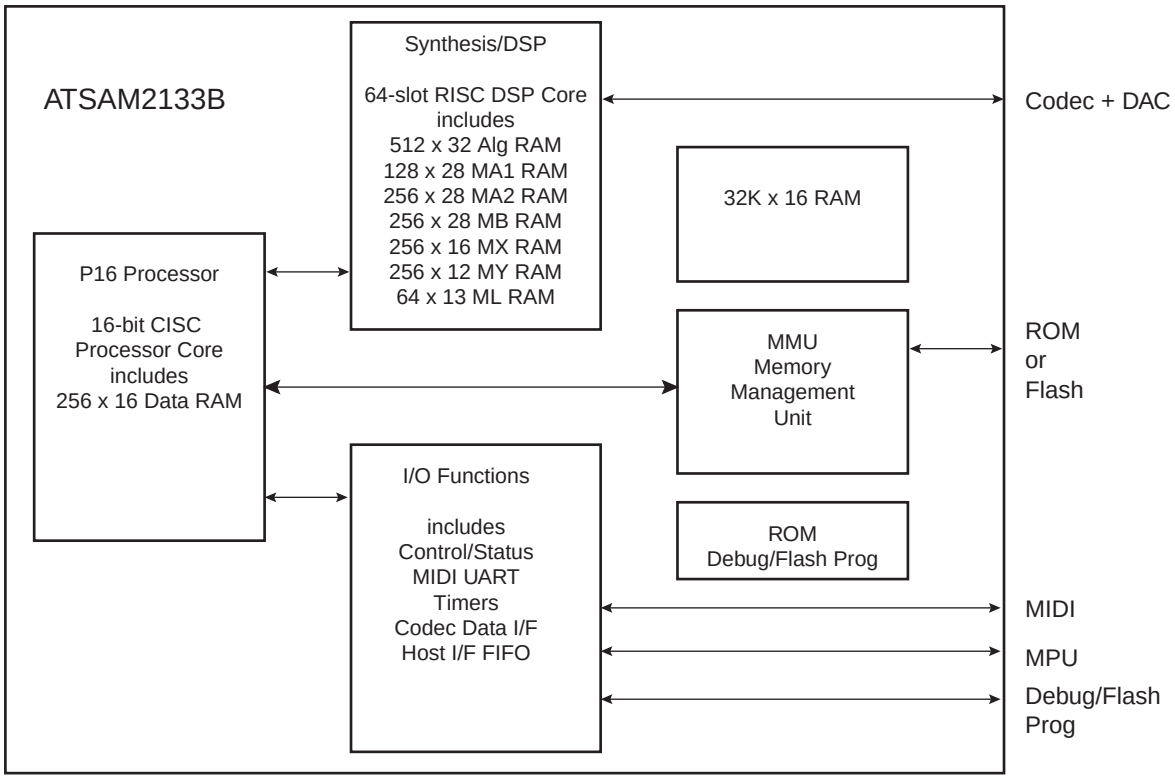


Figure 3. Low-cost Keyboard Instrument



General Description

Block Diagram



Synthesis/DSP Engine

The synthesis/DSP engine operates on a frame timing basis with the frame subdivided into 64 process slots. Each process is, in turn, divided into 16 micro-instructions known as algorithms. Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical application will use half the capacity of the synthesis/DSP engine for synthesis, thus providing state-of-the-art 32-voice wavetable polyphony. The remaining processing power will be used for typical functions such as reverberation, chorus, audio-in processing, surround effect, equalizer, etc.

Frequently-accessed synthesis/DSP parameter data are stored in five banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently, are stored in external ROM or internal 32K x 16 RAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate buses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to six simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

P16 Control Processor and I/O Functions

The P16 control processor is a general-purpose 16-bit CISC processor core that runs from external memory. It includes 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the MPU-401 interface and then controls the Synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly-changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the MPU-401 interface through specialized intelligent peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The MPU-401 interface is implemented using one address line (A0), a chip select signal, read and write strobes from the host and an 8-bit data bus (D0 - D7).

Karaoke and keyboard applications can take advantage of the 8-bit MPU-401 interface to communicate with the ATSAM2133B at high speed, with the MIDI IN and MIDI OUT signals remaining available.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM/Flash and/or internal 32K x 16 RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e., internal RAM) to serve as delay lines for the synthesis/DSP and as data memory for the P16 control processor.

Pin Description

100-lead TQFP Package

Table 1. Pin by Function - 100-lead TQFP Package

Pin Name	Pin Number	Type	Function
GND	10, 16, 31, 36, 45, 56, 68, 76, 80, 84, 96	PWR	Power ground - all GND pins should be returned to digital ground.
VC2	11, 37, 83, 86, 87	PWR	Core power +2.5V ±10%. All V_{C2} pins should be returned to +2.5V. If the built-in power switch is used for minimum power down consumption, then all these pins should be connected to PWROUT, the output of the built-in power switch.
VC3	17, 30, 44, 57, 69, 97	PWR	Periphery power +2.25V to 3.7V. All V_{C3} pins should be returned to nominal +3.3V. V_{C3} should not be lower than V_{C2}.
PWRIN	77	PWR	Power switch input, 2.25V to 2.95V. Even if the power switch feature is not used, this pin must be connected to nominal 2.5V.
PWROUT	78	PWR	Power switch output. Use this pin to supply 2.5V core power by connecting it to all V_{C2} pins.
D0 - D7	6-9, 12-15	I/O	8-bit data bus to host processor. Information on these pins is parallel MIDI (MPU-401 type applications)
$\overline{CS}$	2	IN	Chip select from host, active low.
$\overline{WR}$	4	IN	Write from host, active low.
$\overline{RD}$	3	IN	Read from host, active low.
A0	5	IN	Selects MPU-401 internal registers: 0 = data registers (read/write) 1 = status register (read) control register (write)
IRQ	1	TSOUT	Tri-state output pin, active high.
$\overline{RESET}$	22	IN	Master reset input, active low.
X1, X2	81, 82	-	Crystal connection. Crystal frequency should be Fs*256 (typ 11.2896 MHz). Crystal frequency is internally multiplied by 4 to provide the IC master clock. An external 11.2896 MHz clock can also be used on X1 ($2.5V_{PP}$ max through 47pF capacitor). X2 cannot be used to drive external ICs; use CKOUT instead.
CKOUT	88	OUT	Buffered X2 output, can be used to drive external DAC master clock (256 * Fs)
DABD0 -1	93, 92	OUT	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2 x 32) of serial data per frame. Audio data has up to 20 bits precision. DABD0 can hold additional control data (mute, A/D gain, D/A gain, etc.)
CLBD	94	OUT	Audio data bit clock, provides timing to DABD0 - 1, DAAD.
WSBD	95	OUT	Audio data word select. The timing of WSBD can be selected to be I^2S or Japanese compatible.
DAAD	98	IN	Stereo serial audio data input.
P0 - P3	18 - 21	I/O	General-purpose programmable I/O pins.
DBCLK	90	IN	Debug clock. Should be connected to V_{C3} under normal operation. If DBCLK is found low just after $\overline{RESET}$, then the internal ROM debugger/flash programmer is started.
DBDATA	91	I/O	Debug data. Allows serial communication for debug/flash programming.
DBACK	89	OUT	Debug acknowledge. Toggled each time a bit is received/sent on DBDATA.

Table 1. Pin by Function - 100-lead TQFP Package (Continued)

Pin Name	Pin Number	Type	Function
MIDI IN	100	IN	MIDI IN input
MIDI OUT	99	OUT	MIDI OUT output
WA0 - 22	24 - 29, 32 - 35, 38 - 43, 46 - 52	OUT	External memory address (ROM/Flash). Up to 16 MB.
WD0 - 15	58 - 67, 70 - 75	I/O	External ROM/FLASH data
$\overline{WCS}$	53	OUT	External ROM/FLASH chip select, active low.
$\overline{WWE}$	55	OUT	External FLASH write enable, active low.
$\overline{WOE}$	54	OUT	External ROM/FLASH output enable, active low.
LFT	85	ANA	PLL low-pass filter, should be connected to an external RC network.
TEST	23	IN	Test pin, should be returned to GND.
$\overline{PDWN}$	79	IN	Power down, active low, all outputs except $\overline{WCS}$, $\overline{WWE}$, $\overline{WOE}$ are set to logic 0, the PLL and crystal oscillator are stopped. If the power switch feature is used, then 2.5V supply voltage is removed from the core. To exit from power down, $\overline{PDWN}$ must be set to V_{C2}, then $\overline{RESET}$ applied. When unused, this pin must be connected to V_{C2}.

Table 2. Pinout by Pin Number - 100-lead TQFP Package

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	IRQ	26	WA2	51	WA21	76	GND
2	$\overline{CS}$	27	WA3	52	WA22	77	PWRIN
3	$\overline{RD}$	28	WA4	53	$\overline{WCS}$	78	PWROUT
4	$\overline{WR}$	29	WA5	54	$\overline{WOE}$	79	$\overline{PDWN}$
5	A0	30	VC3	55	$\overline{WWE}$	80	GND
6	D0	31	GND	56	GND	81	X1
7	D1	32	WA6	57	VC3	82	X2
8	D2	33	WA7	58	WD0	83	VC2
9	D3	34	WA8	59	WD1	84	GND
10	GND	35	WA9	60	WD2	85	LFT
11	VC2	36	GND	61	WD3	86	VC2
12	D4	37	VC2	62	WD4	87	VC2
13	D5	38	WA10	63	WD5	88	CKOUT
14	D6	39	WA11	64	WD6	89	DBACK
15	D7	40	WA12	65	WD7	90	DBCLK
16	GND	41	WA13	66	WD8	91	DBDATA
17	VC3	42	WA14	67	WD9	92	DABD1
18	P0	43	WA15	68	GND	93	DABD0
19	P1	44	VC3	69	VC3	94	CLBD
20	P2	45	GND	70	WD10	95	WSBD
21	P3	46	WA16	71	WD11	96	GND
22	$\overline{RESET}$	47	WA17	72	WD12	97	VC3
23	TEST	48	WA18	73	WD13	98	DAAD
24	WA0	49	WA19	74	WD14	99	MIDI OUT
25	WA1	50	WA20	75	WD15	100	MIDI IN

100-ball LFBGA Package

Table 3. Pin by Function - 100-ball LFBGA Package

Pin Name	Pin Number	Type	Function
GND	A3, A9, C7, D5, D10, E1, F7, G4, G5, J5, J8	PWR	Power ground - all GND pins should be returned to digital ground
VC2	B6, C5, C6, E2, H6	PWR	Core power +2.5V ±10%. All V_{C2} pins should be returned to +2.5V. If the built-in power switch is used for minimum power-down consumption, then all these pins should be connected to PWROUT, the output of the built-in power switch.
VC3	C3, D8, G2, G10, H4, H7	PWR	Periphery power 2.25V to 3.7V. All V_{C3} pins should be returned to nominal +3.3V. V_{C3} should be lower than V_{C2}.
PWRIN	A8	PWR	Power switch input, 2.25V to 2.95V. Even if the power switch feature is not used, this pin must be connected to nominal 2.5V
PWROUT	B7	PWR	Power switch output. Use this pin to supply 2.5V core power by connecting it to all V_{C2} pins.
D0 - D7	E4, D1, E3, F4, F3, F5, F2, F1	I/O	8-bit data bus to host processor. Information on these pins is parallel MIDI (MPU-401 type applications).
$\overline{CS}$	C1	IN	Chip select from host, active low.
$\overline{WR}$	C2	IN	Write from host, active low.
$\overline{RD}$	D2	IN	Read from host, active low.
A0	D3	IN	Selects MPU-401 internal registers: 0: data registers (read/write) 1: status register (read) control register (write)
IRQ	B1	TSOUT	Tri-state output pin, active high.
$\overline{RESET}$	H3	IN	Master reset input, active low.
X1, X2	D6, A7	-	Crystal connection. Crystal frequency should be Fs * 256 (typ 11.2896 MHz). Crystal frequency is internally multiplied by 4 to provide the IC master clock. An external 11.2896 MHz clock can also be used on X1 ($2.5V_{PP}$ max through 47 pF capacitor). X2 cannot be used to drive external ICs; use CKOUT instead.
CKOUT	E5	OUT	Buffered X2 output. Can be used to drive external DAC master clock (256 * Fs)
DABD0 - 1	A4, B4	OUT	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2 x 32) of serial data per frame. Audio data precise up to 20 bits. DABD0 can hold additional control data (mute, A/D gain, D/A gain, etc.)
CLBD	C4	OUT	Audio data bit clock, provides timing to DABD0 - 1, DAAD.
WSBD	B3	OUT	Audio data word select. The timing of WSBD can be selected to be I2S or Japanese compatible.
DAAD	A2	IN	Stereo serial audio data input.
P0 - P3	G1, G3, H2, H1	I/O	General-purpose programmable I/O pins.
DBCLK	A5	IN	Debug clock. Should be connected to V_{C3} under normal operation. If DBCLK is found low just after $\overline{RESET}$, then the internal ROM debugger/flash programmer is started
DBDATA	D4	I/O	Debug data. Allows serial communication for debug/flash programming
DBACK	B5	OUT	Debug ack. Toggled each time a bit is received/sent on DBDATA
MIDI IN	A1	IN	MIDI IN input
MIDI OUT	B2	OUT	MIDI OUT output

Table 3. Pin by Function - 100-ball LFBGA Package (Continued)

Pin Name	Pin Number	Type	Function
WA0 - 22	J2, K1, K2, K3, J4, J3, K4, H5, G6, K5, F6, J6, K6, G7, J7, K7, K8, H8, K9, J9, K10, J10, H10	OUT	External memory address (ROM/FLASH). Up to 16 Mega bytes.
WD0 - 15	F8, E7, F10, F9, E8, E6, E9, E10, D7, D9, C9, C10, C8, B10, B9, A10	I/O	External ROM/FLASH data
$\overline{WCS}$	G9	OUT	External ROM/FLASH chip select, active low.
$\overline{WWE}$	G8	OUT	External FLASH write enable, active low.
$\overline{WOE}$	H9	OUT	External ROM/FLASH output enable, active low.
LFT	A6	ANA	PLL low pass filter. Should be connected to an external RC network.
TEST	J1	IN	Test pin. Should be returned to GND.
$\overline{PDWN}$	B8	IN	Power down, active low, all outputs except $\overline{WCS}$, $\overline{WWE}$, $\overline{WOE}$ are set to logic 0, the PLL and crystal oscillator are stopped. If the power switch feature is used, then 2.5V supply voltage is removed from the core. To exit from power down, $\overline{PDWN}$ must be set to V_{C2}, then $\overline{RESET}$ applied. When unused this pin must be connected to V_{C2}.

Table 4. Pinout by Pin Number - 100-ball LFBGA Package

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
A1	MIDI IN	C6	VC2	F1	D7	H6	VC2
A2	DAAD	C7	GND	F2	D6	H7	VC3
A3	GND	C8	WD12	F3	D4	H8	WA17
A4	DABD0	C9	WD10	F4	D3	H9	$\overline{WOE}$
A5	DBCLK	C10	WD11	F5	D5	H10	WA22
A6	LFT	D1	D1	F6	WA10	J1	TEST
A7	X2	D2	$\overline{RD}$	F7	GND	J2	WA0
A8	PWRIN	D3	A0	F8	WD0	J3	WA5
A9	GND	D4	DBDATA	F9	WD3	J4	WA4
A10	WD15	D5	GND	F10	WD2	J5	GND
B1	IRQ	D6	X1	G1	P0	J6	WA11
B2	MIDI OUT	D7	WD8	G2	VC3	J7	WA14
B3	WSBD	D8	VC3	G3	P1	J8	GND
B4	DABD1	D9	WD9	G4	GND	J9	WA19
B5	DBACK	D10	GND	G5	GND	J10	WA21
B6	VC2	E1	GND	G6	WA8	K1	WA1
B7	PWROUT	E2	VC2	G7	WA13	K2	WA2
B8	$\overline{PDWN}$	E3	D2	G8	$\overline{WWE}$	K3	WA3
B9	WD14	E4	D0	G9	$\overline{WCS}$	K4	WA6
B10	WD13	E5	CKOUT	G10	VC3	K5	WA9
C1	$\overline{CS}$	E6	WD5	H1	P3	K6	WA12
C2	$\overline{WR}$	E7	WD1	H2	P2	K7	WA15
C3	VC3	E8	WD4	H3	$\overline{RESET}$	K8	WA16
C4	CLBD	E9	WD6	H4	VC3	K9	WA18
C5	VC2	E10	WD7	H5	WA7	K10	WA20

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Ambient Temperature (Power applied)..... -40°C to + 85°C Storage Temperature ..... -65°C to + 150°C Voltage on Input Pins..... -0.5V to V_{C3} + 0.3V (except X1 and $\overline{PDWN}$) Voltage on X1 and $\overline{PDWN}$ Pins..... -0.5V to V_{C2} + 0.3V V_{C2} Supply Voltage .....-0.5V to + 3V V_{C3} Supply Voltage .....-0.5V to + 4.5V Maximum IOL per I/O pin..... 4 mA Maximum Input Current per Input Pin..... 4 mA Maximum Output Current from PWROUT Pin ..... 525 mA (max duration = 1 sec)	*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{C2}	Supply voltage	2.25	2.5	2.75	V
V_{C3}	Supply voltage	V_{C2}	3.3	3.6	V
PWRIN	Power supply	2.25	2.5	2.95	V
I_{PWROUT}	Power switch output current	-	-	175	mA
t_A	Operating ambient temperature	0	-	70	°C

DC Characteristics

Table 7. DC Characteristics (t_A = 25°C, V_{C2} = 2.5V ± 10%, V_{C3} = 3.3V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage (Except X1, $\overline{PDWN}$)	-0.3	-	1.0	V
V_{IH}	High-level input voltage (Except X1, $\overline{PDWN}$)	2.3	-	V_{C3}+0.3	V
V_{IL}	Low-level input voltage for X1, $\overline{PDWN}$	-0.3	-	0.6	V
V_{IH}	High-level input voltage for X1, $\overline{PDWN}$	2	-	V_{C2}+0.3	V
V_{OL}	Low-level output voltage I_{OL} = -2mA	-	-	0.4	V
V_{OH}	High-level output voltage I_{OH} = 2mA	2.9	-	-	V
	Power consumption (crystal frequency =11.2896 MHz)	-	90		mW
	Power down supply current (using power switch)		1	5	µA
	Drop down from PWRIN to PWROUT (at I_{PWROUT} = 100 mA)		-	0.1	V

Timings

All timing conditions: V_{C2} = 2.5V, V_{C3} = 3.3V, t_A = 25°C, all outputs except X2 and LFT load capacitance = 30 pF.

All timings refer to t_{CK}, the internal master clock period.

The internal master clock frequency is four times the frequency at pin X1. Therefore $t_{CK} = t_{XTAL}/4$.

The sampling rate is given by $1/(t_{CK} \times 1024)$. The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 kHz sampling rate).

Crystal Frequency Selection

There is a trade-off between the crystal frequency and the support of widely-available external ROM/Flash components. Table 8 gives information on selecting the best fit for a given application.

Table 8. Crystal Frequency Selection Parameters

Sample Rate (KHz)	Crystal (MHz)	t_{CK} (ns)	ROM t_A (ns)	Comments
48	12.288	20.35	92	Maximum frequency
44.1	11.2896	22.14	101	Recommended for current designs
37.5	9.60	26.04	120	
31.25	8.00	31.25	146	

Using 11.2896 MHz crystal frequency allows the use of widely-available ROMs with 100 ns access time while providing state-of-the-art 44.1 kHz sampling rate.

PC Host Interface

Figure 4. Host Interface Read Cycle

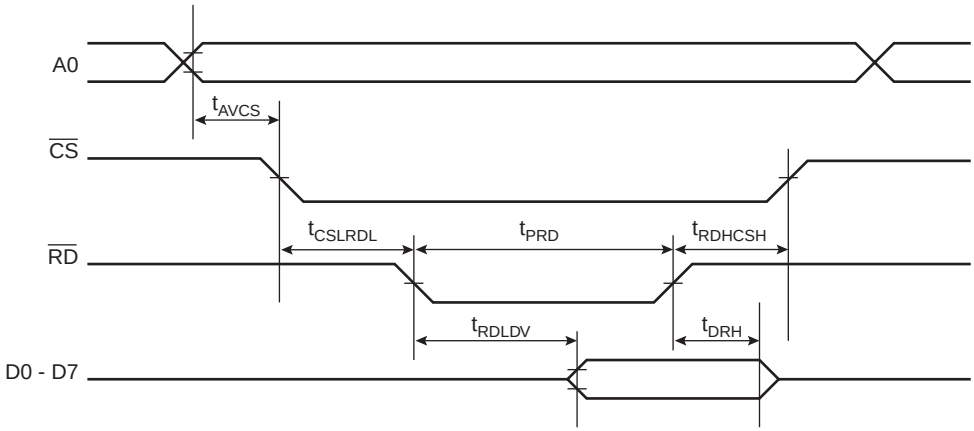


Figure 5. Host Interface Write Cycle

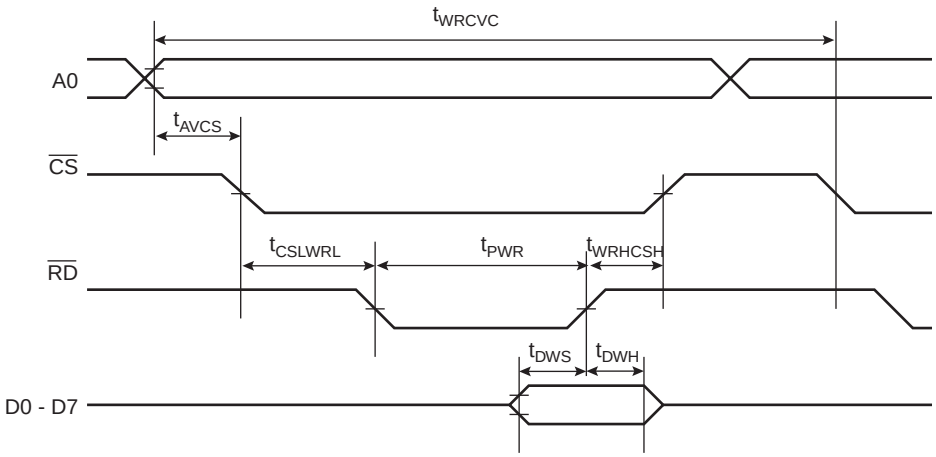


Table 9. PC Host Interface Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address valid to chip select low	0	-	-	ns
t_{CSLRDL}	Chip select low to $\overline{RD}$ low	5	-	-	ns
t_{RDHCSH}	$\overline{RD}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PRD}	$\overline{RD}$ pulse width	50	-	-	ns
t_{RDLDV}	Data out valid from $\overline{RD}$	-	-	20	ns
t_{DRH}	Data out hold from $\overline{RD}$	5	-	10	ns
$t_{CSLRWRL}$	Chip select low to $\overline{WR}$ low	5	-	-	ns
t_{WRHCSH}	$\overline{WR}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PWR}	$\overline{WR}$ pulse width	50	-	-	ns
t_{DWS}	Write data setup time	10	-	-	ns
t_{DWH}	Write data hold time	0	-	-	ns
t_{WRCYC}	Write cycle	128	-	-	tck

External ROM/Flash

Figure 6. ROM/Flash Read Cycle

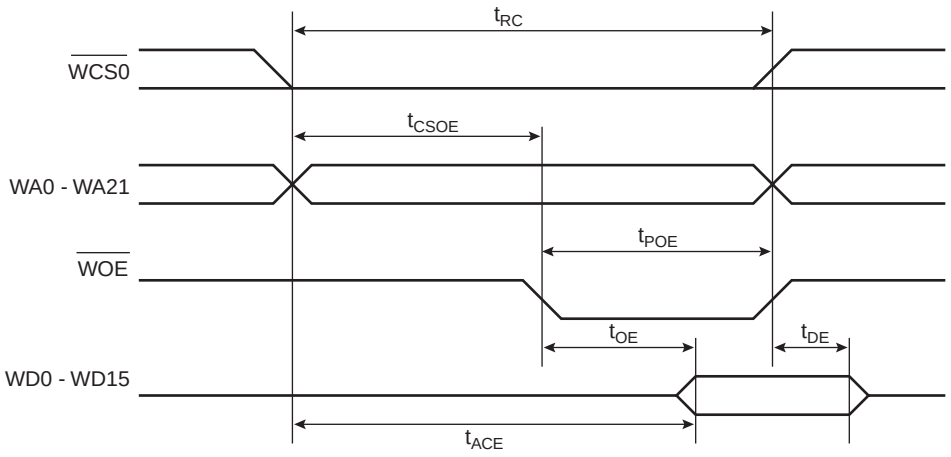


Table 10. External ROM/Flash Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read cycle time	$5 * t_{CK}$	-	$6 * t_{CK}$	ns
t_{CSOE}	Chip select low/address valid to $\overline{WOE}$ low	$2 * t_{CK} - 5$	-	$3 * t_{CK} + 5$	ns
t_{POE}	Output enable pulse width	-	$3 * t_{CK}$	-	ns
t_{ACE}	Chip select/address access time	$5 * t_{CK} - 5$	-	-	ns
t_{OE}	Output enable access time	$3 * t_{CK} - 5$	-	-	ns
t_{DE}	Chip select or $\overline{WOE}$ high to input data Hi-Z	0	-	$2 * t_{CK} - 5$	ns

Figure 7. External Flash Write Cycle

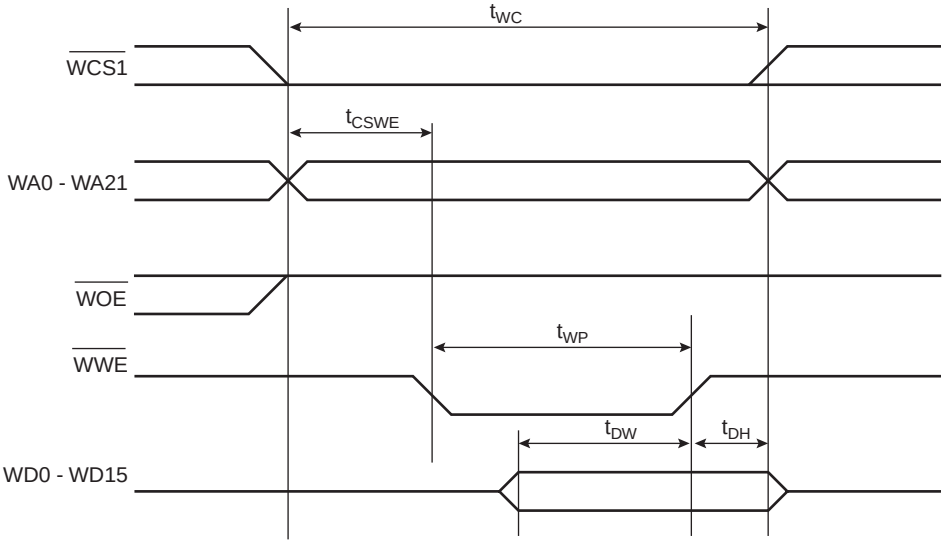


Table 11. External Flash Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{WC}	Write cycle time	$5 * t_{CK}$	-	$6 * t_{CK}$	ns
t_{CSWE}	Write enable low from $\overline{CS}$ or Address or $\overline{WOE}$	$2 * t_{CK} - 10$	-	-	ns
t_{WP}	Write pulse width	-	$4 * t_{CK}$	-	ns
t_{DW}	Data out setup time	$4 * t_{CK} - 10$	-	-	ns
t_{DH}	Data out hold time	10	-	-	ns

Digital Audio

Figure 8. Digital Audio

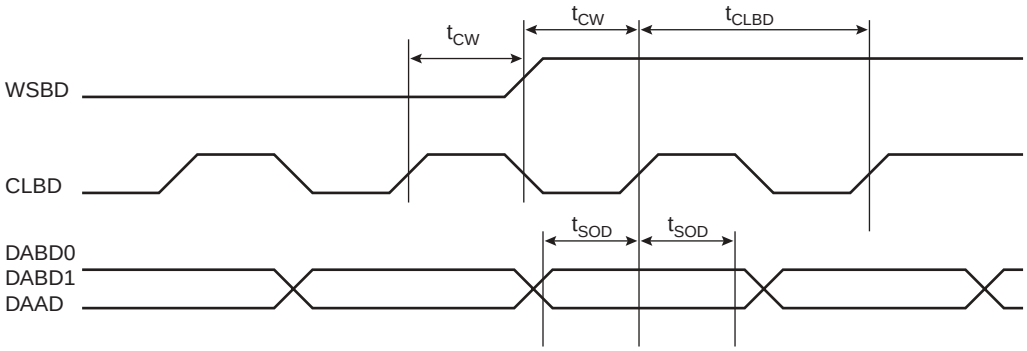
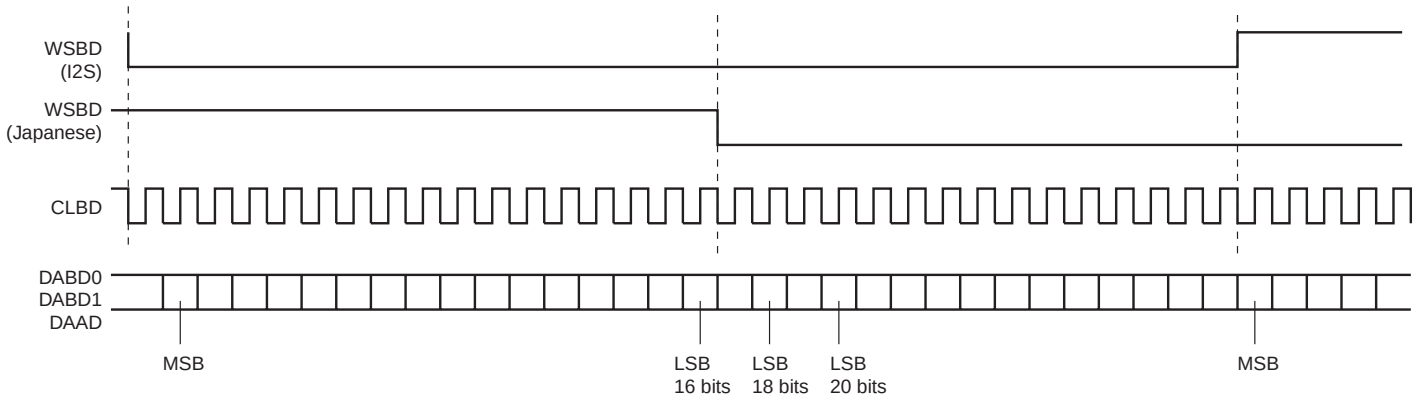


Table 12. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD rising to WSBD change	8 * t_{CK} - 10			ns
t_{SOD}	DABD valid prior/after CLBD rising	8 * t_{CK} - 10			ns
t_{CLBD}	CLBD cycle time		16 * t_{CK}		ns

Figure 9. Digital Audio Frame Format



Notes: 1. Selection between I2S and Japanese format is a firmware option.
2. DAAD is 16 bits only.

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized. This can take about 20 ms.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:

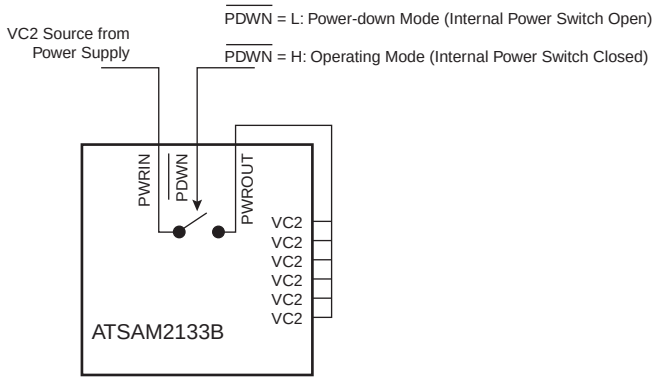
- Synthesis/DSP enters an idle state
- P16 program execution starts from address 0100H in ROM space ($\overline{\text{WCS}}$ low)

If $\overline{\text{PDWN}}$ is asserted low, then the crystal oscillator and PLL are stopped. If the power switch is used, then the chip enters a deep power-down sleep mode, as power is removed from the core. To exit power down, $\overline{\text{PDWN}}$ must be asserted high, then $\overline{\text{RESET}}$ applied.

Power-down mode is managed by an internal power switch. The equivalent schematic and standard connection is shown on the diagram below.

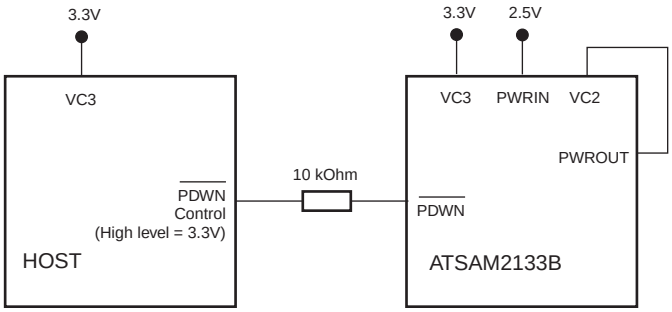
All the VC2 pins must be connected to PWROUT.

Figure 10. Schematic



Note: High level for $\overline{\text{PDWN}}$ is VC2 = 2.5V ±10%.

Figure 11. $\overline{\text{PDWN}}$ Connection



Recommended Board Layout

Like all HCMOS high integration ICs, the following simple rules of board layout are mandatory for reliable operation:

- GND, VC3, VC2 Distribution and Decouplings

All GND, VC3, VC2 pins should be connected. A GND plane is strongly recommended below the ATSAM2133B. The board GND + VC3 distribution should be in grid form.

Recommended VC2 decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. VC3 requires a single 0.1uF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the ATSAM2133B should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from ATSAM2133B.

- Buses

Parallel layout between D0 - D7 and WA0 - WA21/WD0 - WD15 should be avoided. The D0 - D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0 - WA21/WD0 - WD15 that can corrupt address and/or data on these buses.

A ground plane should be implemented below the D0 - D7 bus, which is connected to the host and to the ATSAM2133B GND.

A ground plane should be implemented below the WA0 - WA21/WD0 - WD15 bus, which is connected to the ROM/Flash grounds and to the ATSAM2133B.

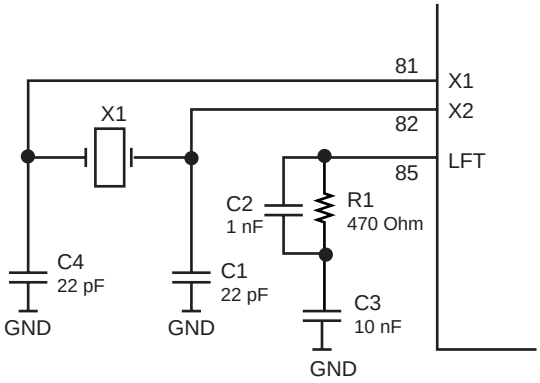
- Analog Section

A specific AGND ground plane should be provided, which is connected to the GND ground by a single trace. No digital signals should cross the AGND plane.

Refer to the Codec vendor recommended layout for correct implementation of the analog section.

Recommended Crystal Compensation and LFT Filter

Figure 12. Recommended Crystal Compensation and LFT Filter



Mechanical Dimensions

100-lead TQFP Package

Figure 13. Thin Plastic 100-lead Quad Flat Pack (TQFP100)

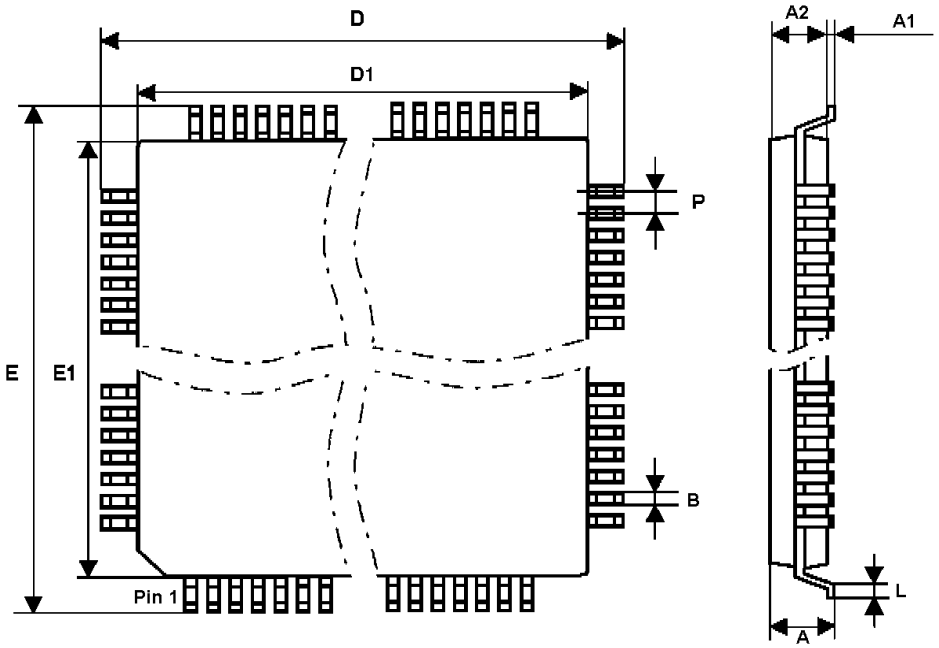
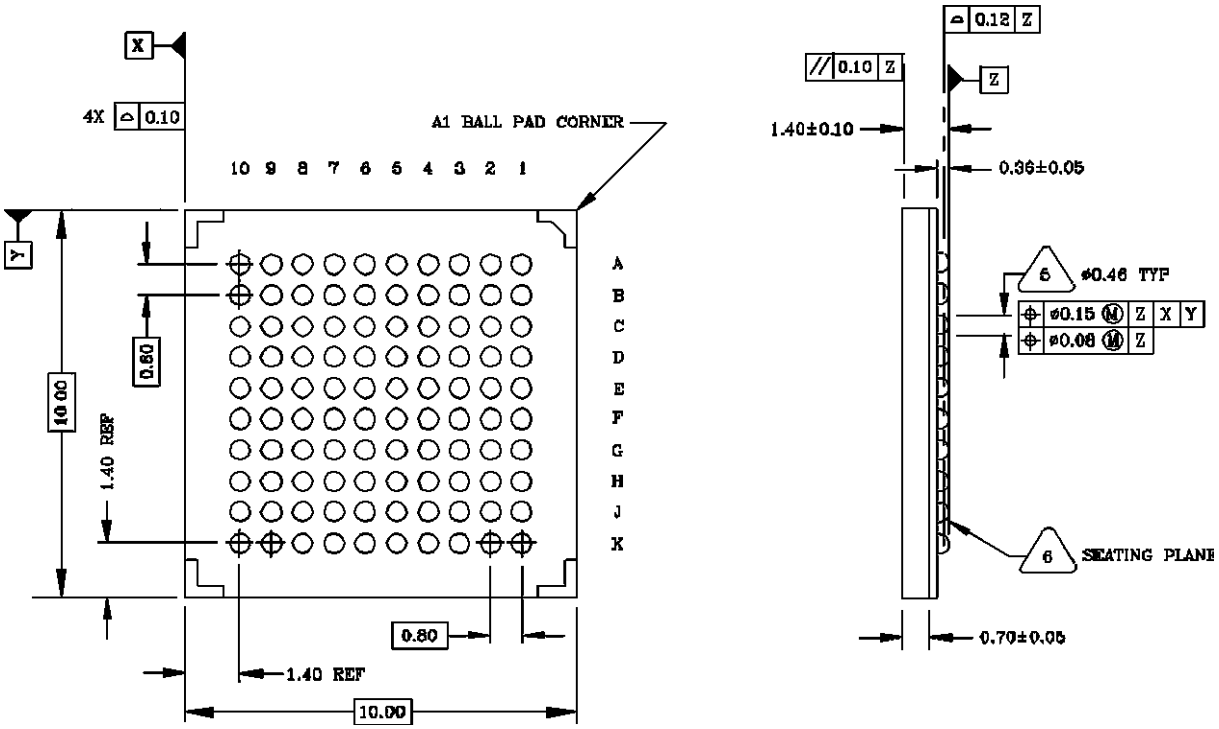


Table 13. 100-lead TQFP Package Dimensions (in mm)

Parameter	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D		14.00	
D1		12.00	
E		14.00	
E1		12.00	
L	0.45	0.60	0.75
P		0.40	
B	0.13	0.18	0.23

100-ball LFBGA Package

Figure 14. Low Profile Fine Pitch 100-ball Grid Array (LFBGA)(Bottom View)



Package Marking

Figure 15. Package Marking

Note: A1 Ball in lower left-hand corner.

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