Features

- 16 Channel GPS Correlator
  - 8192 Search Bins with GPS Acquisition Accelerator
  - Accuracy: 2.5m CEP (Stand-Alone, S/A off)
  - Time to First Fix: 34s (Cold Start)
  - Acquisition Sensitivity: –140 dBm
  - Tracking Sensitivity: –150 dBm
- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Embedded ICE (In-circuit Emulator)
- 128 Kbyte Internal RAM
- 384 Kbyte Internal ROM with u-blox GPS Firmware
- Fully Programmable External Bus Interface (EBI)
  - Maximum External Address Space of 8 Mbytes
  - Up to 4 Chip Selects
  - Software Programmable 8-bit/16-bit External Data Bus
- 6-channel Peripheral Data Controller (PDC)
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 2 External Interrupts
- 32 User-programmable I/O Lines
- 1 USB Device Port
  - Universal Serial Bus (USB) V2.0 Full-speed Device Specification Compliant
  - Embedded USB V2.0 Full-speed Transceiver
  - Suspend/Resume Logic
  - Ping-pong Mode for Isochronous and Bulk Endpoints
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Master/Slave SPI Interface
  - 2 Dedicated Peripheral Data Controller (PDC) Channels
  - 8-bit to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Advanced Power Management Controller (APMC)
  - Peripherals Can Be Deactivated Individually
  - Geared Master Clock to Reduce Power Consumption
  - Sleep State with Disabled Master Clock
  - Hibernate State with 32.768 kHz Master Clock
- Real Time Clock (RTC)
- 2.3V to 3.6V or 1.8V Supply Voltage
- Includes Power Supervisor
- 1.8V to 3.3V User-definable I/O Voltage for Several GPIOs with 5V Tolerance
- 1 Kbyte Battery Backup Memory
- 9 mm × 9 mm 100-pin BGA Package (LFBGA100)

Pb Lead Free

Electrostatic sensitive device.
Observe precautions for handling.

GPS Baseband Processor

ATR0621

Summary

Preliminary

Rev. 4890AS–GPS–09/05

Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

1. Description

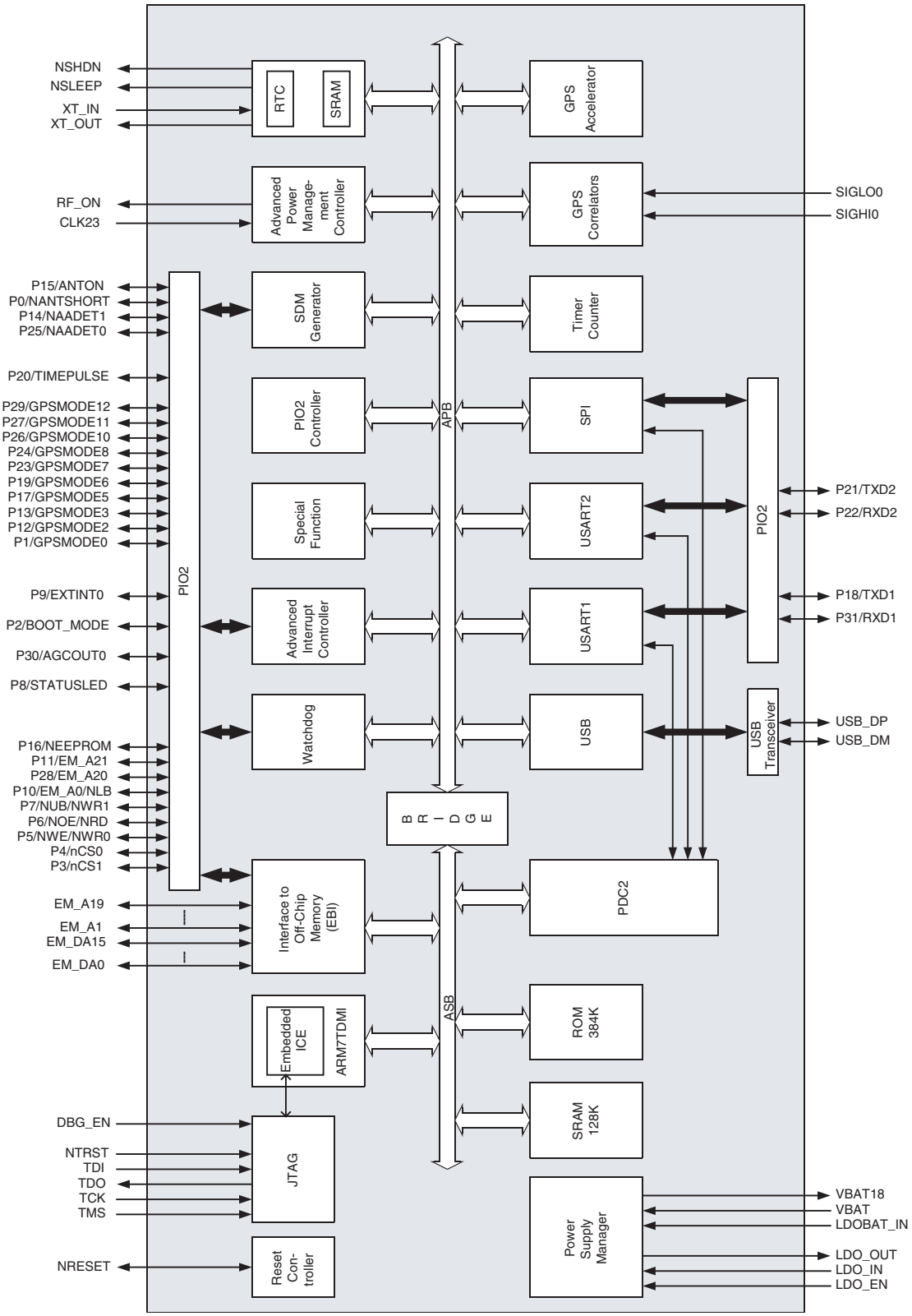
The GPS baseband processor ATR0621 includes a 16-channel GPS correlator and is based on the ARM7TDMI® processor core.

This processor has a high-performance 32-bit RISC architecture and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The ATR0621 has a USB device port. This port is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification. The ATR0621 has a direct connection to off-chip memory, including Flash, through the External Bus Interface (EBI).

The ATR0621 includes full GPS firmware, licensed from u-blox AG, which performs the basic GPS operation, including tracking, acquisition, navigation and position data output. For normal PVT (Position/Velocity/Time) applications, there is no need for off-chip Flash memory or ROM. In order to be able to store configuration settings, connecting a serial EEPROM is supported. For customer-specific applications, a Software Development Kit is available.

The ATR0621 is manufactured using the Atmel high-density CMOS technology. By combining the ARM7TDMI microcontroller core with on-chip SRAM, 16-channel GPS correlator and a wide range of peripheral functions on a monolithic chip, the ATR0621 provides a highly-flexible and cost-effective solution for GPS applications.

Figure 1-1. Block Diagram



2. Architectural Overview

2.1 Description

The ATR0621 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC2) transfers data between the on-chip USARTs/SPI and the on-chip and off-chip memories without processor intervention. Most importantly, the PDC2 removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The ATR0621 peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 3 Mbyte of the 4 Gbyte address space. (Except for the interrupt controller, which has 4 Kbyte address space.) The peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status, and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits, and the third address reads the value stored in the register. A bit can be set or reset by writing a “1” to the corresponding position at the appropriate address. Writing a “0” has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit-manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O (PIO2) Controller. The PIO2 Controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO2 Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI® processor operates in little-endian mode on the ATR0621 GPS Baseband. The processor's internal architecture and the ARM® and Thumb® instruction sets are described in the ARM7TDMI datasheet. The memory map and the on-chip peripherals are described in detail in the ATR0621 full datasheet. The electrical and mechanical characteristics are also documented in the ATR0621 full datasheet.

The ARM standard In-Circuit Emulation debug interface is supported via the JTAG/ICE port of the ATR0621.

Features of the ROM firmware are described in software documentation available from u-blox AG.

3. Pin Configuration

3.1 Pinout

Figure 3-1. Pinout LFBGA100 (Top View)

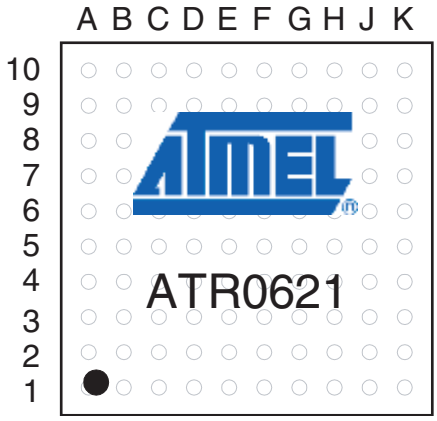


Table 3-1. ATR0621 Pinout

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)(1)	Firmware Label	PIO Bank A		PIO Bank B	
CLK23	G9	IN						
DBG_EN	H4	IN	PD					
EM_A1	A6	OUT						
EM_A2	A5	OUT						
EM_A3	A4	OUT						
EM_A4	A2	OUT						
EM_A5	A3	OUT						
EM_A6	B5	OUT						
EM_A7	B4	OUT						
EM_A8	B2	OUT						
EM_A9	D4	OUT						
EM_A10	C2	OUT						
EM_A11	D6	OUT						
EM_A12	D7	OUT						
EM_A13	C3	OUT						
EM_A14	C1	OUT						
EM_A15	D5	OUT						
EM_A16	C6	OUT						
EM_A17	F8	OUT						

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
3. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.

Table 3-1. ATR0621 Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
EM_A18	B3	OUT						
EM_A19	C5	OUT						
EM_DA0	B6	I/O	PD					
EM_DA1	B10	I/O	PD					
EM_DA2	C7	I/O	PD					
EM_DA3	C10	I/O	PD					
EM_DA4	D10	I/O	PD					
EM_DA5	E7	I/O	PD					
EM_DA6	E9	I/O	PD					
EM_DA7	B7	I/O	PD					
EM_DA8	B8	I/O	PD					
EM_DA9	A9	I/O	PD					
EM_DA10	C8	I/O	PD					
EM_DA11	B9	I/O	PD					
EM_DA12	D8	I/O	PD					
EM_DA13	C9	I/O	PD					
EM_DA14	D9	I/O	PD					
EM_DA15	E8	I/O	PD					
GND	A1	IN						
GND	A10	IN						
GND	K1	IN						
GND	K10	IN						
LDOBAT_IN	K8	IN						
LDO_EN	H7	IN						
LDO_IN	K7	IN						
LDO_OUT	H6	OUT						
NRESET	C4	I/O	Open Drain PU					
NSHDN	G7	OUT						
NSLEEP	J6	OUT						
NTRST	K2	IN	PD					
P0	K9	I/O	PD	NANTSHORT				
P1	G3	I/O	Configurable (PD)	GPSMODE0		AGCOUT1		
P2	G4	I/O	Configurable (PD)	BOOT_MODE		“0”		CLK32K
P3	H5	I/O	OH	NCS1		NCS1		“0”
P4	A7	I/O	OH	NCS0		NCS0		“0”
P5	B1	I/O	OH	NWE/NWR0		NWE/NWR0		“0”

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
3. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.

Table 3-1. ATR0621 Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)(1)	Firmware Label	PIO Bank A		PIO Bank B	
P6	A8	I/O	OH	NOE/NRD		NOE/NRD		“0”
P7	D2	I/O	OH	NUB/NWR1		NUB/NWR1		“0”
P8	G2	I/O		STATUSLED		“0”		
P9	J8	I/O	PU	EXTINT0	EXTINT0			
P10	E4	I/O	OH	EM_A0/NLB		EM_A0/NLB		“0”
P11	H10	I/O	OH	EM_A21		NCS2		EM_A21
P12	F3	I/O	Configurable (PU)	GPSMODE2		NPCS2		
P13	G10	I/O	PU	GPSMODE3	EXTINT1			
P14	J5	I/O	Configurable (PD)	NAADET1		“0”		
P15	K5	I/O	PD	ANTON				
P16	E1	I/O	Configurable (PU)	NEEPROM	SIGHI1			NWD_OVF
P17	J4	I/O	Configurable (PD)	GPSMODE5	SCK1	SCK1		
P18	K4	I/O	Configurable (PU)	TXD1		TXD1		“0”
P19	F1	I/O	Configurable (PU)	GPSMODE6	SIGLO1			“0”
P20	H2	I/O	Configurable (PU)	TIMEPULSE	SCK2	SCK2		TIMEPULSE
P21	F2	I/O	Configurable (PU)	TXD2		TXD2		“0”
P22	H8	I/O	PU	RXD2	RXD2			
P23	H3	I/O	Configurable (PU)	GPSMODE7	SCK	SCK		MCLK_OUT
P24	H1	I/O	Configurable (PU)	GPSMODE8	MOSI	MOSI		“0”
P25	D1	I/O	Configurable (PU)	NAADET0	MISO	MISO		“0”
P26	G8	I/O	Configurable (PU)	GPSMODE10	NSS	NPCS0		“0”
P27	E2	I/O	Configurable (PU)	GPSMODE11		NPCS1		
P28	G1	I/O	OH	EM_A20		NCS3		EM_A20
P29	E3	I/O	Configurable (PU)	GPSMODE12		NPCS3		
P30	G5	I/O	PD	AGCOUT0		AGCOUT0		“0”
P31	H9	I/O	PU	RXD1	RXD1			
RF_ON	K6	OUT	PD					
SIGHI0	F9	OUT						
SIGLO0	E10	OUT						
TCK	J3	IN	PU					
TDI	J2	IN	PU					
TDO	K3	OUT						
TMS	J1	IN	PU					
USB_DM	F10	I/O						
USB_DP	D3	I/O						
VBAT	J7	IN						

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
3. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.

Table 3-1. ATR0621 Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
VBAT18	G6	OUT						
VDD18	E6	IN						
VDD18	F7	IN						
VDD18	F6	IN						
VDDIO[2]	E5	IN						
VDD_USB[3]	F5	IN						
XT_IN	J9	IN						
XT_OUT	J10	OUT						

Notes: 1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset

2. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29

3. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP. For operation of the USB interface, supply of 3.0V to 3.6V is required.

3.2 Signal Description

Table 3-2. ATR0621 Signal Description

Module	Name	Function	Type	Active Level	Comment
EBI	EM_A0 to EM_A21	External Memory Address Bus	Output	–	All valid after reset
	EM_DA0 to EM_DA15	External Memory Data Bus	I/O	–	Internal pull-down resistor
	NCS0 to NCS1	Chip Select	Output	Low	Output High in RESET state
	NCS2 to NCS3	Chip Select	Output	Low	Output High in RESET state
	NWR0	Lower Byte Write Signal	Output	Low	Output High in RESET state
	NWR1	Upper Byte Write Signal	Output	Low	Output High in RESET state
	NRD	Read Signal	Output	Low	Output High in RESET state
	NWE	Write Enable	Output	Low	Output High in RESET state
	NOE	Output Enable	Output	Low	Output High in RESET state
	NUB	Upper Byte Select (16-bit SRAM)	Output	Low	Output High in RESET state
	NLB	Lower Byte Select (16-bit SRAM)	Output	Low	Output High in RESET state
	BOOT_MODE	Boot Mode Input	Input	–	PIO-controlled after reset, internal pull-down resistor
USART	TXD1-2	Transmit Data Output	Output	–	PIO-controlled after reset
	RXD1-2	Receive Data Input	Input	–	PIO-controlled after reset
	SCK1-2	External Synchronous Serial Clock	I/O	–	PIO-controlled after reset
USB	USB_DP	USB Data (D+)	I/O	–	
	USB_DM	USB Data (D-)	I/O	–	
APMC	RF_ON		Output	–	Interface to ATR0600
RTC	NSLEEP	Sleep Output	Output	Low	Interface to ATR0600
	NSHDN	Shutdown Output	Output	Low	Connect to pin LDO_EN
	XT_IN	Oscillator Input	Input	–	RTC oscillator
	XT_OUT	Oscillator Output	Output	–	RTC oscillator

Table 3-2. ATR0621 Signal Description (Continued)

Module	Name	Function	Type	Active Level	Comment
SPI	SCK	SPI Clock	I/O	–	PIO-controlled after reset
	MOSI	Master Out Slave In	I/O	–	PIO-controlled after reset
	MISO	Master In Slave Out	I/O	–	PIO-controlled after reset
	NSS/NPCS0	Slave Select	I/O	Low	PIO-controlled after reset
	NPCS1-3	Slave Select	Output	Low	PIO-controlled after reset
WD	NWD_OVF	Watchdog Timer Overflow	Output	–	PIO-controlled after reset
PIO	P0-31	Programmable I/O Port	I/O	–	Input after reset
GPS	GPSMODE0-12	GPS Mode	Input	–	PIO-controlled after reset
	SIGHI1	Digital IF	Input	–	Interface to ATR0600
	SIGLO1	Digital IF	Input	–	Interface to ATR0600
	SIGHI2	Digital IF	Input	–	PIO-controlled after reset
	SIGLO2	Digital IF	Input	–	PIO-controlled after reset
	TIMEPULSE	GPS synchronized time pulse	Output	–	PIO-controlled after reset
JTAG/ICE	TMS	Test Mode Select	Input	–	Internal pull-up resistor
	TDI	Test Data In	Input	–	Internal pull-up resistor
	TDO	Test Data Out	Output	–	
	TCK	Test Clock	Input	–	Internal pull-up resistor
	NTRST	Test Reset Input	Input	Low	Internal pull-down resistor
	DBG_EN	Debug Enable	Input	–	Internal pull-down resistor
CLOCK	CLK23	Clock Input	Input	–	Interface to ATR0600, Schmitt trigger input
	MCLK_OUT	Master Clock Output	Output	–	PIO-controlled after reset
RESET	NRESET	Reset Input	I/O	Low	Open drain with internal pull-up resistor
POWER	VDD18		Power	–	Core voltage 1.8V
	VBAT18		Power	–	Backup power 1.8V
	VDDIO		Power	–	Variable I/O voltage
	VDD_USB		Power	–	USB voltage 3.0V to 3.6V
	GND		Power	–	Ground
LDOBAT	LDOBAT_IN		Power	–	1.8V to 3.6V
	VBAT		Power	–	1.95V to 3.6V
	VBAT18		Out	–	1.8V backup voltage
LDO18	LDO_IN	LDO In	Power	–	1.65V to 3.6V
	LDO_OUT	LDO Out	Power	–	1.8V core voltage, max. 100 mA
	LDO_EN	LDO Enable	Input	–	

3.3 Setting GPSMODE0 to GPSMODE12

The start-up configuration of a ROM-based system without external non-volatile memory is defined by the status of the GPSMODE pins after system reset. Alternatively, the system can be configured through message commands passed through the serial interface after start-up. If Flash memory is available, configuration data can be stored in Flash memory. If EEPROM memory is connected, configuration data can be stored in EEPROM. *Default* designates settings used by ROM firmware if GPSMODE configuration is disabled (GPSMODE0 =0).

Table 3-3. GPSMODE Functions

Pin	Function
GPSMODE0	Enable configuration with GPSMODE pins
GPSMODE1	This pin is used for *FixNow* functionality and not used for GPSMODE configuration
GPSMODE2	GPS sensitivity settings
GPSMODE3	
GPSMODE4	This pin (NAADET1) is used as active antenna supervisor input and not used for GPSMODE configuration
GPSMODE5	Serial I/O configuration
GPSMODE6	
GPSMODE7	USB Power Mode
GPSMODE8	General I/O Configuration
GPSMODE9	This pin (NAADET0) is used as active antenna supervisor input and not used for GPSMODE configuration
GPSMODE10	General I/O Configuration
GPSMODE11	
GPSMODE12	Serial I/O configuration

3.3.1 Enable GPSMODE Pin Configuration

Table 3-4. Enable Configuration with GPSMODE Pins

GPSMODE0 (Reset = PD)	Description
0	Ignore all GPSMODE pins. The default settings as indicated below are used
1	Use settings as specified with GPSMODE[2, 3, 5 to 8, 10 to12]

3.3.2 Sensitivity Settings

Table 3-5. GPS Sensitivity Settings

GPSMODE3 (Fixed PU)	GPSMODE2 (Reset = PU)	Description
0	0	Auto mode
0	1	Fast mode
1	0	Normal mode (Default)
1	1	High sensitivity

3.3.3 Serial I/O Configuration

The ATR0621 features a two-stage I/O message and protocol selection procedure for the two available serial ports. At the first stage, a certain protocol can be enabled or disabled for a given USART port. Selectable protocols are RTCM, NMEA and UBX. At the second stage, messages can be enabled or disabled for each enabled protocol on each port. In all configurations discussed below, all protocols are enabled on all ports. But output messages are enabled in a way that ports appear to communicate at only one protocol. However, each port will accept any input message in any of the three implemented protocols.

Table 3-6. Serial I/O Configuration

GPSMODE12 (Reset = PU)	GPSMODE6 (Reset = PU)	GPSMODE5 (Reset = PD)	USART1 (Output Protocol/ Baud Rate (kBaud))	USART2 (Output Protocol/ Baud Rate (kBaud))	Messages	Information Messages
0	0	0	UBX/57.6	NMEA/19.2	High	User, Notice, Warning, Error
0	0	1	UBX/38.4	NMEA/9.6	Medium	User, Notice, Warning, Error
0	1	0	UBX/19.2	NMEA/4.8	Low	User, Notice, Warning, Error
0	1	1	–/Auto	–/Auto	Off	None
1	0	0	NMEA/19.2	UBX/57.6	High	User, Notice, Warning, Error
1	0	1	NMEA/4.8	UBX/19.2	Low	User, Notice, Warning, Error
1	1	0	NMEA/9.6	UBX/38.4	Medium	User, Notice, Warning, Error
1	1	1	UBX/115.2	NMEA/19.2	Debug	All

Both USART ports accept input messages in all three supported protocols (NMEA, RTCM and UBX) at the configured baud rate. Input messages of all three protocols can be arbitrarily mixed. Response to a query input message will always use the same protocol as the query input message.

In Auto Mode, no output message is sent out by default, but all input messages are accepted at any supported baud rate. Response to query input commands will be given the same protocol and baud rate as it was used for the query command. Using the respective configuration commands, periodic output messages can be enabled.

The following message settings are used in Table 3-6:

Table 3-7. Supported Messages at Setting *Low*

NMEA Port	Standard	GGA, RMC
UBX Port	NAV	SOL, SVINFO

Table 3-8. Supported Messages at Setting *Medium*

NMEA Port	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA
UBX Port	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK

Table 3-9. Supported Messages at Setting *High*

NMEA Port	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST
	Proprietary	PUBX00, PUBX03, PUBX04
UBX Port	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK
	MON	SCHD, IO, IPC

Table 3-10. Supported Messages at Setting *Debug* (Additional Undocumented Message May be Part of Output Data)

NMEA Port	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST
	Proprietary	PUBX00, PUBX03, PUBX04
UBX Port	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK
	MON	SCHD, IO, IPC
	RXM	RAW (RAW message support requires an additional license)

The following settings apply if GPSMODE configuration is not enabled, that is, GPSMODE = 0 (*ROM-Defaults*):

Table 3-11. Serial I/O Default Setting if GPSMODE Configuration is Deselected (GPSMODE0 = 0)

	USART1/USB NMEA	**USART2 UBX**
Baud Rate (kBaud)	57.6, Auto enabled	57.6, Auto enabled
Input Protocol	UBX, NMEA, RTCM	UBX, NMEA, RTCM
Output Protocol	NMEA	UBX
Messages	GGA, RMC, GSA, GSV	NAV: SOL, SVINFO
Information Messages (UBX INF or NMEA TXT)	User, Notice, Warning, Error	User, Notice, Warning, Error

3.3.4 USB Power Mode

For correct response to the USB host queries, the device has to know its power mode. This is configured via GPSMODE7. If set to *bus powered*, an upper current limit of 100 mA is reported to the USB host; that is, the device classifies itself as a “low-power bus-powered function” with no more than one USB power unit load.

Table 3-12. USB Power Modes

GPSMODE7 (Reset = PU)	**Description**
0	USB device is bus-powered (max. current limit 100 mA)
1	USB device is self-powered (Default)

3.3.5 Active Antenna Supervisor

If GPSMODE configuration is enabled, the two pins P0/NANTSHORT and P15/ANTON, plus one pin of P25/NAADET0/MISO or P14/NAADET1 are initialized as general purpose I/Os and used as follows:

- P15/ANTON is an output which can be used to switch on and off the antenna power supply.
- Input P0/NANTSHORT will indicate an antenna short circuit, that is, zero DC voltage at the antenna, to the firmware. If the antenna is switched off by output P15/ANTON, it is assumed that also input P0/NANTSHORT will signal zero DC voltage, that is, switch to its active low state.
- Input P25/NAADET0/MISO or P14/NAADET1 will indicate that a DC current is sunk into the antenna. In case of short circuit, both P0 and P25/P14 will be active, that is, at low level. If the antenna is switched off by output P15/ANTON, it is assumed that input P25/NAADET0/MISO will also signal zero DC current, that is, switch to its active low state. Which pin is used as NAADET (P14 or P25) depends on the settings of GPSMODE11 and GPSMODE10 (Table 3-14).

Table 3-13. Pin Usage of Active Antenna Supervisor

Pin	Usage	Meaning
P0/NANTSHORT	NANTSHORT	Active antenna short circuit detection High = No antenna DC short circuit present Low = Antenna DC short circuit present
P25/NAADET0/ MISO or P14/NAADET1	NAADET	Active antenna detection input High = No active antenna present Low = Active antenna is present
P15/ANTON	ANTON	Active antenna power on output High = Power supply to active antenna is switched on Low = Power supply to active antenna is switched off

Table 3-14. Antenna Detection I/O Settings

GPSMODE11 (Reset = PU)	GPSMODE10 (Reset = PU)	GPSMODE9 (Reset = PU)	Location of NAADET	Comment
0	0	0	P25/NAADET0/MISO	
0	0	1	P25/NAADET0/MISO	
0	1	0	P14/NAADET1	Reserved for further use. Do not use this setting.
0	1	1	P14/NAADET1 (Default)	
1	0	0	P14/NAADET1	Reserved for further use. Do not use this setting.
1	0	1	P14/NAADET1	Reserved for further use. Do not use this setting.
1	1	0	P25/NAADET0/MISO	
1	1	1	P25/NAADET0/MISO	

The Antenna Supervisor Software will be configured as follows:

1. Enable Control Signal
2. Enable Short Circuit Detection (power down antenna via ANTON if short is detected via NANTSHORT)
3. Enable Open Circuit Detection via NAADET

3.4 External Connections for a Working GPS System

Figure 3-2. Example of an External Connection

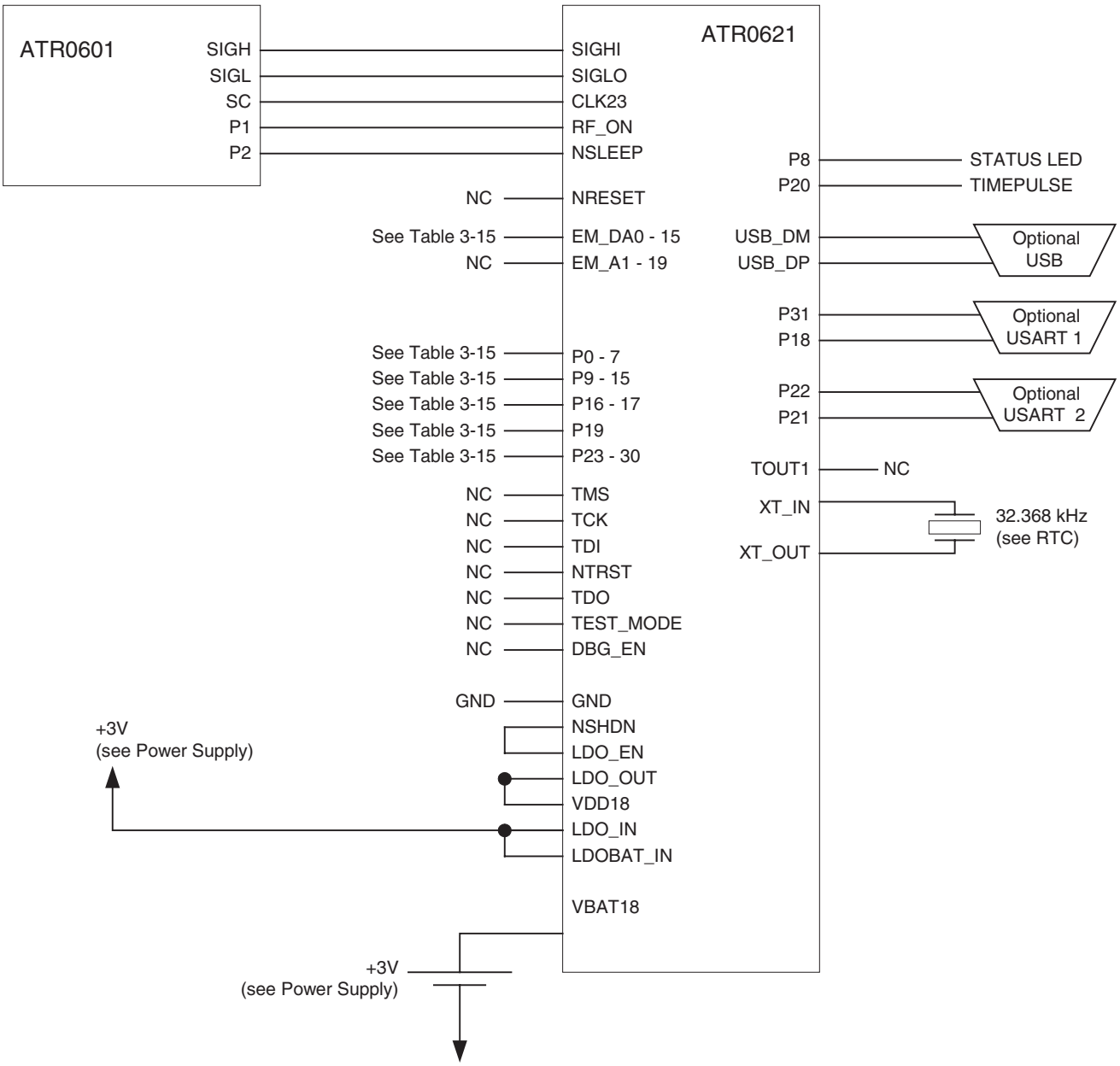


Table 3-15. Recommended Pin Connection

Pin Name	Recommended External Circuit
P0/NANTSHORT	Internal pull-down resistor; can be left open.
P1/GPSMODE0	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if configured as output by user application. If this pin is left open, the GPSMODE pin configuration feature must be completely disabled by user application.
P2/BOOT_MODE	Internal pull-down resistor, **leave open**.
P3/NCS1	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P4/NCS0	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P5/NWE/NWR0	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P6/NOE/NRD	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P7/NUB/NWR1	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P8/STATUSLED	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P9/EXTINT0	**Pull-up resistor to VDD18** or pull-down resistor to GND or connect to GND or VDD18 if unused. Never leave open.
P10/EM_A0/NLB	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P11/EM_A21	Pull-up resistor to VDD18 or **pull-down resistor to GND** (this pin is used as address line EM_A21 by standard firmware, do not connect to GND or VDD18 directly). Never leave open.
P12/NCS2/GPSMODE2	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application, or **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P13/EXTINT1/GPSMODE3/ NCS3	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application, or **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 10. Never leave open.
P14/SCK0/GPSMODE4	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P15/ANTON	Internal pull-down resistor; can be left open.
P16/NWD_OVF	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P17/SCK1/GPSMODE5	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P18/TXD1	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.

Note: "Never leave open" means: This pin needs a defined level, even if VDD18 is not supplied and system is in backup mode.

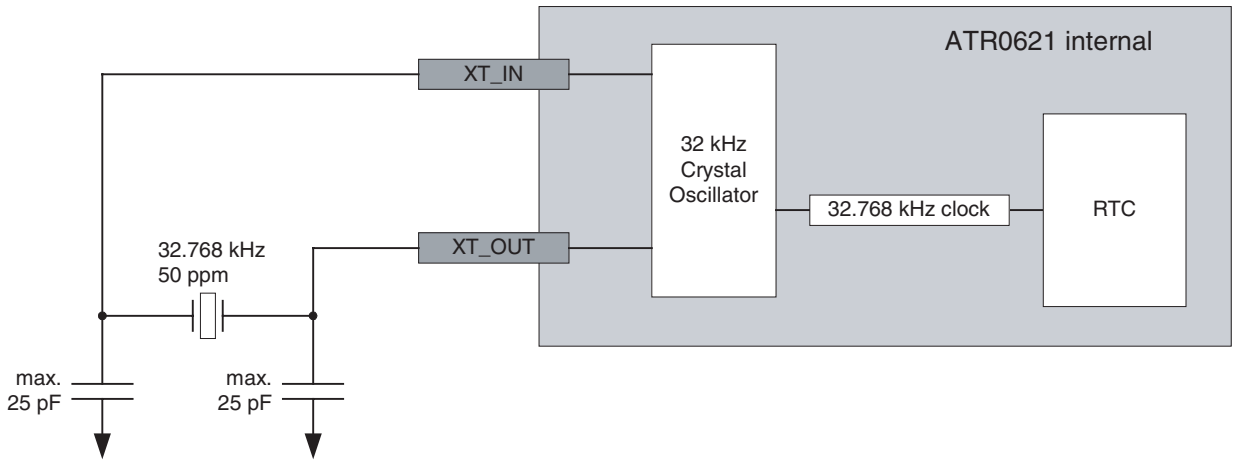
Table 3-15. Recommended Pin Connection (Continued)

Pin Name	Recommended External Circuit
P19/SIGLO2/GPSMODE6	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P20/SCK2/TIMEPULSE	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P21/TXD2	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P22/RXD2	**Pull-up resistor to VDD18** or connect to VDD18 if unused. Pull-down resistor also possible if used as GPIO input by user application. Never leave open.
P23/SCK/GPSMODE7	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P24/MOSI/GPSMODE8	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P25/MISO/GPSMODE9	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P26/NSS/NPCS0/ GPSMODE10	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Use pull-up resistor to VDD18, if SPI is used. Never leave open.
P27/NPCS1/GPSMODE11	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P28/EM_A20/NPCS2	Output in default ROM firmware: **leave open**; only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and not always driven from external sources.
P29/NPCS3/GPSMODE12	Pull-up resistor to VDD18 or pull-down resistor to GND if used as input by user application; **connect to GND** or VDD18 if unused or used as GPSMODE pin only. See GPSMODE definitions in "Setting GPSMODE0 to GPSMODE12" on page 10. Can be left open if not used as GPSMODE pin and configured as output by user application.
P30/AGCOUT0	Internal pull-up resistor, **leave open**.
P31/RXD1	**Pull-up resistor to VDD18** or connect to VDD18 if unused. Pull-down resistor also possible if used as GPIO input by user application. Never leave open.
EM_DA0 to EM_DA15	If no external memory is used, can be left open (internal pull-down). If an external memory is connected to these pins, a defined level is needed when all external memories are inactive.

Note: "Never leave open" means: This pin needs a defined level, even if VDD18 is not supplied and system is in backup mode.

4. Oscillator

Figure 4-1. Crystal Connection



5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Symbol	Min.	Max.	Unit
Operating Free Air Temperature Range			–40	+85	°C
Storage Temperature			–60	+150	°C
DC Supply Voltage	VDD18		–0.3	+1.95	V
DC Supply Voltage	VDDIO		–0.3	+1.95	V
DC Supply Voltage	VDD_USB		–0.3	+3.6	V
DC Supply Voltage	LDO_IN		–0.3	+3.6	V
DC Supply Voltage	LDOBAT_IN		–0.3	+3.6	V
DC Supply Voltage	VBAT		–0.3	+3.6	V
DC Input Voltage	EM_DA0 to EM_DA15, P0, P3 to P7, P10, P11, P15, P28, P30, SIGHI, SIGLO, CLK23, XT_IN, TMS, TCK, TDI, NTRST, DBG_EN, LDO_EN, NRESET		–0.3	+1.95	V
DC Input Voltage	USB_DM, USB_DP		–0.3	+3.6	V
DC Input Voltage	P1, P2, P8, P9, P12 to P14, P16 to P27, P29, P30		–0.3	+5.0	V

Note: Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

6. Power Consumption

Mode	Conditions	Typ.	Unit
Sleep	At 1.8V, no CLK23	0.065(1)	mA
Shutdown	RTC and backup SRAM only	0.007(1)	mA
Normal	Satellite acquisition	25	mA
	Normal tracking on 6 channels with 1 fix/s; each additional active tracking channel adds 0.5 mA	14	mA
	All channels disabled	11	mA

Note: 1. Specified value only

7. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	DC Supply Voltage Core		VDD18	VDD18	1.65	1.8	1.95	V	
1.2	DC Supply Voltage VDDIO Domain(1)		VDDIO	VDDIO	1.65	1.8/3.3	3.6	V	
1.3	DC Supply Voltage USB(2)		VDD_USB	VDDUSB	3.0	3.3	3.6	V	
1.4	DC Supply Voltage Backup Domain(3)		VBAT18	VBAT18	1.65	1.8	1.95	V	
1.5	DC Output Voltage VDD18			$V_{O,18}$	0		VDD18	V	
1.6	DC Output Voltage VDDIO			$V_{O,IO}$	0		VDDIO	V	
1.7	Low-level Input Voltage VDD18 Domain	VDD18 = 1.65V to 1.95V		$V_{IL,18}$	–0.3		0.3 × VDD18	V	
1.8	High-level Input Voltage VDD18 Domain	VDD18 = 1.65V to 1.95V		$V_{IH,18}$	0.7 × VDD18		VDD18 + 0.3	V	
1.9	Low-level Input Voltage VDDIO Domain	VDDIO = 1.65V to 3.6V		$V_{IL,IO}$	–0.3		0.3 × VDDIO	V	
1.10	High-level Input Voltage VDDIO Domain	VDDIO = 1.65V to 3.6V		$V_{IH,IO}$	0.7 × VDDIO		5.0	V	
1.11	Low-level Input Voltage VBAT18 Domain	VBAT18 = 1.65V to 1.95V	P9, P13, P22, P31	$V_{IL,BAT}$	–0.3		0.41	V	
1.12	High-level Input Voltage VBAT18 Domain	VBAT18 = 1.65V to 1.95V	P9, P13, P22, P31	$V_{IH,BAT}$	1.46		5.0	V	
1.13	Low-level Input Voltage USB	VDD_USB = 3.0V to 3.6V	DP, DM	$V_{IL,USB}$	–0.3		0.8	V	
1.14	High-level Input Voltage USB	VDD_USB = 3.0V to 3.6V	DP, DM	$V_{IH,USB}$	2.0		VDD_USB + 0.3	V	

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

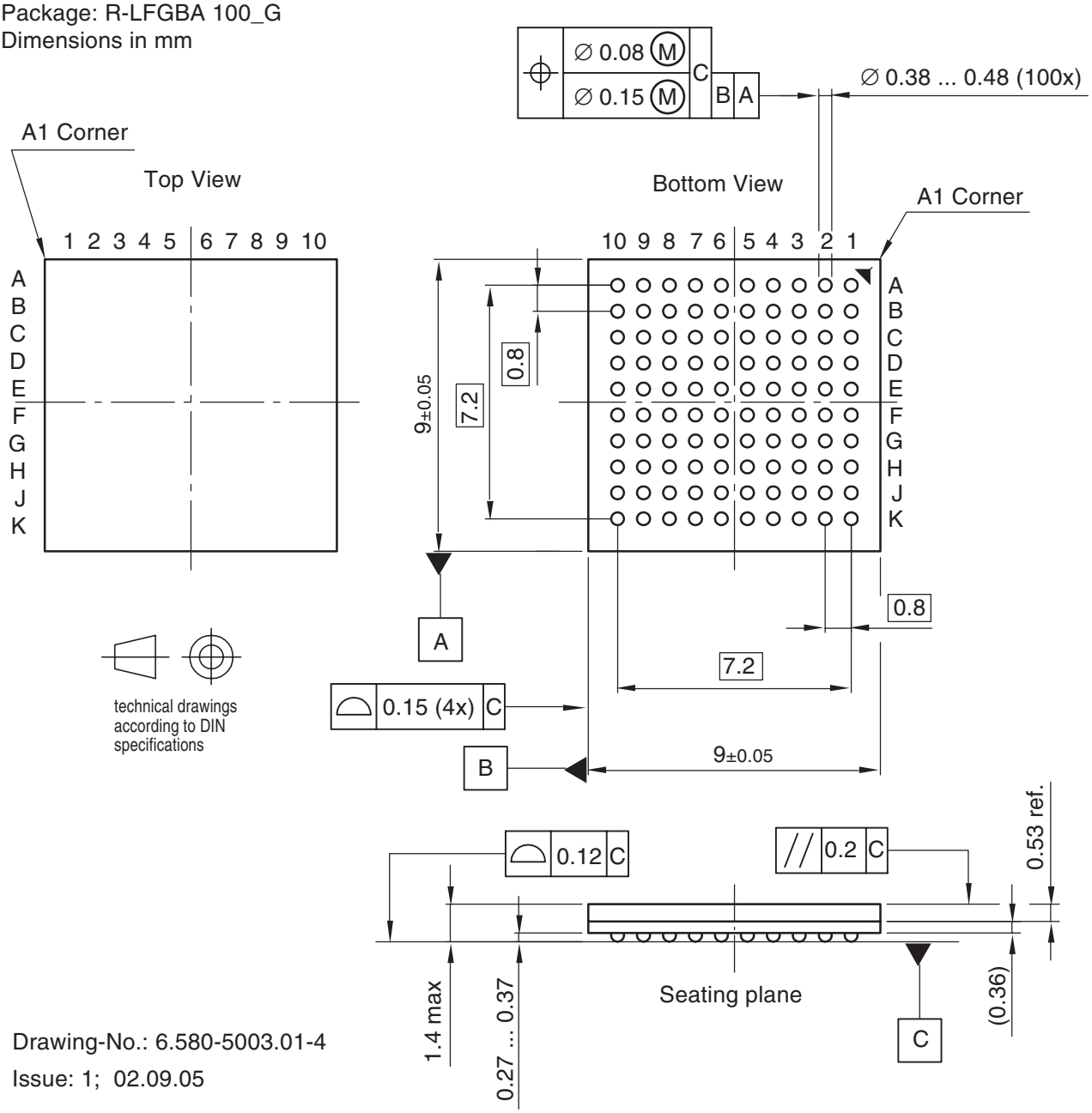
Notes:
1. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
2. Values defined for operating the USB interface. Otherwise VDD_USB may be connected to 1.8V or 0V supply.
3. Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT.

8. Ordering Information

Extended Type Number	Package	Remarks
ATR0621-7FQY	LFBGA100	9 mm × 9 mm, 0.80 mm pitch, Pb-free

9. Package LFBGA100

Package: R-LFGBA 100_G
Dimensions in mm



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