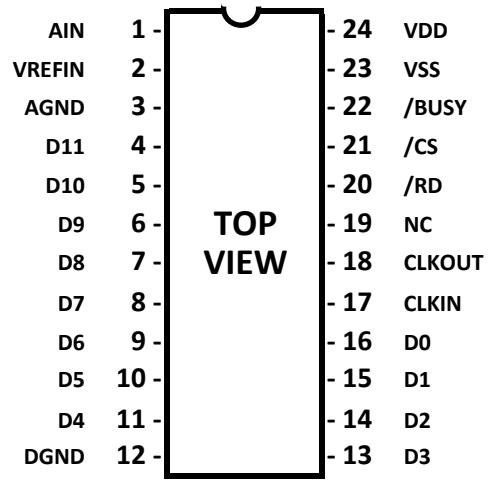
Anloy Technologies

High Speed 12-Bit A/D Converter with External Reference Input

AT912AXS

General Description

The **AT912AXS** is a custom replacement device manufactured by Anloy Technologies designed to be a near identical solution for the obsolete ADC912A in applications where the HBEN function of the ADC912 is not required. The AT912AXS is also custom manufactured to exceed the original ADC912A temperature range of -40°C to +85°C and instead is rated for -55°C to +125°C while still maintaining a footprint compatible with the ADC912AFS layout. The Analog input range is pre selected for 0 to +10V operation, other operation ranges are available.



24 Lead Wide Body Ceramic SOIC

Electrical Specifications

VDD = +5V ± 5%, VSS = -11.4C to -15.75C, VREFIN = -5V, Analog input 0V to 10V, External FCLK = 1.25MHz, Temp Range of -55°C to +125°C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Max	Unit
Static Accuracy					
Integral Nonlinearity	INL		-1	+1	LSB
Differential Nonlinearity	DNL		-1	+1	LSB
Offset Error	VZSE	VDD=+5V, VSS=-12V	-5	+5	LSB
Gain Error	GFSE	VDD=+5V, VSS=-12V	-6	+6	LSB
Analog Input					
Input Voltage Range	VIN		0	10	V
Input Current Range	IIN		0	3	mA
Power Supplies					
Positive Supply Current	IDD	VDD=+5V		7	mA
Negative Supply Current	ISS	VSS=-12V		10	mA
Power Consumption	PDISS	VDD=+5V, VSS=-12V		155	mW
Power Supply Rejection Ratio	PSRR+	ΔVDD=±5%, AIN=10V		4	LSB
	PSRR-	ΔVDD=±5%, AIN=10V		4	LSB

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Electrical Specifications

Digital Inputs					
Logic Input High Voltage	VINH		2.4		V
Logic Input Low Voltage	VINL			0.8	V
Logic Input Current	IIN	/CS, RD; VIN = 0 to VDD		±10	µA
		CLKIN; VIN = 0 to VDD		±20	µA
Digital Input Capacitance	CIN			10	pF
Digital Outputs					
Logic Output High Voltage	VOH	/CS, /RD	4		V
Logic Output Low Voltage	VOL	/CS, /RD		0.4	V
Three-State Output Leakage	IOZ	/CS, /RD		10	µA
Digital Output Capacitance	COUT	Digital Inputs, /CS, /RD, CLKIN		15	pF
Dynamic Performance					
Conversion Time	TC	fCLK = 1.25 MHz			
		Synchronous Clock		10.4	µs
		Asynchronous Clock	10.4	11.2	µs
/CS to /RD Setup Time	t1	(Note 3)	0		ns
/RD to /BUSY Propagation Delay	t2	CL = 50 pF		150	ns
Data Access Time After READ	t3	CL = 100 pF (Note 3)		125	ns
Read Pulse width	t4	(Note 3)	90		ns
/CS to /RD Hold Time	t5	(Note 3)	0		ns
Data Setup after /BUSY	t6	CL = 100 pF		90	ns
Delay between Successive Reads	t10	(Note 3)	350		ns

Note 1: Performance guaranteed over supply range by testing end point errors (power-supply rejection) and the supply extremes

Note 2: VDD=+5V, VSS=-12V, VREF=-5V

Note 3: Guaranteed by Design

Note 4: All inputs are 0V to +5V swing with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V

Absolute Maximum Ratings

VDD to DGND	-0.3V to +7V
VSS to DGND	+0.3V to -7V
VREFIN to DGND	VSS to VDD
AGND to DGND	-0.3V to VDD +0.3V
AIN to AGND	-15V to +15V
Digital Input Voltage to DGND	-0.3V to VDD +0.3V
Digital Output Voltage to DGND	-0.3V to VDD +0.3V
Operational Temperature Range	-55°C to +125°C