ARM®-based 32-bit Cortex®-M4 Wireless BLE MCU with 256 KB Flash, sLib, 11 timers, 1 ADC, 2 CMP, 7 communication interfaces (CAN & OTGFS)

Features

- **Wireless Bluetooth module**
  - Dual core Bluetooth® SIG specification 5.0 compliant
  - 2.4 GHz low-power transceiver
  - Clocks: 16 MHz crystal oscillator, 64 MHz PLL, internal 32 kHz clock
  - Peripherals: 8 x GPIOs with 2-channel PWM, 1 x UART (UART21 connected to MCU USART3)
- **Core: ARM® 32-bit Cortex®-M4 CPU**
  - 150 MHz maximum frequency, with a memory protection unit (MPU)
  - Single-cycle multiplication and hardware division
  - DSP instructions
- **Memories**
  - 256 Kbytes of internal Flash memory
  - 18 Kbytes of boot memory used as a Bootloader
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - 32 Kbytes of SRAM
- **Power control (PWC)**
  - 2.6 to 3.6 V supply
  - Power on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep, and Standby modes
  - V_{BAT} for ERTC and 20 x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - External master clock input
  - 48 MHz internal factory-trimmed high speed clock (HICK), accuracy ±1 % at T_A = 25 °C and ±2 % at T_A = -40 to +105 °C
  - PLL flexible 31 to 500 multiplication and 1 to 15 division factor
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1 x 12-bit 2 MSPS A/D converter, up to 8 external input channels
  - Temperature sensor (V_{TS}) and internal reference voltage (V_{INTRV})
  - 2 x comparators (CMP)
- **DMA**
  - 2 x 7-channel DMA controllers, 14 channels in total
- **Fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 11 timers (TMR)**
  - Up to 6 x 16-bit and 2 x 32-bit general-purpose timers, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarms, subsecond accuracy, and hardware calendar; supports calibration**
- **Up to 7 communication interfaces**
  - I^2C interface for SMBus/PMBus support
  - 3 x USARTs, with ISO7816 interface, LIN, IrDA and modem control
  - SPI (36 Mbit/s)
  - CAN (2.0B Active), with 256-bytes dedicated buffer
  - OTGFS interface, PHY, with 1280-bytes dedicated buffer
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug modes**
  - Serial wire debug (SWD)
- **Operating temperatures: -40 to +105 °C**
- **Packages**
  - QFN48 7 x 7 mm

Table 1. AT32WB415 device summary

Flash	Part number
256 KBytes	AT32WB415CCU7-7

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1 Descriptions

The AT32WB415 supports dual mode Bluetooth 5.0 with programmable protocol specification, 2 Mbit/s data transfer. It also embeds a high-performance RF transceiver where the advanced interference filter and fast self-gain control mechanism makes it possible for the device to run smoothly even in a highly disturbed environment.

The AT32WB415 is based on the high-performance ARM® Cortex®-M4 32-bit RISC core running up to 150 MHz. The Cortex®-M4 core features a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32WB415 embeds high-speed memories (up to 256 KBytes of internal Flash memory and 32 KBytes of SRAM), enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib”, functioning as a security area with code-executable only.

The device features one 12-bit ADC, two analog comparators (CMP), five general-purpose 16-bit timers, two 32-bit general-purpose timer, one advanced timer, and one low-power ERTC. It supports standard and advanced communication interfaces: I^2C, SPI, 3 + 1 USART/UARTs, SDIO, and CAN.

The AT32WB415 operates in the -40 to +105 °C temperature range, with a power supply from 2.6 to 3.6 V. A comprehensive set of power-saving modes meet the requirements of low-power applications.

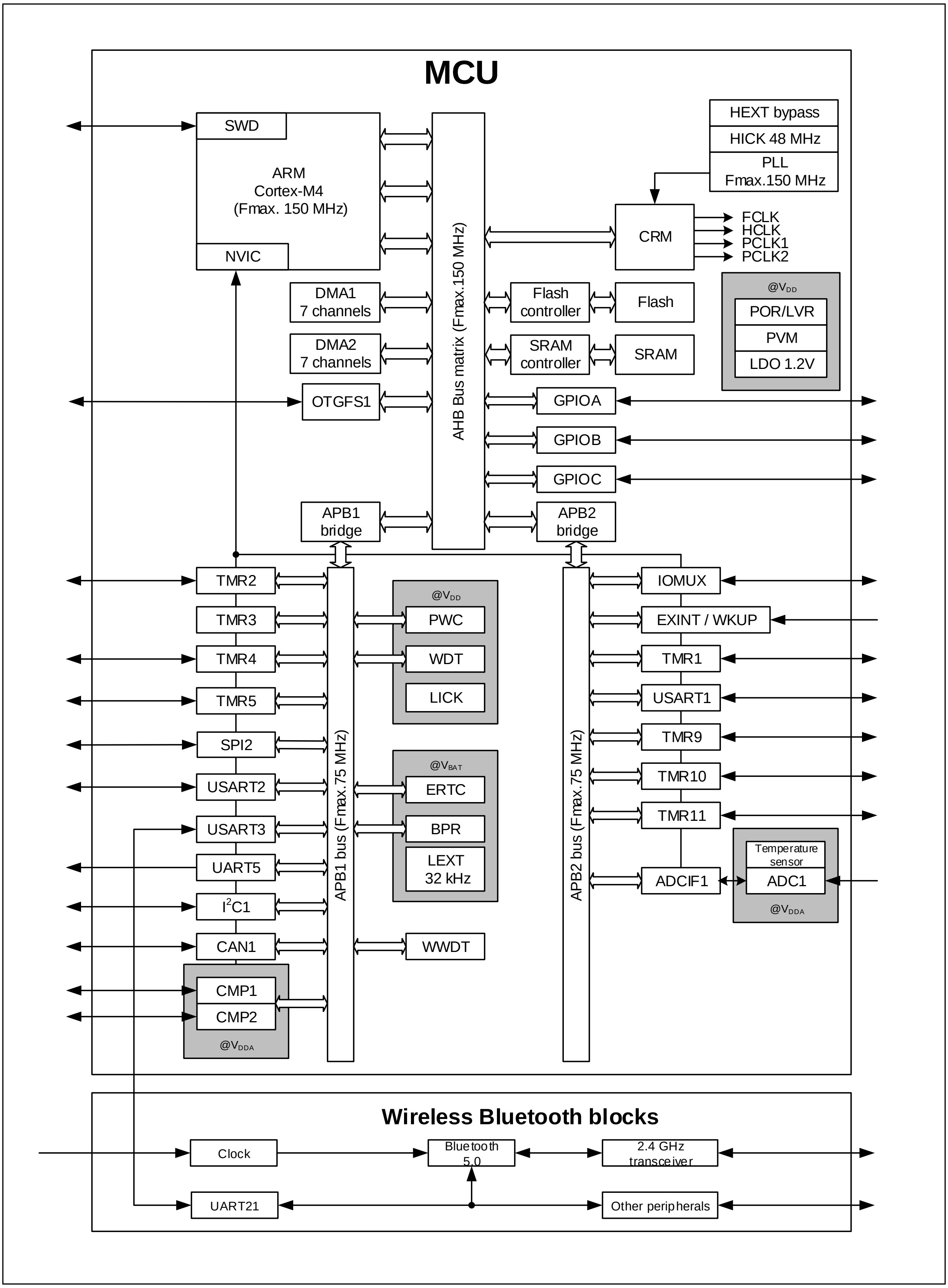
Table 2. AT32WB415 features and peripheral counts

Part Number		AT32WB415CCU7-7
CPU frequency (MHz)		150
Flash (KBytes)		256
SRAM (KBytes)		32
Timers	Advanced	1
	32-bit general-purpose	2
	16-bit general-purpose	5
	SysTick	1
	WDT	1
	WWDT	1
	ERTC	1
Communication	I^2C	1
	SPI	1
	USART(1)	3 (MCU) (2) + 1 (Bluetooth)
	OTGFS	1
	CAN	1
Analog	12-bit ADC numbers/ channels	1
		8
	Comparator	2
GPIO		22 (MCU) + 8 (Bluetooth))
Operating temperatures		-40 °C to +105 °C
Packages		QFN48 7 x 7 mm

(1) The UART interconnected between MCU and Bluetooth blocks is not included.
(2) MCU UART5 has only TX capability.

Figure 1 shows the block diagram of the AT32WB415.

Figure 1. AT32WB415 block diagram



2 Wireless Bluetooth functionality overview

2.1 Introduction

- Dual mode Bluetooth® specification 5.0 compliant
- 2.4 GHz low-power transceiver
- Clock sources
  - 16 MHz crystal
  - 64 MHz PLL
  - 32 kHz internal clock
- Peripherals
  - 8 x GPIOs
  - 2-channel PWM
  - 2 x UARTs (UART21 is connected to MCU USART3)
- True random number generator

2.2 General-purpose I/Os (GPIO)

Each general-purpose I/O port can be configured in input or output mode. GPIO multiplexing function is configurable by software. After a wireless Bluetooth block reset, a programming mode is entered, P04 ~ P07 pins externally connected to the programming mode are able to program the wireless Bluetooth block.

Each of the GPIO ports, as a wake-up source, can wake up the wireless Bluetooth block from shutdown mode. In shutdown mode, a change of the level on the GPIO pin triggers a wake-up routine.

2.3 PWM timers

The wireless Bluetooth block contains up to 6 x 16-bit PWM timers, which can select 32 kHz or 16 MHz clock as their clock sources with a corresponding register.

The PWM timer supports two modes: Timer mode or PWM mode. An interrupt for a wireless Bluetooth block is generated in Timer mode, while a PWM waveform is generated and output on the GPIO pin in PWM mode, in order to drive external devices. Two GPIO pins have their respective PWM output.

2.4 Watchdog

The watchdog uses an internal 32 kHz for wireless Bluetooth blocks. It is a 16-bit timer with up to 16 seconds of clock cycles. It resets the whole wireless Bluetooth blocks when the counter reaches a given timeout value.

2.5 Universal asynchronous receiver transmitter (UART)

Two UARTs (UART21 and UART22) are available in the wireless Bluetooth blocks, in which, the UART21 is connected to a MCU USART3. The UART baud rate can be up to 3.2 MHz.

2.6 Security

There is a true random number generator that provides a better and more secure communication for the whole system.

3 MCU functionality overview

3.1 ARM® Cortex®-M4

The ARM Cortex®-M4 processor is the latest generation of ARM processor for embedded systems. It is a 32-bit high-performance RISC processor that features exceptional code efficiency, outstanding computational performance and advanced response to interrupts. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution.

3.2 Memory

3.2.1 Flash memory

Up to 256 KBytes of embedded Flash is available for storing programs and data. User can configure any part of the embedded Flash memory protected by the sLib, functioning as a security area with code-executable only but non-readable. “sLib” is a mechanism that protects the intelligence of solution vendors and facilitates the second-level development by customers.

There is another 18-KByte boot memory in which the bootloader is stored.

A User System Data block is included, which is used as configuration of the hardware behaviors such as read/erase/write protection and watchdog self-enable. User System Data allows to set erase/write and read protection individually.

3.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU access to memories to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited for the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

3.2.3 Embedded SRAM

32 KBytes of embedded SRAM (read/write) is accessible at CPU clock speed with 0 wait states.

3.3 Interrupts

3.3.1 Nested vectored interrupt controller (NVIC)

The AT32WB415 embeds a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 23 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

3.4 Power control (PWC)

3.4.1 Power supply schemes

- V_{DD} = 2.6~3.6 V: used as an external power supply for GPIOs and the internal blocks such as the internal regulator (LDO), etc.
- V_{DDA} = 2.6~3.6 V: used as an external analog power supply for ADC and CMP. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8~3.6 V: V_{BAT} (through power switch) supplies for ERTC, external crystal 32 kHz (LEXT), and battery powered registers (BPR) when V_{DD} is not present.

3.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR)/low voltage reset (LVR) circuitry. It is always active and allows proper operation starting from 2.6 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

3.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power down.

- Normal mode is used in Run/Sleep mode and can be used in Deepsleep mode;
- Low-power mode can be used in Deepsleep mode;
- Power down mode is used in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

This LDO operates always in its normal mode after reset.

3.4.4 Low-power modes

The AT32WB415 supports three low-power modes:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep** mode

  Deepsleep mode achieves the lowest power consumption while preserving the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT clock. The voltage regulator can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm, the OTGFS or the CMP wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire LDO power domain is powered off. The PLL, the HICK clock and the HEXT clock are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the BPR domain and Standby circuitry. The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUP pin, or an ERTC alarm occurs.

Note: ERTC, WDT, and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode.

3.5 Boot modes

At startup, BOOT0 and BOOT1 pins are used to select one of three boot options:

- Boot from Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in boot memory. It is used to reprogram the Flash memory through USART2 or OTGFS1 device mode (DFU: Device Firmware Update). *Table 3* provides the pin configurations for Bootloader.

Table 3. Pin configurations for Bootloader

Interface	Pins
USART2	PA2: USART2_TX(1) PA3: USART2_RX(1)
OTG1FS1	PA11: OTGFS1_D- PA12: OTGFS1_D+

(1) Note that pins used are not 5 V tolerant.

3.6 Clocks

After a system reset, the internal 48 MHz clock (HICK) through a divided-by-6 divider (8 MHz) is selected as the default CPU clock. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system take the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are used for the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 150 MHz. The maximum frequency of the APB domains is 75 MHz.

3.7 General-purpose I/Os (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating with or without pull-up or pull-down), or as multiplexed peripheral function ports. Most of the GPIO pins are shared with digital or analog peripherals. All GPIOs are high current-capable.

The GPIO's configuration can be locked, if needed, in order to avoid false writing to the GPIO's registers by following a specific sequence.

3.8 Remapping capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 5*, it shows the list of remappable alternate functions and the pins onto which they can be remapped. See AT32WB415 reference manual for software configuration.

3.9 Direct Memory Access Controller (DMA)

AT32WB415 features 14-channel general-purpose DMAs (7 channels for DMA1 and 7 channels for DMA2) that is able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers.

The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used for the main peripherals: SPI, I^2C, USART, advanced and general-purpose timers TMRx and ADC.

3.10 Timers (TMR)

The AT32WB415 device includes an advanced timer, up to 7 general-purpose timers and a SysTick timer.

The table below compares the features of the advanced and general-purpose timers.

Table 4. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	1
General-purpose	TMR2 TMR5	16-bit or 32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3 TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR9	16-bit	Up	Any integer between 1 and 65536	No	2	No
	TMR10 TMR11	16-bit	Up	Any integer between 1 and 65536	No	1	No

3.10.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture.
- Output compare.
- PWM generation (edge or center-aligned modes).
- One-cycle mode output.

If configured as a standard 16-bit timer, it has the same features as that of the TMRx timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMRs which have the same architecture. Thus the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

3.10.2 General-purpose timers (TMRx)

Up to 7 synchronizable general-purpose timers are available in the AT32WB415.

- **TMR2, TMR3, TMR4, and TMR5**

  The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload up/down counter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture/output compare, PWM or one-cycle mode outputs.

  These general-purpose timers can work with the advanced timers via the link feature for synchronization or event chaining. In debug mode, their counters can be frozen. Any of these general-purpose timers can be used for the generation of PWM output. Each timer has its individual DMA request mechanism.

  They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

- **TMR9**

  TMR9 is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-cycle mode output. It can be synchronized with the full-featured general-purpose timers. It can also be used as simple time bases. The counter can be frozen in debug mode.

- **TMR10 and TMR11**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channel for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the full-featured general-purpose timers. They can also be used as simple time bases. The counter can be frozen in debug mode.

3.10.3 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. Its features include:

- A 24-bit down counter.
- Auto-reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source (HCLK or HCLK/8)

3.11 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabling or not configurable through the User System Data. The counter can be frozen in debug mode.

3.12 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.13 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC).
- Twenty 32-bit battery powered registers.

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value is also available in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms and one periodic wakeup from Deepsleep or Standby mode.
- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output.

The alarm register is used to generate an alarm at a given time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

The prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered register (BPR) is a 32-bit register used to store 80 bytes of user application data. Battery powered register is not reset by a system reset or power reset, or when the device wakes up from the Standby mode.

ERTC and 20 x BPR registers are powered through a power switch. When V_{DD} is present, the switch selects V_{DD} as a power supply, or V_{BAT} is used as supply source.

3.14 Communication interfaces

3.14.1 Serial peripheral interface (SPI)

The SPI interface is able to communicate at up to 36 Mbits/s in slave and master modes in half-duplex mode. The prescaler generates several master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card/MMC/SDHC modes. The SPI interface can be served by a DMA controller.

The Chip Select state (CS) is controlled by software, for the SPI_CS is not available. SPI slave mode is less recommended.

3.14.2 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32WB415 embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2, and USART3) and one universal asynchronous receiver transmitter (UART5). Among them, the USART3 is internally connected to the wireless Bluetooth blocks, while the UART5 has only TX capability.

These four interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. They also offer hardware management of CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

All interfaces are able to communicate at a speed of up to 4.6875 Mbit/s.

3.14.3 Inter-integrated-circuit interface (I^2C)

The I^2C bus interface can operate in multi-master and slave modes. It supports standard mode (max. 100 kHz) and fast mode (max. 400 kHz).

The interface supports 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included. The I^2C interface can be served by DMA and supports SMBus 2.0/PMBus.

3.14.4 Controller area network (CAN)

The controller area network (CAN) is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages, and 14 scalable filter banks. It also has dedicated 256 bytes of buffer, which is not shared with any other peripherals.

To guarantee transmission, according to the clock accuracy requirements in CAN 2.0 specification, the CAN clock source should be the PLL clock sourced by HEXT.

3.14.5 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32WB415 embeds one OTG full-speed (12 Mb/s) module that consists of PHY and can be set as a device/host. The OTGFS peripheral has software-configurable endpoint configuration and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock that is generated by a PLL sourced by HEXT.

OTGFS has the major features such as:

- 1280 Kbytes of buffer (not shared with any other peripherals).
- 8 x IN + 8 x OUT endpoints (including endpoint 0, device mode)
- 16 channels (host mode).
- SOF output.
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - In Host mode: full-speed and low speed.
  - In Device mode: full-speed.

3.15 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

3.16 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converters (ADC) is embedded into AT32WB415 device. It supports conversions in single mode or sequential mode. This ADC also shares up to 8 external channels and two internal channels, with the internal channels connected to the temperature sensor (V_{TS}) and the internal reference voltage (V_{INTRV}), respectively. In sequential mode, automatic conversion is performed on a selected group of analog channels.

This ADC can be served by the DMA controller.

A voltage monitor allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is above the programmed threshold value.

The events generated by the general-purpose timers (TMRx) and advanced timer (TMR1) can be linked to the regular conversion and preempted conversion of ADC, respectively. ADC conversion can be synchronized with clocks through the application program.

3.16.1 Temperature sensor (V_{TS})

The temperature sensor has to generate a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The offset of this line varies from one chip to another due to process variations. The internal temperature sensor is more suited for the applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

3.16.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage output for the ADC. V_{INTRV} is internally connected to the ADC1_IN17 channel.

3.17 Comparator (CMP)

The AT32WB415 embeds two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis, speed, selectable output polarity.

The reference voltage can be one of the following:

- External I/O;
- Internal reference voltage (V_{INTRV}) or its submultiple (1/4, 1/2, 3/4). Refer to *Table 49* for more information on internal reference voltage.

The comparator can wake up Deepsleep mode. They can redirect output to timers, and can be also combined into a window comparator.

3.18 Programming and debugging interface

The ARM® SWD interface is embedded in the AT32WB415 device. It is a serial wire debug interface that enables a serial wire debugger to be connected to the PA13 and PA14 of the target device for programming and debugging purposes.

Bluetooth module is programmed with codes through another set of SPI interface via P04, P05, P06 and P07 pins.

4 Pin functional definitions

Figure 2. AT32WB415 QFN48 pinout

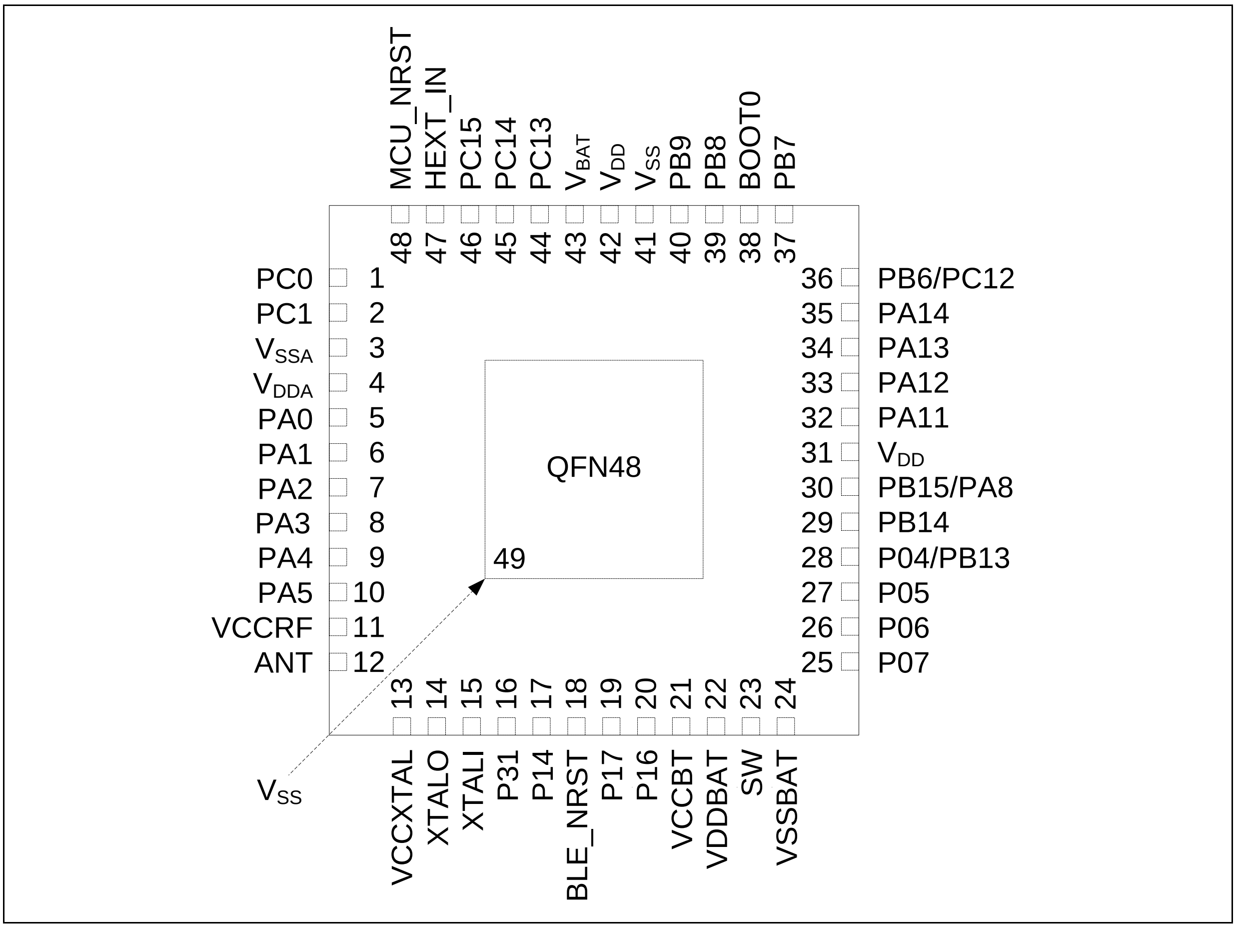


Table 5. AT32WB415 series pin definitions

Pin number	Pin name	Type(1)	IO level(2)	Main function	Multiplexed functions(3)	
					Default	Remap
1	PC0	I/O	-	MCU PC0	ADC1_IN10	-
2	PC1	I/O	-	MCU PC1	ADC1_IN11	-
3	V_{SSA}	S	-	V_{SSA}	MCU analog ground	
4	V_{DDA}	S	-	V_{DDA}	MCU analog power	
5	PA0-WKUP	I/O	-	MCU PA0	ADC1_IN0 / WKUP / CMP1_OUT(4) / CMP1_INP2 / CMP1_INM6 / USART2_CTS / TMR2_CH1(4) / TMR2_EXT(4) / TMR5_CH1(4)	TMR1_EXT
6	PA1	I/O	-	MCU PA1	ADC1_IN1 / CMP1_INP1 / USART2_RTS / TMR2_CH2(4) / TMR5_CH2(4)	-
7	PA2	I/O	-	MCU PA2	ADC1_IN2 / CMP2_OUT(4) / CMP2_INP2 / CMP2_INM6 / USART2_TX / TMR2_CH3(4) / TMR5_CH3 / TMR9_CH1(4)	-
8	PA3	I/O	-	MCU PA3	ADC1_IN3 / CMP2_INP1 / USART2_RX / TMR2_CH4(4) / TMR5_CH4 / TMR9_CH2(4)	-

Pin number	Pin name	Type[1]	IO level[2]	Main function	Multiplexed functions[3]	
					Default	Remap
9	PA4	I/O	-	MCU PA4	ADC1_IN4 / CMP1_INM4 / CMP2_INM4 / USART2_CK	-
10	PA5	I/O	-	MCU PA5	ADC1_IN5 / CMP1_INP0 / CMP1_INM5 / CMP2_INM5	-
11	VCCRF	S	-	VCCRF	Bluetooth RF power supply 1.6 V input	
12	ANT	RF	-	ANT	Bluetooth RF signal	
13	VCCXTAL	S	-	VCCXTAL	Bluetooth crystal power supply 1.6 V input	
14	XTALO	O	-	XTALO	Bluetooth 16 MHz crystal output	
15	XTALI	I	-	XTALI	Bluetooth 16 MHz crystal input	
16	P31	I/O	-	P31	-	
17	P14	I/O	-	P14	Bluetooth PWM4	
18	BLE_NRST	I	-	BLE_NRST	Bluetooth reset pin, low level active	
19	P17	I/O	-	P17	Bluetooth UART22_RX	
20	P16	I/O	-	P16	Bluetooth UART22_TX	
21	VCCBT	S	-	VCCBT	Bluetooth power supply 1.6 V input	
22	VDDBAT	S	-	VDDBAT	Bluetooth power supply 3.3 V	
23	SW	S	-	SW	Bluetooth DC-DC power (1.6 output after LC filtering)	
24	VSSBAT	S	-	VSSBAT	Bluetooth power ground	
25	P07	I/O	-	P07	Bluetooth programming CS/Bluetooth PWM5	
26	P06	I/O	-	P06	SCK for Bluetooth programming	
27	P05	I/O	-	P05	MISO for Bluetooth programming	
28[5]	P04	I/O	-	P04	MOSI for Bluetooth programming	
	PB13	I/O	FT	MCU PB13	TMR1_CH1C[4] / SPI2_SCK[4]	-
29	PB14	I/O	FT	MCU PB14	TMR1_CH2C[4] / SPI2_MISO[4]	TMR9_CH1
30[5]	PB15	I/O	FT	MCU PB15	TMR1_CH3C[4] / ERTC_REFIN SPI2_MOSI[4]	TMR9_CH2
	PA8	I/O	FT	MCU PA8	CLKOUT / TMR1_CH1	-
31	V_{DD}	S	-	V_{DD}	MCU digital power	
32	PA11	I/O	-	MCU PA11	OTGFS1_D- / CAN1_RX[4] / TMR1_CH4	CMP1_OUT
33	PA12	I/O	-	MCU PA12	OTGFS1_D+ / CAN1_TX[4] / TMR1_EXT	CMP2_OUT
34	PA13	I/O	FT	MCU JTMS-SWDIO	-	PA13
35	PA14	I/O	FT	MCU JTCK-SWCLK	-	PA14
36[5]	PC12	I/O	FT	MCU PC12	UART5_TX	-
	PB6	I/O	FT	MCU PB6	I2C1_SCL[4] / TMR4_CH1	USART1_TX
37	PB7	I/O	FT	MCU PB7	I2C1_SDA[4] / TMR4_CH2	USART1_RX
38	BOOT0	I	-	BOOT0	-	-
39	PB8	I/O	FT	MCU PB8	TMR4_CH3 / TMR10_CH1[4]	I2C1_SCL / CAN1_RX
40	PB9	I/O	FT	MCU PB9	TMR4_CH4 / TMR11_CH1[4]	I2C1_SDA / CAN1_TX

Pin number	Pin name	Type(1)	IO level(2)	Main function	Multiplexed functions(3)	
					Default	Remap
41	V_{SS}	S	-	V_{SS}	MCU digital ground	
42	V_{DD}	S	-	V_{DD}	MCU digital power	
43	V_{BAT}	S	-	V_{BAT}	MCU battery power supply	
44	PC13(6)	I/O	-	MCU PC13	TAMPER-ERTC(7)	-
45	PC14(6)	I/O	-	MCU PC14	LEXT_IN(7)	-
46	PC15(6)	I/O	-	MCU PC15	LEXT_OUT(7)	-
47	HEXT _IN(8)	I/O	-	HEXT _IN	HEXT_IN	-
48	MCU_NRST	I/O	-	MCU_NRST	MCU reset pin, low level active	
49	EPAD	S	-	V_{SS}	MCU digital ground	
Interconnection	PA6	I	-	MCU PA6	-	USART3_RX
	P00	O	-	P00	Bluetooth UART21_TX	
Interconnection	PA7	O	-	MCU PA7	-	USART3_TX
	P01	I	-	P01	Bluetooth UART21_RX	
Internal	PB2 / BOOT1	-	-	BOOT1	This MCU pin is always connected to V_{SS} internally (PB2 is not available).	
-	MCU PA9, PA10, PA15, PB0, PB1, PB3~5, PB10~12, PC0~11, PD2, PF4~7 are disconnected. *Note: It is good advice to configure these pins as an output mode and low level to enhance anti-interference capability and prevent extra leakage.*					

(1) I = input, O = output, S = supply, RF= radio frequency

(2) FT = 5 V-tolerant

(3) If several peripherals share the same GPI/O pin, only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding CRM peripheral clock enable register) in order to avoid conflict between functions.

(4) Multiplexed function can be remapped by software to some other port pins (if available on the used package).

(5) Internal GPIOs are wired to external pins. Thus only one of the GPIO pins and its multiplexed function can be enabled at a time, while the other GPIO pin (disabled) has to be configured in analog or floating input mode.

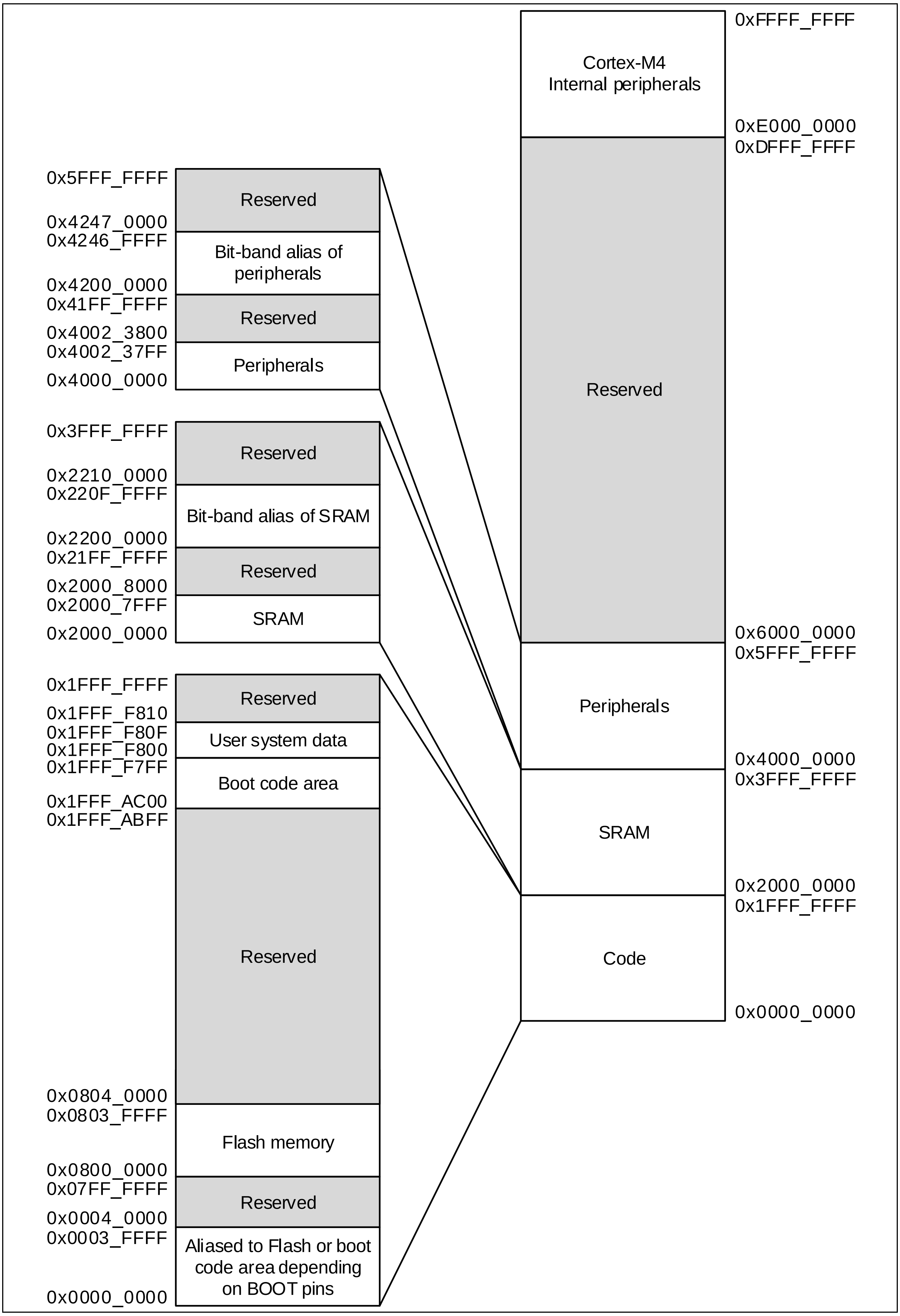
(6) PC13, PC14, and PC15 are supplied through a power switch. As the switch only sources a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited not to be used as a current source (e.g. to drive an LED).

(7) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset).

(8) Bypass mode is always enabled whenever HEXT is enabled.

5 Memory mapping

Figure 3. Memory map



6 Bluetooth electrical characteristics

Table 6. General operating conditions

Symbol	Description	Min	Typ	Max	Unit
V_{DD}	Operating voltage	2.6	3.3	3.6	V
V_{DC-DC}	DC-DC output voltage	1.4	1.6	1.8	°C
T_A	Ambient temperature	-40	25	105	°C

Table 7. Current characteristics

Symbol	Mode	Description	Min	Typ	Max	Unit
I_{DD}	Deepsleep mode	-	-	0.5	-	μA
	Sleep mode	RF OFF, 32 kHz clock ON, digital circuit hold	-	1.8	-	μA
	Run mode	Receive, V_{DD} = 3.3 V, DC-DC voltage regulator ON	-	5.1	-	mA
		Transmit, -1 dBm, V_{DD} = 3.3 V, DC-DC voltage regulator ON	-	4.8	-	mA

Table 8. GPIO characteristics

Symbol	Parameter	Description	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-	0	-	0.3	V
V_{IH}	Input high level voltage	-	V_{DD} - 0.3	-	V_{DD} + 0.3	V
V_{OL}	Output low level voltage	I_{OL} = 250 μA	0	-	0.3	V
V_{OH}	Output high level voltage	I_{OH} = -250 μA	V_{DD} - 0.3	-	V_{DD}	V

Table 9. RF characteristics

Symbol	Parameter	Description	Min	Typ	Max	Unit
General RF characteristics						
FOP	Operating frequency	-	2400	-	2480	MHz
FXTAL	Crystal frequency	-	-	16	-	MHz
RFSK	RF data transfer rate	-	-	1	2	Mbps
Transmit (1 Mbps mode)						
PO	Output power	-	-20	-1	+4	dbm
PBW	Modulation 20db bandwidth	-	-	-	1	MHz
PRF	Out of band emission	2 MHz	-	-20	-	dB
		3 MHz	-	-58	-	
Dev	Transmit FM deviation	-	115	250	300	kHz
Drift	Transmit drift in any position	-	-	-	400	Hz/μs
Receive (BLE mode)						
Max input	1E-3 BER	-	-	-10	-	dBm
RXSENS	1E-3 BER sensitivity	-	-	-96	-97	dBm
INTMOD	Intermodulation	P_{IN} = -64 dbm, P_{unwant} = -50 dbm; f0 = 2 x f1 - f2, f2 - f1 = 3	-	-25	-22	dBm

Symbol	Parameter	Description	Min	Typ	Max	Unit
		or 4 or 5 MHz				
C/ICO	Common channel C/I	-	-	7	-	dB
C/I1ST	ACS C/I 1 MHz	-	-9		-6	dB
C/I2ND	ACS C/I 2 MHz	-	-	-44	-	dB
C/I3RD	ACS C/I 3 MHz	-	-	-50	-	dB
C/I1STI	ACS C/I image channel	-	-	-25	-	dB
C/I2NDI	ACS C/I 1 MHz	-	-35		-	dB
Block	Block	@ 2339 MHz and 2484 MHz	-	-15	-	dBm
		@ 2 GHz and 3 GHz	-	-15	-	
Lkg	Leakage	@ < 1 GHz	-	-71		dBm
		@ > 1 GHz	-	-56	-	

7 MCU electrical characteristics

7.1 Test conditions

7.1.1 Minimum and maximum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

7.1.2 Typical values

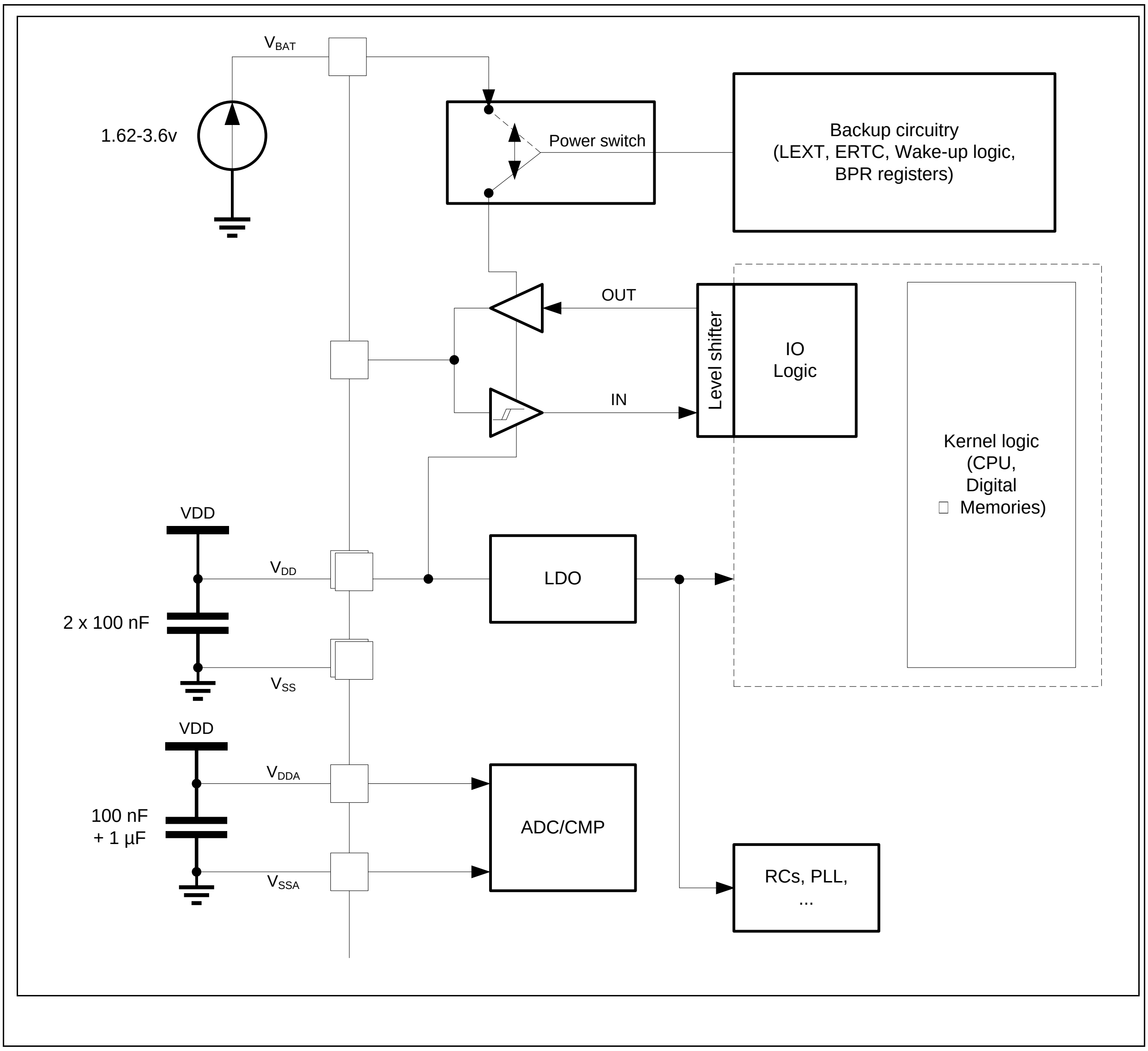
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

7.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

7.1.4 Power supply scheme

Figure 4. Power supply scheme



7.2 Absolute maximum values

7.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 10*, *Table 11*, and *Table 12*, it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 10. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on FT GPIO	V_{SS}-0.3	6.0	
	Input voltage on any other GPIO	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 11. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power line (source)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIOs and control pin	-25	

Table 12. Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

7.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2017/JS-002-2018 standard.

Table 13. ESD values

Symbol	Parameter	Conditions	Class	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2018	III	±1000	

Static latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 14. Static latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (±200 mA)

7.3 Specifications

7.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	150	MHz
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-	0	75	MHz
V_{DD}	Digital operating voltage	-	2.6	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}	V_{DD}		V
V_{BAT}	Battery powered domain voltage	-	1.8	3.6	V
T_A	Ambient temperature	-	-40	105	°C

7.3.2 Operating conditions at power-up / power-down

Table 16. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞(1)	ms/V
	V_{DD} fall time rate		20	∞	µs/V

(1) When the V_{DD} power-on rate is below 6 ms/V, make sure that the V_{DD} is higher than V_{POR} + 0.1V before accessing BPR registers.

7.3.3 Embedded reset and power control block characteristics

Table 17. Embedded reset and power management block characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	2.05	2.3	2.5	V
V_{LVR}	Low voltage reset threshold	1.85(2)	2.15	2.35	V
$V_{LVRhyst}$	LVR hysteresis	-	180	-	mV
$T_{RSTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	600	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 5. Power on reset and low voltage reset waveform

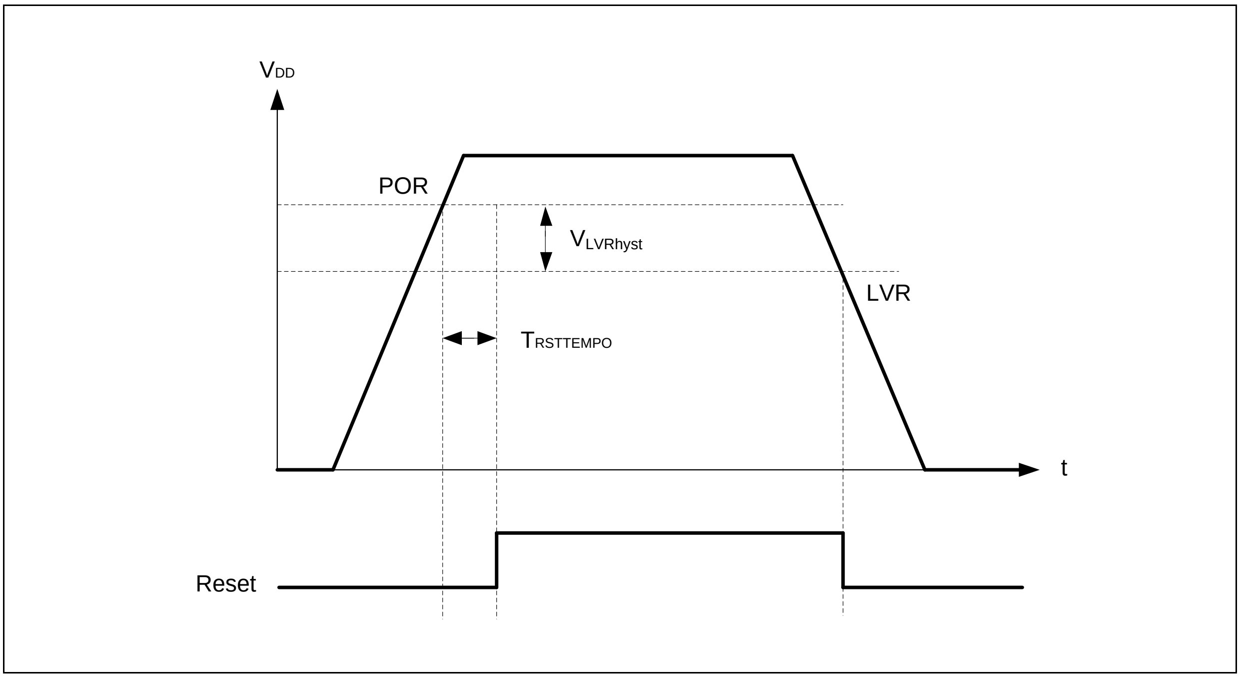


Table 18. Programmable voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge (1)	2.19	2.28	2.37	V
		Falling edge (1)	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge (1)	2.28	2.38	2.48	V
		Falling edge (1)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge (2)	2.38	2.48	2.58	V
		Falling edge (2)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge (2)	2.47	2.58	2.69	V
		Falling edge (2)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge (2)	2.57	2.68	2.79	V
		Falling edge (2)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge (2)	2.66	2.78	2.9	V
		Falling edge (2)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HSY_P} (2)	PVM hysteresis	-	-	100	-	mV

(1) PVMSEL[2:0] = 001, 010 level may not be used because it is lower than V_{POR}.
(2) Guaranteed by characterization results, not tested in production.

7.3.4 Memory characteristics

Table 19. Internal Flash memory characteristics(1)

Symbol	Parameter	Typ	Max	Unit
T_{PROG}	Programming time	40	42	μs
t_{SE}	Page erase time	6.6	8	ms
t_{ME}	Mass erase time	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 20. Internal Flash memory endurance and data retention(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

7.3.5 Supply current characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 32 MHz, 1 wait state from 33 to 64 MHz, 2 wait states from 65 to 96 MHz, 3 wait states from 97 to 128 MHz, and 4 wait states above).
- Prefetch ON.
- When the peripherals are enabled:
  - If f_{HCLK} > 72 MHz, $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$;
  - If $f_{HCLK} \leq$ 72 MHz, $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

Table 21. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				All peripherals	All peripherals	
I_{DD}	Current supply in Run mode	High speed external crystal (HEXT)(1)(2)	150 MHz	43.5	20.1	mA
			120 MHz	36.2	17.6	
			108 MHz	32.1	15.3	
			72 MHz	24.6	11.4	
			48 MHz	17.6	8.8	
			36 MHz	13.1	6.54	
			24 MHz	9.62	5.24	
			16 MHz	6.98	4.06	
			8 MHz	4.13	2.79	
			4 MHz	2.98	2.32	
			2 MHz	2.41	2.09	
			1 MHz	2.13	1.97	
			500 kHz	1.99	1.91	
			125 kHz	1.88	1.87	
		High speed internal clock (HICK)(2)	150 MHz	43.5	20.0	mA
			120 MHz	35.5	16.7	
			108 MHz	32.1	15.2	
			72 MHz	24.0	10.8	
			48 MHz	16.9	8.06	
			36 MHz	13.0	6.44	
			24 MHz	9.52	5.13	
			16 MHz	6.88	3.96	
			8 MHz	3.84	2.49	
			4 MHz	2.68	2.02	
			2 MHz	2.11	1.79	
			1 MHz	1.83	1.67	
			500 kHz	1.69	1.61	
			125 kHz	1.59	1.57	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 22. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ All peripherals	Typ All peripherals	Unit
I_{DD}	Current supply in Sleep mode	High speed external crystal (HEXT)(1)(2)	150 MHz	33.5	5.29	mA
			120 MHz	27.4	4.83	
			108 MHz	24.8	4.47	
			72 MHz	19.0	3.48	
			48 MHz	13.4	2.97	
			36 MHz	10.3	2.49	
			24 MHz	7.50	2.31	
			16 MHz	5.35	1.91	
			8 MHz	2.79	1.17	
			4 MHz	1.88	1.08	
			2 MHz	1.43	1.06	
			1 MHz	1.20	1.03	
			500 kHz	1.09	1.02	
			125 kHz	1.01	0.99	
		High speed internal clock (HICK)(2)	150 MHz	33.4	5.22	mA
			120 MHz	27.4	4.74	
			108 MHz	24.7	4.35	
			72 MHz	18.9	3.39	
			48 MHz	13.3	2.88	
			36 MHz	10.2	2.39	
			24 MHz	7.42	2.21	
			16 MHz	5.26	1.79	
			8 MHz	2.70	1.10	
			4 MHz	1.79	0.98	
			2 MHz	1.33	0.96	
			1 MHz	1.11	0.91	
			500 kHz	1.00	0.90	
			125 kHz	0.92	0.89	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 23. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max T_A = 105 °C	Unit
I_{DD}	Current supply in Run mode	High speed external crystal (HEXT)(1), all peripherals enabled	150 MHz	55.6	mA
			120 MHz	48.4	
			108 MHz	44.0	
			72 MHz	36.1	
			48 MHz	28.8	
			36 MHz	24.1	
			24 MHz	20.5	
			16 MHz	17.7	
			8 MHz	14.7	
		High speed external crystal (HEXT)(1), all peripherals disabled	150 MHz	31.1	mA
			120 MHz	28.7	
			108 MHz	26.3	
			72 MHz	22.3	
			48 MHz	19.5	
			36 MHz	17.2	
			24 MHz	15.8	
			16 MHz	14.6	
			8 MHz	13.4	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 24. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max T_A = 105 °C	Unit
I_{DD}	Current supply in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled	150 MHz	46.1	mA
			120 MHz	39.7	
			108 MHz	37.0	
			72 MHz	30.9	
			48 MHz	24.9	
			36 MHz	21.7	
			24 MHz	18.8	
			16 MHz	16.5	
			8 MHz	13.8	
		High speed external crystal (HEXT)(1), all peripherals disabled	150 MHz	16.5	mA
			120 MHz	16.0	
			108 MHz	15.6	
			72 MHz	14.6	
			48 MHz	14.1	
			36 MHz	13.5	
			24 MHz	13.4	
			16 MHz	12.9	
			8 MHz	12.1	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 25. Typical and maximum current consumptions in Deepsleep and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max(2)			Unit
			V_{DD} = 2.6 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Current supply in Deepsleep mode	LDO in run mode, HICK and HEXT OFF, WDT OFF	735	740	See(3)	4000	6600	μA
		LDO in low-power mode, LPDS1=1, HICK and HEXT OFF, WDT OFF	675	680		3480	6000	
	Current supply in Standby mode	LEXT and ERTC OFF	2.5	3.6	4.8	7.0	10.3	
		LEXT and ERTC ON	4.3	6.6	7.5	10.0	13.7	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) This value may be several times the typical value due to process variations.

Figure 6. Typical current consumption in Deepsleep mode with LDO in run mode vs. temperature at different V_{DD}

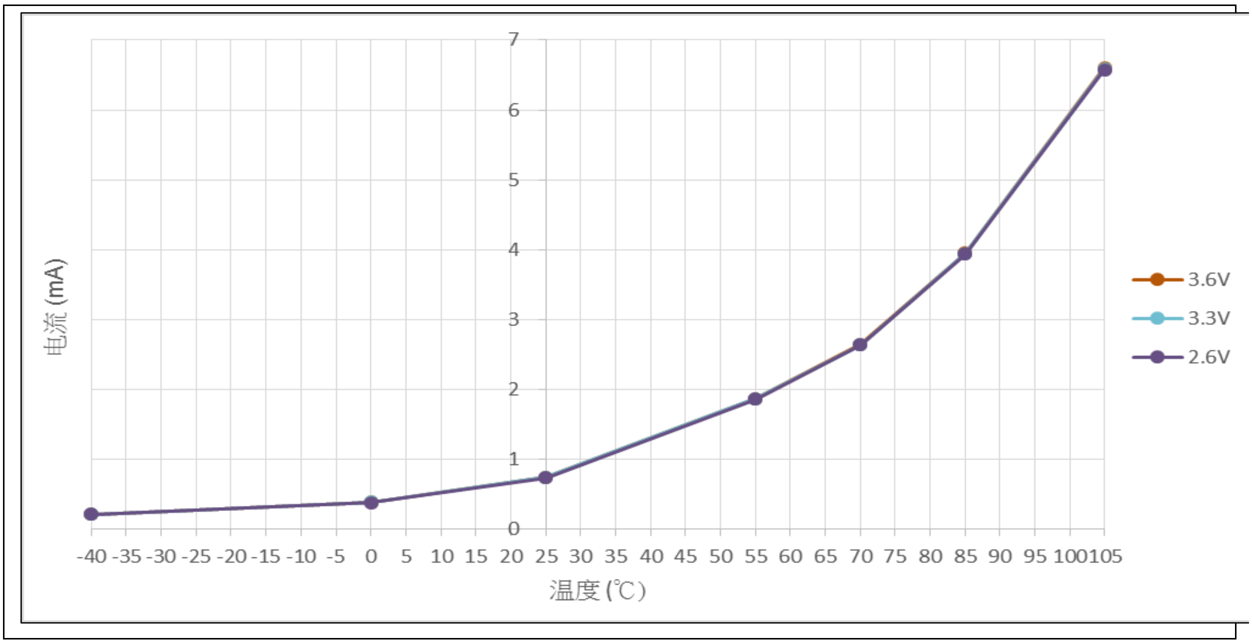


Figure 7. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different V_{DD}

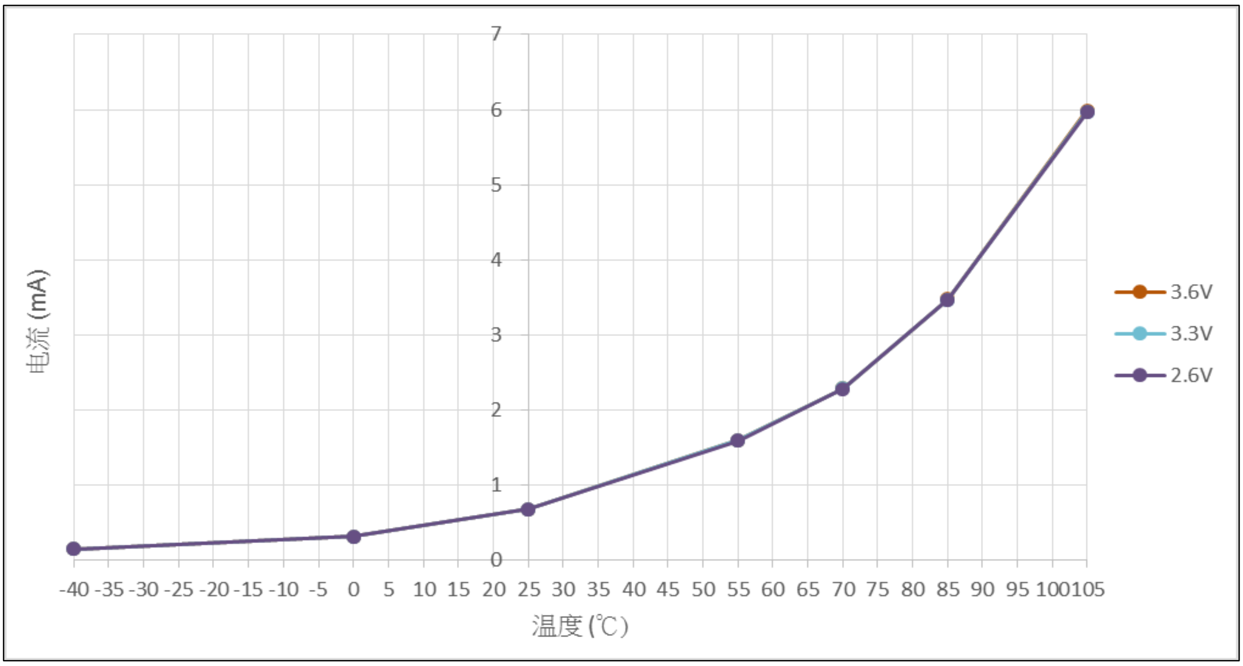


Figure 8. Typical current consumption in Standby mode vs. temperature at different V_{DD}

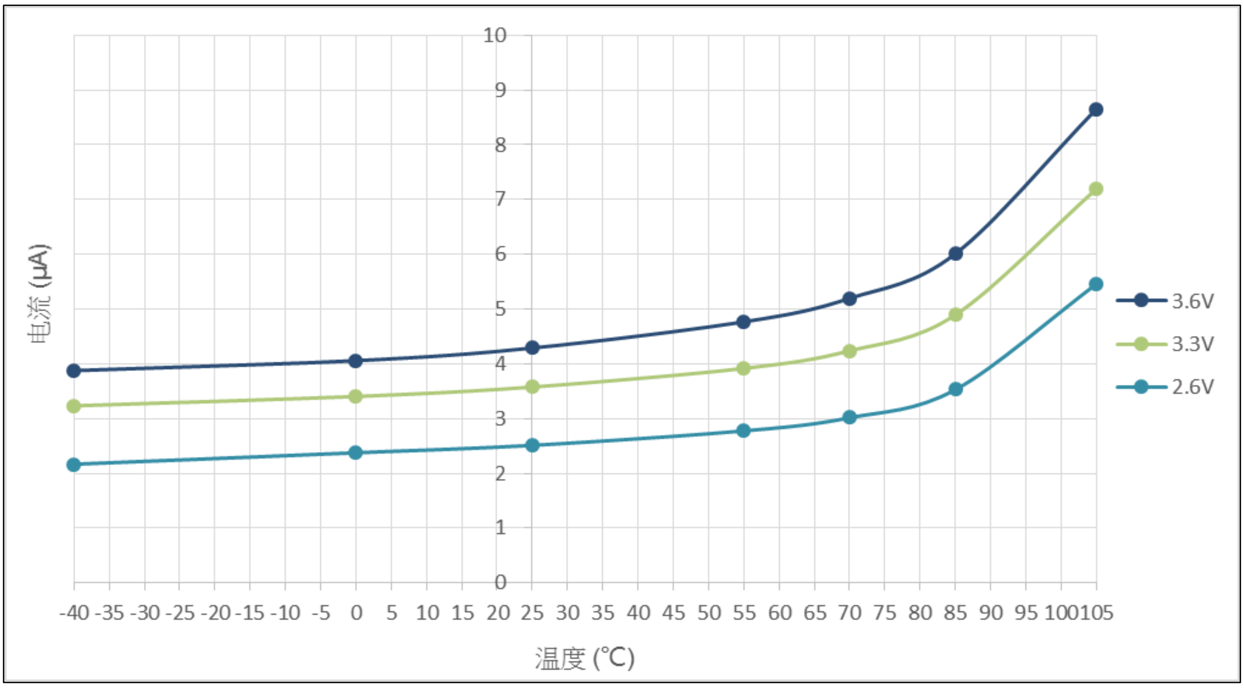
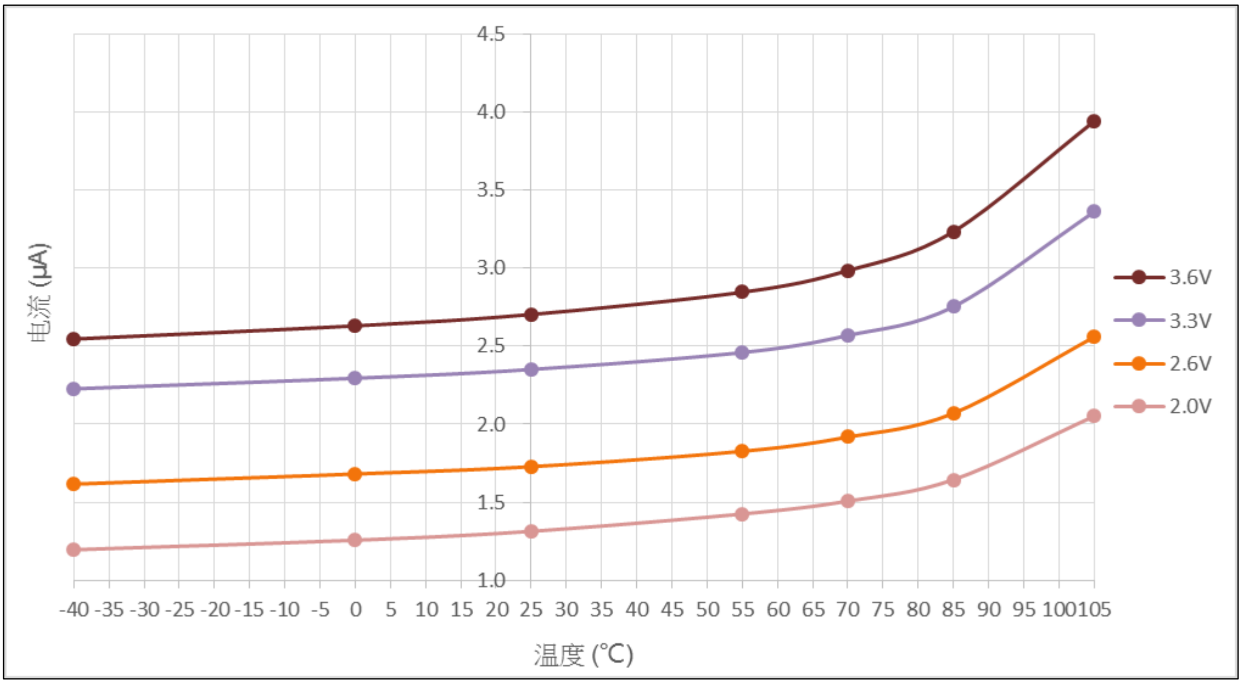


Table 26. Typical and maximum current consumptions on V_{BAT}

Symbol	Parameter	Conditions	Typ[1]			Max[2]			Unit
			V_{BAT} = 2.0 V	V_{BAT} = 2.6 V	V_{BAT} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Current supply on V_{BAT}	LEXT and RTC ON, V_{DD} < V_{LVR}	1.3	1.7	2.4	2.8	3.7	4.6	μA

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 9. Typical current consumption on V_{BAT} (LEXT and ERTC ON) vs. temperature at different V_{BAT} values



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 27. Peripheral current consumption

Peripheral		Typ	Unit
AHB	DMA1	9.32	μA/MHz
	DMA2	9.41	
	GPIOA	1.25	
	GPIOB	1.33	
	GPIOC	1.27	
	CRC	1.64	
	OTGFS1	46.3	
APB1	TMR2	8.96	
	TMR3	6.76	
	TMR4	6.73	
	TMR5	8.97	
	SPI2	2.84	
	USART2	2.40	
	USART3	2.53	
	UART5	2.68	
	I^2C1	2.66	
	CAN1	3.56	
	WWDT	0.45	
	PWC	0.38	
	CMP	0.81	
APB2	IOMUX	2.53	μA/MHz
	USART1	2.48	
	TMR1	8.74	
	TMR9	4.03	
	TMR10	2.56	
	TMR11	2.60	
	ADC1	6.92	

7.3.6 External clock source characteristics

High-speed external clock generated from an external clock source

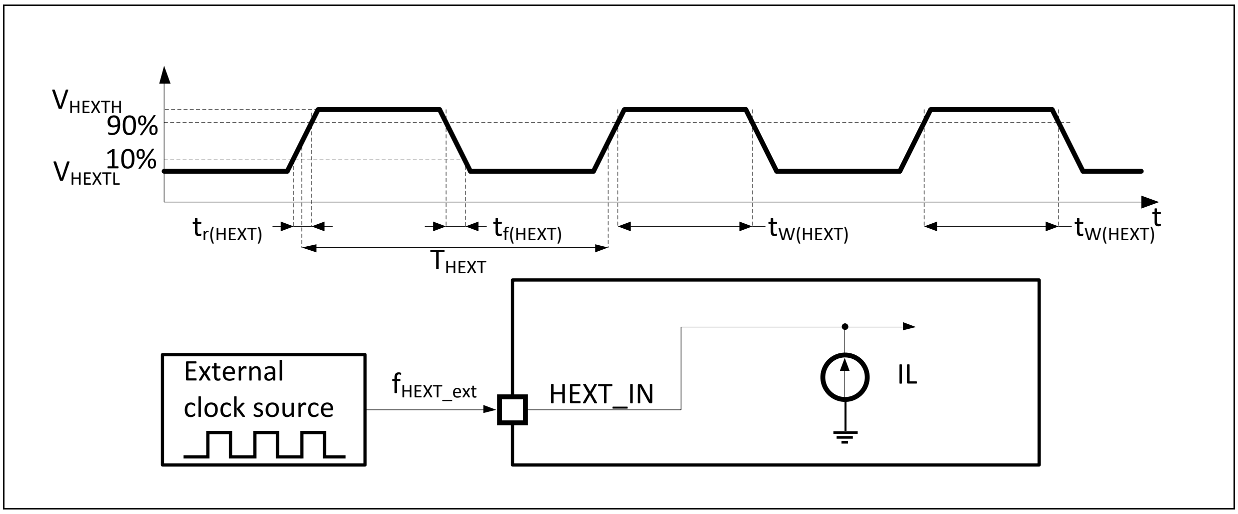
The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 28. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 10. HEXT external source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. LEXT 32.768 kHz crystal characteristics(1)(2)

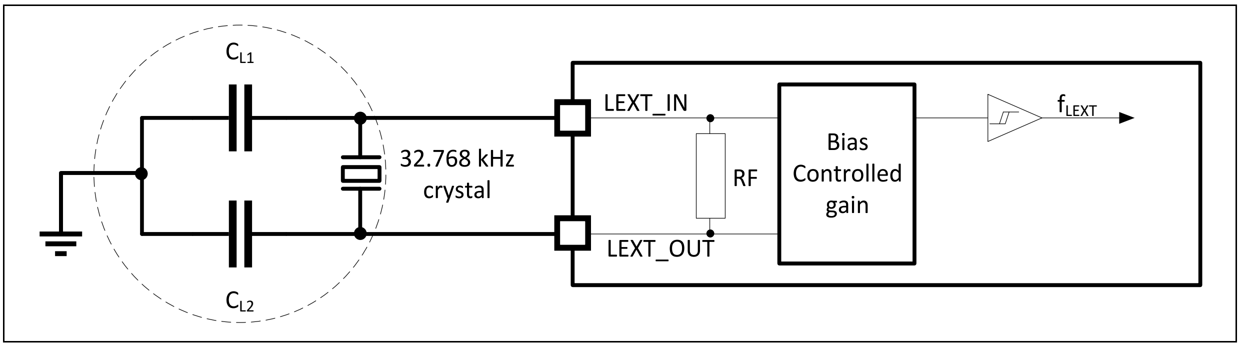
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	200	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use good quality ceramic capacitors in the 5 pF to 20 pF range and select a crystal or resonator meeting the requirements. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 11. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

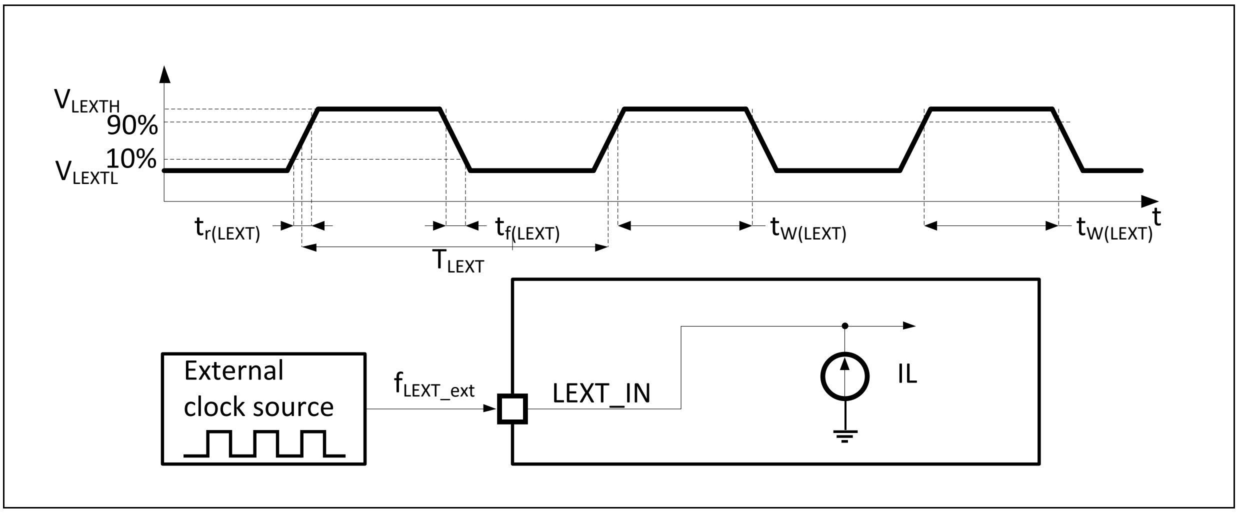
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 30. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 12. LEXT external source AC timing diagram



7.3.7 Internal clock source characteristics

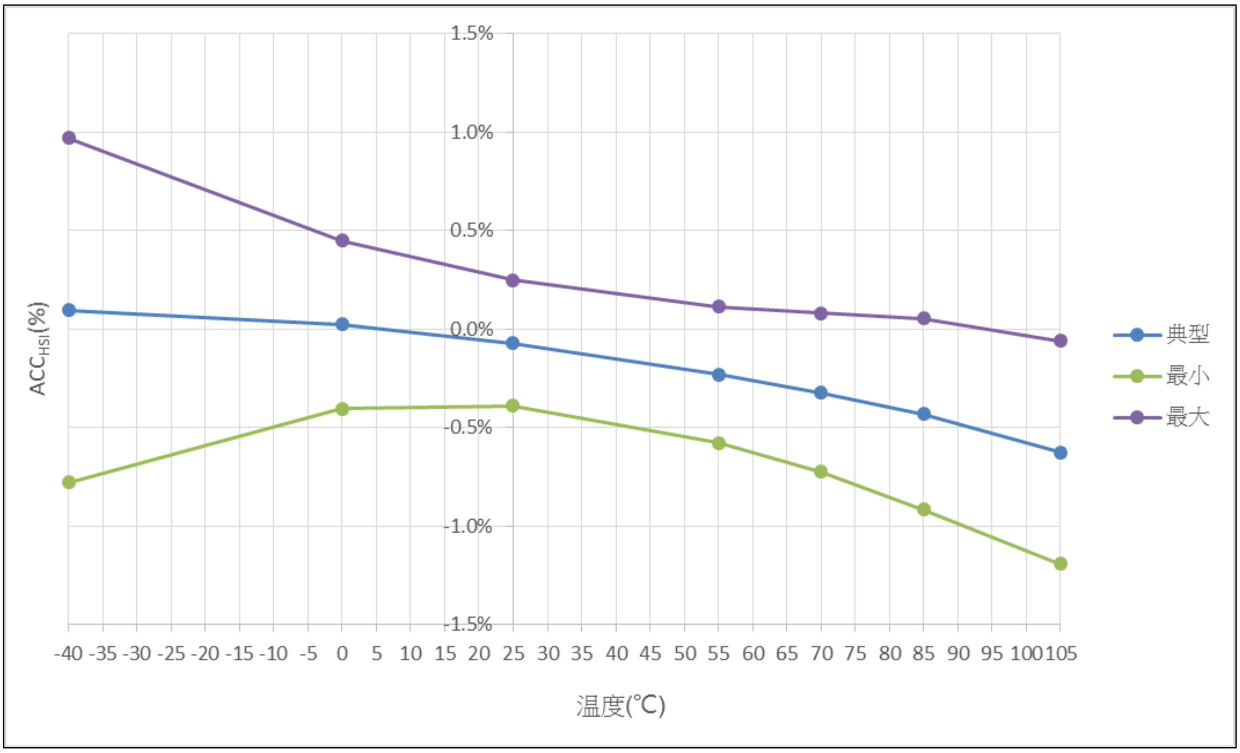
High-speed internal clock (HICK)

Table 31. HICK clock characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	HICK clock accuracy	User-trimmed with the CRM_CTRL register [1]		-1	-	1	%
		Factory-calibrated[2]	T_A = -40 ~ 105 °C	-2		1.5	%
			T_A = -40 ~ 85 °C	-1.5	-	1.5	
			T_A = 25 °C	-1	0.5	1	
$t_{SU(HICK)}$[2]	HICK clock startup time	-		-	-	10	μs
$I_{DD(HICK)}$[2]	HICK clock power consumption	-		-	200	215	μA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 13. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 32. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}[1]	Frequency	-	30	40	60	kHz

(1) Guaranteed by characterization results, not tested in production.

7.3.8 PLL characteristics

Table 33. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplication output clock	16	-	150	MHz
t_{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Take case of using the appropriate multiplication factors to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

7.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: HICK is used as a clock source.

Table 34. Low-power mode wakeup time

Symbol	Parameter Conditions	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	4.2	μs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode (LDO in run mode)	300	μs
	Wakeup from Deepsleep mode (LDO in low-power mode)	360	
$t_{WUSTDBY}$	Wakeup from Standby mode	600	μs

7.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 35. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied on V_{DD} and V_{SS} pins through coupling/decoupling network conforming to IEC 61000-4-4 to induce a functional error. There is a 47 μF capacitor on the inlets of V_{DD} and V_{SS}. Each pair of V_{DD} and V_{SS} has a 0.1μF bypass capacitor.	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 150 MHz, conforms to IEC 61000-4-4	4A (±4 kV)
		V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at a component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user applications and the software in particular. Therefore it is recommended to carry out EMC optimization and prequalification tests in relation with the EMC level.

7.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 36. GPIO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	–0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	Standard GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT GPIO input high level voltage	-		-	5.5	
V_{hys}	Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input leakage current(2)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard GPIOs	-	-	±1	µA
		$V_{SS} \leq V_{IN} \leq$ 5.5V FT GPIO	-	-	±10	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	60	75	110	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)(4)	$V_{IN} = V_{DD}$	60	80	120	kΩ
C_{IO}	GPIO pin capacitance	-	-	5	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.
(3) When FT pin input is higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
(4) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in *Section 7.2.1*:

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 11*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 11*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 37. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Maximum sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		2.4	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 38. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$	Pulse width of external signals detected by EXINT controller	10	-	ns

7.3.12 NRST pin characteristics

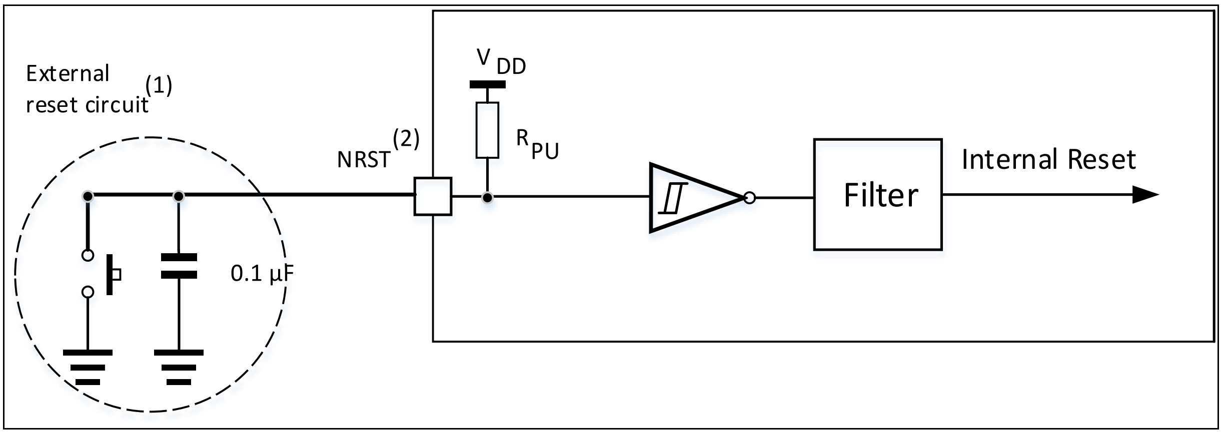
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	400	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{ILV(NRST)}$ (1)	NRST input low level invalid time	-	-	-	33.3	μs
$t_{ILNV(NRST)}$ (1)	NRST input low level valid time	-	66.7	-	-	μs

(1) Guaranteed by design.

Figure 14. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin goes below the V_{IL} (NRST) max level specified in *Table 39*. Otherwise the reset will not be performed by the device.

7.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Table 40. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 150 MHz	6.7	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}/2$	MHz

7.3.14 SPI / I²S characteristics

Table 41. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})$[1]	SPI clock frequency [2][3]	Master mode	-	36	MHz
		Slave receive mode	-	36	
		Slave transmit mode	-	32	
$t_{w(SCKH)}$[1] $t_{w(SCKL)}$[1]	SCK high and low time	Master mode, prescaler = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}$[1]	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}$[1]		Slave mode	5	-	
$t_{h(MI)}$[1]	Data input hold time	Master mode	4	-	ns
$t_{h(SI)}$[1]		Slave mode	5	-	
$t_{a(SO)}$[1][4]	Data output access time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{dis(SO)}$[1][5]	Data output disable time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{v(SO)}$[1]	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$[1]	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{h(SO)}$[1]	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}$[1]		Master mode (after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency in slave mode should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales office for technical support.
(4) Min time is the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 15. SPI timing diagram - slave mode and CPHA = 0

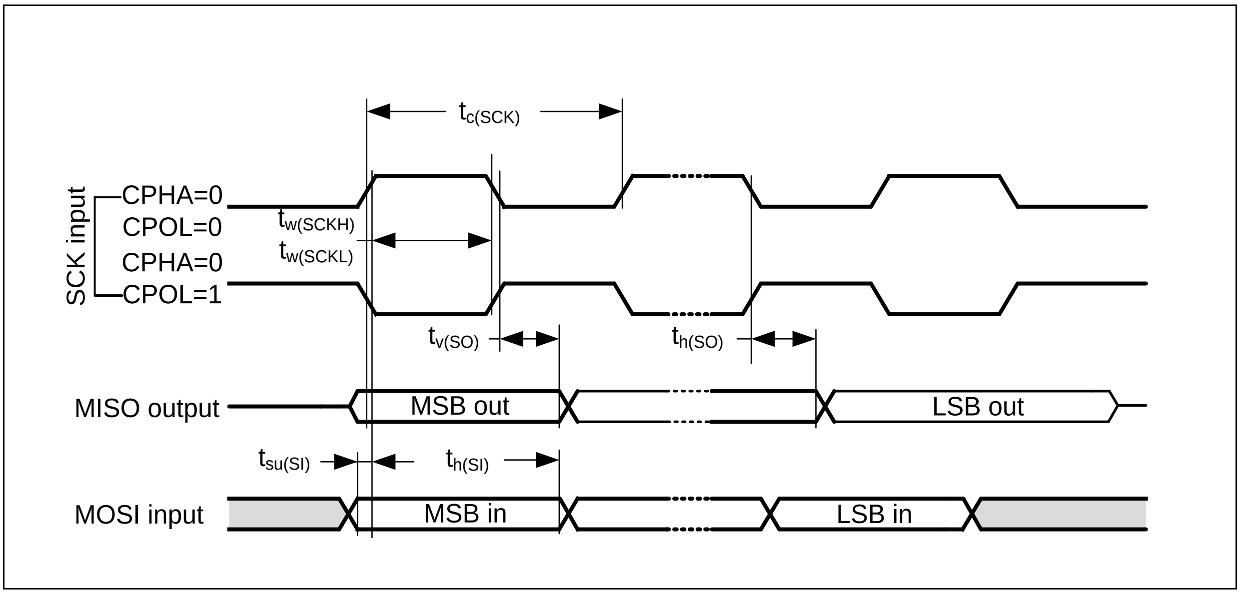


Figure 16. SPI timing diagram - slave mode and CPHA = 1

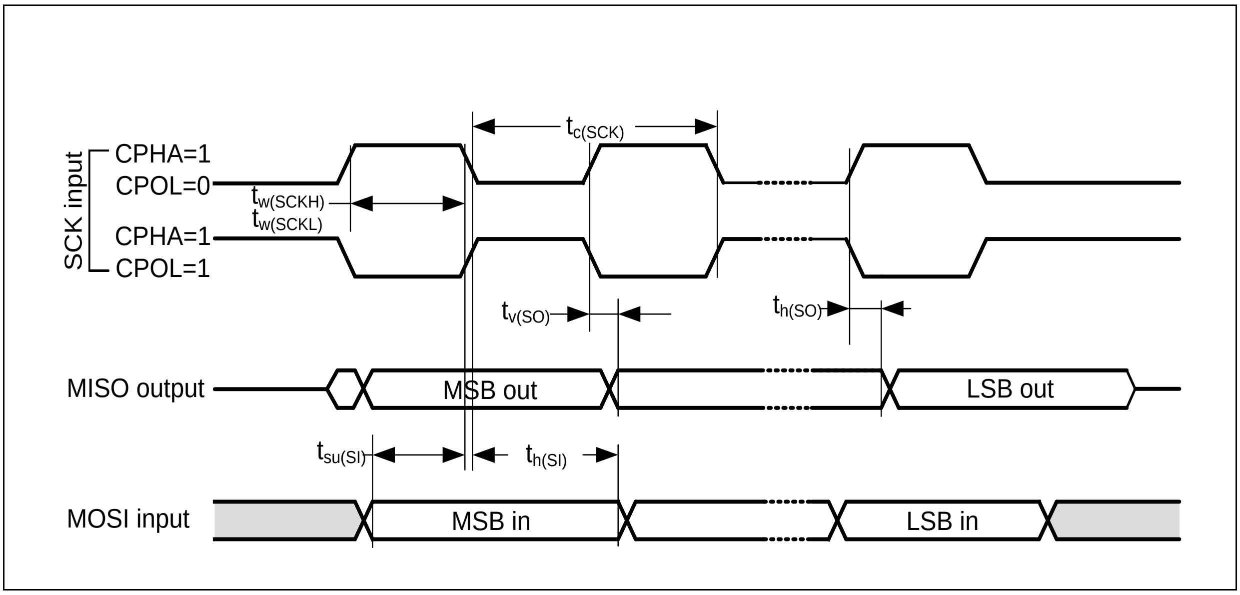
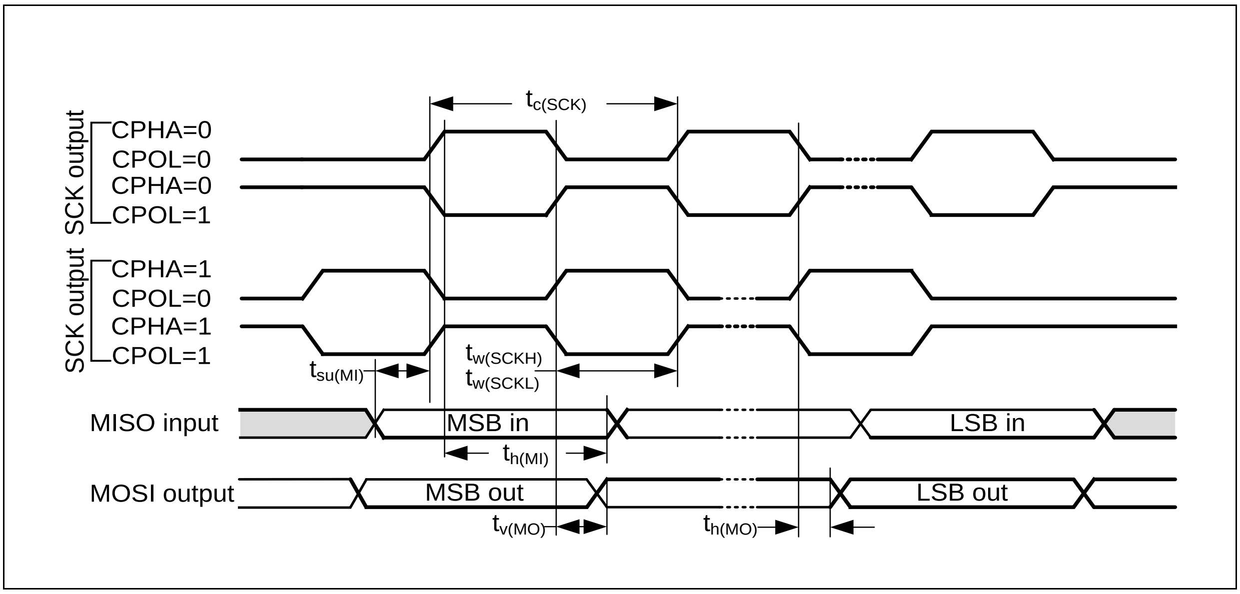


Figure 17. SPI timing diagram - master mode



7.3.15 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not "true" open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface supports standard mode (max. 100 kHz) and fast mode (max. 400 kHz). I²C bus frequency is up to 1 MHz. To obtain a complete set of solutions or more information, please contact your local ARTERY sales team for further support.

7.3.16 OTGFS characteristics

Table 42. OTGFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 43. OTGFS DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	OTGFS operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I (OTGFS_D+/D-)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PU}		OTGFS_D+ internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ
R_{PD}		OTGFS_D+/D- internal pull-up	V_{IN} = V_{DD}	15	19	25	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32WB415 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by design, not tested in production.
(4) R_L is the load connected on the USB drivers.

Figure 18. OTGFS timings: definition of data signal rise and fall time

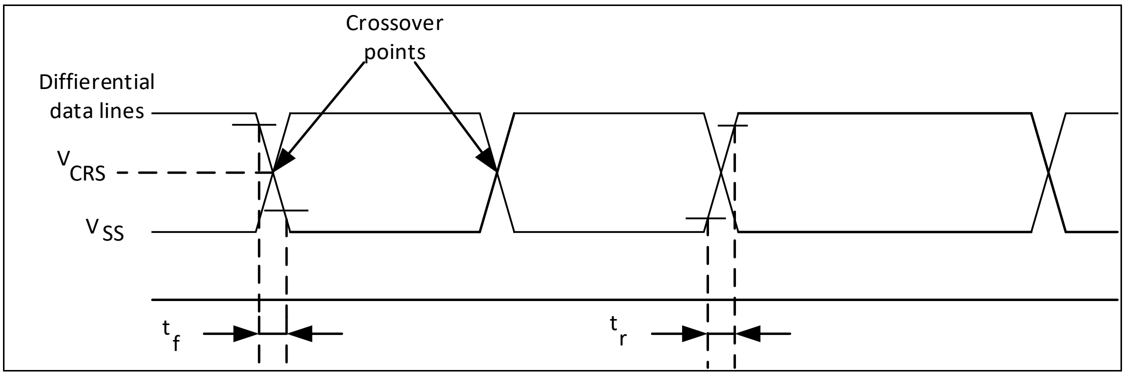


Table 44. OTGFS electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time (2)	$C_L \leq 50$ pF	4	20	ns
t_f	Fall Time (2)	$C_L \leq 50$ pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

7.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 15*.

Note: It is recommended to perform a calibration after each power-up.

Table 45. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.6	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	560(1)	660	µA
f_{ADC}	ADC clock frequency		0.6	-	28	MHz
f_S(2)	Sampling rate		0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-} internally connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 46* and *Table 48* for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	15	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.14			µs
		-	172			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	ns
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	µs
		-	14 ~ 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} is internally connected to V_{DDA} whereas V_{REF-} is internally connected to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 45*.

Table 46 and *Table 48* are used to define the maximum external impedance allowed for an error below 1 LSB.

Table 46. R_{AIN} max for f_{ADC} = 14 MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.25
7.5	0.54	1.3
13.5	0.96	2.5
28.5	2.04	5.0
41.5	2.96	8.0
55.5	3.96	10.5
71.5	5.11	13.5
239.5	17.11	40

(1) Guaranteed by design.

Table 47. R_{AIN} max for f_{ADC} = 28 MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (kΩ)(1)
1.5	0.05	0.1
7.5	0.27	0.6
13.5	0.48	1.2
28.5	1.02	2.5
41.5	1.48	4.0
55.5	1.98	5.2
71.5	2.55	7.0
239.5	8.55	20

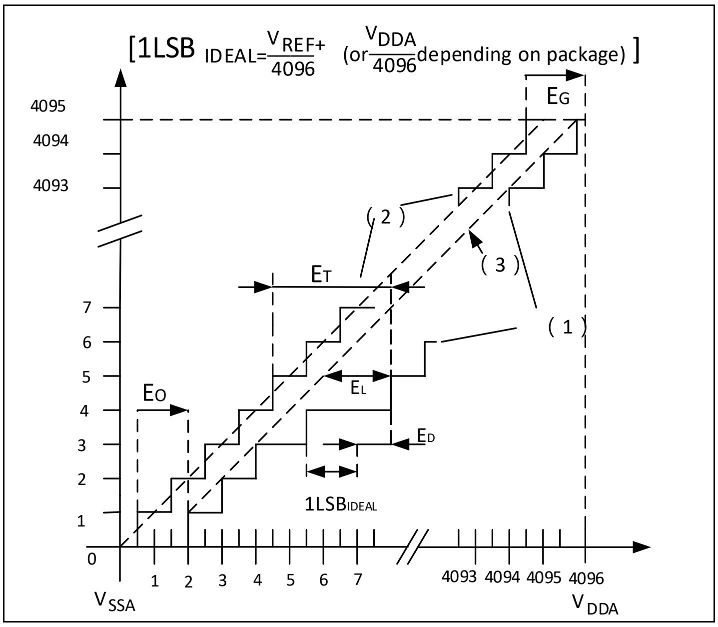
(1) Guaranteed by design.

Table 48. ADC accuracy (1)(2)

Symbol	Parameter	Test Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C	±2	±3	LSB
EO	Offset error		±1	±1.6	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±0.6	±1	
EL	Integral linearity error		±1	±2	
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.6 to 3.6 V T_A = -40 ~ 105 °C	±2	±4	LSB
EO	Offset error		±1	±2	
EG	Gain error		±1.5	±3.5	
ED	Differential linearity error		±0.6	+1.5/-1	
EL	Integral linearity error		±1	±2	

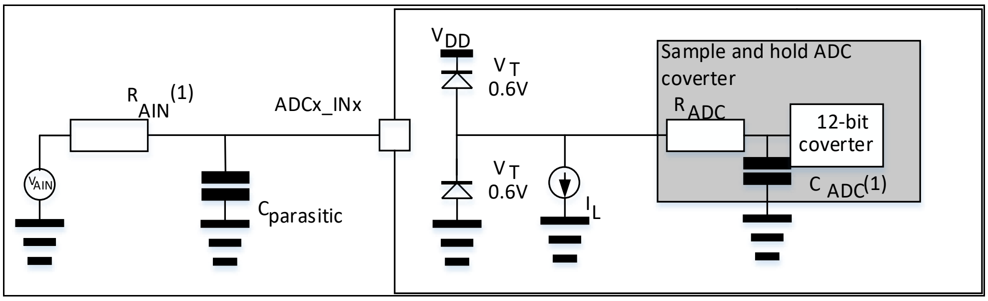
(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

Figure 19. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 20. Typical connection diagram using the ADC



(1) Refer to *Table 45* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 4.* The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

7.3.18 Internal reference voltage (V_{INTRV}) characteristics

Table 49. Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.17	1.20	1.23	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading internal reference voltage	-	5.1	-	-	μs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

7.3.19 Temperature sensor (V_{TS}) characteristics

Table 50. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±2	±5	ºC
Avg_Slope(1(2))	Average slope	-4.13	-4.34	-4.54	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	1.26	1.32	1.38	V
t_{START}(3)	Startup time	-	-	100	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

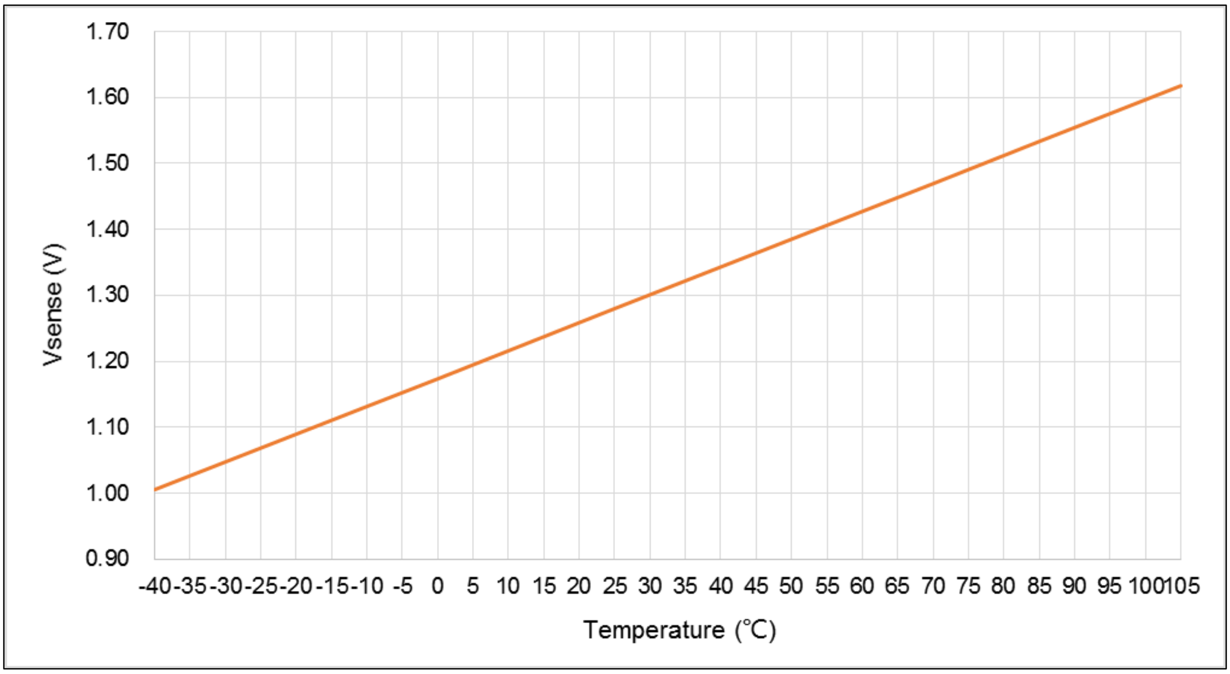
Temperature (in °C) = {(V_{25} - V_{TS}) / Avg_Slope} + 25.

Where,

V_{25} = V_{TS} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{TS} (given in mV/° C).

Figure 21. V_{TS} vs. temperature



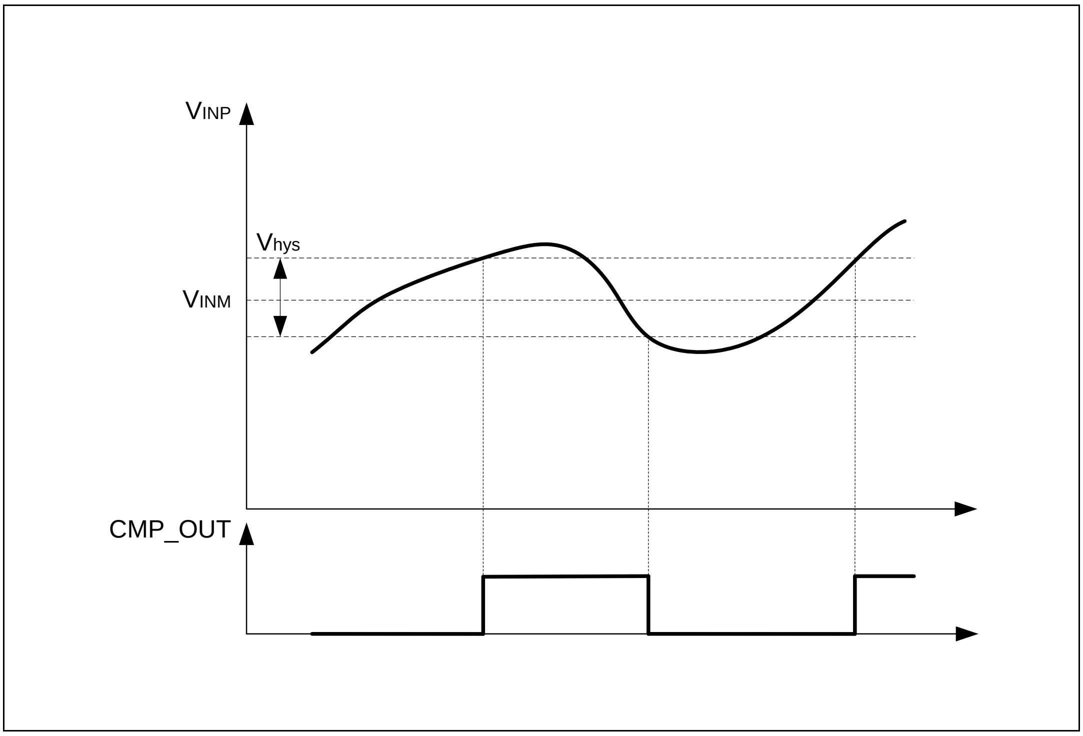
7.3.20 CMP characteristics

Table 51. CMP characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.6	-	3.6	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	V
t_{START}	Startup time	High speed mode		-	2.0	3.2	μs
		Low power mode		-	3.6	5.5	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	High speed mode		-	105	320	ns
		Low power mode		-	1.2	3	μs
V_{offset}	Offset voltage	-		-	±3	±10	mV
V_{hys}	Hysteresis	No hysteresis		-	0	-	mV
		High speed mode	Low hysteresis	40	65	100	
			Medium hysteresis	120	180	280	
			High hysteresis	200	320	450	
		Low power mode	Low hysteresis	15	25	35	
			Medium hysteresis	50	70	90	
			High hysteresis	90	120	160	
I_{DDA}	Current consumption	High speed mode		-	120	165	μA
		Low power mode		-	1.9	3.5	

(1) Guaranteed by characterization results, not tested in production.

Figure 22. CMP hysteresis



8 Package information

Figure 23. QFN48 – 7 x 7 mm 48 pin quad flat no-leads package outline

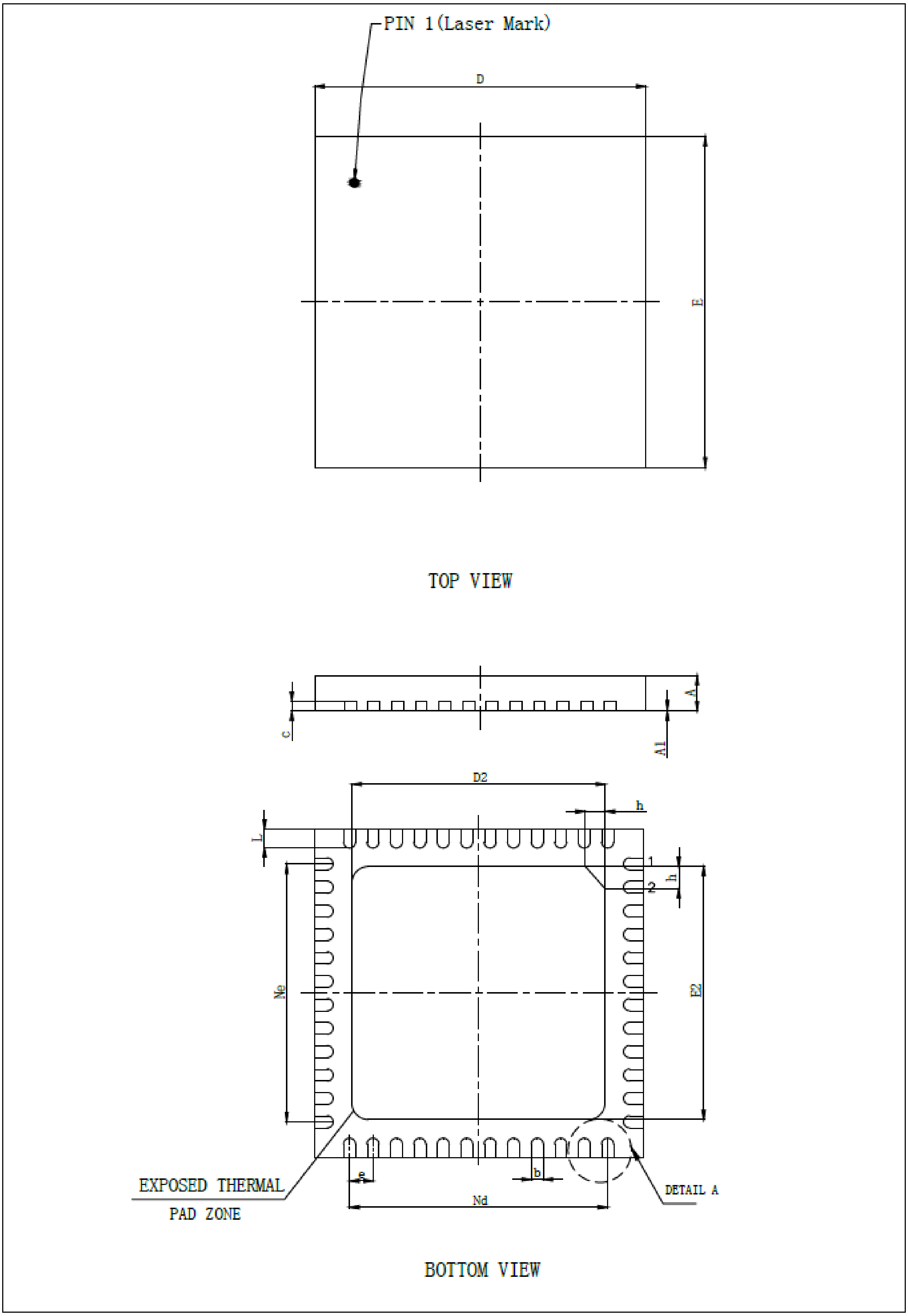
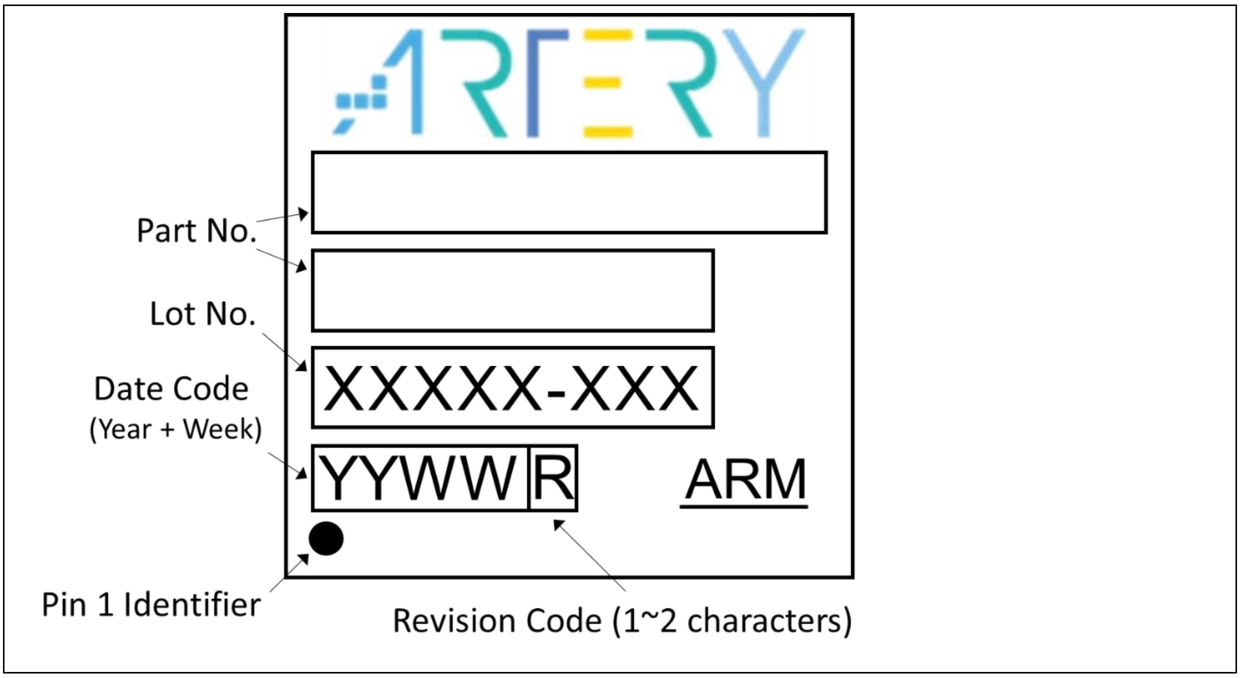


Table 52. QFN48 – 7 x 7 mm 48 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.23
D	6.90	7.00	7.10
D2	5.30	5.40	5.50
E	6.90	7.00	7.10
E2	5.30	5.40	5.50
e	0.50 BSC.		
Nd	5.50 BSC.		
Ne	5.50 BSC.		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Device silkscreen is shown in Figure 24:

Figure 24. Marking example



(1) Not in scale.

9 Part numbering

Table 53. AT32WB415 series part numbering

Examples:	AT32 WB 4 1 5 C C U 7 -7
Product family	AT32
AT32 = ARM-based 32-bit microcontroller	
Product type	WB
WB = Wireless Bluetooth communication	
Core	4
4 = Cortex^{TM}-M4	
Product series	1
1 = Value line	
Product application	5
5 = OTGFS series	
Pin count	C
C = 48 pins	
Internal Flash memory size	C
C = 256 Kbytes of Flash memory	
Package type	U
U = QFN	
Temperature range	7
7 = -40 °C to +105 °C	
Package information	-7
-7 = QFN48 - 7 x 7 mm	

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

10 Document revision history

Table 54. Document revision history

Date	Version	Change
2022.1.24	2.00	Initial release.
2023.7.7	2.01	1. Modified DC-DC output voltage to 1.6 V in *Table 5.* 2. Added Section *3.18 Programming and debugging interface.*
2023.10.17	2.02	1. Added note (3) of *Table 36*. 2. Added contents in *3.14.4*. 3. Modified the fourth paragraph in IMPORTANT NOTICE.