ARM®-based 32-bit Cortex®-M4 MCU with FPU, 64 to 128 KB Flash, sLib, 11 timers, 8 communication interfaces (1 CAN or CANFD), 2 ADCs, 2 DACs, 2 CMPs, 4 OPs

Features

- **Core: ARM® 32-bit Cortex®-M4 CPU with FPU**
  - 180 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 64 to 128 Kbytes of Flash memory
  - 28 Kbytes of boot memory used as a Bootloader or as a general instruction/data memory (one-time configurable)
  - 1 Kbyte of OTP memory
  - sLib: configurable part of main Flash as a library area with code executable but secured, non-readable
  - 16 Kbytes of SRAM
- **Power control (PWC)**
  - 2.4 to 3.6 V supply
  - Power-on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep and Standby modes, with 4 WKUP pins used for Standby mode wakeup
  - 20x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal (HEXT)
  - 48 MHz internal factory-trimmed high speed clock (HICK), ±1 % accuracy at 25 °C and ± 2.5% accuracy at -40 °C to +105 °C
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 2x 12-bit 2.5 MSPS A/D converters, up to 18 external input channels; internal channels connected with OP; each channel has independent data register
  - Temperature sensor (V_{TS}) and internal reference voltage (V_{INTRV})
  - 2x 6-bit D/A converters connected with CMP and OP
  - 2x comparators (CMP) with output blanking feature
  - 4x operational amplifiers (OP), 8.5 MHz bandwidth, support PGA mode, with built-in clamping diode for input
- **DMA**
  - 1x 7-channel DMA controller with flexible mapping capability
- **Up to 46 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 11 timers (TMR)**
  - 1x 16-bit 8-channel advanced timer, including 4 pairs of complementary PWM outputs with dead-time generator and emergency brake
  - Up to 5x 16-bit general-purpose timers, each with up to 4 IC/OC/PWM or pulse counter and incremental encoder input
  - 2x 16-bit basic timers
  - 2x watchdog timers (general WDT and windowed WDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarm, subsecond accuracy, and hardware calendar, calibration feature**
- **Up to 8 communication interfaces**
  - 2x I^2C interfaces (SMBus/PMBus)
  - 2x USART interfaces, support master synchronization SPI and modem control, ISO7816 interface, LIN, IrDA, and RS485 driver enable, TX/RX swap
  - 2x SPI interfaces (36 Mbit/s), both with multiplexed half-duplex I^2S
  - 1x CAN with dedicated 1408-byte buffer (AT32M416 supports CAN FD)
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Serial wire debug (SWD)**
- **Operating temperatures: -40 to +105 °C**
- **Packages**
  - LQFP48 7 x 7 mm
  - LQFP32 7 x 7 mm
  - QFN32 4 x 4 mm
  - TSSOP24 7.8 x 4.4 mm

Table 1. AT32M412 device summary

Flash	Part number
128 Kbytes	AT32M412CBT7, AT32M412KBT7, AT32M412KBU7-4, AT32M412EBP7
64 Kbytes	AT32M412C8T7, AT32M412K8T7, AT32M412K8U7-4, AT32M412E8P7

Table 2. AT32M416 device summary

Flash	Part number
128 Kbytes	AT32M416CBT7, AT32M416KBT7, AT32M416KBU7-4, AT32M416EBP7
64 Kbytes	AT32M416C8T7, AT32M416K8T7, AT32M416K8U7-4, AT32M416E8P7

Contents

List of tables

List of figures

1 Descriptions

The AT32M412/416 series are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex®-M4 core features a single-precision Floating Point Unit (FPU) supporting all ARM® single-precision data processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

The AT32M412/416 series incorporate high-speed on-chip memories, including up to 128 Kbytes of Flash memory, 16 Kbytes of SRAM, and 28 Kbytes of boot memory that can be used as a Bootloader or as a general instruction/data memory (one-time configurable) to achieve the maximum of 128+28 Kbytes, as well as 1 Kbyte of OTP data storage space. Any block of the embedded Flash memory can be protected by the “sLib” (security library), functioning as a security area with code-executable only.

The AT32M412/416 series have analog modules including two 12-bit ADCs, two 6-bit DACs, two comparators (CMP) and four operational amplifiers (OP) with PGA feature. Digital modules include six 16-bit general-purpose timers (one advanced PWM timer used for motor control), two basic timers and one low-power ERTC. They also feature standard and advanced communication interfaces: up to two I^2Cs, two SPIs (multiplexed as half-duplex I^2Ss), two USARTs, one CAN or CANFD, and one infrared transmitter. With support on interconnection among most on-chip peripherals, the AT32M412/416 series are suitable for motor control applications.

The AT32M412/416 series operate in the -40 to +105 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32M412/416 devices are supplied in different package types. They are pin-to-pin, software and functionally compatible throughout the AT32M412/416 series, except that the configurations of peripherals are not fully identical depending on the package types.

Table 3. AT32M412 features and peripheral counts

Part number		AT32M412xxP7		AT32M412xxU7-4		AT32M412xxT7			
		E8	EB	K8	KB	K8	KB	C8	CB
Frequency (MHz)		180							
Flash (KB)		64	128	64	128	64	128	64	128
SRAM (KB)		16	16	16	16	16	16	16	16
Timers	Advanced	1		1		1		1	
	16-bit general-purpose	5		5		5		5	
	Basic	2		2		2		2	
	SysTick	1		1		1		1	
	WDT	1		1		1		1	
	WWDT	1		1		1		1	
	ERTC	1		1		1		1	
Communication interfaces	I^2C	2		2		2		2	
	SPI(1)	2		2		2		2	
	I^2S (half-duplex)(1)	2		2		2		2	
	USART	2		2		2		2	
	CAN	1		1		1		1	
	IRTMR	1		1		1		1	
Analog	12-bit ADC numbers/ channels	2							
		9		12		12		18	
	6-bit DAC numbers	2							
	CMP	2							
	OP	3(2)		3(3)		3(3)		4	
GPIO		22		31		30		46	
Operating temperature		-40 °C to +105 °C							
Packages		TSSOP24 7.8 x 4.4 mm		QFN32 4 x 4 mm		LQFP32 7 x 7 mm		LQFP48 7 x 7 mm	

(1) Half-duplex I^2S share the same pin with SPI.
(2) For TSSOP24 package, OP3 does not have an external pin for negative input, and OP4 is not available.
(3) For QFN32 and LQFP32 packages, OP4 is not available.

Table 4. AT32M416 features and peripheral counts

Part number		AT32M416xxP7		AT32M416xxU7-4		AT32M416xxT7			
		E8	EB	K8	KB	K8	KB	C8	CB
Frequency (MHz)		180							
Flash (KB)		64	128	64	128	64	128	64	128
SRAM (KB)		16	16	16	16	16	16	16	16
Timers	Advanced	1		1		1		1	
	16-bit general-purpose	5		5		5		5	
	Basic	2		2		2		2	
	SysTick	1		1		1		1	
	WDT	1		1		1		1	
	WWDT	1		1		1		1	
	ERTC	1		1		1		1	
Communication interfaces	I^2C	2		2		2		2	
	SPI(1)	2		2		2		2	
	I^2S (half-duplex)(1)	2		2		2		2	
	USART	2		2		2		2	
	CANFD	1		1		1		1	
	IRTMR	1		1		1		1	
Analog	12-bit ADC numbers/ channels	2							
		9		12		12		18	
	6-bit DAC numbers	2							
	CMP	2							
	OP	3(2)		3(3)		3(3)		4	
GPIO		22		31		30		46	
Operating temperature		-40 °C to +105 °C							
Packages		TSSOP24 7.8 x 4.4 mm		QFN32 4 x 4 mm		LQFP32 7 x 7 mm		LQFP48 7 x 7 mm	

(1) Half-duplex I^2S share the same pin with SPI.
(2) For TSSOP24 package, OP3 does not have an external pin for negative input, and OP4 is not available.
(3) For QFN32 and LQFP32 packages, OP4 is not available.

2 Functionality overview

2.1 ARM®Cortex®-M4 with FPU

The ARM® Cortex®-M4 processor is the latest generation of ARM® processor for embedded systems. It is a 32-bit RISC high-performance processor that features exceptional code efficiency, outstanding computing power and advanced response to interrupts. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution. Its single-precision FPU (floating point unit) speeds up floating point calculations while avoiding saturation.

2.2 Memory

2.2.1 Flash

Up to 128 Kbytes of embedded Flash is available for storing programs and data. Any part of the embedded Flash memory can be protected by “sLib” (security library), a security area that is code-executable only but non-readable. The “sLib” is a mechanism designed to protect the intelligence of solution venders and facilitate the second-level development by customers.

There is another 28-Kbyte boot memory in which the Bootloader is stored. If it is not needed, this boot memory can be used as a general instruction/data memory (one-time configurable) instead. It can be used to achieve the maximum of 128+28 Kbytes of memory.

The 1 Kbyte of OTP (one-time programmable) is used for storing user data. The content in OTP can be programmed for one time only, and cannot be erased.

A User System Data block is available for hardware configurations such as access/erase/program protection, and watchdog self-enable. User System Data allows the independent configuration of Flash memory erase/program and access protection. There are two levels of memory access protection: low-level protection and high-level protection.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 SRAM

Up to 16 Kbytes of embedded SRAM is accessible (read/write) at CPU clock speed with 0 wait states.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32M412/416 series embed a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt controller (EXINT), which is connected directly to NVIC, consists of 22 edge detectors for generating interrupt requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connect up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.4~3.6 V: power supply for internal blocks such as GPIOs, regulator (LDO), ERTC, external 32 KHz crystal (LEXT), battery powered registers (BPR) via V_{DD}/V_{DDA} pins.
- V_{DDA} = 2.4~3.6 V: power supply for ADC, DAC, CMP and OP via V_{DD}/V_{DDA} pins. V_{DDA} and V_{SSA} are internally connected to V_{DD} and V_{SS}, respectively.

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR) and low voltage reset (LVR) circuitry. It is always active and allows proper operation starting from 2.4 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt is generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power down.

- Normal mode: used in Run/Sleep mode or in Deepsleep mode
- Low-power mode: can be used in Deepsleep mode
- Power down mode: used in Standby mode. The LDO output is in high impedance and the kernel circuitry is powered down, and the contents of the registers and SRAM are lost.

The LDO operates in normal mode after chip reset.

The LDO can be used for output voltage adjustment. In addition to the default 1.2 V, the 1.3 V output voltage can be selected by software. For the corresponding maximum AHB clock frequency of different LDO output voltage, refer to *Table 14*. For details about LDO voltage switch and system clock configuration, refer to *AT32M412/416 Series Reference Manual*.

2.4.4 Low-power modes

The AT32M412/416 series support three low-power modes:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Deepsleep mode

  Deepsleep mode achieves low-power consumption while keeping the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The voltage regulator (LDO) can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm/wakeup/tamper/timestamp event, or CMP wakeup signal.

- Standby mode

  The Standby mode is used to acquire the lowest power consumption. The internal LDO is switched off so that the entire LDO power domain is powered down. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for ERTC and BPR registers and standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm/wakeup/tamper/timestamp occurs.

Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. WDT depends on the User System Data settings.

2.5 Boot modes

At startup, BOOT0 pin and nBOOT1 bit in the User System Data are used to select one of three boot options:

- Boot from Flash memory
- Boot from boot memory
- Boot from embedded SRAM

The Bootloader is stored in the boot memory. It is used to reprogram the Flash memory through USART1, USART2, I^2C1, I^2C2, CAN1/CANFD1 or SPI1. Of them, CAN1/CANFD1 must be used in conjunction with one of the following HEXT oscillators: 4, 6, 8, 12, 14.7456, 16, 20, 24 or 25 MHz. *Table 5* provides the part number and pin configurations for Bootloader.

Table 5. Part numbers and pin configurations for bootloader

Peripherals	Part numbers	Pin
USART1	All	PA9: USART1_TX PA10: USART1_RX
USART2	All	PA2: USART2_TX PA3: USART2_RX
I²C1	All	PB6: I2C1_SCL PB7: I2C1_SDA
I²C2	AT32M412Cx, AT32M412Kx AT32M416Cx, AT32M416Kx	PB10: I2C2_SCL PB3: I2C2_SDA
CAN1	AT32M412Cx, AT32M412Ex AT32M416Cx, AT32M416Ex	PB5: CAN1_RX PB13: CAN1_TX
SPI1	All	PA4: SPI1_CS PA5: SPI1_SCK PA6: SPI1_MISO PA7: SPI1_MOSI

2.6 Peripheral interconnection

To guarantee flexible applications, most peripherals of the AT32M412/416 series are interconnected, so that they can operate with greater efficiency and reduce software or core workload. *Table 6* shows the peripheral interconnection of AT32M412/416 devices. For details about the interconnections between analog peripherals, and analog module and GPIO, refer to *Appendix A*.

Table 6. Peripheral interconnections

Source peripheral	Target peripheral	Description
TMR	TMR	1. Timer synchronization or concatenation 2. TMR3 and TMR4 input blanking timing
	ADC, DAC	Internal trigger signal source
	DMA	Transfer trigger
	CMP	Output blanking timing
	IRTMR	Master signal and carrier signal source
USART	IRTMR	Master signal source
ADC	TMR	Voltage monitoring result used as timer internal EXT count input
DAC	CMP	Configurable internal negative reference voltage input
	OP	Configurable internal positive voltage source input
CMP	TMR	1. Timer internal channel signal input 2. Timer internal EXT count input 3. Timer internal BRK signal input 4. Timer CxORAW clear signal source
V_{TS}, V_{INTRV}, OP	ADC	Internal channel signal source
Core, PVM	TMR	Timer internal BRK signal input
CLKOUT, HEXT division, RTC clock, LEXT, LICK	TMR	Clock sources used as TMR11 internal channel input for frequency measurement or calibration

2.7 Clocks

The internal 48 MHz clock (HICK) divided by 6 (that is 8 MHz) is selected as the default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are available to allow the configuration of the AHB and the APB (APB1, APB2 and APB3) frequencies. The maximum frequency of the AHB/APB1/APB2 domain is 180 MHz, and APB3 90 MHz.

2.8 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins is in analog mode at reset, by default. After reset, each of them can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as multiplexed functions. Most of the GPIO pins are shared with digital or analog multiplexed functions. All GPIOs are high current-capable.

The GPIO's configuration can be locked if needed, in order to avoid false writing to the GPIO's registers by following a specific sequence.

2.9 Direct Memory Access Controller (DMA)

The AT32M412/416 features a 7-channel general-purpose DMA which is able to manage memory-to-memory, peripheral-to-peripheral, and memory-to-peripheral transfer. These DMA channels support fully flexible mapping for connecting to various peripherals.

The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software, and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPIs/I^2Ss, I^2Cs, USARTs, all timers (TMRs), ADCs and DACs.

2.10 Timers (TMR)

The AT32M412/416 series include an advanced timer, five general-purpose timers, two basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 7. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output
Advanced	TMR1	16-bit	Up, down up/down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TMR3 TMR4	16-bit	Up, down up/down	Any integer between 1 and 65536	Yes	4	No
	TMR9	16-bit	Up, down up/down	Any integer between 1 and 65536	Yes	2	2
	TMR10 TMR11	16-bit	Up, down up/down	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6 TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.10.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen as a four-phase multiplexed on eight channels. It has complementary PWM outputs with programmable dead-time insertion. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-period mode output

If configured as a standard 16-bit timer, it has the same features as that of the TMRx timer. If configured as a 16-bit PWM generator, it boasts full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen, and the PWM outputs are disabled to turn off any power switch driven by these outputs.

Many features are identical with those of the general-purpose TMRs that have the same architecture. Thus, the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

2.10.2 General-purpose timers (TMR3, TMR4 and TMR9~11)

Up to five synchronizable general-purpose timers are available in the AT32M412/416.

- **TMR3 and TMR4**

  TMR3 and TMR4 are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They can offer up to four independent channels on the largest package. Each channel can be used for input capture/output compare, PWM or one-period mode output.

  TMR3 and TMR4 can work with the advanced timer via the link feature for synchronization or event chaining. In debug mode, counters can be frozen. Any of these general-purpose timers

can be used for the generation of PWM output. Each timer has its individual DMA request mechanism. They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

In addition, TMR3 and TMR4 feature input blanking function. External channels 1~3 of each timer can be selected for both timers, thus to improve the application flexibility for motor control.

- **TMR9, TMR10 and TMR11**

  These timers are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. TMR9 has two independent channels and two complementary channels; TMR10 and TMR11 has one independent channels and one complementary channel. Each channel can be used for input capture/output compare, PWM, or one-period mode output. They can work together via the timer link feature for synchronization or event chaining. In debug mode, counter can be frozen. Each of these timers has its separate DMA request mechanism.

2.10.3 Basic timers (TMR6 and TMR7)

Both timers are mainly used to generate DAC trigger signals, and each of them can be used as a generic 16-bit time base.

2.10.4 SysTick timer

This timer is dedicated to real-time operating systems, but it could also be used as a standard downcounter. Its features include:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock sources (HCLK or HCLK/8)

2.11 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabled or not through the User System Data. The counter can be frozen in debug mode.

2.12 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock and works an early warning interrupt feature. The counter can be frozen in debug mode.

2.13 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- 20x 32-bit battery powered registers (BPR)

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Support sub-seconds value in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic interrupts wake up Deepsleep or Standby mode.
- Calibrate 1~32767 ERTC clock pulses during running, which can be used for ERTC synchronization with the main clock.
- Digital calibration circuit has 1 ppm resolution to compensate for the inaccuracy of quartz crystal.
- Anti-tamper detection pin has a programmable filter; MCU wakes up from Deepsleep or Standby mode when a tamper event is detected.
- Timestamp function can be used for storing calendar contents. It is triggered by an event on the timestamp pin or a tamper event. MCU wakes up from Deepsleep or Standby mode when a timestamp event is detected.
- Reference clock detection: the more accurate second clock source (50 or 60 Hz) can be used to improve calendar accuracy.

There are two sets of alarm registers used to generate the alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

A prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 80 bytes of user application data. Battery powered registers are not reset by a system reset, nor when the device is woken up from the Standby mode.

2.14 Communication interfaces

2.14.1 Serial peripheral interface (SPI)

There are two SPIs able to communicate at up to 36 Mbit/s in slave and master modes. The prescaler can be used to generate multiple master mode frequencies. The frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD/MMC/SDHC card modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communication in master and slave modes.

2.14.2 Inter-integrated sound interface (I^2S)

Two standard I^2S interfaces (multiplexed with SPI) are available, which can be operate in master or slave mode. These interfaces can be configured to operate with 16/24/32 resolution, as input or output channels. Audio sampling frequencies from 8 kHz to 192 kHz are supported. When any of the I^2S interfaces is configured in master mode, its master clock can be output at 256 times the sampling frequency. Both I^2Ss can be served by the DMA controller.

2.14.3 Universal synchronous/asynchronous receiver transmitter (USART)

The AT32M412/416 series embed two universal synchronous/asynchronous receiver transmitters (USART1 and USART2).

These two USART interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. These two USART interfaces also provide hardware management of the CTS and RTS signals, RS485 driver enable signal, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. These two USART interfaces can be served by the DMA controller. TX/RX pins are swappable.

USART1 and USART2 are able to communicate at up to 11.25 Mbit/s.

2.14.4 Inter-integrated-circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multi-master and slave modes. They can support standard mode (up to 100 kHz), fast mode (up to 400 kHz) and fast mode plus (up to 1 MHz). Some GPIOs provide ultra-high sink current of 20 mA.

They support 7-bit/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.14.5 Controller area network (CAN)

One CAN interface is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. the AT32M416 series also supports CAN FD V1.0. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has two transmit buffers (one primary transmit buffer, and one secondary transmit buffer with three-level depth), and one receive buffer with six-level depth, and sixteen programmable receive filters. It also has a dedicated 1408-byte buffer, which is not shared with any other peripherals.

To guarantee CAN transmission quality, the CAN protocol states that its clock source must come from the HEXT-based PLL clock.

2.14.6 Infrared transmitter (IRTMR)

The AT32M412/416 series offer an infrared transmitter solution. The solution is based on the internal connection between TMR10 and USART1, or USART2 and TMR11. TMR11 is used to provide carrier frequency, and TMR10, USART1 or USART2 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR10 channel 1 and TMR11 channel 1 must be correctly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming output compare channels of these two timers.

2.15 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.16 12-bit analog-to-digital converter (ADC)

The AT32M412/416 series embed two 12-bit analog-to-digital converters (ADC) to provide the below main features:

- 12/10/8/6-bit configurable resolution, with self-calibration function
- Up to 2.5 MSPS conversion rate with 12-bit resolution; conversion time can be shorten by reducing the resolution
- Up to 18 external channels
- Internal channels: internal temperature sensor (V_{TS}), internal reference voltage (V_{INTRV}), and internal outputs of four operational amplifiers (OP1~4)
- Sampling time can be set independently for each channel
- Independent ordinary conversion data register for each channel
- Oversampling ratio adjustable from 2 to 256, up to equivalent to 16-bit resolution
- Conversion can be initiated:
  - By software for both ordinary and preempted conversions
  - By hardware triggers with configurable polarity (internal timer events or GPIO input events) for both ordinary and preempted conversions
- Conversion modes:
  - Each ADC can convert a single channel or a sequence of channels
  - Convert the selected channel once per trigger in sequence mode
  - Convert the selected channel continuously in repetition mode
  - Partition mode
- Conversion control in simultaneous mode or shift mode of ADC in single slave mode
- Voltage monitoring on one, multiple or all channels; an interrupt is generated when the monitored voltage is out of the threshold
- Both ADCs can be served by DMA

2.16.1 Temperature sensor (V_{TS})

The temperature sensor generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel that is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.16.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable 1.2 V output source for ADCs. The V_{INTRV} is internally connected to ADC1_IN17 input channel.

2.16.3 Operational amplifier (OP) internal output

The operational amplifier internal outputs are internally connected to ADC internal inputs. At this point, the OP external output pin can be used as GPIO or multiplexed function.

2.17 6-bit digital-to-analog converter (DAC)

The AT32M412/416 series embed two 6-bit digital-to-analog converters (DAC) to convert to digital signals to two analog voltage outputs to the comparator (CMP) and operational amplifiers (OP) (used as programmable internal reference voltage) or to external pins (no output buffer, with low drive capability).

The DAC main features include:

- Two DACs, and each has an output channel
- Monotonic output
- Synchronized update capability
- Dual DAC for independent or simultaneous conversions
- DMA capability for each DAC
- External triggers for conversion
- Configurable source of input reference voltage (V_{DDA} or V_{INTRV})

The AT32M412/416 series have multiple inputs for DAC conversion trigger. The DAC conversion can be triggered by timer update output, and the update output can be connected to different DMA channels.

2.18 Comparator (CMP)

The AT32M412/416 series embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis, speed, selectable output polarity, output blanking and noise filter.

The reference voltage can be one of the following:

- External GPIO
- Internal DAC output
- Shared pins of OP1~3 outputs and partial CMP inputs

The comparator can wake up from Deepsleep mode at an interrupt. It can also remap output to timer brake.

2.19 Operational amplifier (OP)

The AT32M412/416 series embed four rail-to-rail operational amplifiers (OP) that can be used for flexible connection with external components. The operational amplifier can be configured internally as a voltage follower or as a programmable gain amplifier (PGA). Inputs embed a clamping diode; the output can be connected to internal ADC or external pin.

The OP main features include:

- 8.5 MHz bandwidth
- Offset voltage calibration (below 3 mV after calibration)
- Rail-to-rail input/output
- PGA supports non-inverting gain of 2x, 4x, 8x, 16x, 32x or 64x, and inverting gain of -1x, -3x, -7x, -15x or -63x

Note: Calibrate before using the operational amplifier; otherwise, the offset error does not conform to the value given in Datasheet.

2.20 Serial wire debug (SWD) / serial wire output (SWO)

The ARM® SWD interface is embedded in the AT32M412/416 series. It is a serial wire debug port that enables either a serial wire debug to be connected to the target for programming and debugging purposes. In addition, the SWO feature is available for asynchronous tracing in debug mode.

3 Pin functional definitions

Figure 1. AT32M412/416 LQFP48 pinout

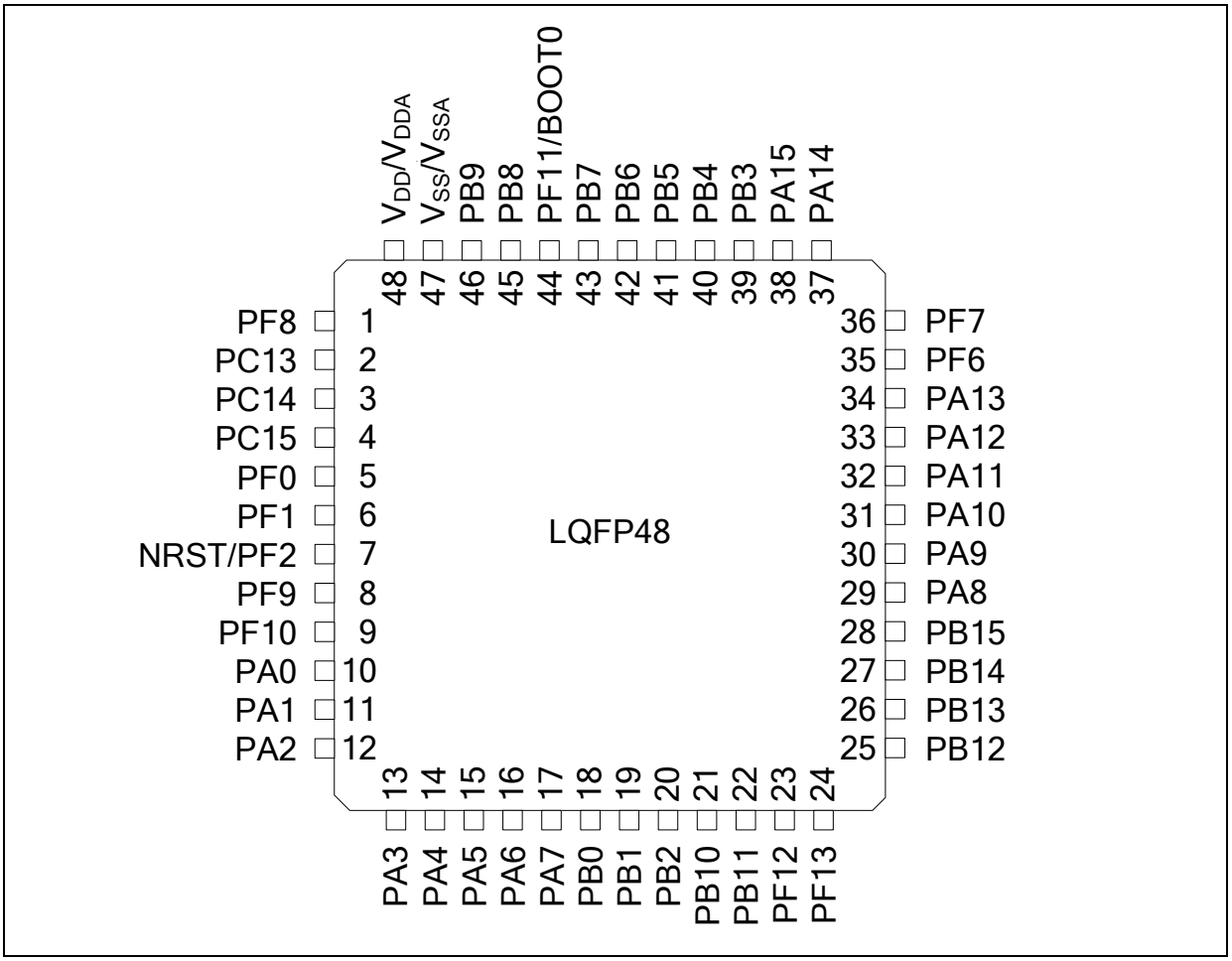


Figure 2. AT32M412/416 LQFP32 pinout

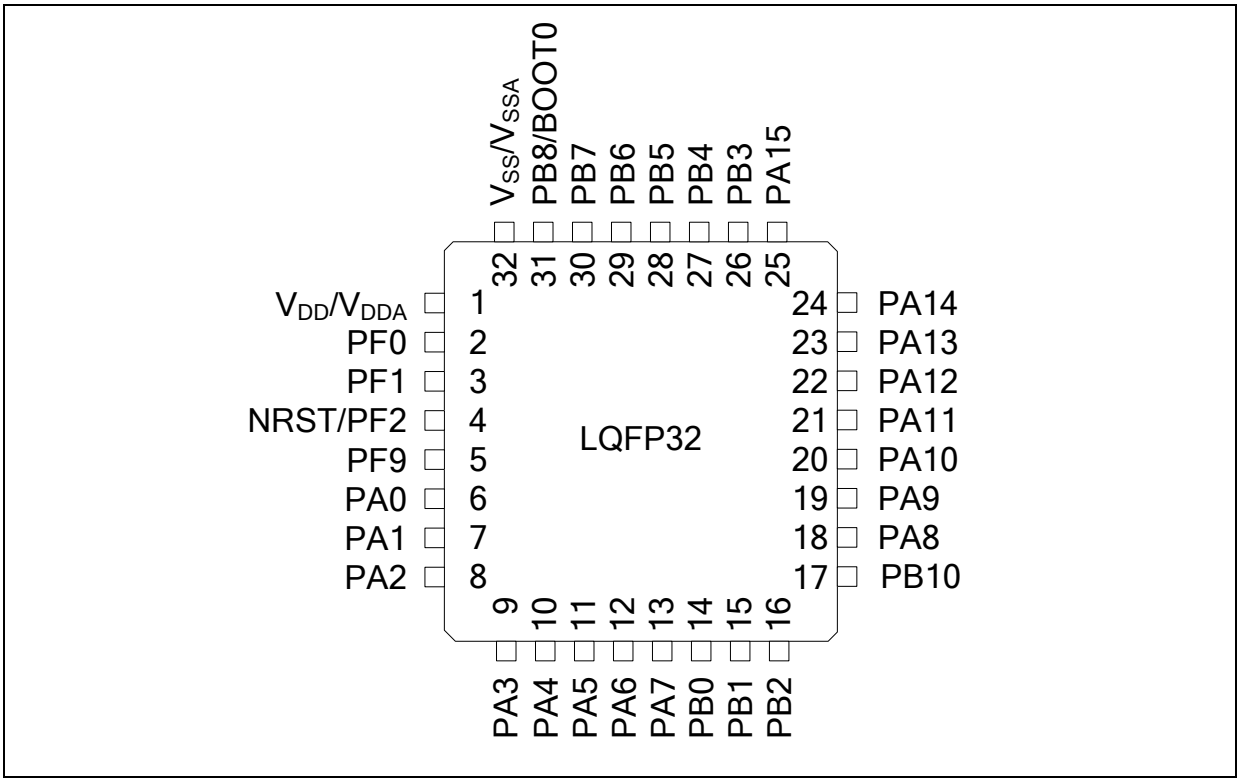


Figure 3. AT32M412/416 QFN32 pinout

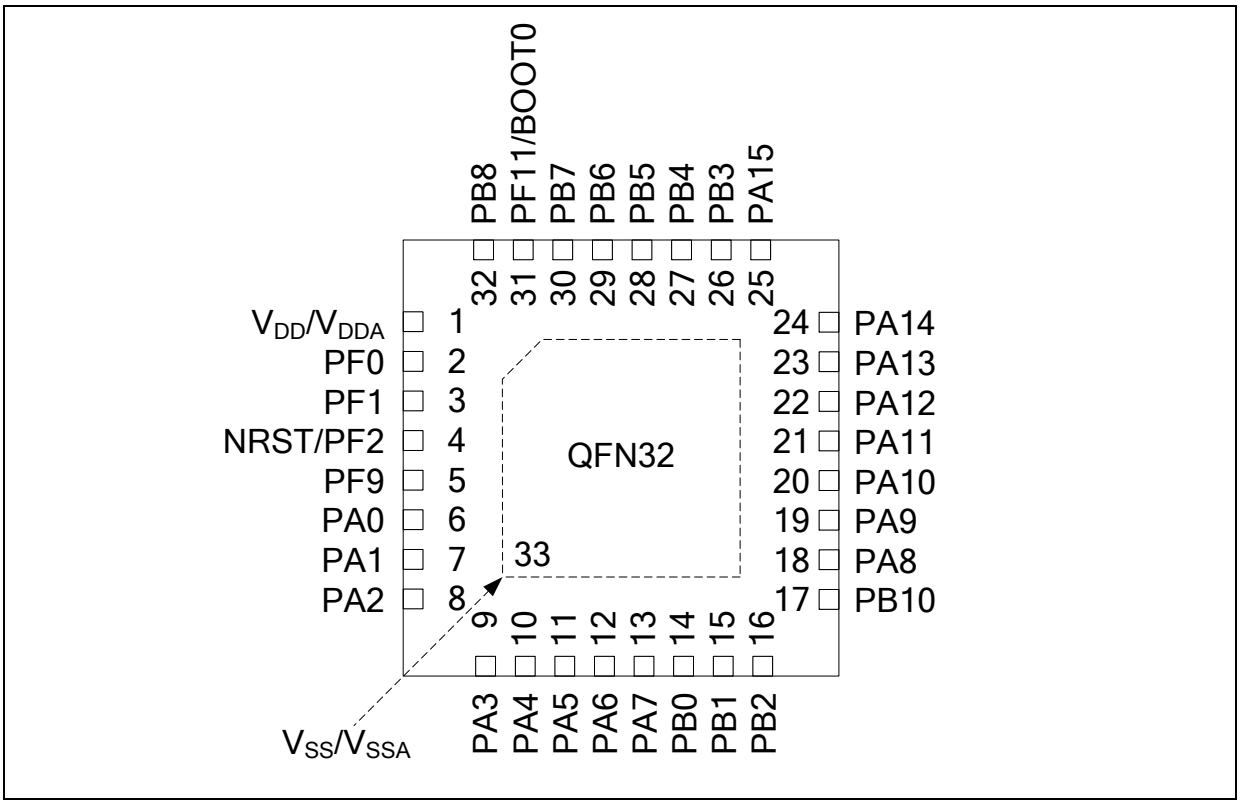
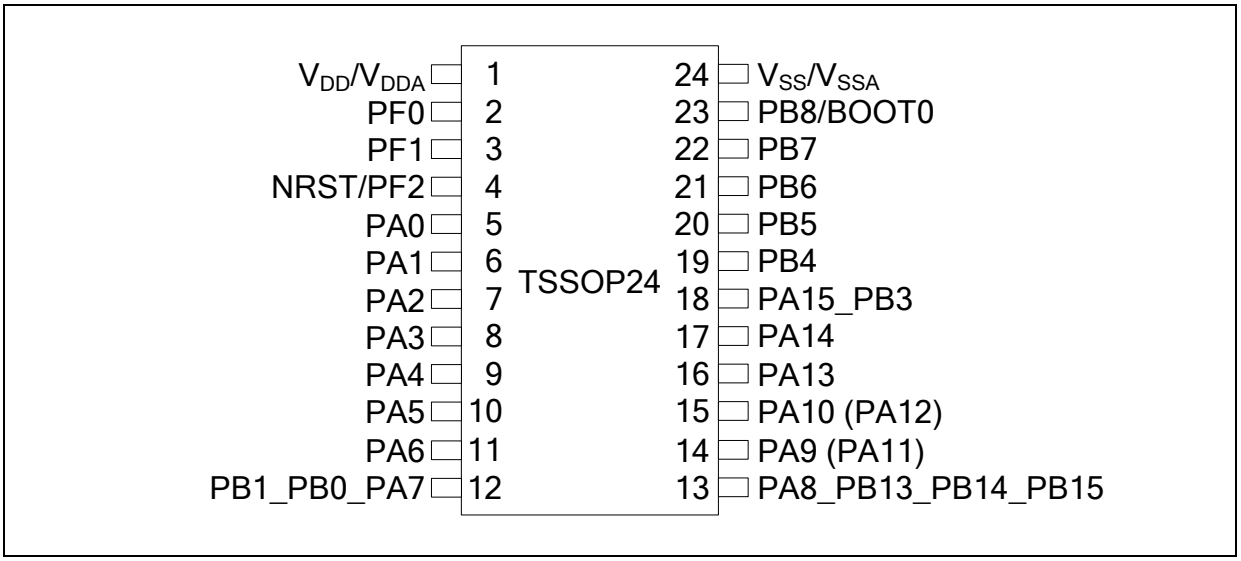


Figure 4. AT32M412/416 TSSOP24 pinout



The table below is the pin definition of the AT32M412/416. The "-" represents that there is no such pinout on the related package. Unless descriptions in () under pin name, the functions during reset and after reset are the same as those of the actual pin name. Unless otherwise specified, all GPIOs are set as analog mode during reset and after reset. Pin multiplexed functions are selected through GPIOx_MUXx register, and the additional functions are directly selected/enabled through peripheral registers.

Table 8. AT32M412/416 series pin definitions

Pin number				Pin name (function after reset)	Type(1)	GPIO level(2)	Multiplexed function (3)	Additional functions
TSSOP24	QFN32	LQFP32	LQFP48					
-	-	-	1	PF8	I/O	FT	-	-
-	-	-	2	PC13(4)	I/O	FT	TMR1_BRK / TMR1_CH1C / TMR1_CH4C	RTC_OUT1 / TAMP_1 / WKUP2
-	-	-	3	PC14(4)	I/O	TC	TMR1_BRK2	LEXT_IN
-	-	-	4	PC15(4)	I/O	TC	TMR9_BRK	LEXT_OUT
2	2	2	5	PF0	I/O	FT	TMR1_CH1 / TMR11_CH1 / I2C1_SDA / SPI2_CS / I2S2_WS / USART1_RX / TMR1_CH3C	HEXT_IN
3	3	3	6	PF1	I/O	FT	TMR1_CH2C / TMR9_CH1C / I2C1_SCL / SPI2_SCK / I2S2_CK / USART1_TX	HEXT_OUT
4	4	4	7	NRST/PF2 ((5))	I/O	TC	CLKOUT	Device reset input / internal reset output (active low)
-	5	5	8	PF9	I/O	FTa	TMR4_CH1 / TMR9_CH1	ADC1_IN23
-	-	-	9	PF10	I/O	FTa	TMR4_CH2 / TMR9_CH2	ADC1_IN24
5	6	6	10	PA0	I/O	FTa	TMR1_EXT / TMR9_CH2C / I2C2_SCL / SPI2_SCK / I2S2_CK / USART2_CTS / USART2_RX / CMP1_OUT	ADC12_IN0 / CMP1_INP2 / CMP1_INM6 / TAMP_2 / WKUP1
6	7	7	11	PA1	I/O	FTa	ERTC_REFIN / TMR9_CH1C / I2C2_SDA / SPI1_SCK / I2S1_CK / I2C1_SMBA / USART2_RTS_DE	ADC2_IN1 / CMP1_INP1 / CMP1_INM0 / OP1_INP0 / OP3_INP2
7	8	8	12	PA2	I/O	FTa	TMR9_CH1 / SPI1_MOSI / I2S1_SD / USART2_TX / CAN1_RX / CMP2_OUT	ADC12_IN2 / CMP1_INM7 / CMP2_INP2 / CMP2_INM6 / OP1_OUT
8	9	9	13	PA3	I/O	FTa	TMR9_CH2 / SPI2_MISO / I2S2_MCK / USART2_RX / CAN1_TX	ADC2_IN3 / CMP2_INP1 / OP1_INP1 / OP1_INM0
9	10	10	14	PA4	I/O	FTa	TMR3_CH2 / I2C1_SCL / SPI1_CS / I2S1_WS / SPI2_CS / I2S2_WS / USART2_CK	ADC12_IN4 / DAC1_OUT / CMP1_INM4 / CMP2_INM4
10	11	11	15	PA5	I/O	FTa	TMR10_CH1C / SPI1_SCK / I2S1_CK	ADC2_IN5 / DAC2_OUT / CMP1_INP0 / CMP1_INM5 / CMP2_INM5 / OP2_INM0
11	12	12	16	PA6	I/O	FTa	TMR1_BRK / TMR3_CH1 / TMR10_CH1 / SPI1_MISO / I2S1_MCK / I2S2_MCK / CMP1_OUT	ADC12_IN6 / CMP2_INM7 / OP2_OUT
12(6)	13	13	17	PA7	I/O	FTa	TMR1_CH1C / TMR3_CH2 / TMR11_CH1 / SPI1_MOSI / I2S1_SD / I2C2_SCL / CMP2_OUT	ADC2_IN7 / CMP2_INP0 / OP1_INP2 / OP2_INP0
12(6)	14	14	18	PB0	I/O	FTa	TMR1_CH2C / TMR3_CH3 / SPI1_MISO / I2S1_MCK / USART2_RX / CMP1_OUT	ADC2_IN8 / OP2_INP2 / OP3_INP0

Pin number				Pin name (function after reset)	Type[1]	GPIO level[2]	Multiplexed function [3]	Additional functions
TSSOP24	QFN32	LQFP32	LQFP48					
12[6]	15	15	19	PB1	I/O	FTa	TMR1_CH3C / TMR3_CH4 / SPI1_MOSI / I2S1_SD / SPI2_SCK / I2S2_CK / USART2_CK	ADC12_IN9 / CMP1_INP3 / CMP1_INM1 / OP3_OUT
-	16	16	20	PB2	I/O	FTa	TMR3_EXT / I2C1_SMBA / SPI2_MISO / I2S2_MCK	ADC2_IN10 / OP3_INM0
-	17	17	21	PB10	I/O	FTa	TMR1_BRK / I2C2_SCL / SPI2_SCK / I2S2_CK / CMP1_OUT	OP3_INM1 / OP4_INM0
-	-	-	22	PB11	I/O	FTa	TMR10_BRK / I2C2_SDA / SPI2_MOSI / I2S2_SD / CMP2_OUT	ADC12_IN11 / OP4_INP2
-	-	-	23	PF12	I/O	FTa	-	ADC1_IN26
-	-	-	24	PF13	I/O	FT	-	-
-	-	-	25	PB12	I/O	FTa	TMR1_BRK / TMR9_BRK / I2C2_SMBA / SPI2_CS / I2S2_WS / CAN1_RX / TMR9_CH2C	ADC12_IN12 / OP4_OUT
13[6]	-	-	26	PB13	I/O	FTa	CLKOUT / TMR1_CH1C / TMR9_CH1C / I2C2_SCL / SPI2_SCK / I2S2_CK / CAN1_TX	OP3_INP1 / OP4_INP0
13[6]	-	-	27	PB14	I/O	FTa	TMR1_CH2C / TMR9_CH1 / I2C2_SDA / SPI2_MISO / I2S2_MCK	ADC12_IN14 / OP2_INP1
13[6]	-	-	28	PB15	I/O	FTa	ERTC_REFIN / TMR1_CH3C / TMR9_CH1C / SPI2_MOSI / I2S2_SD / TMR9_CH2	ADC1_IN15 / WKUP7
13[6]	18	18	29	PA8	I/O	FT	CLKOUT / TMR1_CH1 / TMR4_EXT / I2C1_SDA / I2S2_MCK / I2C2_SCL / USART1_CK / USART2_TX	-
14	19	19	30	PA9	I/O	FT	CLKOUT / TMR1_CH2 / TMR9_BRK / I2C1_SCL / SPI2_SCK / I2S2_CK / I2C2_SMBA / USART1_TX	-
15	20	20	31	PA10	I/O	FT	ERTC_REFIN / TMR1_CH3 / TMR11_BRK / I2C1_SDA / SPI2_MISO / I2S2_MCK / I2C1_SMBA / USART1_RX	-
14[7]	21	21	32	PA11	I/O	FTf	TMR1_CH4 / TMR4_CH1 / I2C2_SCL / SPI2_MOSI / I2S2_SD / I2C1_SMBA / USART1_CTS / USART2_TX / CAN1_RX / TMR1_CH1C / TMR1_BRK2 / CMP1_OUT	-
15[7]	22	22	33	PA12	I/O	FTf	TMR1_EXT / TMR4_CH2 / TMR10_CH1 / I2C2_SDA / SPI2_MISO / I2S2_MCK / USART1_RTS_DE / USART2_RX / CAN1_TX / TMR1_CH2C / CMP2_OUT	-
16	23	23	34	PA13 (SWDIO)[8]	I/O	FT	PA13 / IR_OUT / TMR4_CH3 / TMR10_CH1C / I2C1_SDA / SPI2_MISO / I2S2_MCK / I2C1_SCL	-
-	-	-	35	PF6	I/O	FT	I2C2_SCL	-
-	-	-	36	PF7	I/O	FT	I2C2_SDA	-
17	24	24	37	PA14 (SWCLK)[8]	I/O	FT	PA14 / TMR1_BRK / I2C1_SMBA / SPI2_MOSI / I2S2_SD / I2C1_SDA / USART2_TX	-

Pin number				Pin name (function after reset)	Type(1)	GPIO level(2)	Multiplexed function (3)	Additional functions
TSSOP24	QFN32	LQFP32	LQFP48					
18(6)	25	25	38	PA15	I/O	FT	TMR1_BRK / I2C1_SCL / SPI1_CS / I2S1_WS / SPI2_CS / I2S2_WS / USART1_TX / USART2_RX	-
18(6)	26	26	39	PB3 (SWO)(8)	I/O	FT	PB3 / TMR1_CH2 / TMR3_CH3 / TMR4_EXT / I2C2_SDA / SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / USART1_RTS_DE / USART2_TX / TMR3_EXT	-
19	27	27	40	PB4	I/O	FT	TMR1_CH4C / TMR3_CH1 / TMR11_BRK / I2C2_SDA / SPI1_MISO / I2S1_MCK / SPI2_MISO / I2S2_MCK / USART1_CTS / USART2_RX / TMR10_CH1	-
20	28	28	41	PB5	I/O	FT	TMR3_CH2 / TMR10_BRK / I2C1_SMBA / SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / USART1_CK / USART2_CK / CAN1_RX / TMR11_CH1 / CMP2_OUT	WKUP6
21	29	29	42	PB6	I/O	FT	TMR1_CH3C / TMR4_CH1 / TMR10_CH1C / I2C1_SCL / I2S1_MCK / SPI2_CS / I2S2_WS / USART1_TX / CAN1_TX	-
22	30	30	43	PB7	I/O	FT	TMR1_CH1C / TMR4_CH2 / TMR11_CH1C / I2C1_SDA / SPI2_MOSI / I2S2_SD / USART1_RX / CAN1_STB / TMR3_CH4	-
-	31	-	44	BOOT0/PF11(9) (PF11)	I/O	TC	-	Boot mode 0
23	-	31	-	BOOT0/PB8(9) (PB8)	I/O	TC	-	Boot mode 0
-	32	-	45	PB8(10)	I/O	FTf	TMR1_CH2C / TMR4_CH3 / TMR10_CH1 / I2C1_SCL / SPI2_SCK/ I2S2_CK / USART1_TX / CAN1_RX / TMR1_BRK / TMR9_BRK / CMP1_OUT	-
-	-	-	46	PB9	I/O	FTf	IR_OUT / TMR1_CH3C / TMR4_CH4 / TMR11_CH1 / I2C1_SDA / SPI2_CS / I2S2_WS / I2C2_SDA / CAN1_TX / CMP2_OUT	-
24	-	32	47	V_{SS}/V_{SSA}	S	-	Digital ground / analog ground	
1	1	1	48	V_{DD}/V_{DDA}	S	-	Digital power supply / analog power supply	
-	33	-	-	EPAD - V_{SS}/V_{SSA}	S	-	Digital ground / analog ground	

(1) I = input, O = output, S = power supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability.

(3) Available features depend on the selected model. EVENTOUT feature is available on any GPIO.

(4) PC13, PC14 and PC15 are in the master function state at the first power-on of battery powered domain, and their states are controlled by the battery powered domain registers (these registers are not reset by master reset) even after reset. For details about GPIO control, refer to the battery powered domain and BPR registers contents in *AT32M412/416 Series Reference Manual*.

(5) After power on reset, NRST/PF2 are used as NRST in input pull-up state. It can be configured to PF2 by software. Its function is not affected by other resets.

(6) To maximize pin functionalities and improve current souring/sinking strength, these pins are internal pads wire bonded on a single pin. Therefore, attention must be paid to settings of different pads to avoid interference between functions or short circuit. The chip is not designed with a protection mechanism against such misoperation.

(7) PA11/PA12 and their multiplexed functions can be remapped by software to replace the original PA9/PA10 and their multiplexed functions.

(8) After reset, PA13/PA14/PB3 pins are configured as multiplexed function SWDIO/SWCLK/SWO. In this case, the internal pull-up resistor on SWDIO/SWO pins and internal pull-down resistor on SWCLK pin are activated.

(9) When multiplexed with BOOT0, PF11 or PB8 can only be set as general-purpose push-pull mode. An external pull-down resistor (3.3 kΩ or below) to ground is required.

(10) During the period from reset release to software executable, the hardware enables a pull-down resistor (about 200 μs) for PB8 and then restores it to its default state.

4 Electrical characteristics

4.1 Test conditions

4.1.1 Maximum and minimum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

4.1.2 Typical values

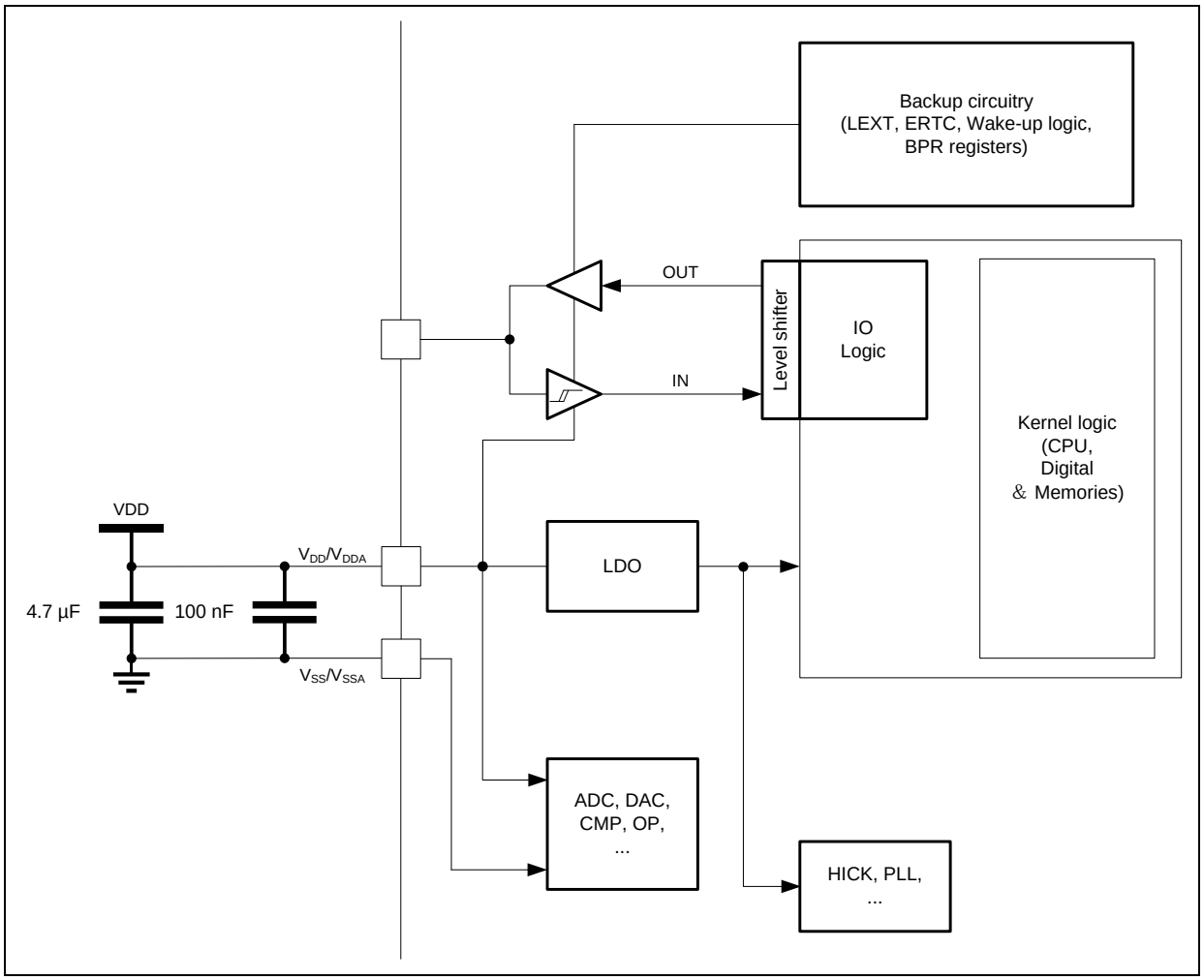
Typical values are based on T_A = 25 °C and V_{DD} = 3.3 V.

4.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

4.1.4 Power supply scheme

Figure 5. Power supply scheme



4.2 Absolute maximum values

4.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 9*, *Table 10* and *Table 11*, it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 9. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DD} and V_{DDA})	-0.3	4.0	V
V_{IN}	Input voltage on TC GPIOs	V_{SS}-0.3	4.0	
	Input voltage on FT, FTa and FTf GPIOs	V_{SS}-0.3	6.0	
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 10. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	100	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIO and control pin	-25	

Table 11. Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2023/JS-002-2022 standard.

Table 12. ESD values

Symbol	Parameter	Conditions	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conform to JS-001-2023	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conform to JS-002-2022	III	±2000	

Static latch-up

Tests compliant with JESD78F latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 13. Latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conform to JESD78F	II level A (±200 mA)

4.3 Specifications

4.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Condition		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	LDO voltage	1.3 V	0	180	MHz
			1.2 V	0	150	
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-		0	f_{HCLK}	MHz
f_{PCLK3}	Internal APB3 clock frequency	-		0	90	MHz
V_{DD}	Digital operating voltage	-		2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}		V_{DD}		V
P_D	Power dissipation: T_A = 105 °C	LQFP48 (7 x 7 mm)		-	229	mW
		LQFP32 (7 x 7 mm)		-	225	
		QFN32 (4 x 4 mm)		-	326	
		TSSOP24 (7.8 x 4.4 mm)		-	229	
T_A	Ambient temperature	-		-40	105	°C

4.3.2 Operating conditions at power-up / power-down

Table 15. Operating conditions at power-up / power-down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	μs/V
	V_{DD} fall time rate		20	∞	μs/V

4.3.3 Embedded reset and power control block characteristics

Table 16. Embedded reset and power control block characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	1.73	2.06	2.4	V
V_{LVR}	Low voltage reset threshold	1.62(2)	1.88	2.16	V
$V_{LVRhyst}$	LVR hysteresis	-	180	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	890	-	μs

(1) Guaranteed by characterization results, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 6. Power on reset and low voltage reset waveform

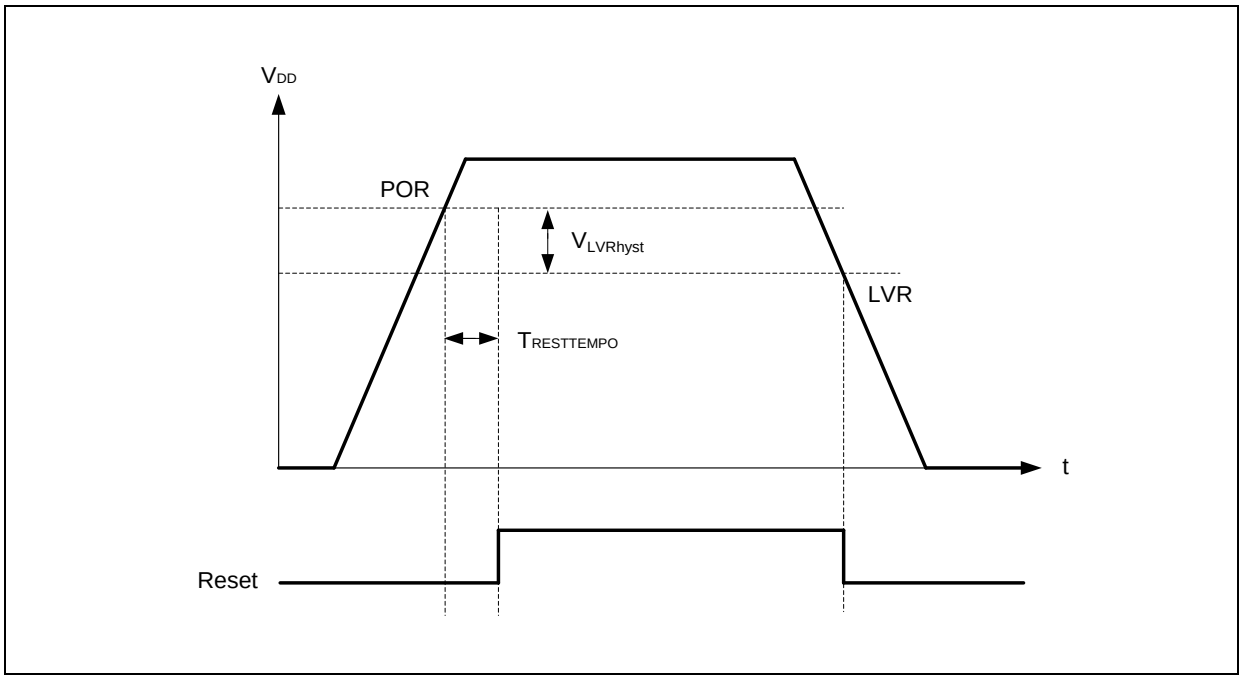


Table 17. Programmable voltage regulator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge(1)	2.28	2.38	2.48	V
		Falling edge(1)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge(1)	2.38	2.48	2.58	V
		Falling edge(1)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge(1)	2.47	2.58	2.69	V
		Falling edge(1)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge(1)	2.57	2.68	2.79	V
		Falling edge(1)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge(1)	2.66	2.78	2.9	V
		Falling edge(1)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(1)	PVM hysteresis	-	-	100	-	mV
$I_{DD(PVM)}$(1)	PVM current dissipation	-	-	20	30	µA

(1) Guaranteed by characterization results, not tested in production.

4.3.4 Memory characteristics

Table 18. Flash memory characteristics(1)

Symbol	Parameter	Typ	Max	Unit
T_{PROG}	Programming time	60	65	μs
t_{ERASE}	Sector erase time	6.6	8	ms
t_{ME}	Mass erase time	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 19. Flash memory endurance and data retention(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	year

(1) Guaranteed by design, not tested in production.

4.3.5 Supply current characteristics

The current consumption, obtained by characterization results and not tested in production, is subject to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin toggling rate, and executed binary code.

Typical and maximum current consumption

The device is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on the f_{HCLK} frequency (0 ~ 32 MHz: zero wait state; 33 ~ 64 MHz: one wait state; 65 ~ 96 MHz: two wait states; 97 ~ 128 MHz: three wait states; 129 ~ 160 MHz: four wait states; above 160 MHz: five wait states).
- Prefetch ON.
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/8$.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition, and the maximum values are measured with V_{DD} = 3.6 V.

Table 20. Typical current consumption in Run mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage	Typ		Unit
					All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1)(2)	180 MHz	1.3 V	46.6	25.4	mA
			168 MHz	1.3 V	43.6	23.8	
			150 MHz	1.2 V	36.2	19.8	
			120 MHz	1.2 V	29.7	16.5	
			108 MHz	1.2 V	26.8	15.0	
			72 MHz	1.2 V	18.3	10.3	
			64 MHz	1.2 V	16.4	9.32	
			48 MHz	1.2 V	12.9	7.60	
			36 MHz	1.2 V	9.99	5.98	
			24 MHz	1.2 V	7.36	4.69	
			16 MHz	1.2 V	5.30	3.51	
			8 MHz	1.2 V	2.93	2.02	
			4 MHz	1.2 V	2.04	1.57	
			2 MHz	1.2 V	1.59	1.35	
			1 MHz	1.2 V	1.38	1.24	
		High speed internal crystal (HICK)(2)	180 MHz	1.3 V	46.3	25.1	mA
			168 MHz	1.3 V	43.3	23.4	
			150 MHz	1.2 V	35.9	19.5	
			120 MHz	1.2 V	29.3	16.1	
			108 MHz	1.2 V	26.5	14.6	
			72 MHz	1.2 V	17.9	9.95	
			64 MHz	1.2 V	16.0	8.93	
			48 MHz	1.2 V	12.5	7.18	
			36 MHz	1.2 V	9.56	5.57	
			24 MHz	1.2 V	6.93	4.28	
			16 MHz	1.2 V	4.86	3.09	
			8 MHz	1.2 V	2.47	1.59	
			4 MHz	1.2 V	1.58	1.14	
			2 MHz	1.2 V	1.13	0.92	
			1 MHz	1.2 V	0.91	0.81	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 21. Typical current consumption in Sleep mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage	Typ		Unit
					All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1)(2)	180 MHz	1.3 V	34.9	12.9	mA
			168 MHz	1.3 V	32.7	12.1	
			150 MHz	1.2 V	27.1	10.1	
			120 MHz	1.2 V	22.4	8.74	
			108 MHz	1.2 V	20.3	7.98	
			72 MHz	1.2 V	13.9	5.70	
			64 MHz	1.2 V	12.5	5.20	
			48 MHz	1.2 V	9.98	4.50	
			36 MHz	1.2 V	7.78	3.67	
			24 MHz	1.2 V	5.89	3.15	
			16 MHz	1.2 V	4.33	2.49	
			8 MHz	1.2 V	2.44	1.51	
			4 MHz	1.2 V	1.80	1.32	
			2 MHz	1.2 V	1.48	1.22	
			1 MHz	1.2 V	1.32	1.18	
		High speed internal crystal (HICK)(2)	180 MHz	1.3 V	34.6	12.5	mA
			168 MHz	1.3 V	32.3	11.7	
			150 MHz	1.2 V	26.8	9.75	
			120 MHz	1.2 V	22.0	8.35	
			108 MHz	1.2 V	19.9	7.58	
			72 MHz	1.2 V	13.5	5.29	
			64 MHz	1.2 V	12.1	4.79	
			48 MHz	1.2 V	9.56	4.09	
			36 MHz	1.2 V	7.35	3.25	
			24 MHz	1.2 V	5.46	2.73	
			16 MHz	1.2 V	3.88	2.07	
			8 MHz	1.2 V	1.98	1.08	
			4 MHz	1.2 V	1.34	0.89	
			2 MHz	1.2 V	1.01	0.79	
			1 MHz	1.2 V	0.86	0.75	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 22. Maximum current consumption in Run mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1), all peripherals enabled	180 MHz	1.3 V	47.5	48.3	mA
			168 MHz	1.3 V	44.5	45.4	
			150 MHz	1.2 V	36.9	37.6	
			120 MHz	1.2 V	30.3	31.0	
			108 MHz	1.2 V	27.5	28.2	
			72 MHz	1.2 V	19.0	19.7	
			64 MHz	1.2 V	17.1	17.8	
			48 MHz	1.2 V	13.6	14.4	
			36 MHz	1.2 V	10.7	11.5	
			24 MHz	1.2 V	8.12	8.85	
			16 MHz	1.2 V	6.07	6.81	
			8 MHz	1.2 V	3.71	4.44	
		High speed external crystal (HEXT)(1), all peripherals disabled	180 MHz	1.3 V	26.2	27.1	mA
			168 MHz	1.3 V	24.6	25.5	
			150 MHz	1.2 V	20.5	21.2	
			120 MHz	1.2 V	17.2	17.9	
			108 MHz	1.2 V	15.7	16.4	
			72 MHz	1.2 V	11.1	11.8	
			64 MHz	1.2 V	10.1	10.8	
			48 MHz	1.2 V	8.34	9.07	
			36 MHz	1.2 V	6.74	7.47	
			24 MHz	1.2 V	5.46	6.19	
			16 MHz	1.2 V	4.29	5.01	
			8 MHz	1.2 V	2.80	3.52	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.

Table 23. Maximum current consumption in Sleep mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled	180 MHz	1.3 V	35.8	36.6	mA
			168 MHz	1.3 V	33.5	34.4	
			150 MHz	1.2 V	27.8	28.5	
			120 MHz	1.2 V	23.1	23.8	
			108 MHz	1.2 V	21.0	21.7	
			72 MHz	1.2 V	14.6	15.4	
			64 MHz	1.2 V	13.2	14.0	
			48 MHz	1.2 V	10.7	11.5	
			36 MHz	1.2 V	8.53	9.27	
			24 MHz	1.2 V	6.66	7.40	
			16 MHz	1.2 V	5.10	5.83	
			8 MHz	1.2 V	3.22	3.95	
		High speed external crystal (HEXT)(1), all peripherals disabled	180 MHz	1.3 V	13.8	14.7	mA
			168 MHz	1.3 V	13.0	13.9	
			150 MHz	1.2 V	10.9	11.7	
			120 MHz	1.2 V	9.51	10.3	
			108 MHz	1.2 V	8.75	9.50	
			72 MHz	1.2 V	6.48	7.22	
			64 MHz	1.2 V	5.98	6.71	
			48 MHz	1.2 V	5.28	6.02	
			36 MHz	1.2 V	4.45	5.18	
			24 MHz	1.2 V	3.93	4.66	
			16 MHz	1.2 V	3.27	4.00	
			8 MHz	1.2 V	2.29	3.02	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.

Table 24. Typical and maximum current consumptions in Deepsleep and Standby modes

Sym.	Parameter	Condition	Typ(1)		Max(2)			Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode	LDO in Run mode, HICK and HEXT OFF, WDT OFF	271	275	325	1030	1720	µA
		LDO in extra low-power mode, HICK and HEXT OFF, WDT OFF	135	138	160	570	1000	
	Supply current in Standby mode	LEXT and ERTC OFF	2.5	3.8	4.9	6.7	9.4	µA
		LEXT and ERTC ON	3.4	5.0	6.2	8.1	10.9	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 7. Typical current consumption in Deepsleep mode with LDO in Run mode vs. temperature at different V_{DD}

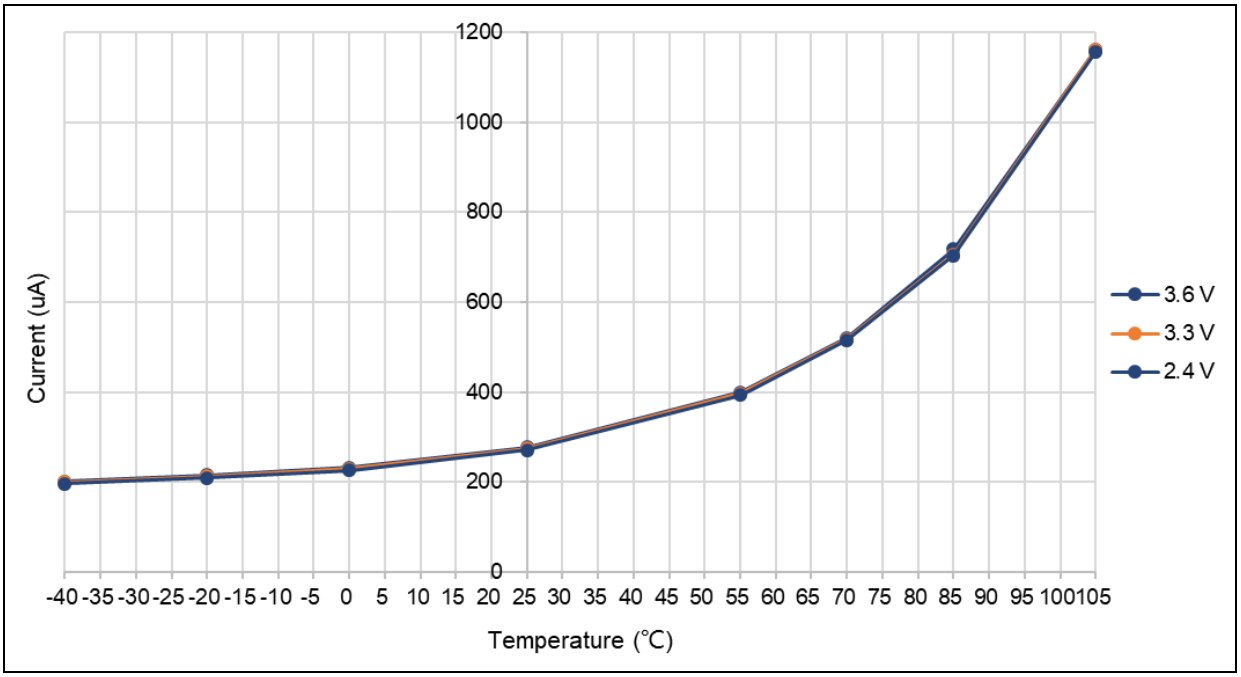


Figure 8. Typical current consumption in Deepsleep mode with LDO in extra low-power mode vs. temperature at different V_{DD}

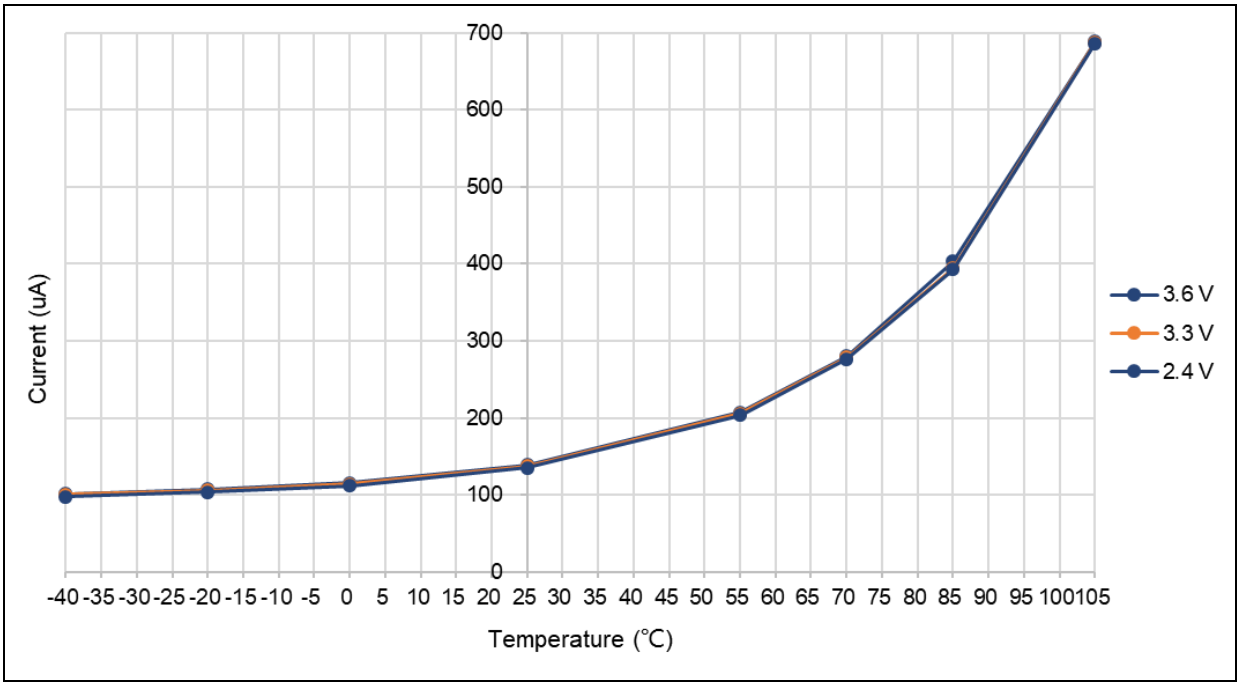
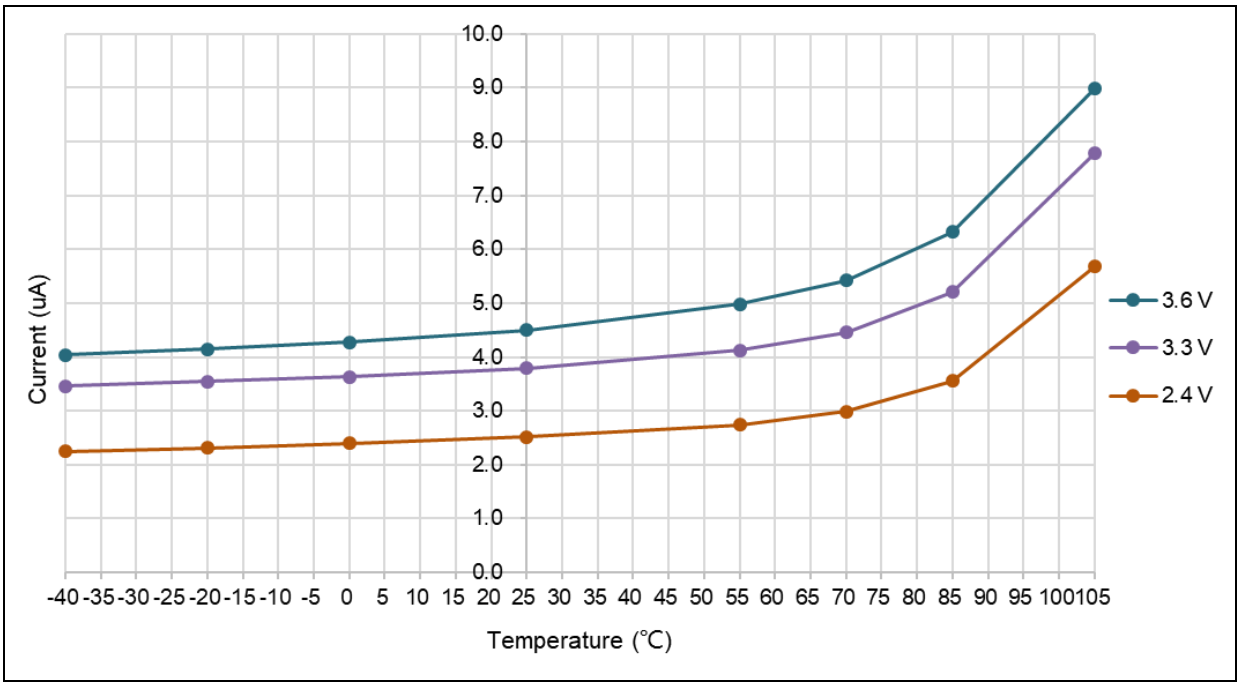


Figure 9. Typical current consumption in Standby mode vs. temperature at different V_{DD}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 25. Peripheral current consumption

Peripheral		LDO voltage		Unit
		1.3 V	1.2 V	
AHB	DMA1	7.10	6.58	μA/MHz
	SRAM	0.64	0.61	
	Flash	20.04	18.47	
	GPIOA	0.60	0.56	
	GPIOB	0.60	0.57	
	GPIOC	0.59	0.56	
	GPIOF	0.58	0.54	
	CRC	0.50	0.48	
APB1	TMR3	9.94	9.18	
	TMR4	10.10	9.33	
	TMR6	0.48	0.46	
	TMR7	0.48	0.45	
	WWDT	0.14	0.12	
	SPI2/I^2S2	2.89	2.67	
	USART2	3.93	3.63	
	I^2C1	7.25	6.69	
	I^2C2	7.54	6.95	
	CAN1	5.32	4.95	
	PWC	0.75	0.69	
	DAC1/2	1.14	1.06	
APB2	SCFG + CMP1/2 + OP1/2/3/4	3.58	3.31	
	SPI1/I^2S1	2.98	2.76	
	USART1	3.72	3.43	
	TMR1	16.61	15.35	
	TMR9	8.54	7.88	
	TMR10	4.69	4.32	
	TMR11	4.77	4.40	
	ADC1	14.54	13.43	
	ADC2	14.26	13.17	

4.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be generated with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

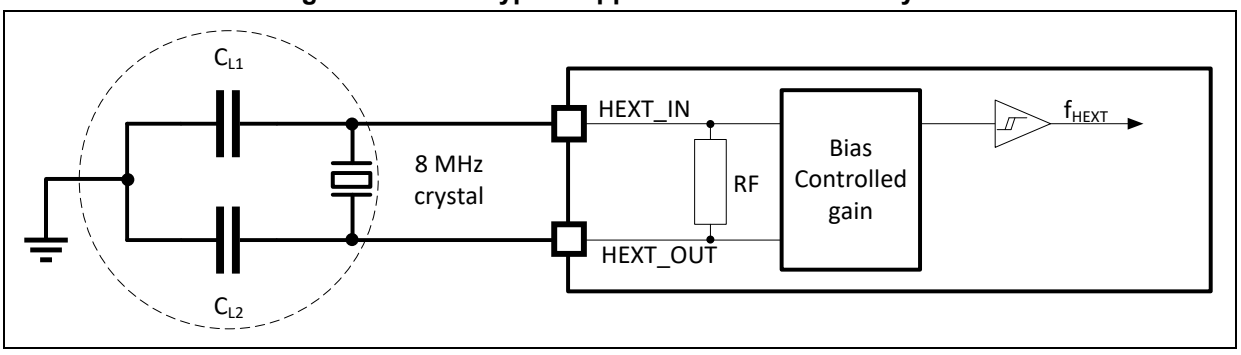
Table 26. HEXT 4 ~ 25 MHz crystal characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HEXT}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	8 MHz, HEXTDRV = 0x2	-	1.2	-	ms
$I_{DD(HEXT)}$	Current consumption	8 MHz, HEXTDRV = 0x2	-	420	560	μA

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough estimate of the combined pin and board capacitance) when selecting C_{L1} and C_{L2}.

Figure 10. HEXT typical application with 8 MHz crystal



High-speed external clock generated from an external source

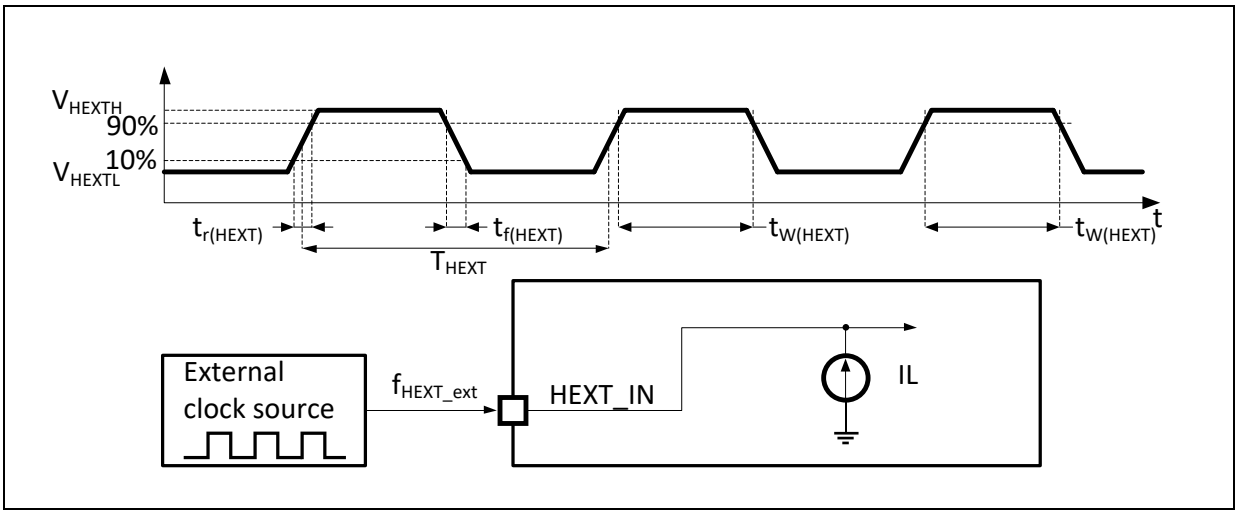
The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 27. HEXT external source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$Duty_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 11. High-speed external clock source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be generated with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 28. LEXT 32.768 kHz crystal characteristics(1)(2)

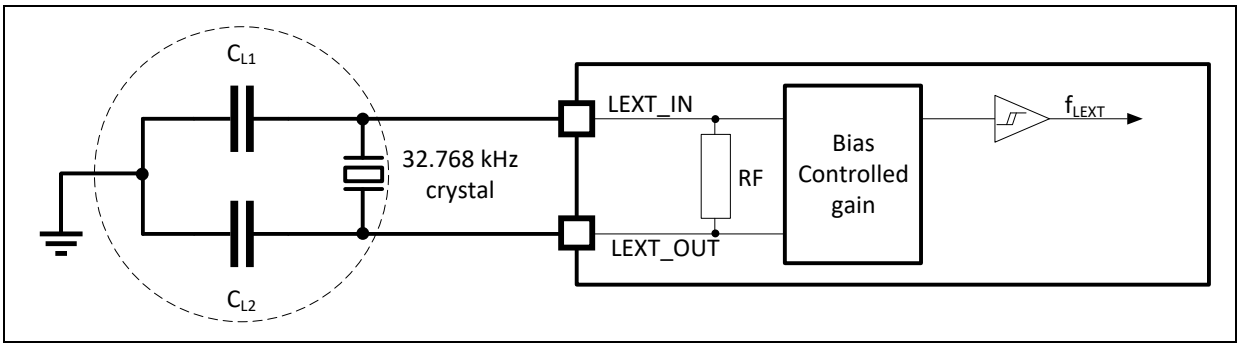
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	LEXTDRV = 0x3	-	90	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range and select to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 12. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

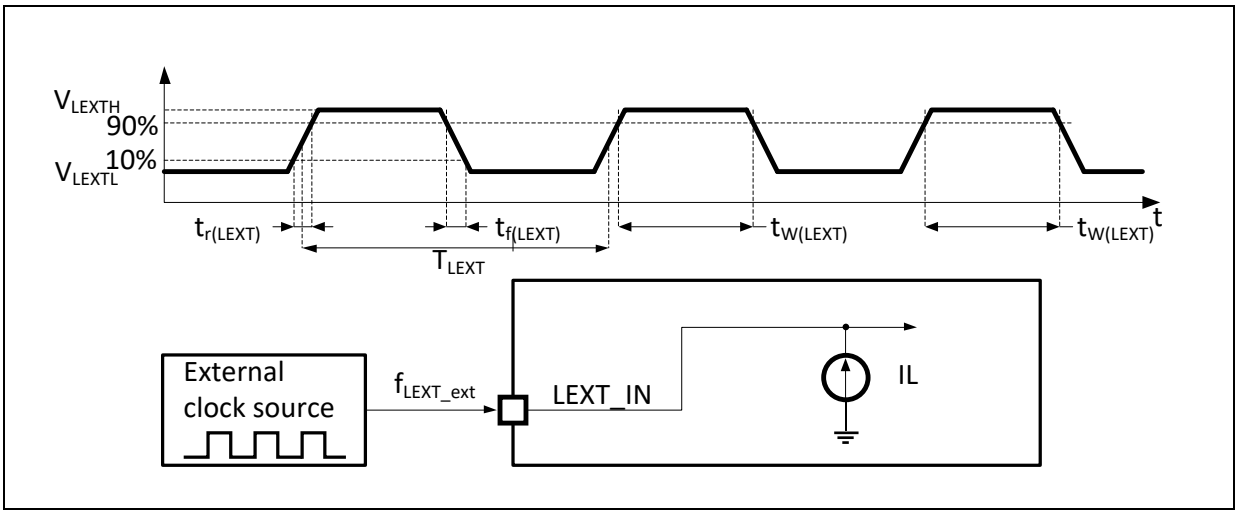
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 29. Low-speed external source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LEXT_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$Duty_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 13. Low-speed external clock source AC timing diagram



4.3.7 Internal clock source characteristics

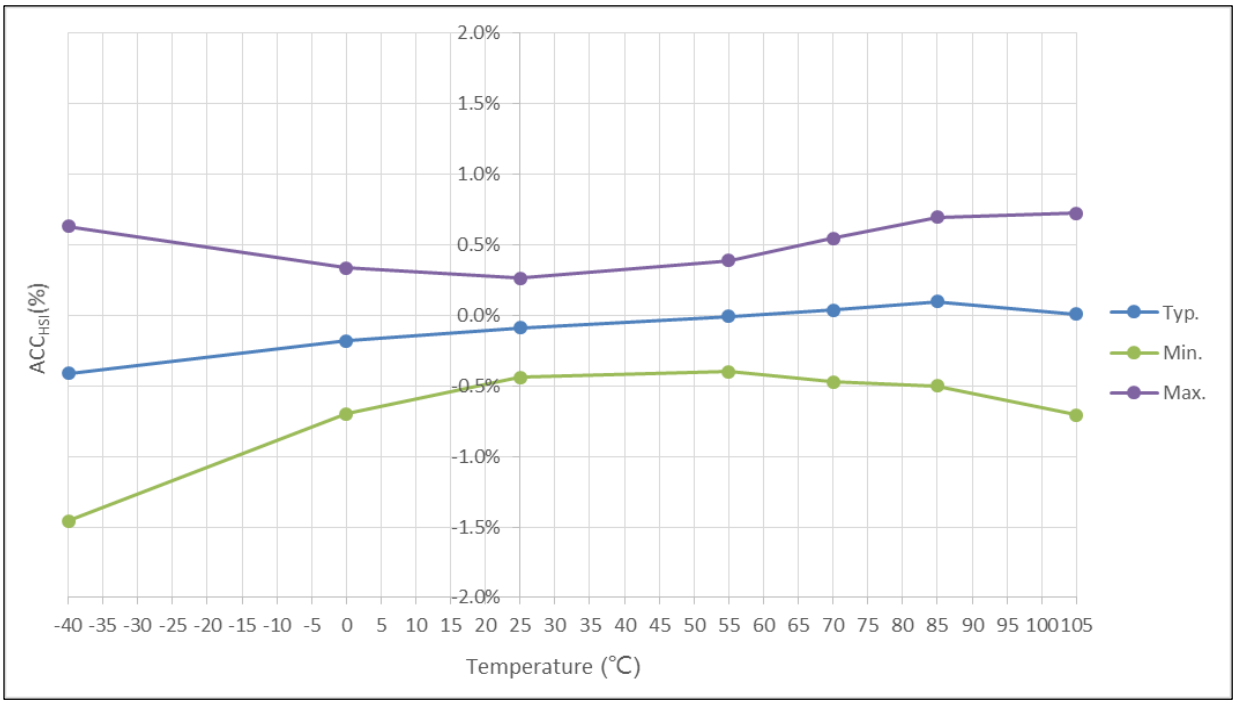
High-speed internal clock (HICK)

Table 30. HICK clock characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy	User-trimmed with the CRM_CTRL register(1)		-1	-	1	%
		Factory-calibrated(2)	T_A = -40 ~ 105 °C	-2	-	1.5	%
			T_A = -40 ~ 85 °C	-2	-	1.2	%
			T_A = 0 ~ 70 °C	-1.5	-	1.2	%
			T_A = 25 °C	-1	-	1	%
$t_{SU(HICK)}$(2)	Startup time	-		-	0.8	1.0	µs
$I_{DD(HICK)}$(2)	Power consumption	-		-	300	350	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 14. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 31. LICK clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	25	35	45	kHz

(1) Guaranteed by characterization results, not tested in production.

4.3.8 PLL characteristics

Table 32. PLL characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	180	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Use the appropriate multiplier factor to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

4.3.9 Wakeup time from low-power mode

The wakeup times given in the table below are measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK

Table 33. Low-power mode wakeup time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	3.3	µs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode (LDO in Run mode)	480	µs
	Wakeup from Deepsleep mode (LDO in extra low-power mode)	540	
$t_{WUSTDBY}$	Wakeup from Standby mode	820	µs

4.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 34. EMS characteristics

Sym.	Parameter	Condition	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional error. Both V_{DD} and V_{SS} have a 47 µF capacitor on their entries. Each V_{DD} and V_{SS} pair has 0.1 µF bypass capacitor.	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 180 MHz	4/A (4 kV)
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 150 MHz	
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 8 MHz	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user

application and the software in particular. Therefore, it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

4.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 35. GPIO static characteristics

Sym.	Parameter	Condition		Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-		-0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	TCGPIO input high level voltage	-		0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT, FTa and FTf GPIO input high level voltage	-			-	5.5	
V_{hys}	Schmitt trigger voltage hysteresis(1)	-		200	-	-	mV
				5% V_{DD}	-	-	-
I_{lkg}	Input floating mode leakage current(2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIOs		-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5$ V FT, FTa and FTf GPIOs		-	-	±1	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	GPIOs other than PF2	60	80	130	kΩ
			PF2	30	40	50	
R_{PD}	Weak pull-down equivalent resistor(3)(4)	$V_{IN} = V_{DD}$	GPIOs other than PF2	60	70	130	kΩ
			PF2	30	40	50	
C_{IO}	GPIO pin capacitance	-		-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
(2) Leakage could be higher than the max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT, FTa and FTf pins.
(4) The weak pull-down resistor of BOOT0 is active automatically during reset.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins that can drive current must be controlled to respect the absolute maximum rating defined in *Section 4.2.1*.

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 10*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 10*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 36. Output voltage characteristics

Symbol	Parameter	Condition	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS port, I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL port, I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL port, I_{IO} = 5 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Maximum sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS port, I_{IO} = 15 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL port, I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Ultra high sinking strength(2)					
V_{OL}	Output low level voltage	I_{IO} = 25 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OL}	Output low level voltage	I_{IO} = 18 mA, 2.4 V ≤ V_{DD} < 2.7 V			

(1) Guaranteed by characterization results, not tested in production.
(2) When GPIO ultra high sinking strength is enabled, its V_{OH} is the same as that of maximum sourcing strength.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 37. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$(1)	Pulse width of external signals detected by EXINT controller	10	-	ns

(1) Guaranteed by design, not tested in production.

4.3.12 NRST pin characteristics

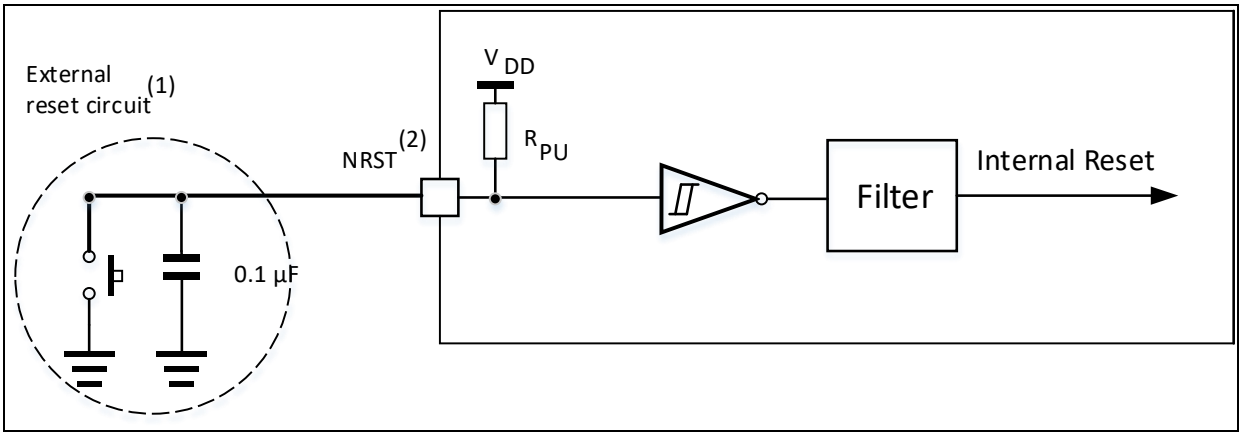
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 38. NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.3	-	0.72	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$(2)	NRST Schmitt trigger voltage hysteresis	-	-	400	-	mV
R_{PU}(2)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level inactive	-	-	-	40	μs
$t_{ILNV(NRST)}$(1)	NRST input low level active	-	80	-	-	μs

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 15. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 38*. Otherwise, the reset will not be performed by the device.

4.3.13 TMR characteristics

The parameters given in the table below are guaranteed by design.

Table 39. Timer characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 180 MHz	5.56	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz

4.3.14 SPI characteristics

Table 40. SPI characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency$^{(2)(3)}$	Master mode	-	36	MHz
		Slave receive mode	-	36	
		Slave transmit mode	-	32	
$t_{su(CS)}^{(1)}$	CS setup time	Slave mode	$2t_{PCLK}$	-	ns
$t_{h(CS)}^{(1)}$	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, prescaler factor = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode	4	-	ns
$t_{h(SI)}^{(1)}$		Slave mode	5	-	
$t_{a(SO)}^{(1)(4)}$	Data output access time	Slave mode	t_{PCLK}	$2t_{PCLK}$ + 25	ns
$t_{dis(SO)}^{(1)(5)}$	Data output disable time	Slave mode	t_{PCLK}	$2t_{PCLK}$ + 25	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency in slave mode should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is the minimum time to drive the output, and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output, and the max time is for the maximum time to put the data in Hi-Z.

Figure 16. SPI timing diagram – slave mode and CPHA = 0

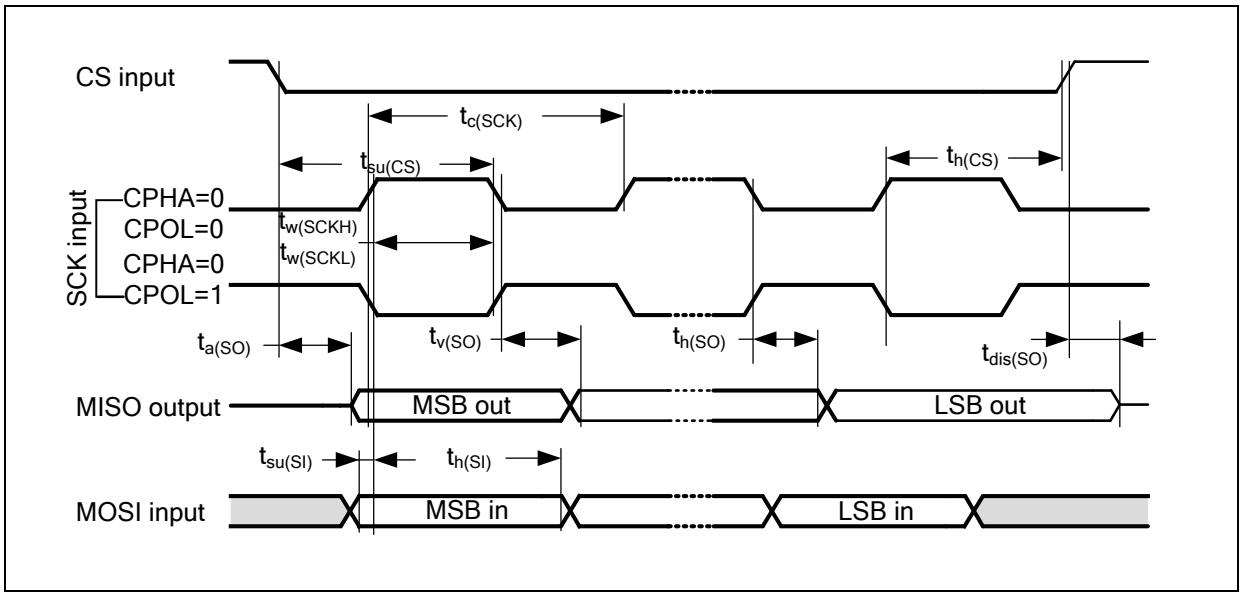


Figure 17. SPI timing diagram – slave mode and CPHA = 1

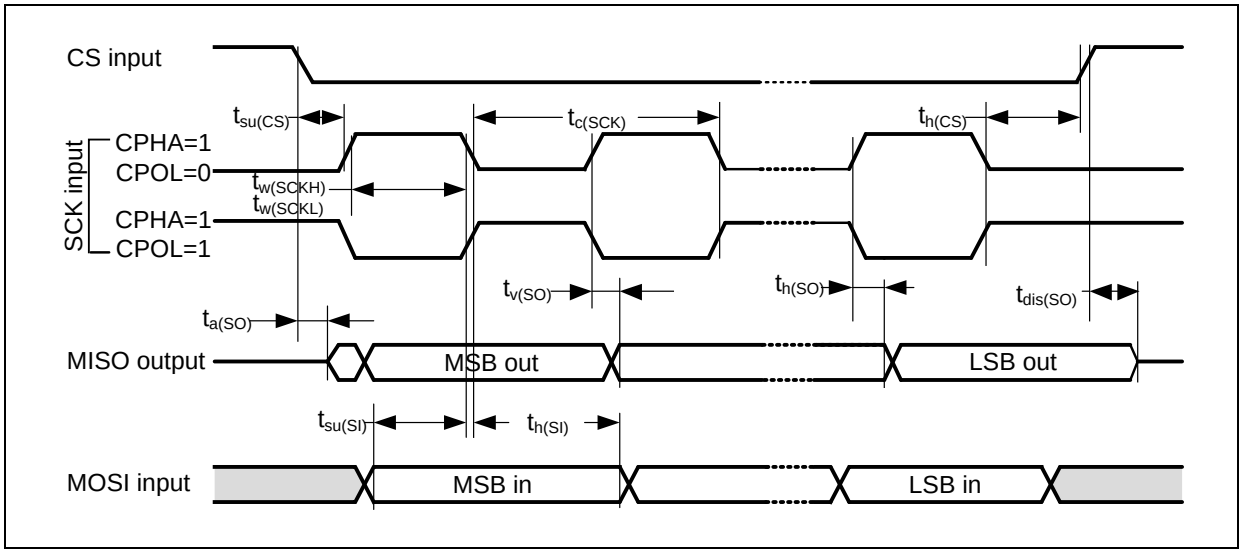
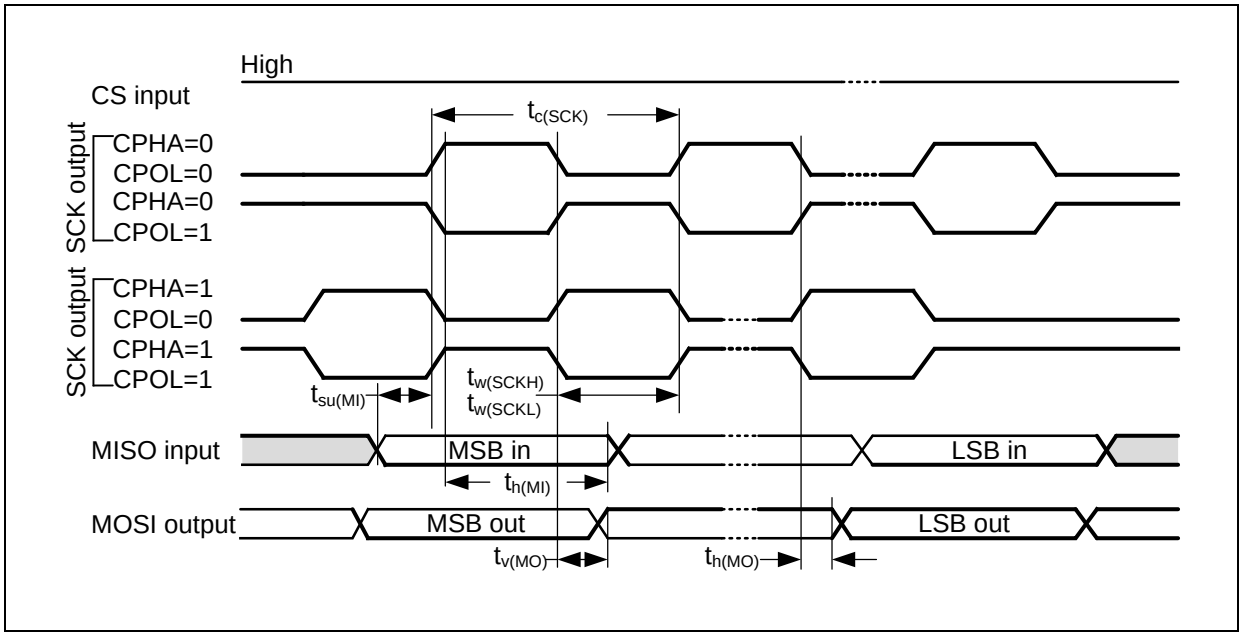


Figure 18. SPI timing diagram – master mode



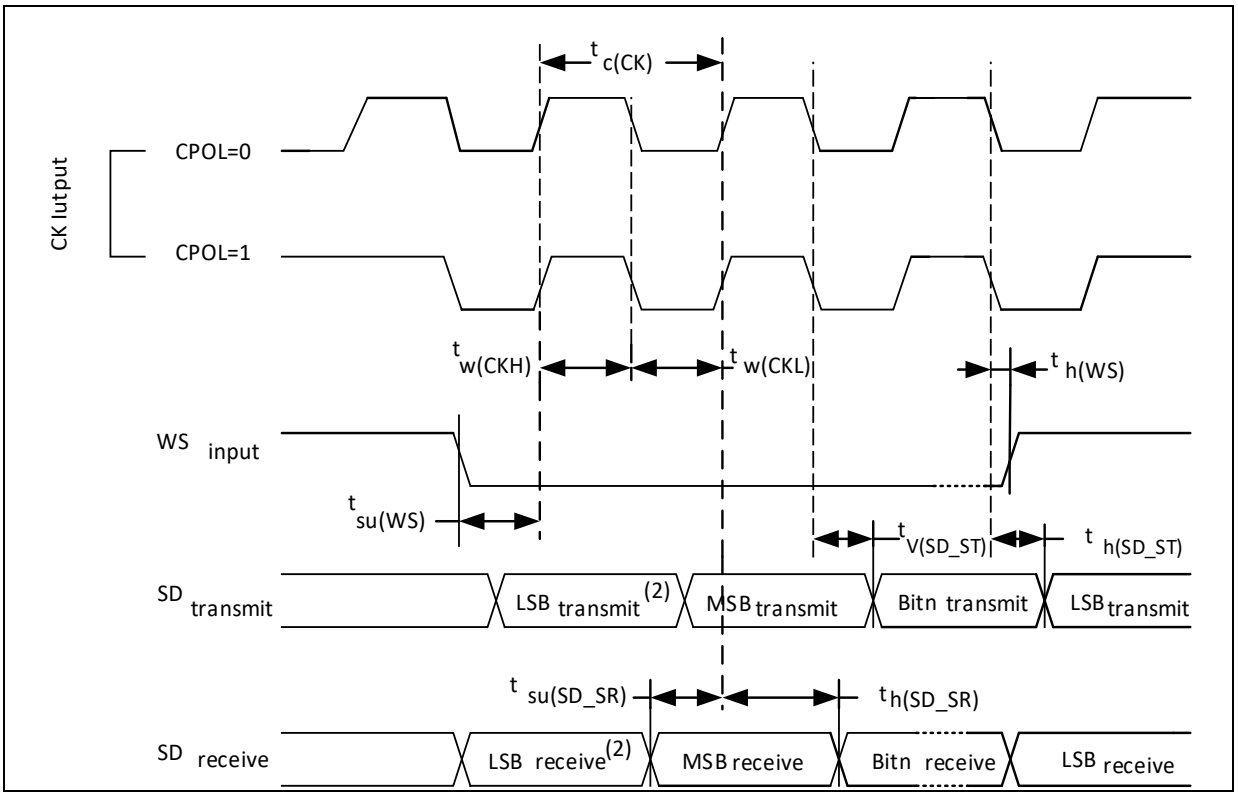
4.3.15 I²S characteristics

Table 41. I²S characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	0	4	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	4	
$t_{su(WS)}$(1)	WS setup time	Slave mode	9	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

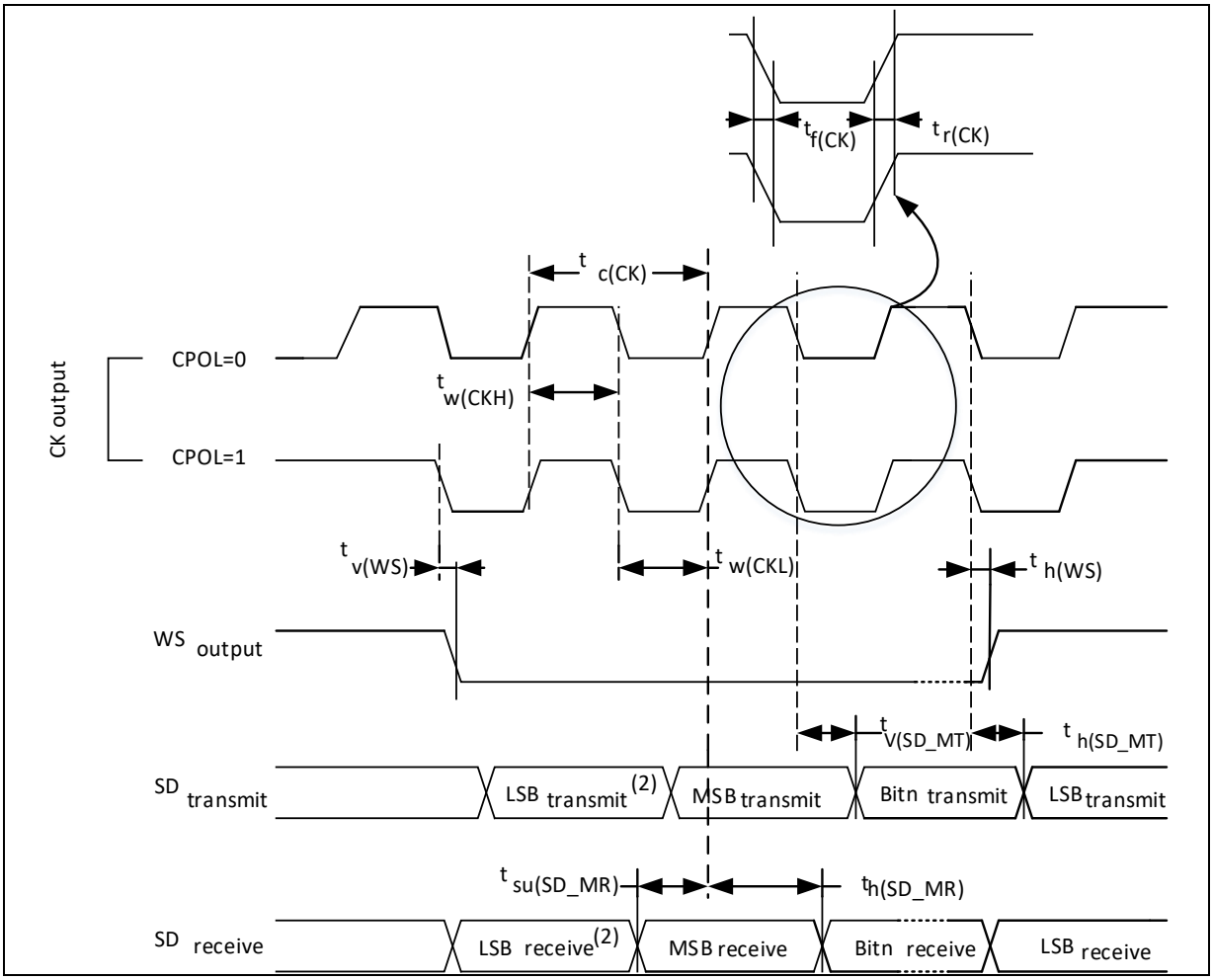
(1) Guaranteed by design, not tested in production.
(2) Dependent on f_{PCLK}. For example, when f_{PCLK} = 8 MHz, t_{PCLK} = 1/f_{PCLK} = 125 ns.

Figure 19. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 20. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

4.3.16 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and VDD is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz).

4.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Note: It is recommended to perform a calibration after each power-up.

Table 42. ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}(1)	Analog supply voltage	-	2.4	-	3.6	V
I_{DDA}(1)	Analog supply current	-	-	600(1)	720	μA
f_{ADC}	ADC clock frequency	-	0.6	-	35	MHz
f_S(2)	Sampling rate	-	0.05	-	2.5	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 35 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-} connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 43* and *Table 44*			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	10	13	pF
t_{latr}(2)	Trigger conversion latency	f_{ADC} = 35 MHz	-	-	71.4	ns
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 35 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 35 MHz	0.5	-	9	μs
		-	14~252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} may be connected to V_{DDA} internally, and V_{REF-} to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency listed in *Table 42*.

Table 43 and *Table 44* define the maximum external impedance allowed for an error below 1 LSB.

Table 43. R_{AIN} max when f_{ADC} = 14 MHz(1)

T_S (cycle)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.11	0.35
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

(1) Guaranteed by design.

Table 44. R_{AIN} max when f_{ADC} = 35 MHz(1)

T_S (cycle)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

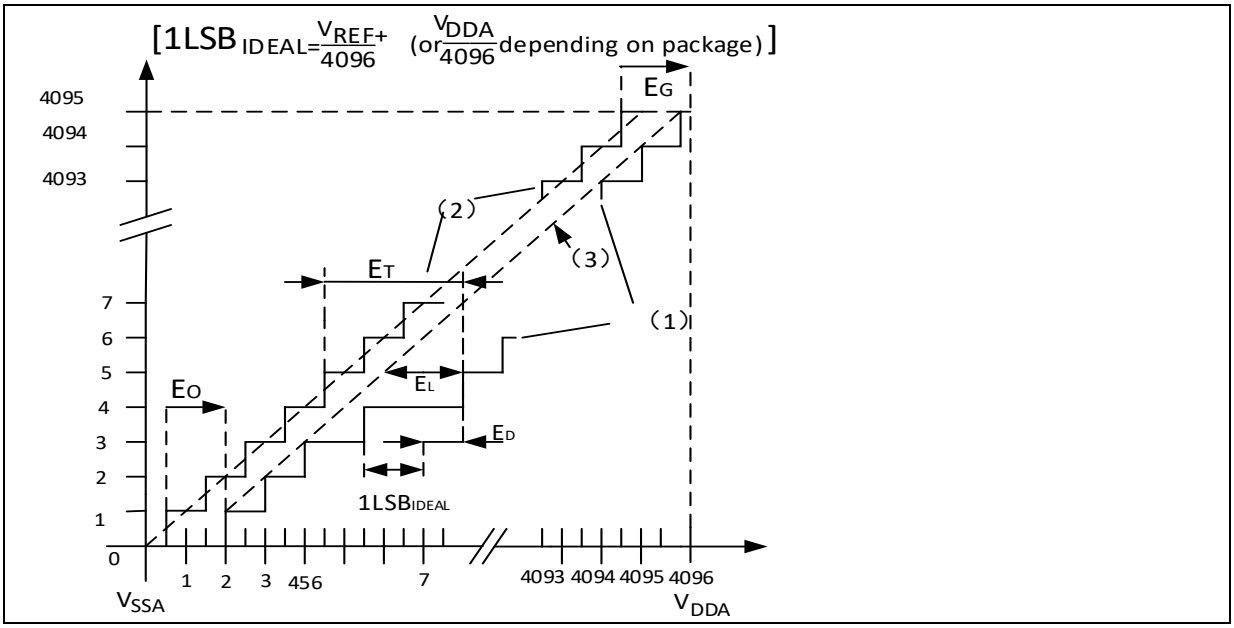
(1) Guaranteed by design.

Table 45. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 70 MHz, f_{ADC} = 35 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0~3.6 V, T_A = 25 °C	±2.5	±4	LSB
EO	Offset error		±1	±2	
EG	Gain error		-1.5	-3.5	
ED	Differential linearity error		±1	+1.5/-1	
EL	Integral linearity error		±1.5	±2.5	
ET	Total unadjusted error	f_{PCLK2} = 70 MHz, f_{ADC} = 35 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4~3.6 V, T_A = -40 ~ 105 °C	±3	±5	LSB
EO	Offset error		±1.5	±2	
EG	Gain error		-2	-4	
ED	Differential linearity error		+1.2/-1	+2/-1	
EL	Integral linearity error		±2	±3	

(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

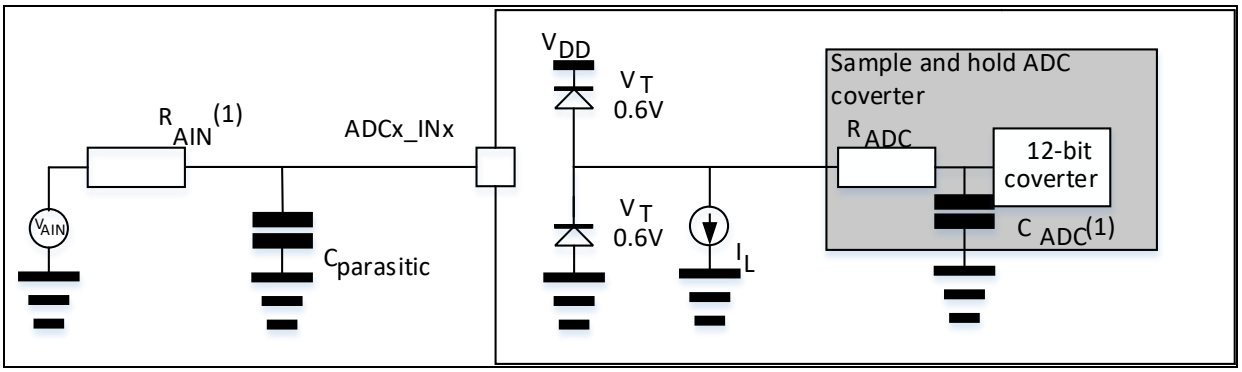
Figure 21. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
E_T = Maximum deviation between the actual and the ideal transfer curves.

E_O = Deviation between the first actual transition and the first ideal one.
E_G = Deviation between the last ideal transition and the last actual one.
E_D = Maximum deviation between actual steps and the ideal one.
E_L = Maximum deviation between any actual transition and the end point correlation line.

Figure 22. Typical connection diagram using the ADC



(1) Refer to *Table 42* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 5*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

4.3.18 Internal reference voltage (V_{INTRV}) characteristics

Table 46. Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

4.3.19 Temperature sensor (V_{TS}) characteristics

Table 47. Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	T_A = -20 ~ 85 °C	-	±1	±2	ºC
		T_A = -40 ~ 105 °C	-	-	±3	
Avg_Slope(1)(2)	Average slope	-	-4.11	-4.25	-4.39	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	-	1.16	1.28	1.40	V
t_{START}(3)	Setup time	-	-	-	100	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

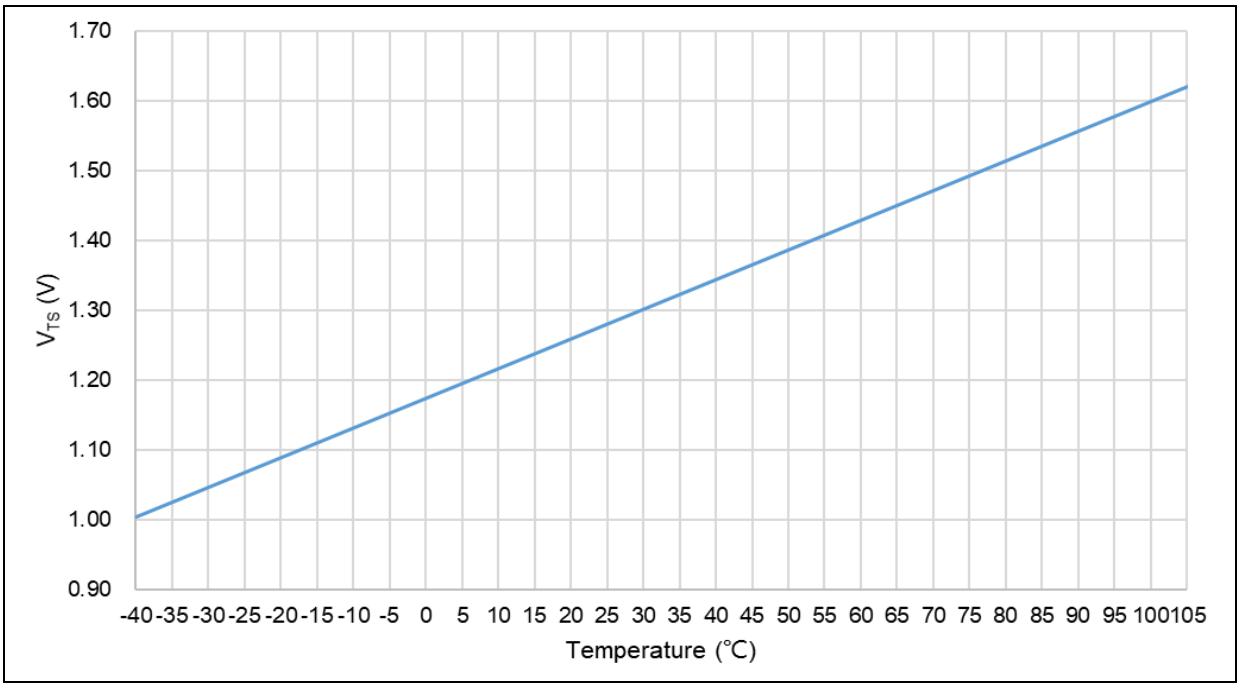
Temperature (°C) = {(V_{25} – V_{TS}) / Avg_Slope} + 25

where,

V_{25} = V_{TS} value for 25 °C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{TS} (given in mV/°C)

Figure 23. V_{TS} vs. temperature



4.3.20 6-bit DAC characteristics

Table 48. DAC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V_{SSA}(1)	Analog supply ground	-	0	-	0	V
V_{REF+}(2)	Reference voltage	-	1.16	-	3.6	V
R_O(3)	Output impedance	-	-	68	-	kΩ
DAC_OUT(4)	Lower DAC_OUT voltage	-	-	1.5	30	mV
	Higher DAC_OUT voltage	-	-	-	V_{REF+} - 70 mV	V
I_{DDA}(1)(4)	DAC DC current consumption in quiescent mode	-	-	14	20	μA
DNL(4)	Differential non linearity	-	-	±0.1	±0.3	LSB
INL(4)	Integral non linearity (difference between measured value at Code i and a line drawn between DAC_OUT max and DAC_OUT min)	-	-	±0.1	±0.5	LSB
Offset(4)	Offset error (difference between measured value at Code (0x20) and the ideal value = V_{REF+}/2)	-	-	±0.2	±1	LSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Gain(4)	Gain error	-	-	±0.2	±1	LSB
tSETTLING(3)	Setting time	Output to CMP or OP	-	5	10	µs
		Output to GPIO	-	8	-	
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1 LSB)	Output to CMP or OP	-	-	1	MSPS
		Output to GPIO	-	0.2	-	
tWAKEUP(3)	Wakeup time from off state (setting the EN bit in the DAC control register)	-	-	-	8	µs

(1) V_{REF-} is internally connected to V_{SSA}.
(2) V_{REF+} can be V_{DDA} or V_{INTRV}, selected by software.
(3) Guaranteed by design, not tested in production.
(4) Guaranteed by characterization results, not tested in production.

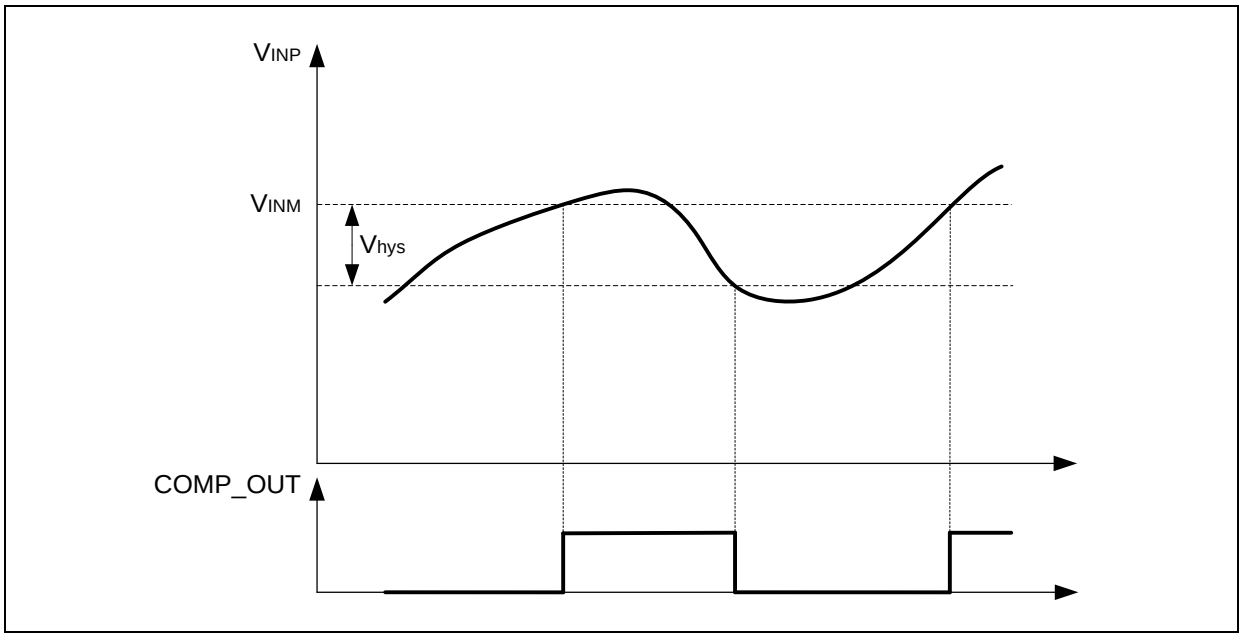
4.3.21 Comparator (CMP) characteristics

Table 49. Comparator characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power voltage	-	2.4	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
t_{START}	Startup time	High speed mode	-	0.8	1.8	µs
		Medium speed mode	-	1.5	3	
		Low power mode	-	2.4	4	
		Ultra low power mode	-	5	8	
t_D	Propagation delay for 200 mV step, with 100 mV override	High speed mode	-	40	80	ns
		Medium speed mode	-	100	160	
		Low power mode	-	160	300	
		Ultra low power mode	-	400	800	
V_{offset}	Offset voltage	-	-	±4	±15	mV
V_{hys}	Hysteresis	No hysteresis	-	0	1	mV
		Low hysteresis	5	15	25	
		Medium hysteresis	15	30	45	
		High hysteresis	30	60	120	
I_{DDA}	Analog supply current	High speed mode	-	55	85	µA
		Medium speed mode	-	18	30	
		Low power mode	-	8	15	
		Ultra low power mode	-	3.5	9	

(1) Guaranteed by characterization results, not tested in production.

Figure 24. CMP hysteresis



4.3.22 Operational amplifier (OP) characteristics

Table 50. OP characteristics(1)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DDA}(2)	Analog supply voltage	-		2.4	-	3.6	V
I_{DDA}(2)	Analog supply current	Output to GPIO	General mode	-	1.24	1.63	mA
			High speed mode	-	1.28	1.67	
		Output to ADC	General mode	-	310	400	µA
			High speed mode	-	350	440	
V_{OFFSET}(2)	Offset voltage (after calibration)(3)	-		-	1.5	3	mV
ΔV_{OFFSET}	Offset voltage drift	-		-	±10	-	µV/ºC
V_{COMM}	Common mode input range	-		0	-	V_{DDA}	V
I_{bias}	Input bias current	-		-	±20	±1000	nA
V_{OUT}(2)	Output voltage range	-		0.1	-	V_{DDA} – 0.1	V
I_{LOAD}	Driving current	Non-PGA mode		-	-	500	µA
		PGA mode		-	-	270	
R_{LOAD}	Resistive load	-		4	-	-	kΩ
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	-		-	100	-	dB
PSRR	Power supply rejection ratio	-		-	80	-	dB
GBW(2)	Gain bandwidth	Voltage follower mode		5	8.5	-	MHz
SR(2)	Slew rate	General mode		4.5	8	-	V/µs
		High speed mode		16	30	-	
A_O	Open loop gain	-		60	85	-	dB
φm	Phase margin	-		-	60	-	degree
GM	Gain margin	-		-	10	-	dB
t_{WAKEUP}(2)	Wakeup time from OFF state	-		-	2	3	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
G_{PGA_NINV}(2)	PGA non-inverting gain	Gain = 2	-1	-	1	%
		Gain = 4	-1	-	1	
		Gain = 8	-1	-	1	
		Gain = 16	-1	-	1	
		Gain = 32	-2	-	2	
		Gain = 64	-2	-	2	
G_{PGA_INV}(2)	PGA inverting gain	Gain = -1	-1	-	1	%
		Gain = -3	-1	-	1	
		Gain = -7	-1	-	1	
		Gain = -15	-1	-	1	
		Gain = -31	-2	-	2	
		Gain = -63	-2	-	2	
R_{INM_VSSA}	PGA internal resistor between inverting input and V_{SSA}	-	-	10	-	kΩ
R_{INM_OUT}	PGA internal resistor between inverting input and output	Gain = 2 or -1	-	10	-	kΩ
		Gain = 4 or -3	-	30	-	
		Gain = 8 or -7	-	70	-	
		Gain = 16 or -15	-	150	-	
		Gain = 32 or -31	-	310	-	
		Gain = 64 or -63	-	630	-	
BW_{PGA_NINV}	PGA non-inverting gain bandwidth	Gain = 2	-	GBW / 2	-	MHz
		Gain = 4	-	GBW / 4	-	
		Gain = 8	-	GBW / 8	-	
		Gain = 16	-	GBW / 16	-	
		Gain = 32	-	GBW / 32	-	
		Gain = 64	-	GBW / 64	-	
BW_{PGA_INV}	PGA inverting gain bandwidth	Gain = -1	-	GBW / 2	-	MHz
		Gain = -3	-	GBW / 4	-	
		Gain = -7	-	GBW / 8	-	
		Gain = -15	-	GBW / 16	-	
		Gain = -31	-	GBW / 32	-	
		Gain = -63	-	GBW / 64	-	
eN	Voltage-noise density	1 kHz, R_{LOAD} = 4 kΩ	-	250	-	nV/√Hz
		10 kHz, R_{LOAD} = 4 kΩ	-	90	-	
T_{S_OP}	ADC sampling time when reading the OP internal output	±0.5 LSB accuracy	-	-	250	ns
		±0.1 % accuracy	-	-	200	
$t_{RECOVERY}$	Overload recovery time	General mode	-	-	800	ns
		High speed mode	-	-	300	
V_{CLAMP}	Clamping diode clamp voltage	1 μA	-	650	-	mV
		100 μA	-	750	-	
		5 mA	-	850	-	

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.
(3) Calibrate before using the operational amplifier; otherwise, the offset error does not conform to this value.

5 Package information

5.1 LQFP48 – 7 x 7 mm

Figure 25. LQFP48 – 7 x 7 mm 48-pin low-profile quad flat package outline

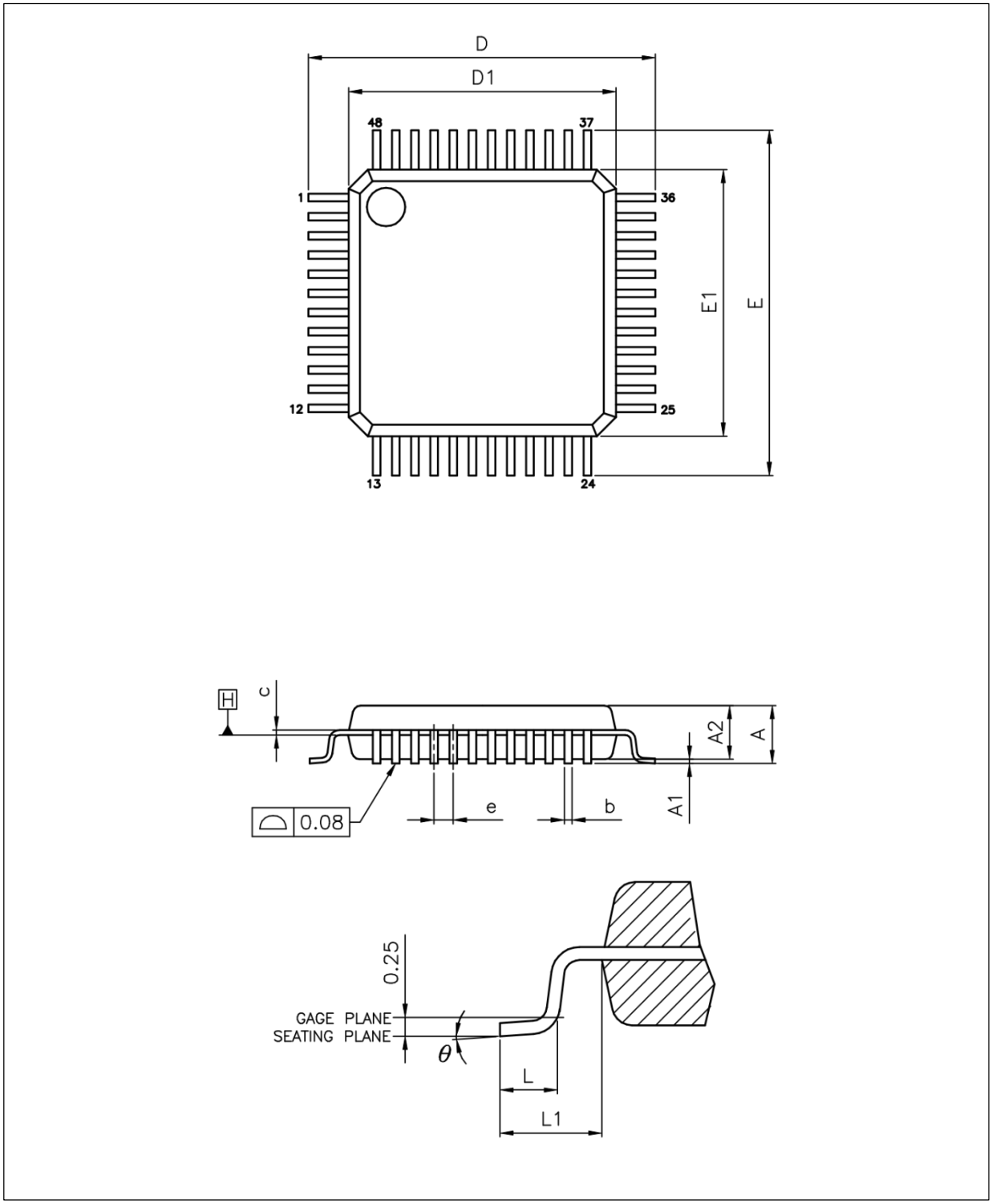


Figure 51. LQFP48 – 7 x 7 mm 48-pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

5.2 LQFP32 – 7 x 7 mm

Figure 26. LQFP32 – 7 x 7 mm 32-pin low-profile quad flat package outline

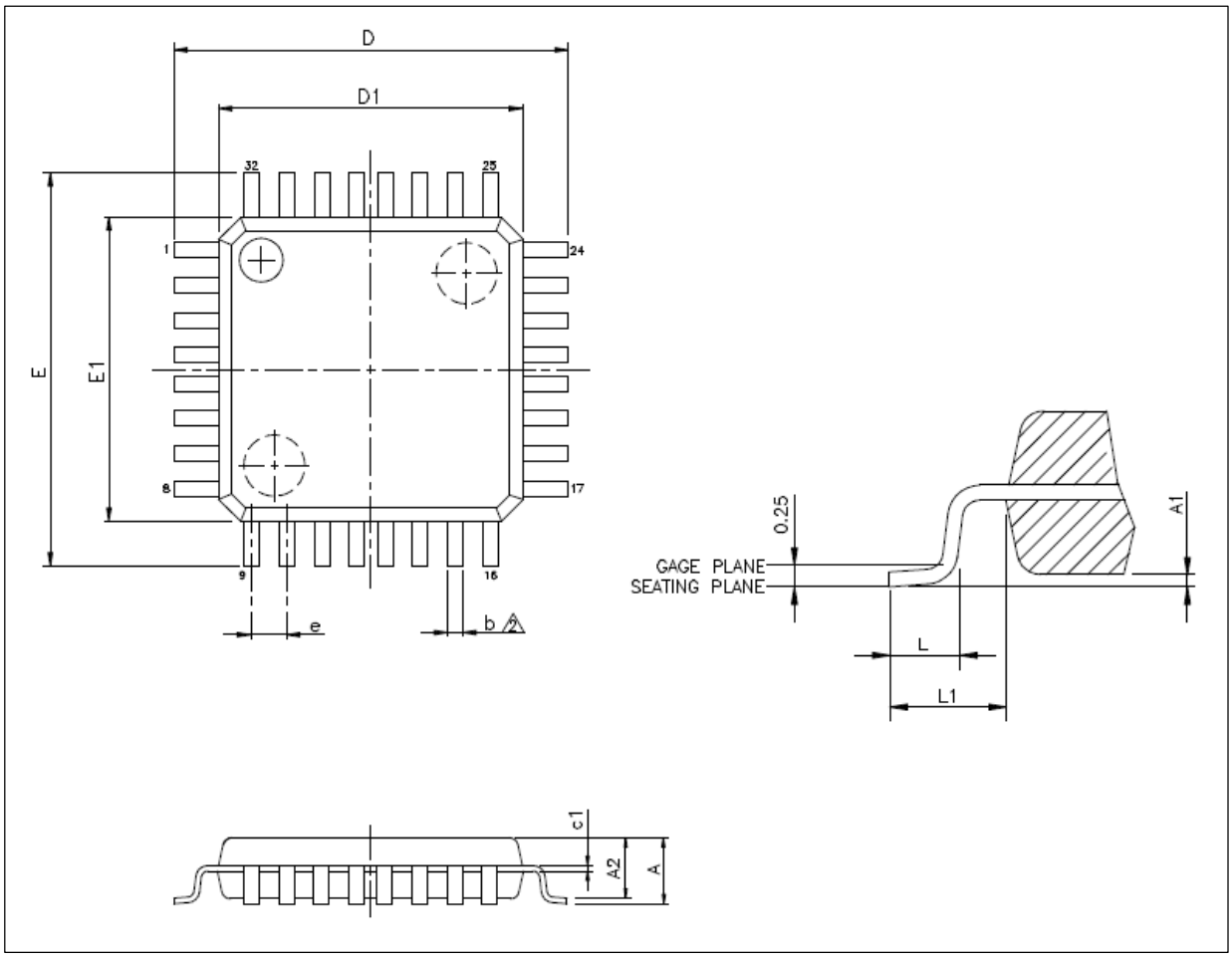


Table 52. LQFP32 – 7 x 7 mm 32-pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
b	0.30	-	0.45
c	0.09	-	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80 BSC.		
L	0.45	-	0.75
L1	1.00 REF.		

5.3 QFN32 – 4 x 4 mm

Figure 27. QFN32 – 4 x 4 mm 32-pin quad flat no-leads package outline

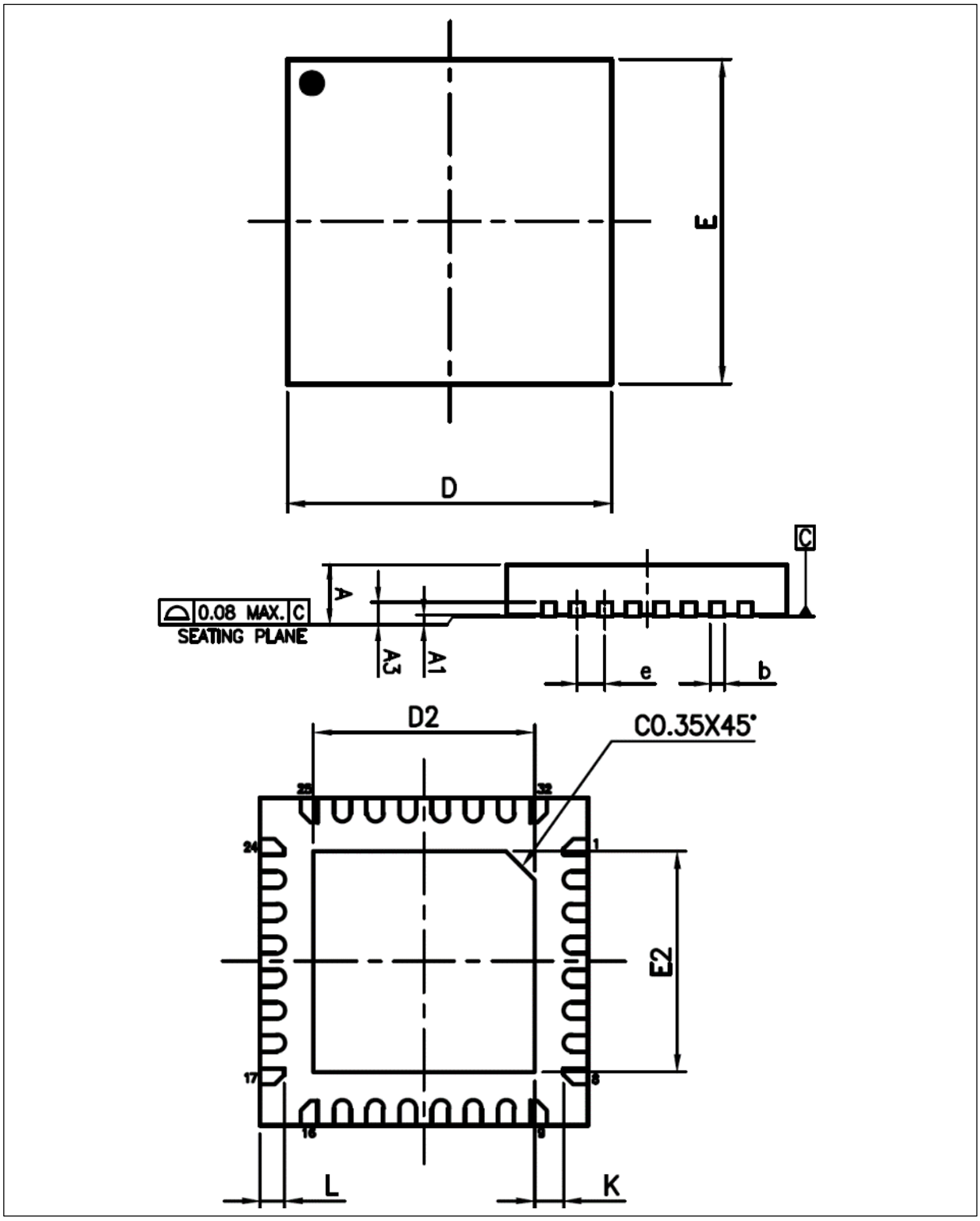


Table 53. QFN32 – 4 x 4 mm 32-pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

5.4 TSSOP24 – 7.8 x 4.4 mm

Figure 28. TSSOP24 – 7.8 x 4.4 mm 24-pin thin-shrink small outline package

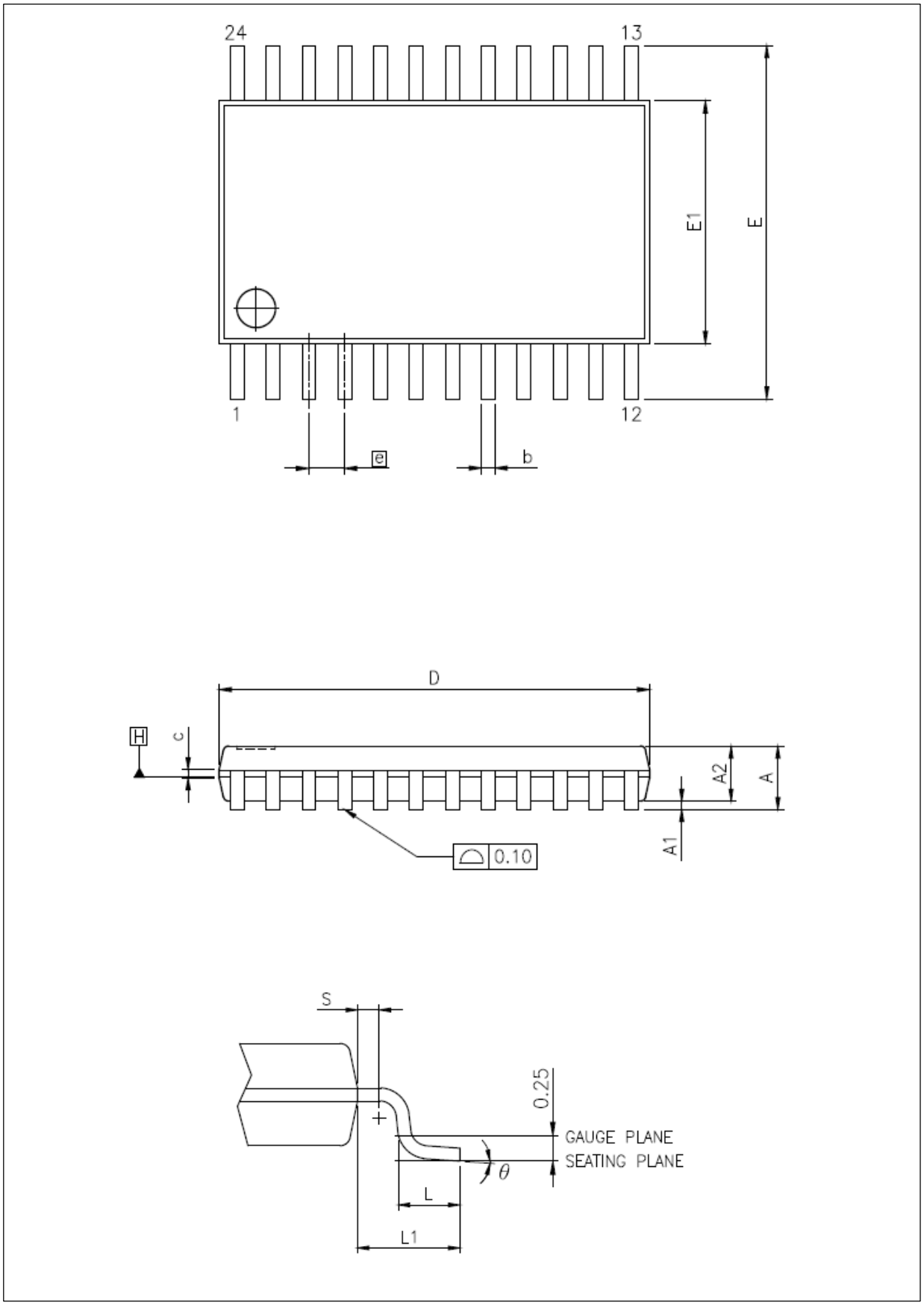


Table 54. TSSOP24 – 7.8 x 4.4 mm 24-pin thin-shrink small outline package mechanical data

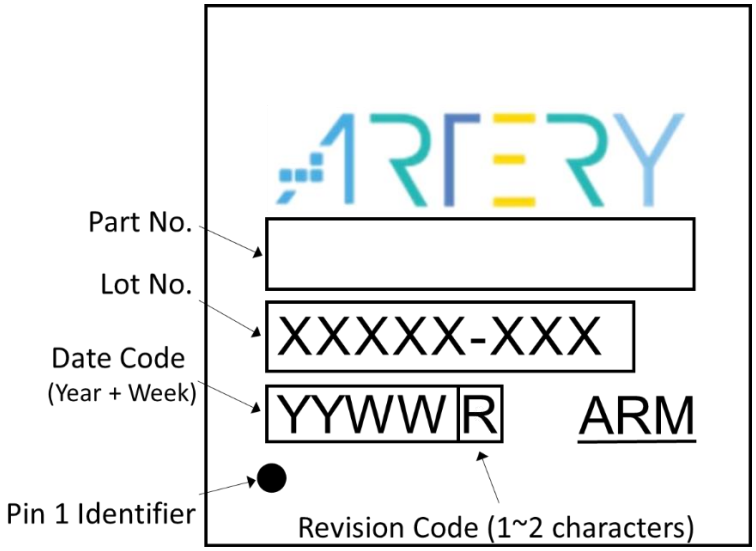
Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC.		
L1	1.00 REF.		
L	0.45	0.60	0.75
S	0.20	-	-
Θ	0°	-	8°

5.5 Device marking

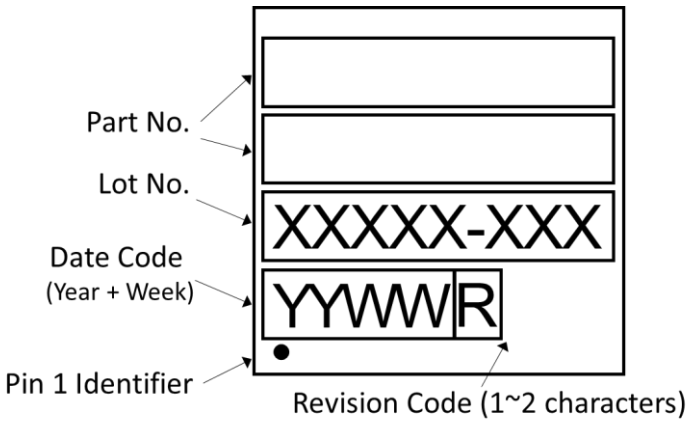
The AT32M412/416 series has three types of packaging labels depending on package types.

Figure 29. Marking example

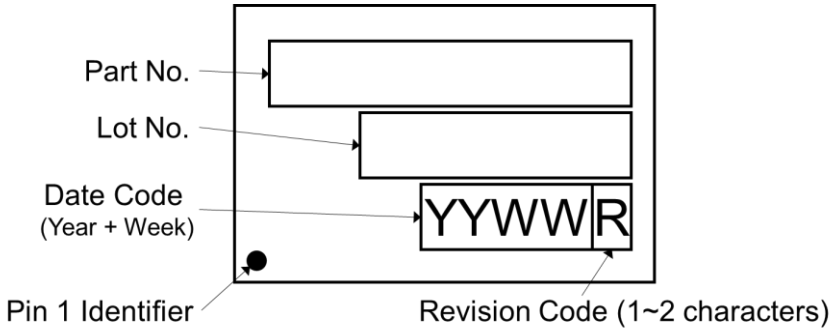
LQFP48, LQFP32



QFN32



TSSOP24



(1) Not to scale.

5.6 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6 mm thickness. They are guaranteed by design, not tested in production.

Table 55. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient – LQFP48 – 7 x 7 mm	87.4	°C/W
	Thermal resistance junction-ambient – LQFP32 – 7 x 7 mm	89.0	
	Thermal resistance junction-ambient – QFN32 – 4 x 4 mm	61.3	
	Thermal resistance junction-ambient – TSSOP24 – 7.8 x 4.4 mm	87.3	

6 Part numbering

Table 56. AT32M412/416 series part numbering

Example: AT32 M 4 1 2 C B T 7

Product family

AT32 = ARM®-based 32-bit microcontroller

Product type

M = Motor control

Core

4 = Cortex®-M4

Product series

1 = Value line

Product application

2 = CAN series

6 = CANFD series

Pin count

C = 48 pins

K = 32 pins

E = 24 pins

Internal Flash memory size

B = 128 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

Package type

T = LQFP

U = QFN

P = TSSOP

Temperature range

7 = -40 °C to +105 °C

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

7 Revision history

Table 57. Document revision history

Date	Version	Revision note
2024.8.8	2.00	Initial release

Appendix A

For the AT32M412/416 series, the interconnection between analog module and GPIO, and interconnection between analog peripherals are shown in *Figure 30* and *Figure 31*.

Figure 30. Interconnection between analog module and GPIOs

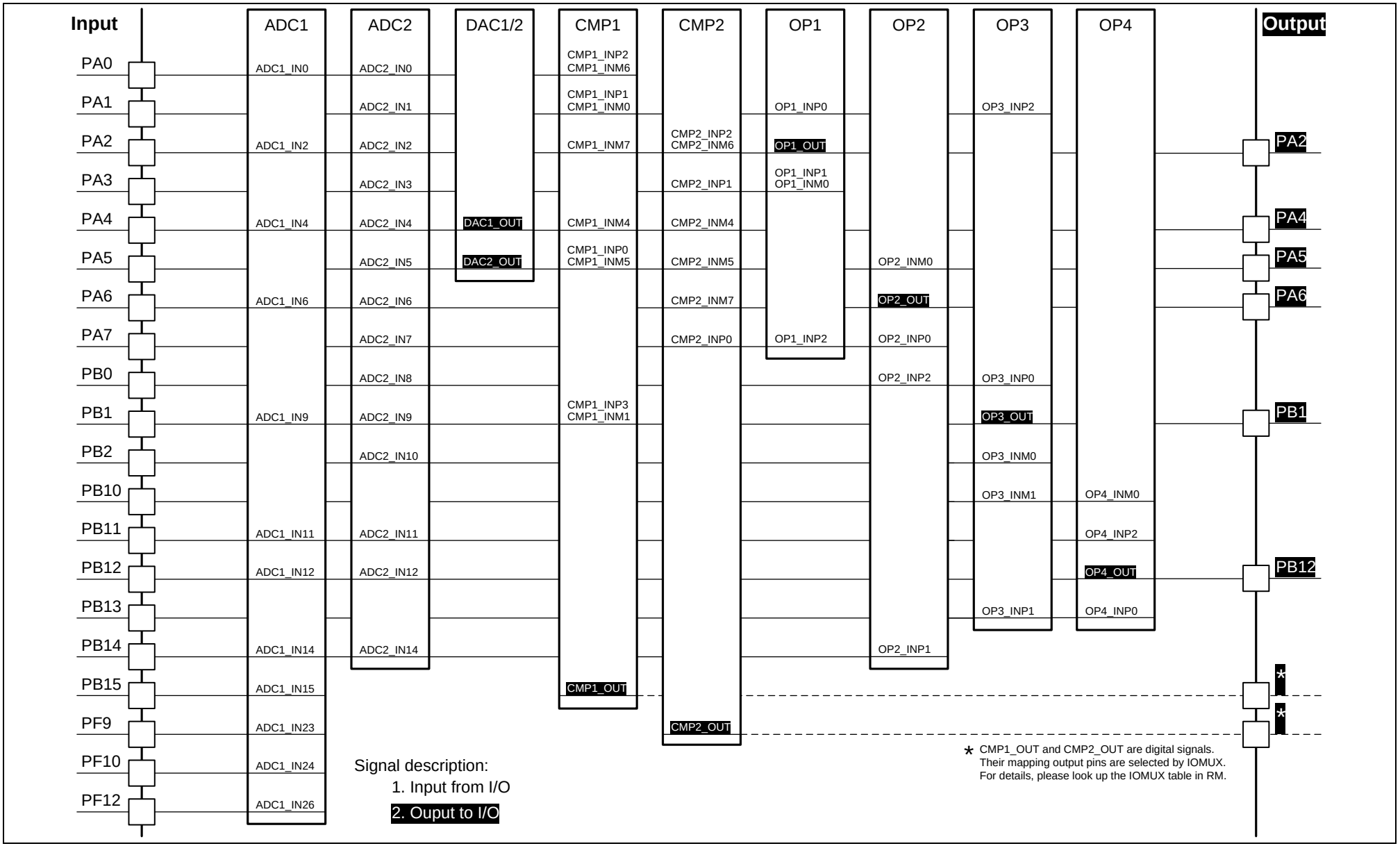
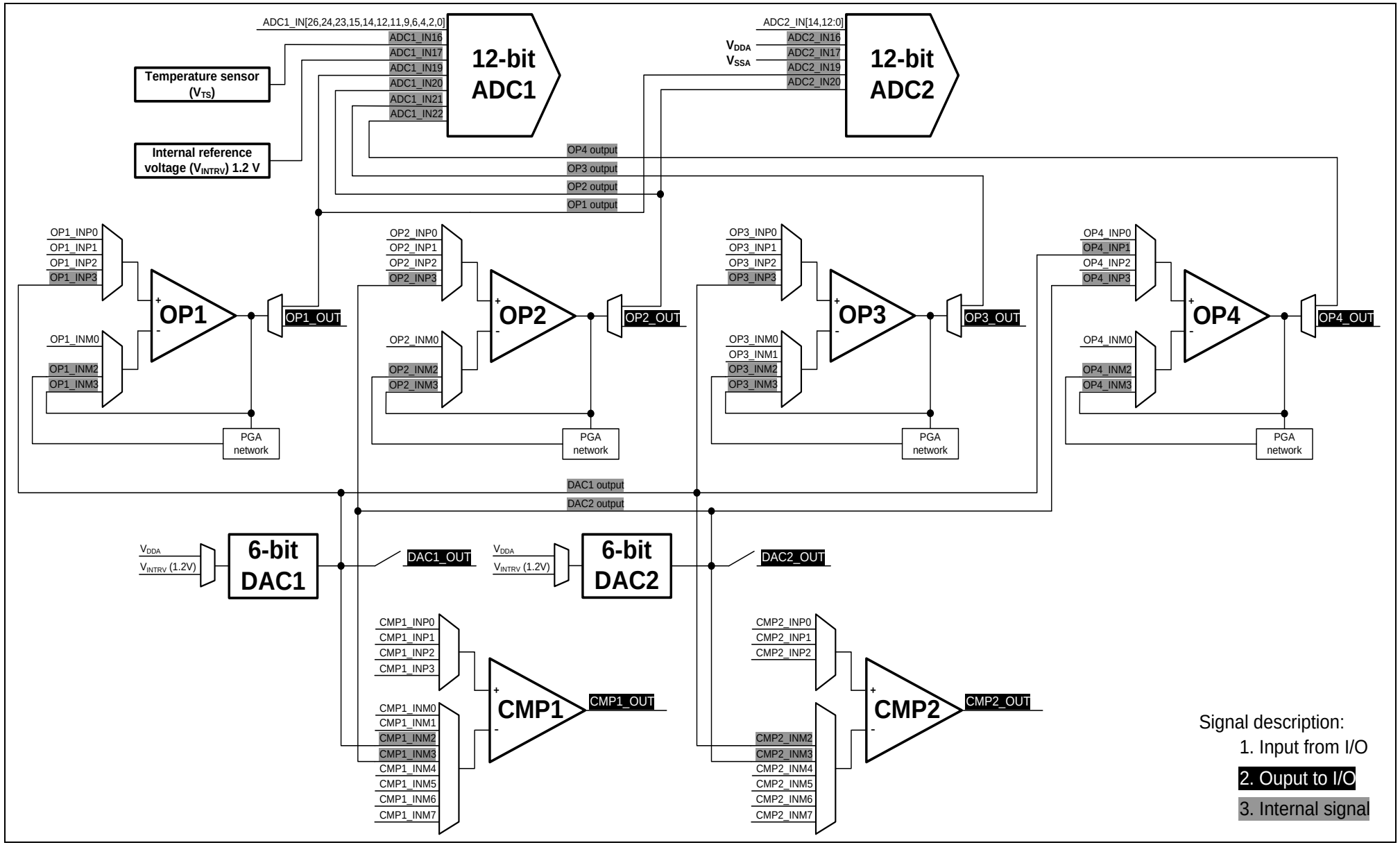


Figure 31. Interconnection between analog peripherals



IMPORTANT NOTICE – PLEASE READ CAREFULLY

Purchasers are solely responsible for the selection and use of ARTERY's products and services, and ARTERY assumes no liability whatsoever relating to the choice, selection or use of the ARTERY products and services described herein.

No license, express or implied, to any intellectual property rights is granted under this document. If any part of this document deals with any third party products or services, it shall not be deemed a license granted by ARTERY for the use of such third party products or services, or any intellectual property contained therein, or considered as a warranty regarding the use in any manner of such third party products or services or any intellectual property contained therein.

Unless otherwise specified in ARTERY's terms and conditions of sale, ARTERY provides no warranties, express or implied, regarding the use and/or sale of ARTERY products, including but not limited to any implied warranties of merchantability, fitness for a particular purpose (and their equivalents under the laws of any jurisdiction), or infringement on any patent, copyright or other intellectual property right.

Purchasers hereby agree that ARTERY's products are not designed or authorized for use in: (A) any application with special requirements of safety such as life support and active implantable device, or system with functional safety requirements; (B) any aircraft application; (C) any aerospace application or environment; (D) any weapon application, and/or (E) or other uses where the failure of the device or product could result in personal injury, death, property damage. Purchasers' unauthorized use of them in the aforementioned applications, even if with a written notice, is solely at purchasers' risk, and Purchasers are solely responsible for meeting all legal and regulatory requirements in such use.

Resale of ARTERY products with provisions different from the statements and/or technical characteristics stated in this document shall immediately void any warranty grant by ARTERY for ARTERY's products or services described herein and shall not create or expand any liability of ARTERY in any manner whatsoever.