ARM®-based 32-bit Cortex®-M4 MCU with 64 to 256 KB Flash, sLib, 11 timers, 1 ADC, 2 CMP, 12 communication interfaces (OTGFS, CAN)

Features

- **Core: ARM® 32-bit Cortex®-M4 CPU**
  - 150 MHz maximum frequency, with a memory protection unit (MPU)
  - Single-cycle multiplication and hardware division
  - DSP instructions
- **Memories**
  - 64 to 256 Kbytes of internal Flash memory
  - 18 Kbytes of boot code area used as a Bootloader
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - 32 Kbytes of SRAM
- **Power control (PWC)**
  - 2.6 to 3.6 V supply
  - Power on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep, and Standby modes
  - V_{BAT} for LEXT, ERTC and 20 x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal (HEXT)
  - 48 MHz internal factory-trimmed high speed clock (HICK), 1 % accuracy at T_A = 25 °C and 2 % accuracy at T_A = -40 to +105 °C
  - PLL flexible 31 to 500 multiplication and 1 to 15 division factor
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1 x 12-bit 2 MSPS A/D converter, up to 16 input channels
  - Temperature sensor (V_{TS}) and internal reference voltage (V_{INTRV})
  - 2 x comparators (CMP)
- **DMA: two 7-channel DMA controllers**
- **Up to 55 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 11 timers (TMR)**
  - 1 x 16-bit 7-channel advanced timer, 3 pairs of complementray channel PWM outputs with dead-time generator and emergency stop
  - Up to 5 x 16-bit and 2 x 32-bit timers, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarm, subsecond accuracy, and hardware calendar; supports calibration**
- **Up to 12 communication interfaces**
  - 2 x I^2C interfaces for SMBus/PMBus support
  - 5 x USARTs, support master synchronous SPI and modem control, with ISO7816 interface, LIN and IrDA
  - 2 x SPIs (36 Mbit/s), both with I^2S interface multiplexed
  - CAN interface (2.0B Active), with 256 bytes of dedicated buffers
  - OTGFS interface with on-chip PHY, with 1280 bytes of dedicated buffers
  - SDIO interface
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Debug modes**
  - Serial wire debug (SWD) and JTAG interfaces
- **Operating temperatures: -40 to +105 °C**

- **Packages**
  - LQFP64 10 x 10 mm
  - LQFP64 7 x 7 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm
  - QFN32 4 x 4 mm

Table 1. AT32F415 device summary

Flash	Part number
256 KBytes	AT32F415RCT7, AT32F415RCT7-7, AT32F415CCT7, AT32F415CCU7, AT32F415KCU7-4
128 KBytes	AT32F415RBT7, AT32F415RBT7-7, AT32F415CBT7, AT32F415CBU7, AT32F415KBU7-4
64 KBytes	AT32F415R8T7, AT32F415R8T7-7, AT32F415C8T7, AT32F415K8U7-4

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1 Descriptions

The AT32F415 series is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating a frequency of up to 150 MHz. The Cortex®-M4 core features a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F415 series incorporates high-speed embedded memories (up to 256 KBytes of internal Flash memory and 32 KBytes of SRAM), a wide range of enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib” (security library), a security area with code-executable only.

The AT32F415 series offers one 12-bit ADC, two analog comparators (CMP), five general-purpose 16-bit timers, two 32-bit general-purpose timers, one advanced timer, and one low-power ERTC. It supports standard and advanced communication interfaces: two I^2Cs, two SPIs (both multiplexed as I^2Ss), five USARTs, one SDIO, one OTGFS interface and one CAN.

The AT32F415 series operates in the -40 to +105 °C temperature range, with a power supply from 2.6 to 3.6 V. A comprehensive set of power-saving modes meet the requirements of low-power applications.

The AT32F415 series offers devices in various packages. They are fully pin-to-pin, software and functionality compatible with the entire AT32F415 series devices, except that the configurations of peripherals are not completely identical, depending on the packages types.

Table 2. AT32F415 features and peripheral counts

Part Number		AT32F415xxU7-4			AT32F415 xxU7		AT32F415xxT7			AT32F415xxT7-7			AT32F415xxT7		
		K8	KB	KC	CB	CC	C8	CB	CC	R8	RB	RC	R8	RB	RC
CPU frequency (MHz)		150													
Flash (KBytes)		64	128	256	128	256	64	128	256	64	128	256	64	128	256
SRAM (KBytes)		32													
Timers	Advanced	1			1		1			1			1		
	32-bit general-purpose	2			2		2			2			2		
	16-bit general-purpose	5			5		5			5			5		
	SysTick	1			1		1			1			1		
	WDT	1			1		1			1			1		
	WWDT	1			1		1			1			1		
	ERTC	1			1		1			1			1		
Communication	I^2C	2			2		2			2			2		
	SPI(1)	2			2		2			2			2		
	I^2S (half-duplex)(1)	2(2)			2(2)		2(2)			2			2		
	USART + UART	2(3) + 0			3 + 0		3 + 0			3 + 2			3 + 2		
	SDIO	1(4)			1(4)		1(4)			1			1		
	OTGFS	1			1		1			1			1		
	CAN	1			1		1			1			1		
Analog	12-bit ADC numbers/ channels	1													
		10			10		10			16			16		
	Comparator	2													
GPIO		27			39		39			55			55		
Operating temperatures		-40 to +105 °C													
Packages		QFN32 4 x 4 mm			QFN48 6 x 6 mm		LQFP48 7 x 7 mm			LQFP64 7 x 7 mm			LQFP64 10 x 10 mm		

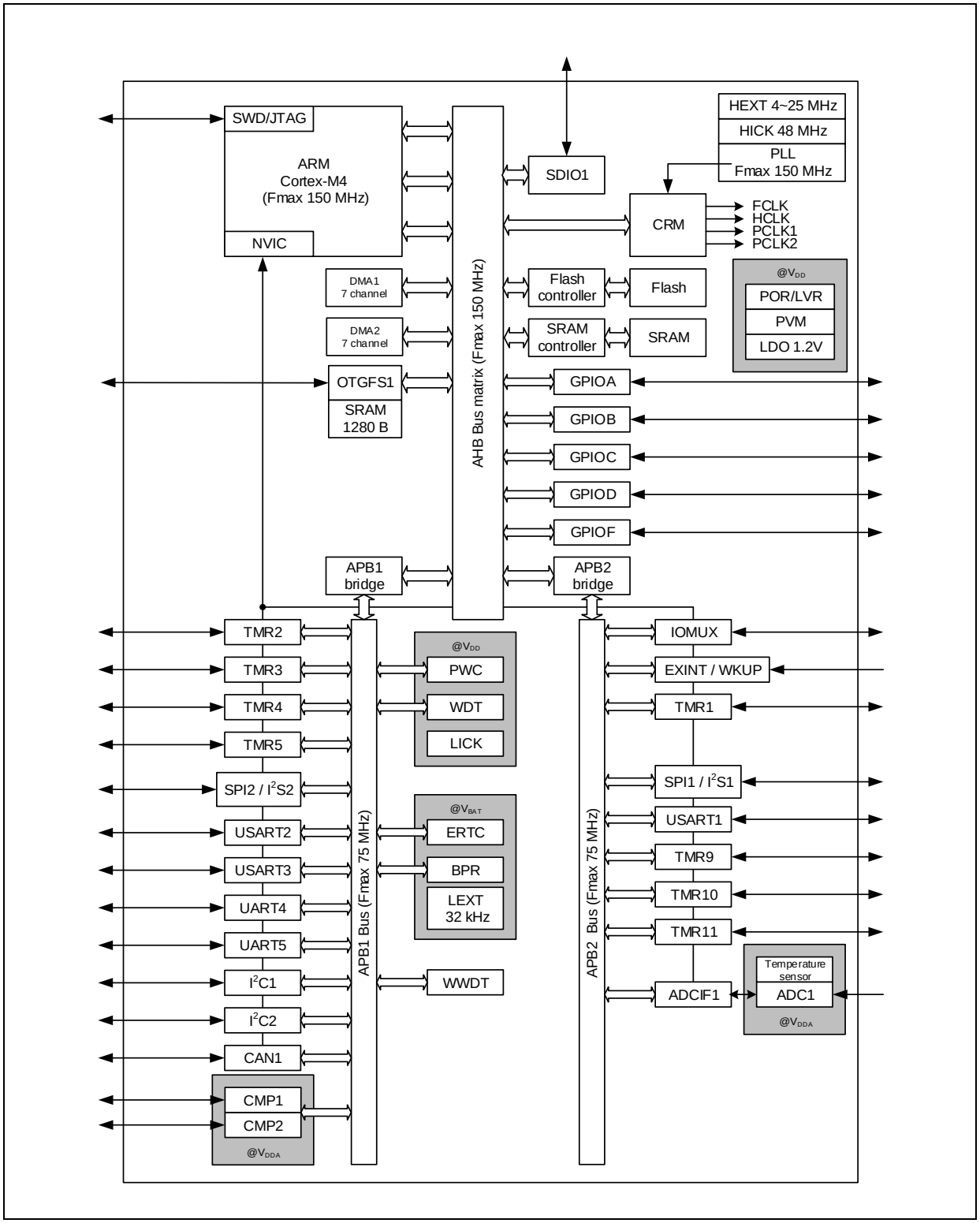
(1) Half-duplex I^2S shares the same pin with SPI.
(2) Only I^2S1 exists MCK pin on LQFP48, QFN48, and QFN32 packages.
(3) No USART3 is available on QFN32 packages.
(4) SDIO1 supports maximum 4-bit (D0~D3) mode on LQFP48, QFN48, and QFN32 packages.

2 Functional overview

2.1 ARM® Cortex®-M4

The ARM Cortex®-M4 processor is the latest generation of ARM processor for embedded systems. It is a 32-bit RISC high-performance processor that features exceptional code efficiency, outstanding computing power and advanced interrupt response mechanism. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution. *Figure 1* shows the general block diagram of the AT32F415.

Figure 1. AT32F415 block diagram



2.2 Memory

2.2.1 Internal Flash memory

Up to 256 KBytes of embedded Flash is available for storing programs and data. Any part of the embedded Flash memory can be protected by the sLib (security library), a security area that is code-executable only but non-readable. The “sLib” is a mechanism designed to protect the intelligence of solution vendors and facilitate the second-level development by customers.

There is another 18-KByte boot code area in which the bootloader is stored.

A User System Data block is included, which is used to configure the hardware behaviors such as read/erase/write protection and watchdog self-enable. User System Data allows to set erase/write and read protection individually.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the entire 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 Embedded SRAM

The device offers 32 KBytes of embedded SRAM (read/write) is accessible at CPU clock speed with 0 wait states.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F415 embeds a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 core. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 23 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.6～3.6 V: external power supply for GPIOs and the internal block such as the internal regulator (LDO), provided externally through V_{DD} pins.
- V_{DDA} = 2.6～3.6 V: external analog power supply for ADC and CMP. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8～3.6 V: power supply for V_{BAT} domain through the external battery or super capacitor, or or through V_{DD} when the external battery or super capacitor is not present. V_{BAT} (through power switch) supplies for ERTC, external crystal 32 kHz (LEXT), and battery powered registers (BPR) when V_{DD} is not present.

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR)/low voltage reset (LVR) circuitry. It is always active and allows proper operation starting from 2.6 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal mode, low-power mode, and power down mode.

- Normal mode: It is used in Run/Sleep mode and can be used in Deepsleep mode;
- Low-power mode: It can be used in Deepsleep mode;
- Power down mode: It is used in Standby mode. The regulator output (LDO) is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

This LDO operates always in its normal mode after reset.

2.4.4 Low-power modes

The AT32F415 supports three low-power modes:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep mode**

  Deepsleep mode achieves the lowest power consumption while holding the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The voltage regulator can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm, the OTGFS or the CMP wakeup.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire LDO power domain is powered off. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for ERTC registers, BPR domain registers and Standby circuitry.

  The device leaves Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUP pin, or an ERTC alarm occurs.

Note: ERTC, WDT, and the corresponding clock sources are not stopped while entering Deepsleep or Standby mode.

2.5 Boot modes

At startup, BOOT0 and BOOT1 are used to select one of three boot options:

- Boot from the internal Flash memory;
- Boot from boot code area;
- Boot from embedded SRAM.

The bootloader is stored in boot code area. It is used to reprogram the Flash memory through USART1, USART2, and OTGFS1. *Table 3* provides the pin configurations for Bootloader.

Table 3. Pin configurations for Bootloader

Interface	Pins
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX(1) PA3: USART2_RX(1)
OTGFS1	PA11: OTGFS1_D- PA12: OTGFS1_D+

(1) Note that pins used are not 5 V tolerant.

2.6 Clocks

On reset, the internal 48 MHz clock (HICK) divided by 6 (that is 8 MHz), is selected as the default CPU clock. The application can select an external 4 to 25 MHz clock (HEXT) as a system clock. This clock can be monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system take the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are available to allow the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 150 MHz. The maximum frequency of the APB domains is 75 MHz.

2.7 General-purpose input / output (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating with or without pull-up or pull-down), or as multiplexed functions. Most of the GPIO pins are shared with digital or analog multiple functions. All GPIOs are high current-capable.

The GPIO's configuration can be locked, if needed, in order to avoid false writing to the GPIO's registers by following a specific sequence.

2.8 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 5*, it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the AT32F415 reference manual for software considerations.

2.9 Direct Memory Access Controller (DMA)

AT32F415 features two general-purpose DMA ports (7 channels for DMA1 and 7 channels for DMA2). They are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. These DMA channels can be connected to peripherals for the purpose of flexible mapping.

The DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI and I^2S, I^2C, USART, advanced and general-purpose timers TMRx (except TMR9~11), SDIO, and ADC.

2.10 Timers (TMR)

The AT32F415 device includes an advanced timer, seven general-purpose timers and a SysTick timer.

The table below compares the features of the advanced and general-purpose timers.

Table 4. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR2 TMR5	16-bit or 32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3 TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR9	16-bit	Up	Any integer between 1 and 65536	No	2	No
	TMR10 TMR11	16-bit	Up	Any integer between 1 and 65536	No	1	No

2.10.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen a three-phase PWM generator multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time insertion. It can also be seen as a complete general-purpose timer. Their 4 independent channels can be used for:

- Input capture.
- Output compare.
- PWM generation (edge or center-aligned modes).
- One-cycle mode output.

If configured as a standard 16-bit timer, it has the same features as that of the TMRx timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMRs which have the same architecture. Thus the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

2.10.2 General-purpose timers (TMR2~5 and TMR9~11)

There are seven synchronizable general-purpose timers embedded in the AT32F415.

- **TMR2, TMR3, TMR4, and TMR5**

  The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload up/down counter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture/output compare, PWM or one-cycle mode outputs.

  These general-purpose timers can work with the advanced timers via the timer link feature for synchronization or event chaining. In debug mode, their counters can be frozen. Any of these general-purpose timers can be used for the generation of PWM output. Each timer has its individual DMA request mechanism.

  They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

- **TMR9**

  TMR9 is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-cycle mode output. It can be synchronized with the full-featured general-purpose timers. It can also be used as simple time bases. The counter can be frozen in debug mode.

- **TMR10 and TMR11**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channel for input capture/output compare, PWM, or one-cycle mode output. They can be synchronized with the full-featured general-purpose timers. They can also be used as simple time bases. The counter can be frozen in debug mode.

2.10.3 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. Its features include:

- A 24-bit down counter.
- Auto-reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source (HICK or HICK/8)

2.11 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabled through User System Data. The counter can be frozen in debug mode.

2.12 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.13 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC).
- Twenty 32-bit battery powered registers.

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Sub-second value in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms and one periodic wakeup capability from Deepsleep or Standby mode.
- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output.

The alarm registers are used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

A prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 80 bytes of user application data. Battery powered registers are not reset by a system, or when the device wakes up from the Standby mode.

ERTC and BPR are powered through a power switch. When V_{DD} exists, the switch selects V_{DD} as power supply, or V_{BAT} is used as supply source.

2.14 Communication interfaces

2.14.1 Serial peripheral interface (SPI)

There are up to two SPI interfaces able to communicate at up to 36 Mbits/s in slave and master modes in half-duplex and full-duplex mode. The prescaler generates multiple master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card/MMC/SDHC modes. Both SPIs can be served by the DMA controller.

2.14.2 Inter-integrated sound interface (I^2S)

Two standard I^2S interfaces (multiplexed with SPI) are available which can be operated in master or slave mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies ranges from 8 kHz up to 192 kHz. When I^2S configured in master mode, the master clock can be output at 256 times the sampling frequency. Both I^2Ss can be served by the DMA controller.

2.14.3 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32F415 series embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2, and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. USART1, USART2, and USART3 also offer hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

All interfaces are able to communicate at a speed of up to 4.6875 Mbit/s.

2.14.4 Inter-integrated-circuit interface (I^2C)

Two I^2C bus interfaces can operate in multi-master and slave modes. They can support standard mode (max. 100 kHz) and fast mode (max. 400 kHz). The I^2C bus frequency can be increased up to 1 MHz. For more details, please contact your local Artery sales office for technical support.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included. They can be served by DMA and they support SMBus 2.0/PMBus.

2.14.5 Secure digital input/output interface (SDIO)

One SD/SDIO/MMC host interface is available to support MultiMediaCard System Specification Version 4.2 in three different data bus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The two different data bus modes supported in the SDIO Card Specification Version 2.0 are: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.14.6 Controller area network (CAN)

The controller area network (CAN) is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive buffers with 3 stages, and 14 scalable filter banks. It also has a dedicated 256 Bytes buffer, which is not shared with any other peripheral.

To guarantee CAN transmission quality, the CAN 2.0 protocol states that its clock souce must come from the HEXT-based PLL clock.

2.14.7 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32F415 series embeds an OTG full-speed device (12 Mbit/s) with integrated transceivers (PHY). It has software-configurable endpoint setting and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock that is generated by the HEXT-based PLL.

OTGFS has the major features such as:

- Dedicated 1280 KBytes buffer (not shared with any other peripheral).
- 4 bi-directional endpoints support number 0 through 3; Starting from Silicon reversion code C, the firmware supports endpoint 3 to be configured as endpoint 4.
- 8 channels (host mode).
- SOF output.
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - In Host mode: full-speed and low speed.
  - In Device mode: full-speed.

2.15 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.16 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converters (ADC) is embedded into AT32F415 device. It supports conversions in single mode or sequential mode. This ADC also shares up to 16 external channels and two internal channels, the latter (internal channels) connected to the temperature sensor (V_{TS}) and the internal reference voltage (V_{INTRV}), respectively. In sequence mode, automatic conversion is performed on a selected group of analog channels.

This ADC can be served by the DMA controller.

A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is above the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and advanced timer (TMR1) can be connected to the regular conversion and preempted conversion of ADC, respectively. ADC conversion can be synchronized with clocks through the application program.

2.16.1 Temperature sensor (V_{TS})

The temperature sensor has to generate a voltage VTS that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.16.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage output for the ADC. V_{INTRV} is internally connected to the ADC1_IN17 channel.

2.17 Comparator (CMP)

The AT32F415 series embeds two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis, speed, selectable output polarity.

The reference voltage can be one of the following:

- External I/O;
- Internal reference voltage (V_{INTRV}) or its submultiple (1/4, 1/2, 3/4).

These two comparators can wake up the device from Deepsleep mode, redirect output remapping to timers and can be combined as a window comparator.

2.18 Debug: serial wire debugger (SWD) / JTAG interfaces

The ARM®SWD/JTAG interface is embedded, consisting of a serial wire debug interface and JTAG port. It enables a serial wire debugger or a JTAG probe to be connected to the target for programming and debugging. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK.

3 Pin functional definitions

Figure 2. AT32F415 LQFP64 pinout

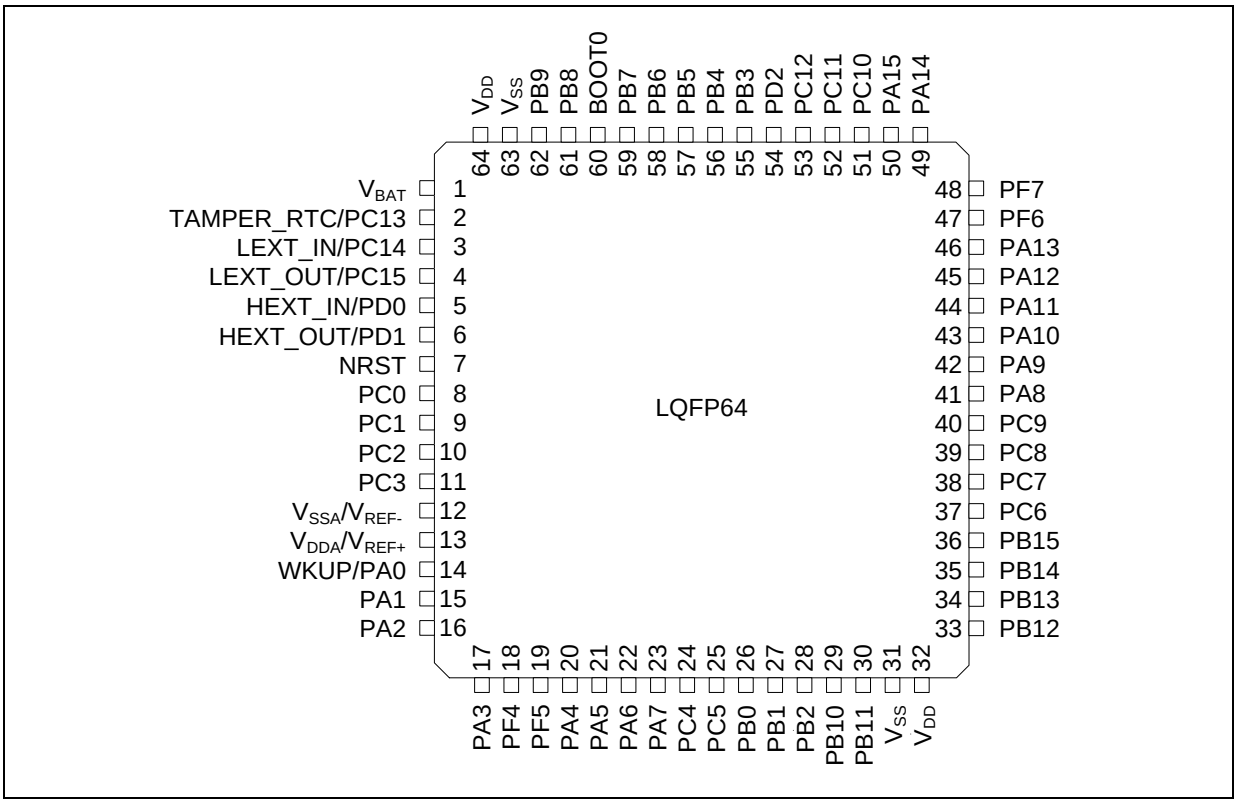


Figure 3. AT32F415 LQFP48 pinout

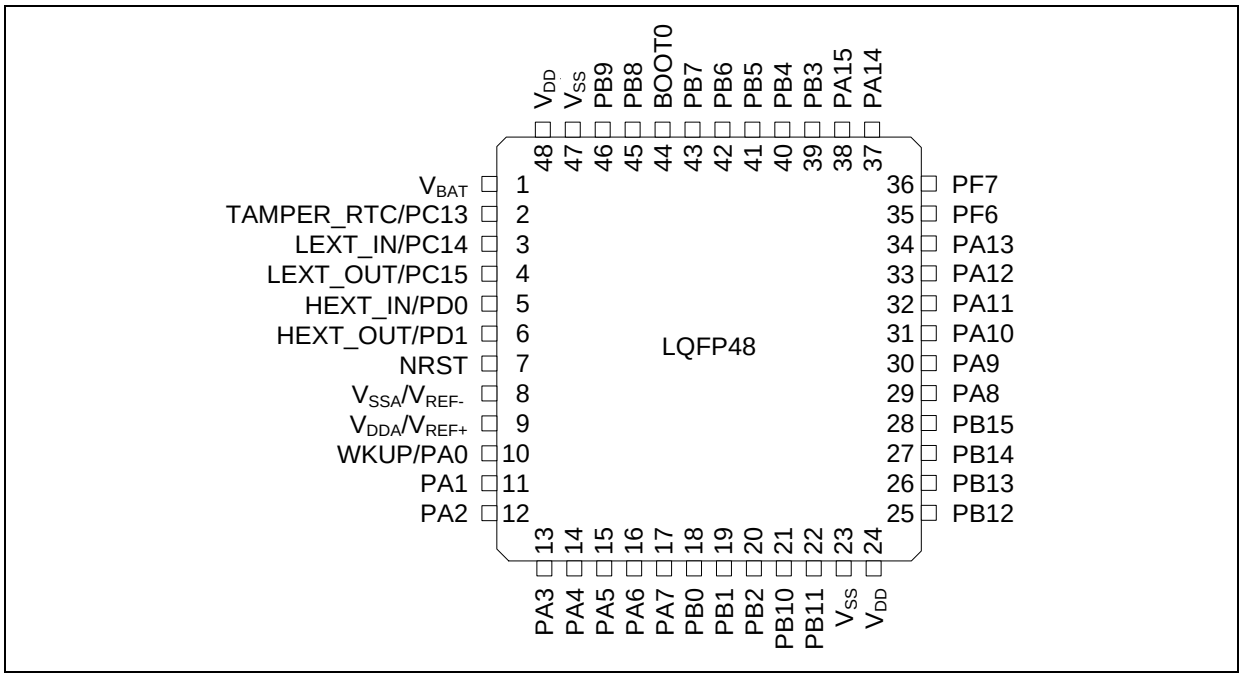


Figure 4. AT32F415 QFN48 pinout

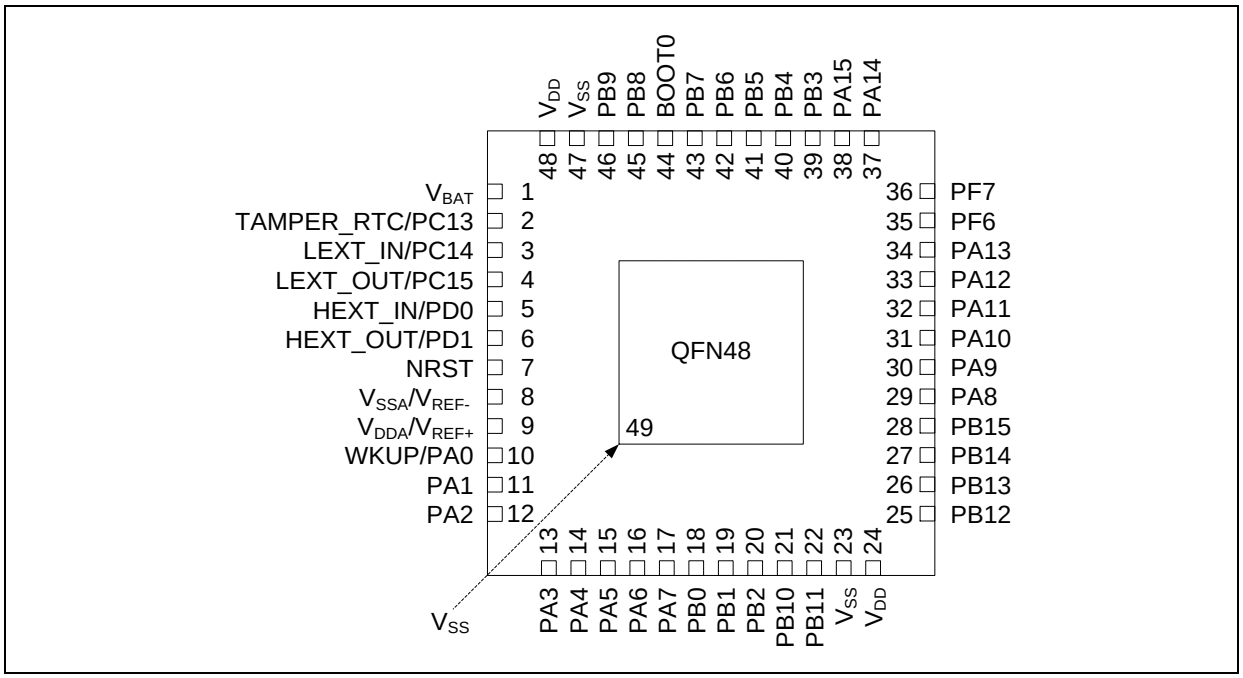
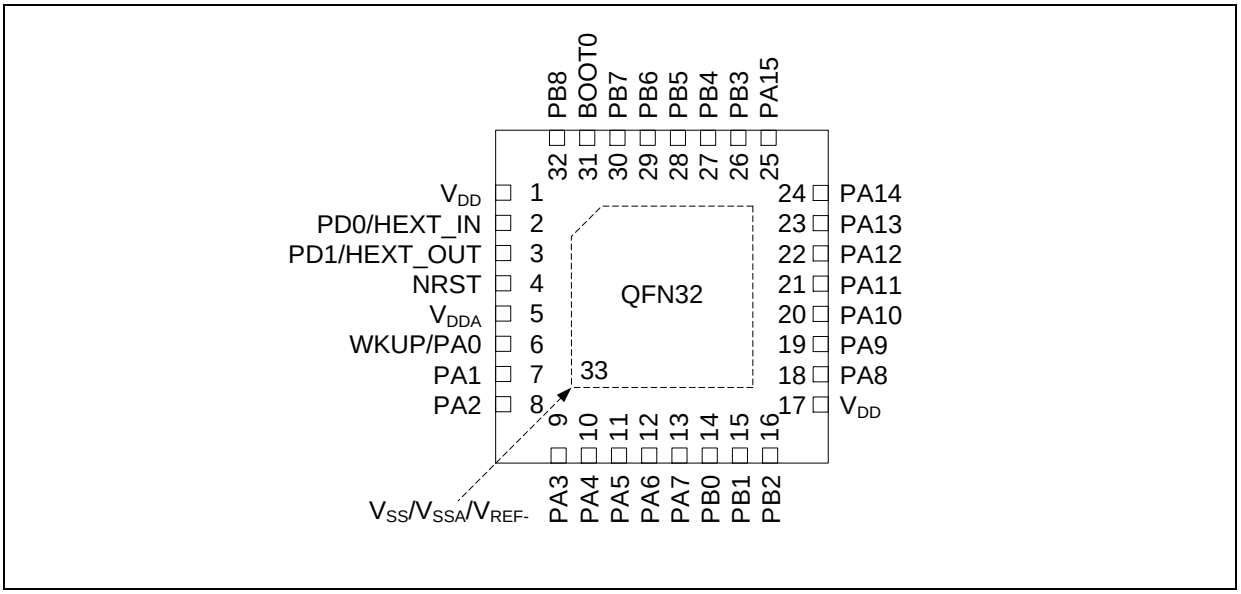


Figure 5. AT32F415 QFN32 pinout



The table below is the pin definition of the AT32F415. ”-” represents that there is no such pinout on the related package. The multi-functions list follows priority from high to low. In principle, the analog signals have priority over the digital signals, and the digital output signals have priority over the digital input signals.

Table 5. AT32F415 series pin definitions

Pin number			Pin name	Type(1)	IO level(2)	Main function	Alternate functions(3)	
QFN32	LQFP48/ QFN48	LQFP64					Default	Remap
-	1	1	V_{BAT}	S	-	V_{BAT}	-	-
-	2	2	PC13(4)	I/O	-	PC13	TAMPER-RTC(5)	-
-	3	3	PC14(4)	I/O	-	PC14	LEXT_IN(5)	-
-	4	4	PC15(4)	I/O	-	PC15	LEXT_OUT(5)	-
2	5	5	PD0(6)	I/O	-	HEXT_IN	HEXT_IN	PD0
3	6	6	PD1(6)	I/O	-	HEXT_OUT	HEXT_OUT	PD1
4	7	7	NRST	I/O	-	NRST	-	-
-	-	8	PC0	I/O	-	PC0	ADC1_IN10	SDIO1_D0
-	-	9	PC1	I/O	-	PC1	ADC1_IN11	SDIO1_D1
-	-	10	PC2	I/O	-	PC2	ADC1_IN12	SDIO1_D2
-	-	11	PC3	I/O	-	PC3	ADC1_IN13	SDIO1_D3
-	8	12	V_{SSA}	S	-	V_{SSA}	-	-
5	9	13	V_{DDA}	S	-	V_{DDA}	-	-
6	10	14	PA0-WKUP	I/O	-	PA0	ADC1_IN0 / WKUP / CMP1_OUT(7) / CMP1_INP2 / CMP1_INM6 / USART2_CTS / TMR2_CH1(7) / TMR2_EXT(7) / TMR5_CH1(7)	TMR1_EXT
7	11	15	PA1	I/O	-	PA1	ADC1_IN1 / CMP1_INP1 / USART2_RTS / TMR2_CH2(7) / TMR5_CH2(7)	-
8	12	16	PA2	I/O	-	PA2	ADC1_IN2 / CMP2_OUT(7) / CMP2_INP2 / CMP2_INM6 / USART2_TX / TMR2_CH3(7) / TMR5_CH3 / TMR9_CH1(7)	SDIO1_CK
9	13	17	PA3	I/O	-	PA3	ADC1_IN3 / CMP2_INP1 / USART2_RX / TMR2_CH4(7) / TMR5_CH4 / TMR9_CH2(7)	SDIO1_CMD
-	-	18	PF4	I/O	FT	PF4	-	UART4_TX / TMR5_CH1
-	-	19	PF5	I/O	FT	PF5	-	UART4_RX / TMR5_CH2
10	14	20	PA4	I/O	-	PA4	ADC1_IN4 / CMP1_INM4 / CMP2_INM4 / USART2_CK / SPI1_CS(7) / I2S1_WS(7)	SDIO1_D4 / SDIO1_D0
11	15	21	PA5	I/O	-	PA5	ADC1_IN5 / CMP1_INP0 / CMP1_INM5 / CMP2_INM5 / SPI1_SCK(7) / I2S1_CK(7)	USART3_CK / SDIO1_D5 / SDIO1_D1
12	16	22	PA6	I/O	-	PA6	ADC1_IN6 / SPI1_MISO(7) / TMR3_CH1(7)	CMP1_OUT / USART3_RX / SDIO1_D6 / SDIO1_D2 / TMR1_BRK / TMR10_CH1

Pin number			Pin name	Type(1)	IO level(2)	Main function	Alternate functions(3)	
QFN32	LQFP48/ QFN48	LQFP64					Default	Remap
13	17	23	PA7	I/O	-	PA7	ADC1_IN7 / CMP2_INP0 / SPI1_MOSI(7) / I2S1_SD(7) / TMR3_CH2(7)	CMP2_OUT / USART3_TX / SDIO1_D7 / SDIO1_D3 / TMR1_CH1C / TMR11_CH1
-	-	24	PC4	I/O	-	PC4	ADC1_IN14	SDIO1_CK
-	-	25	PC5	I/O	-	PC5	ADC1_IN15	SDIO1_CMD
14	18	26	PB0	I/O	-	PB0	ADC1_IN8 / I2S1_MCK(7) / TMR3_CH3(7)	USART3_RTS / TMR1_CH2C
15	19	27	PB1	I/O	-	PB1	ADC1_IN9 / TMR3_CH4(7)	USART3_CTS / TMR1_CH3C
16	20	28	PB2	I/O	FT	PB2/ BOOT1(8)	-	-
-	21	29	PB10	I/O	FT	PB10	I2C2_SCL(7) / USART3_TX(7)	TMR2_CH3
-	22	30	PB11	I/O	FT	PB11	I2C2_SDA(7) / USART3_RX(7)	TMR2_CH4
-	23	31	V_{SS}	S	-	V_{SS}	-	-
17	24	32	V_{DD}	S	-	V_{DD}	-	-
-	25	33	PB12	I/O	FT	PB12	USART3_CK(7) / I2C2_SMBA(7) / SPI2_CS(7) / I2S2_WS(7) / TMR1_BRK(7)	-
-	26	34	PB13	I/O	FT	PB13	TMR1_CH1C(7) / USART3_CTS(7) / SPI2_SCK(7) / I2S2_CK(7)	-
-	27	35	PB14	I/O	FT	PB14	TMR1_CH2C(7) / USART3_RTS(7) / SPI2_MISO(7)	TMR9_CH1
-	28	36	PB15	I/O	FT	PB15	TMR1_CH3C(7) / ERTC_REFIN SPI2_MOSI(7) / I2S2_SD(7)	TMR9_CH2
-	-	37	PC6	I/O	FT	PC6	I2S2_MCK(7) / SDIO1_D6(7)	TMR1_CH1 / TMR3_CH1
-	-	38	PC7	I/O	FT	PC7	SDIO1_D7(7)	I2S2_MCK / TMR1_CH2 / TMR3_CH2
-	-	39	PC8	I/O	FT	PC8	SDIO1_D0(7)	TMR1_CH3 / TMR3_CH3
-	-	40	PC9	I/O	FT	PC9	SDIO1_D1(7)	I2C2_SDA / TMR1_CH4 / TMR3_CH4
18	29	41	PA8	I/O	FT	PA8	OTGFS1_SOF / CLKOUT / USART1_CK / TMR1_CH1	I2C2_SCL
19	30	42	PA9	I/O	FT	PA9	OTGFS1_VBUS(9) / USART1_TX(7) / TMR1_CH2	I2C2_SMBA
20	31	43	PA10	I/O	-	PA10	OTGFS1_ID / USART1_RX(7) / TMR1_CH3	-
21	32	44	PA11	I/O	-	PA11	OTGFS1_D- / USART1_CTS / CAN1_RX(7) / TMR1_CH4	CMP1_OUT
22	33	45	PA12	I/O	-	PA12	OTGFS1_D+ / USART1_RTS / CAN1_TX(7) / TMR1_EXT	CMP2_OUT
23	34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	35	47	PF6	I/O	FT	PF6	-	I2C1_SCL / I2C2_SCL
-	36	48	PF7	I/O	FT	PF7	-	I2C1_SDA / I2C2_SDA
24	37	49	PA14	I/O	FT	JTCK-SWCLK	-	PA14

Pin number			Pin name	Type(1)	IO level(2)	Main function	Alternate functions(3)	
QFN32	LQFP48/ QFN48	LQFP64					Default	Remap
25	38	50	PA15	I/O	FT	JTDI	-	PA15 / SPI1_CS / I2S1_WS / SPI2_CS / I2S2_WS / TMR2_CH1 / TMR2_EXT
-	-	51	PC10	I/O	FT	PC10	UART4_TX(7) / SDIO1_D2(7)	USART3_TX
-	-	52	PC11	I/O	FT	PC11	UART4_RX(7) / SDIO1_D3(7)	USART3_RX
-	-	53	PC12	I/O	FT	PC12	UART5_TX / SDIO1_CK(7)	USART3_CK
-	-	54	PD2	I/O	FT	PD2	UART5_RX / SDIO1_CMD(7) / TMR3_EXT	-
26	39	55	PB3	I/O	FT	JTDO	-	PB3 / SWO / SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / TMR2_CH2
27	40	56	PB4	I/O	FT	NJTRST	-	PB4 / SPI1_MISO / SPI2_MISO / I2C2_SDA / TMR3_CH1
28	41	57	PB5	I/O	FT	PB5	I2C1_SMBA	SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / TMR3_CH2
29	42	58	PB6	I/O	FT	PB6	I2C1_SCL(7) / TMR4_CH1	USART1_TX / I2S1_MCK
30	43	59	PB7	I/O	FT	PB7	I2C1_SDA(7) / TMR4_CH2	USART1_RX
31	44	60	BOOT0	I	-	BOOT0	-	-
32	45	61	PB8	I/O	FT	PB8	SDIO1_D4(7) / TMR4_CH3 / TMR10_CH1(7)	I2C1_SCL / CAN1_RX
-	46	62	PB9	I/O	FT	PB9	SDIO1_D5(7) / TMR4_CH4 / TMR11_CH1(7)	I2C1_SDA / CAN1_TX
-	47	63	V_{SS}	S	-	V_{SS}	-	-
1	48	64	V_{DD}	S	-	V_{DD}	-	-
-	-/49	-	V_{SS}	S	-	V_{SS}	-	-
33	-	-	V_{SS}/V_{SSA}	S	-	V_{SS}/V_{SSA}	-	-

(1) I = input, O = output, S = supply.

(2) FT = 5 V-tolerant GPIO.

(3) If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding CRM peripheral clock enable register). Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only two USARTs, they will be called USART1 and USART2. Refer to *Table 2*.

(4) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only sources a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited not to be used as a current source (e.g. to drive an LED).

(5) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset).

(6) The pins number 5 and 6 of the LQFP64, LQFP48, and QFN48 packages and the pins number 2 and 3 of the QFN32 packages are configured as HEXT_IN/HEXT_OUT after reset, the functionality of PD0 and PD1 can be remapped by software on these pins.

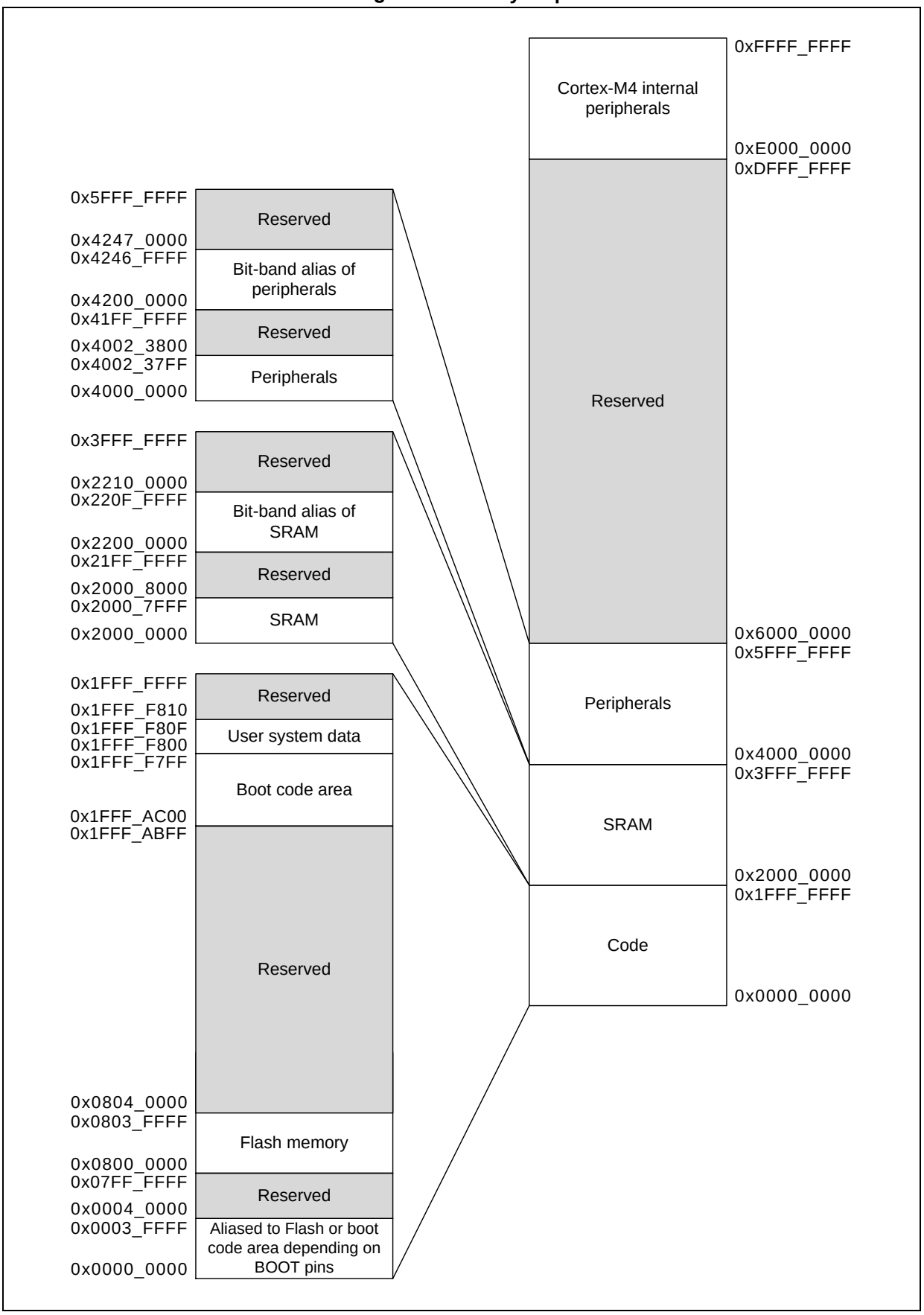
(7) This alternate function can be remapped by software to some other port pins (if available on the used package).

(8) If booting from user Flash is selected and PB2 is not used, PB2 is suggested to be externally pulled down.

(9) When OTGFS1 is used and configured as device mode, PA9 should keep high level. Its GPIO and other alternative functions could not be used. Starting from Silicon reversion code C, there is no such limitation as above.

4 Memory mapping

Figure 6. Memory map



5 Electrical characteristics

5.1 Parameter conditions

5.1.1 Minimum and maximum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

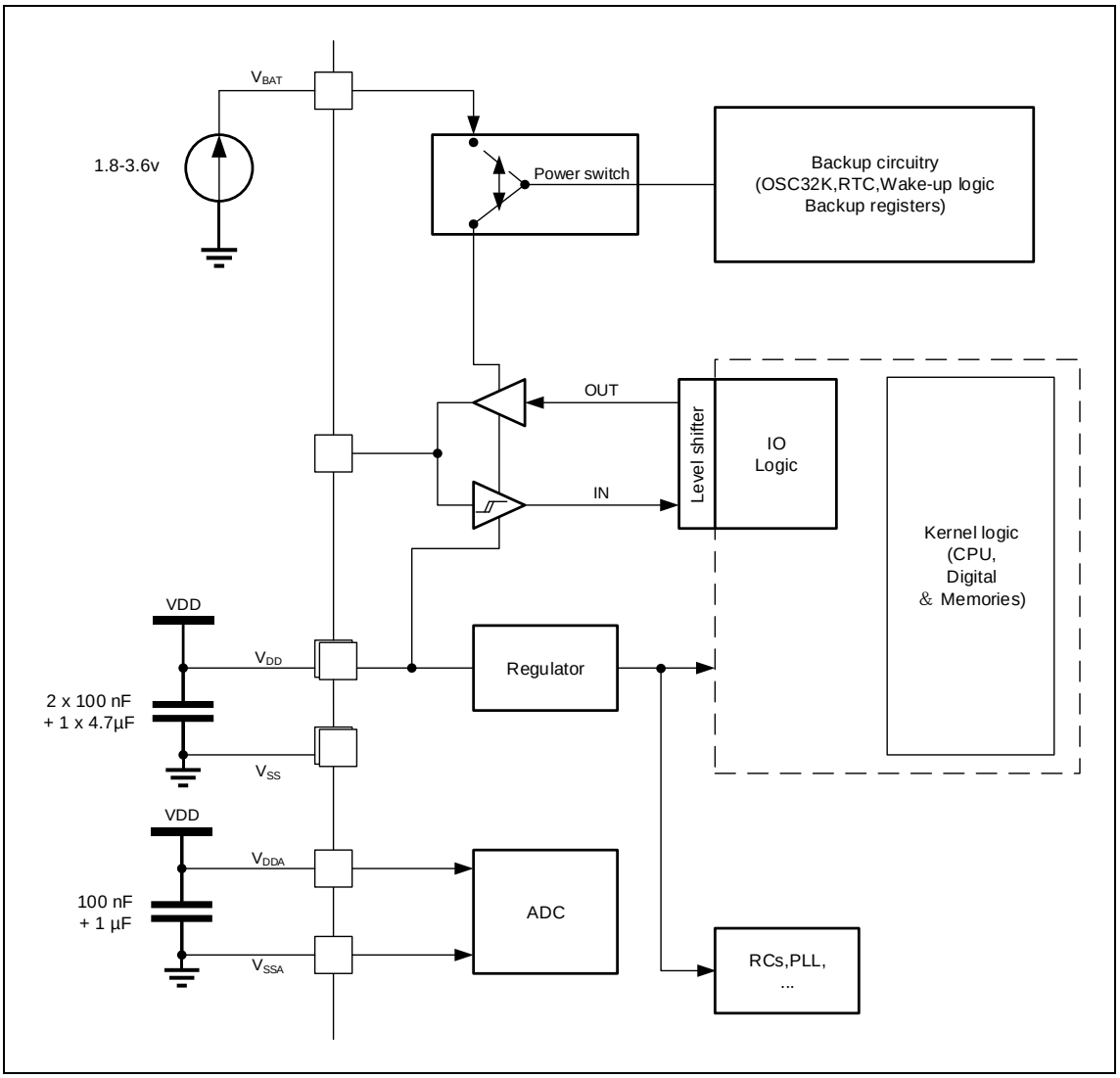
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

5.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

5.1.4 Power supply scheme

Figure 7. Power supply scheme



5.2 Absolute maximum values

5.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 6*, *Table 7*, and *Table 8,* it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 6. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	4.0	V
V_{IN}	Input voltage on FT GPIO	V_{SS}-0.3	6.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 7. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIOs and control pin	-25	

Table 8. Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

5.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2017/JS-002-2018 standard.

Table 9. ESD values

Symbol	Parameter	Conditions	Class	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2018	III	±1000	

Static latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 10. Latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (±200 mA)

5.3 Specifications

5.3.1 General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	150	MHz
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-	0	75	MHz
V_{DD}	Digital operating voltage	-	2.6	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}	V_{DD}		V
V_{BAT}	Battery powered domain voltage	-	1.8	3.6	
P_D	Power dissipation: T_A = 105 °C	LQFP64 (10 x 10 mm)	-	266	mW
		LQFP64 (7 x 7 mm)	-	249	
		LQFP48 (7 x 7 mm)	-	260	
		QFN48 (6 x 6 mm)	-	515	
		QFN32 (4 x 4 mm)		335	
T_A	Ambient temperature	-	-40	105	°C

5.3.2 Operating conditions at power-up / power-down

Table 12. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞(1)	ms/V
	V_{DD} fall time rate		20	∞	μs/V

(1) If V_{DD} rising time rate is slower than 6 ms/V, the code could access the backup registers only after V_{DD} higher than V_{POR} + 0.1V.

5.3.3 Embedded reset and power control block characteristics

Table 13. Embedded reset and power management block characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}(	Power on reset threshold	2.05	2.3	2.5	V
V_{LVR}	Low voltage reset threshold	1.85(2)	2.15	2.35	V
$V_{LVRhyst}$	LVR hysteresis	-	180	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	600	-	μs

(1) Guaranteed by design, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 8. Power on reset and low voltage reset waveform

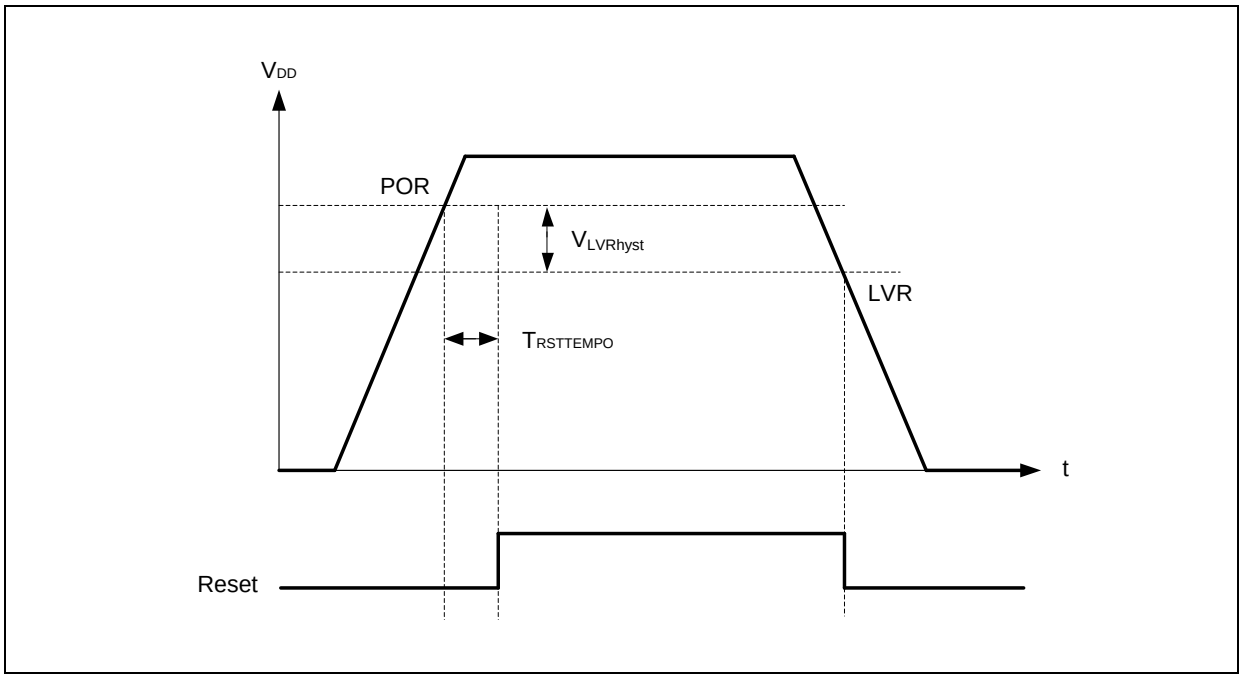


Table 14. Programmable voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge(1)	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL [2:0] = 010)	Rising edge(1)	2.28	2.38	2.48	V
		Falling edge(1)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL [2:0] = 011)	Rising edge(2)	2.38	2.48	2.58	V
		Falling edge(2)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL [2:0] = 100)	Rising edge(2)	2.47	2.58	2.69	V
		Falling edge(2)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL [2:0] = 101)	Rising edge(2)	2.57	2.68	2.79	V
		Falling edge(2)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL [2:0] = 110)	Rising edge(2)	2.66	2.78	2.9	V
		Falling edge(2)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL [2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(2)	PVM hysteresis	-	-	100	-	mV

(1) PVMSEL [2:0] = 001, 010 level may not be used because it is lower than V_{POR}.
(2) Guaranteed by characterization results, not tested in production.

5.3.4 Memory characteristics

Table 15. Internal Flash memory characteristics(1)

Symbol	Parameter	Typ	Max	Unit
T_{PROG}	Programming time	40	42	μs
t_{SE}	Sector erase time	6.6	8	ms
t_{ME}	Mass erase time	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 16. Internal Flash memory endurance and data retention(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 32 MHz, 1 wait state from 33 to 64 MHz, 2 wait stateS from 65 to 96 MHz, 3 wait stateS from 97 to 128 MHz, and 4 wait states for beyond 128 MHz).
- Prefetch ON.
- When the peripherals are enabled:
  - If $f_{HCLK} > 75$ MHz, $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$
  - If $f_{HCLK} \leq 75$ MHz, $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

Table 17. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1)(2)	150 MHz	43.5	20.1	mA
			120 MHz	36.2	17.6	
			108 MHz	32.1	15.3	
			72 MHz	24.6	11.4	
			48 MHz	17.6	8.8	
			36 MHz	13.1	6.54	
			24 MHz	9.62	5.24	
			16 MHz	6.98	4.06	
			8 MHz	4.13	2.79	
			4 MHz	2.98	2.32	
			2 MHz	2.41	2.09	
			1 MHz	2.13	1.97	
			500 kHz	1.99	1.91	
			125 kHz	1.88	1.87	
		High speed internal clock (HICK)(2)	150 MHz	43.5	20.0	mA
			120 MHz	35.5	16.7	
			108 MHz	32.1	15.2	
			72 MHz	24.0	10.8	
			48 MHz	16.9	8.06	
			36 MHz	13.0	6.44	
			24 MHz	9.52	5.13	
			16 MHz	6.88	3.96	
			8 MHz	3.84	2.49	
			4 MHz	2.68	2.02	
			2 MHz	2.11	1.79	
			1 MHz	1.83	1.67	
			500 kHz	1.69	1.61	
			125 kHz	1.59	1.57	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1)(2)	150 MHz	34.3	5.99	mA
			120 MHz	28.2	5.52	
			108 MHz	25.6	5.21	
			72 MHz	19.7	4.18	
			48 MHz	14.0	3.67	
			36 MHz	11.0	3.18	
			24 MHz	8.18	3.00	
			16 MHz	6.03	2.66	
			8 MHz	3.48	1.87	
			4 MHz	2.57	1.78	
			2 MHz	2.12	1.74	
			1 MHz	1.90	1.71	
			500 kHz	1.79	1.78	
			125 kHz	1.71	1.69	
		High speed internal clock (HICK)(2)	150 MHz	34.3	5.94	mA
			120 MHz	28.2	5.42	
			108 MHz	25.5	5.03	
			72 MHz	19.7	4.07	
			48 MHz	14.0	3.56	
			36 MHz	10.9	3.08	
			24 MHz	8.08	2.90	
			16 MHz	5.93	2.47	
			8 MHz	3.38	1.84	
			4 MHz	2.47	1.67	
			2 MHz	2.02	1.71	
			1 MHz	1.80	1.60	
			500 kHz	1.69	1.59	
			125 kHz	1.61	1.58	

(1) External clock is 8 MHz.
(2) PLL is on when f_{HCLK} > 8 MHz.

Table 19. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max T_A = 105 °C	Unit
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1), all peripherals enabled	150 MHz	55.6	mA
			120 MHz	48.4	
			108 MHz	44.0	
			72 MHz	36.1	
			48 MHz	28.8	
			36 MHz	24.1	
			24 MHz	20.5	
			16 MHz	17.7	
			8 MHz	14.7	
		High speed external crystal (HEXT)(1), all peripherals disabled	150 MHz	31.1	mA
			120 MHz	28.7	
			108 MHz	26.3	
			72 MHz	22.3	
			48 MHz	19.5	
			36 MHz	17.2	
			24 MHz	15.8	
			16 MHz	14.6	
			8 MHz	13.4	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 20. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max T_A = 105 °C	Unit
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled	150 MHz	46.1	mA
			120 MHz	39.7	
			108 MHz	37.0	
			72 MHz	30.9	
			48 MHz	24.9	
			36 MHz	21.7	
			24 MHz	18.8	
			16 MHz	16.5	
			8 MHz	13.8	
		High speed external crystal (HEXT)(1), all peripherals disabled	150 MHz	16.5	mA
			120 MHz	16.0	
			108 MHz	15.6	
			72 MHz	14.6	
			48 MHz	14.1	
			36 MHz	13.5	
			24 MHz	13.4	
			16 MHz	12.9	
			8 MHz	12.1	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 21. Typical and maximum current consumptions in Deepsleep and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max(2)			Unit
			V_{DD} = 2.6 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode	LDO in Run mode, HICK and HEXT OFF, WDT OFF	735	740	Refer to note (3)	4000	6600	µA
		LDO in low-power mode, LPDS1=1, HICK and HEXT OFF, WDT OFF	675	680		3480	6000	
	Supply current in Standby mode	LEXT and ERTC OFF	2.5	3.6	4.8	7.0	10.3	
		LEXT and ERTC ON	4.3	6.6	7.5	10.0	13.7	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) The value may be several times the typical values due to process variation.

Figure 9. Typical current consumption in Deepsleep mode with LDO in run mode vs. temperature at different V_{DD}

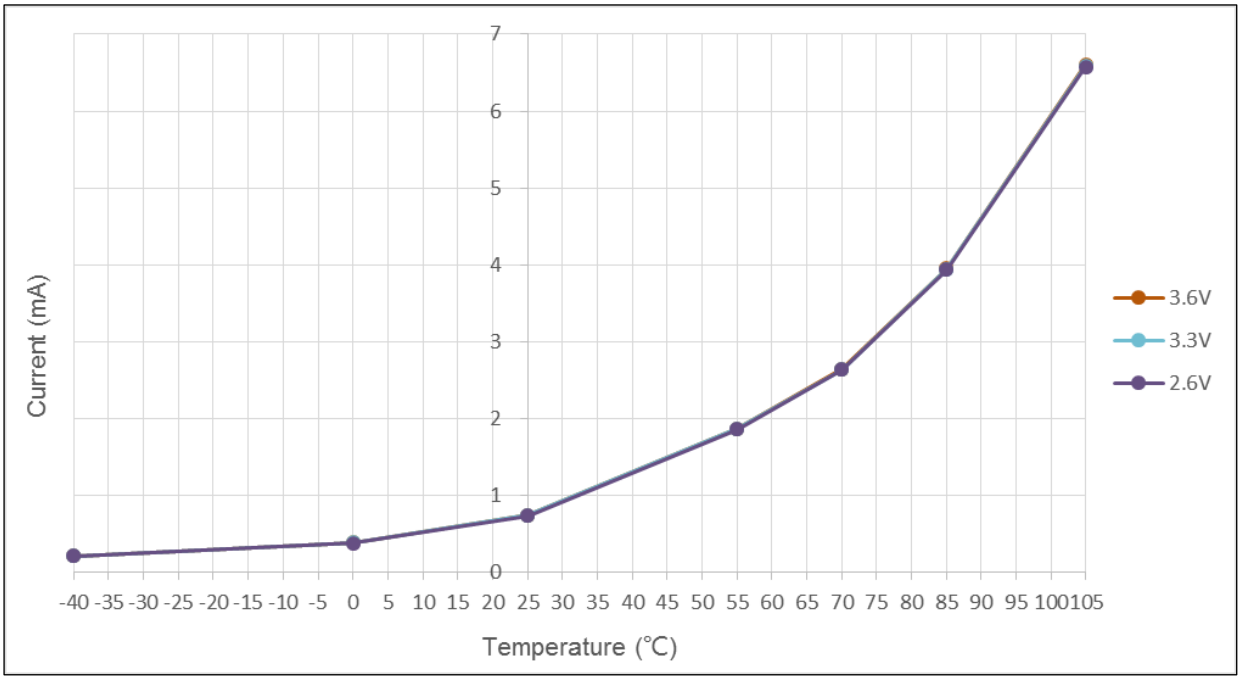


Figure 10. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different V_{DD}

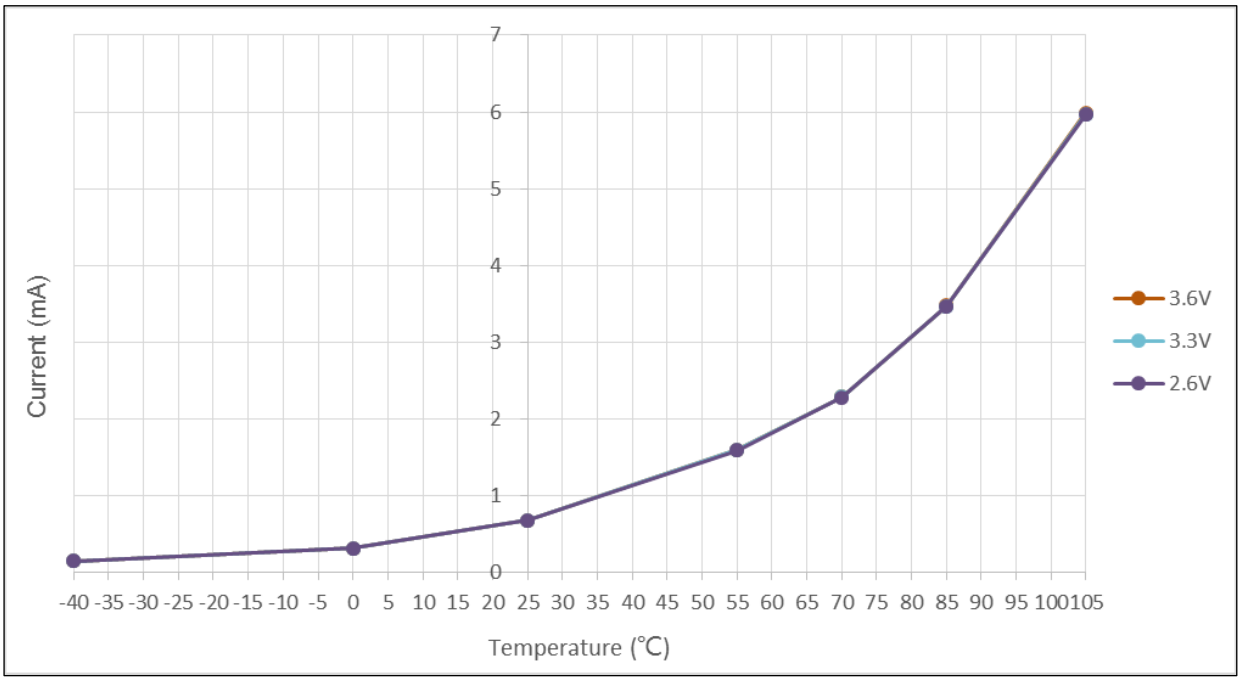


Figure 11. Typical current consumption in Standby mode vs. temperature at different V_{DD}

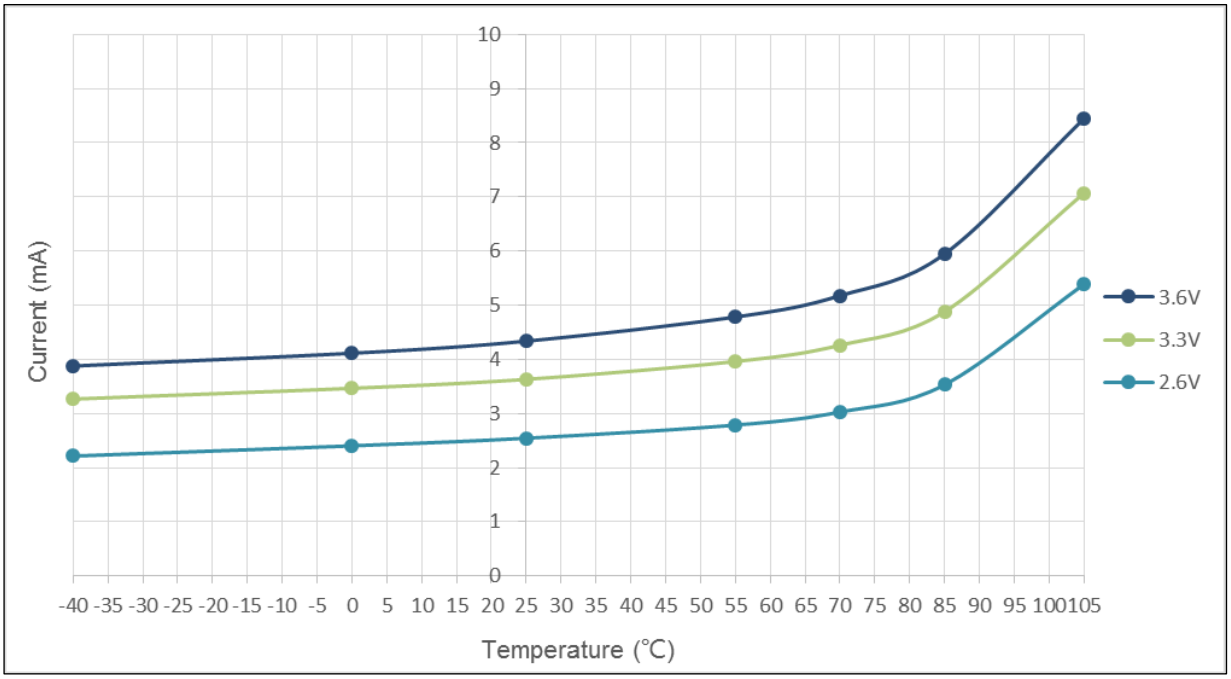
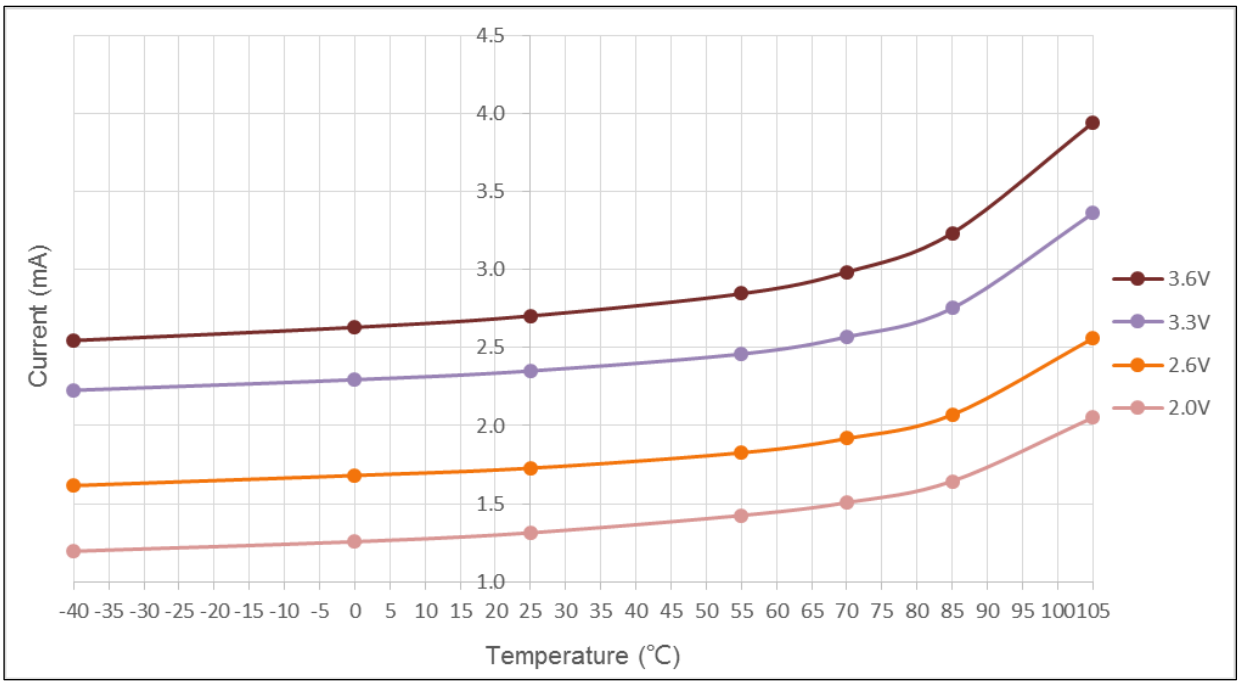


Table 22. Typical and maximum current consumptions on V_{BAT}

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			V_{BAT} = 2.0 V	V_{BAT} = 2.6 V	V_{BAT} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	V_{BAT} supply current	LEXT and ERTC ON, $V_{DD} < V_{LVR}$	1.3	1.7	2.4	2.8	3.7	4.6	µA

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 12. Typical current consumption on V_{BAT} with LEXT and ERTC on vs. temperature at different V_{BAT} values



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 23. Peripheral current consumption

Peripheral		Typ	Unit
AHB	DMA1	9.32	μA/MHz
	DMA2	9.41	
	GPIOA	1.25	
	GPIOB	1.33	
	GPIOC	1.27	
	GPIOD	1.23	
	GPIOF	1.24	
	CRC	1.64	
	SDIO1	19.3	
	OTGFS1	46.3	
APB1	TMR2	8.96	
	TMR3	6.76	
	TMR4	6.73	
	TMR5	8.97	
	SPI2/I^{2}S2	2.84	
	USART2	2.40	
	USART3	2.53	
	UART4	2.46	
	UART5	2.68	
	I^{2}C1	2.66	
	I^{2}C2	2.53	
	CAN1	3.56	
	WWDT	0.45	
	PWC	0.38	
	CMP1/2	0.81	
APB2	IOMUX	2.53	
	SPI1/I^{2}S1	2.75	
	USART1	2.48	
	TMR1	8.74	
	TMR9	4.03	
	TMR10	2.56	
	TMR11	2.60	
	ADC1	6.92	

5.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

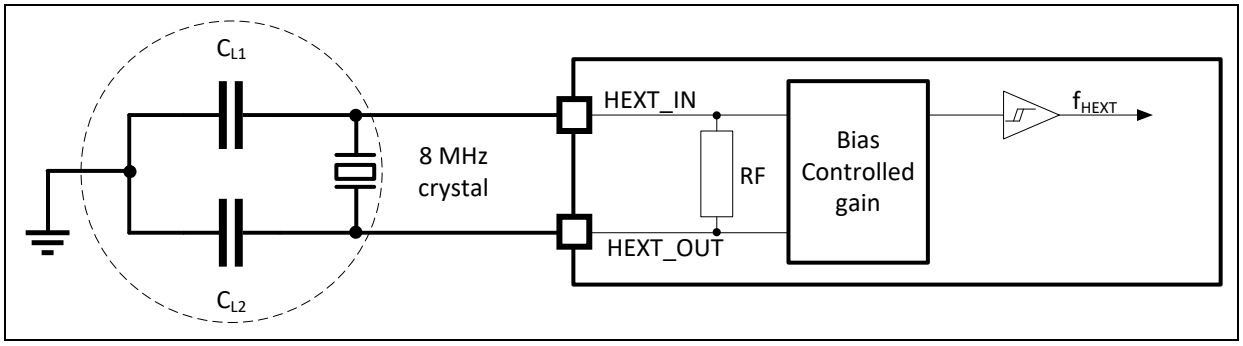
Table 24. HEXT 4-25 MHz crystal characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	V_{DD} is stabilized	-	800	-	µs

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough estimate of the combined pin and board capacitance) when selecting C_{L1} and C_{L2}.

Figure 13. HEXT typical application with an 8 MHz crystal



High-speed external clock generated from an external source

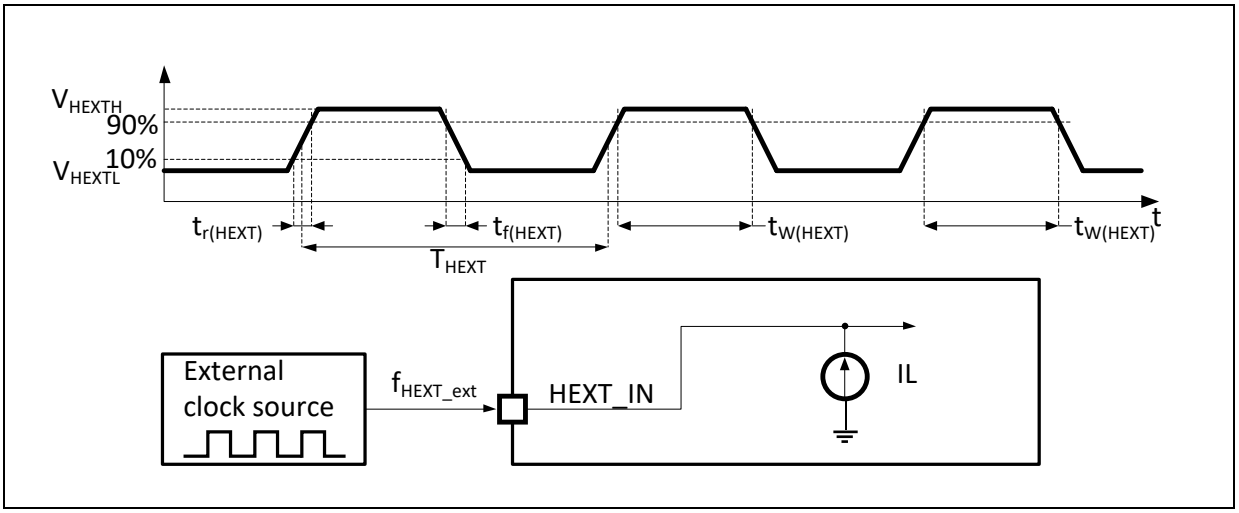
The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 25. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 14. HEXT external source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 26. LEXT 32.768 kHz crystal characteristics(1)(2)

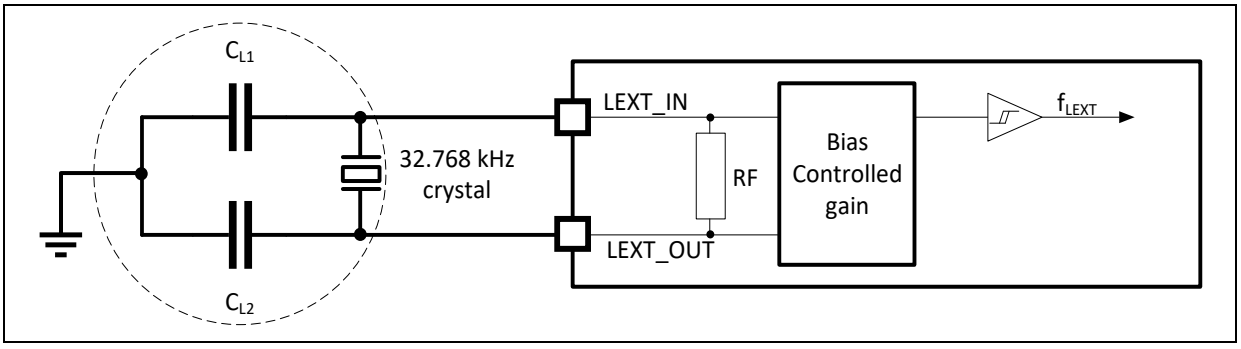
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	200	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range and select to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 15. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

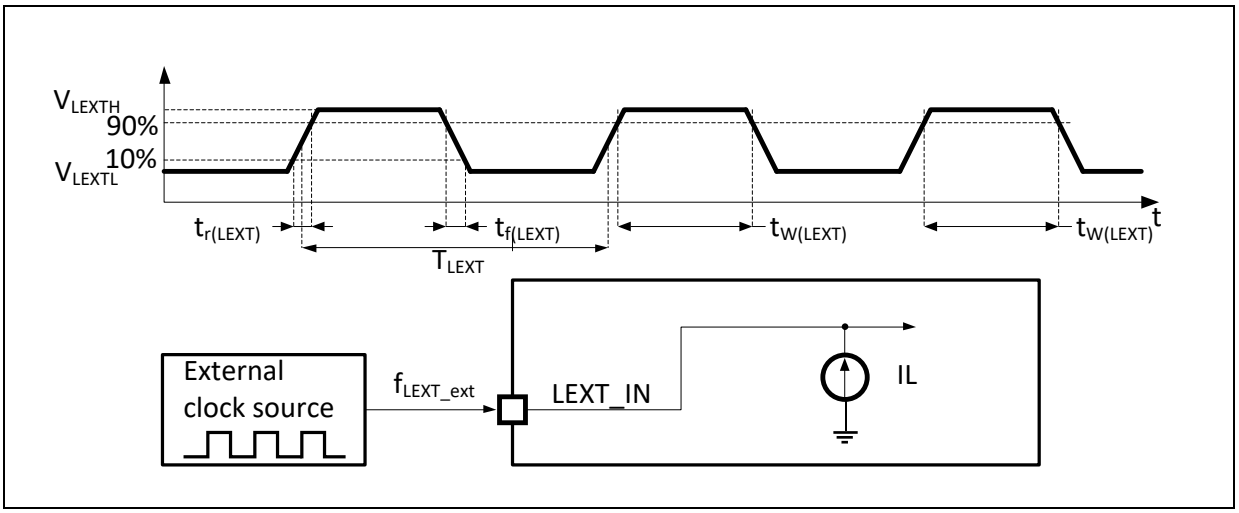
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 27. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)	-	450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)	-	-	-	50	ns
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 16. LEXT external source AC timing diagram



5.3.7 Internal clock source characteristics

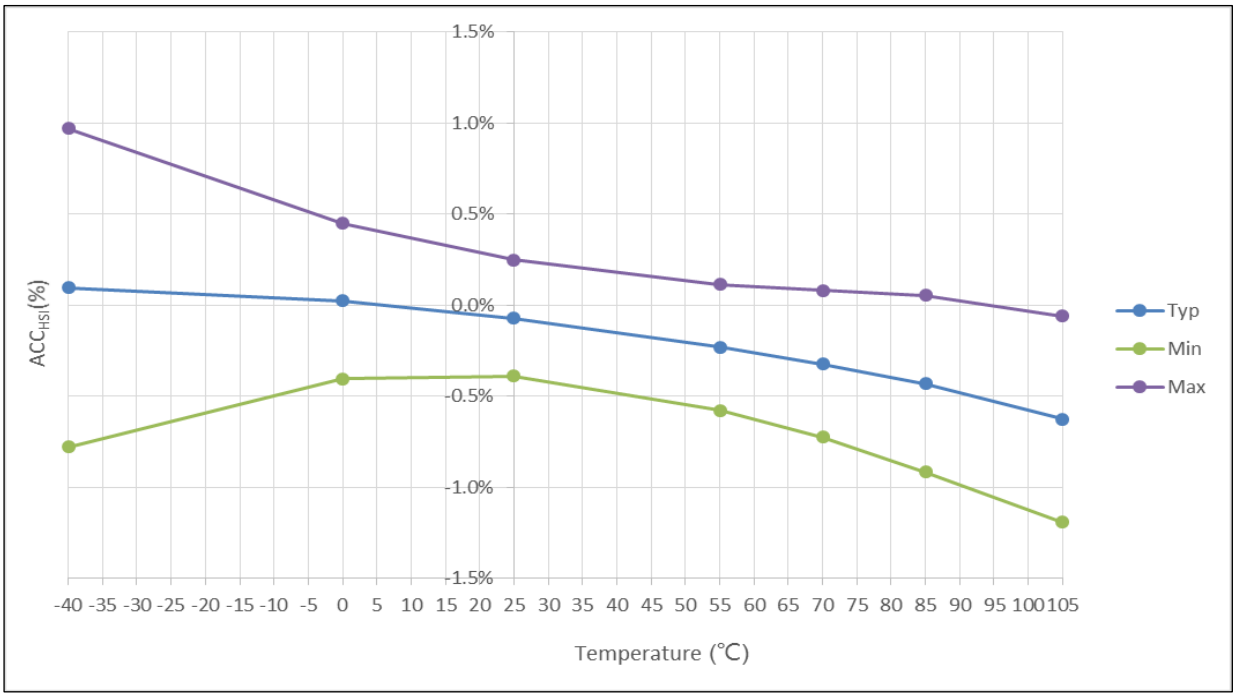
High-speed internal clock (HICK)

Table 28. HICK clock characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CRM_CTRL register(1)		-1	-	1	%
		Factory-calibrated(2)	T_A = -40 ~ 105 °C	-2		1.5	%
			T_A = -40 ~ 85 °C	-1.5	-	1.5	
			T_A = 25 °C	-1	0.5	1	
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-		-	-	10	µs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-		-	200	215	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 17. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 29. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	30	40	60	kHz

(1) Guaranteed by characterization results, not tested in production.

5.3.8 PLL characteristics

Table 30. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	150	MHz
t_{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Take case of using the appropriate multiplier factors to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

5.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK.

Table 31. Low-power mode wakeup time

Symbol	Parameter Conditions	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	4.2	μs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode (LDO in normal mode)	300	μs
	Wakeup from Deepsleep mode (LDO in low-power mode)	360	
$t_{WUSTDBY}$	Wakeup from Standby mode	600	μs

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 32. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional error, V_{DD} and V_{SS} input has one 47 μF capacitor and each V_{DD} and V_{SS} pin pair 0.1 μF	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 150 MHz, conforms to IEC 61000-4-4	4A (±4 kV)
		V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

5.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 33. GPIO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	–0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	Standard GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT GPIO input high level voltage	-		-	5.5	
V_{hys}	Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input leakage current(2)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard GPIOs	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5V$ FT GPIO	-	-	±10	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	60	75	110	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)(4)	$V_{IN} = V_{DD}$	60	80	120	kΩ
C_{IO}	GPIO pin capacitance	-	-	5	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT, and FTa pins.
(4) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in *Section 5.2.1*:

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
Maximum sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}(1)	Output high level voltage		2.4	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 35. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$	Pulse width of external signals detected by EXINT controller	10	-	ns

5.3.12 NRST pin characteristics

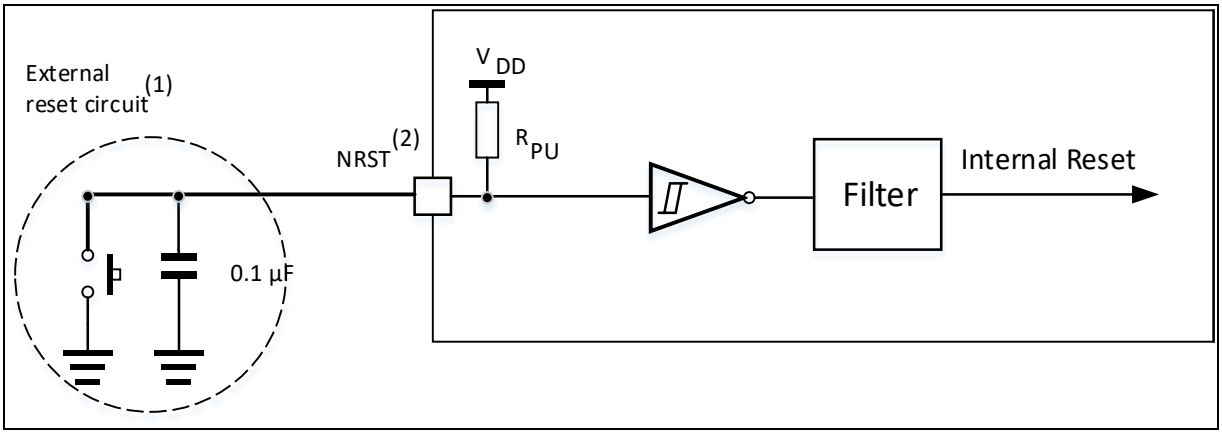
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	400	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level inactive	-	-	-	33.3	µs
$t_{ILNV(NRST)}$(1)	NRST input low level active	-	66.7	-	-	µs

(1) Guaranteed by design.

Figure 18. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the V_{IL} (NRST) max level specified in *Table 36*. Otherwise the reset will not be performed by the device.

5.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Table 37. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 150 MHz	6.7	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz

5.3.14 SPI characteristics

Table 38. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency$^{(2)(3)}$	Master mode	-	36	MHz
		Slave receive mode	-	36	
		Slave transmit mode	-	32	
$t_{su(CS)}^{(1)}$	CS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(CS)}^{(1)}$	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode prescaler = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input setup time	Master mode	4	-	ns
$t_{h(SI)}^{(1)}$		Slave mode	5	-	
$t_{a(SO)}^{(1)(4)}$	Data output access time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{dis(SO)}^{(1)(5)}$	Data output disable time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales office for technical support.
(4) Min time is the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 19. SPI timing diagram - slave mode and CPHA = 0

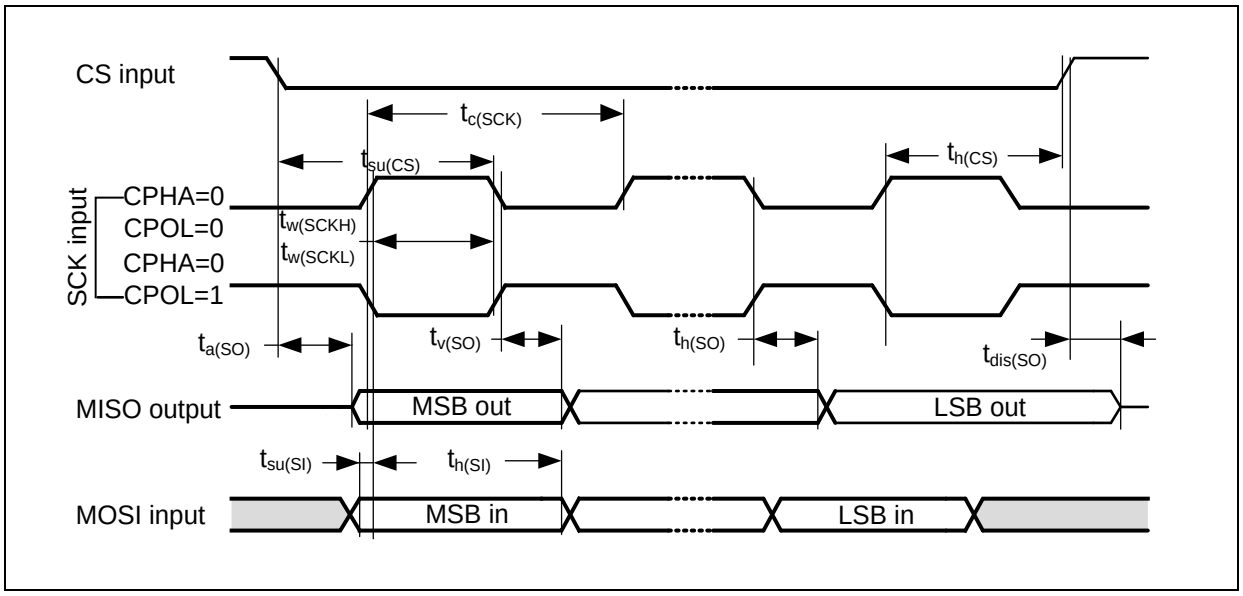


Figure 20. SPI timing diagram - slave mode and CPHA = 1

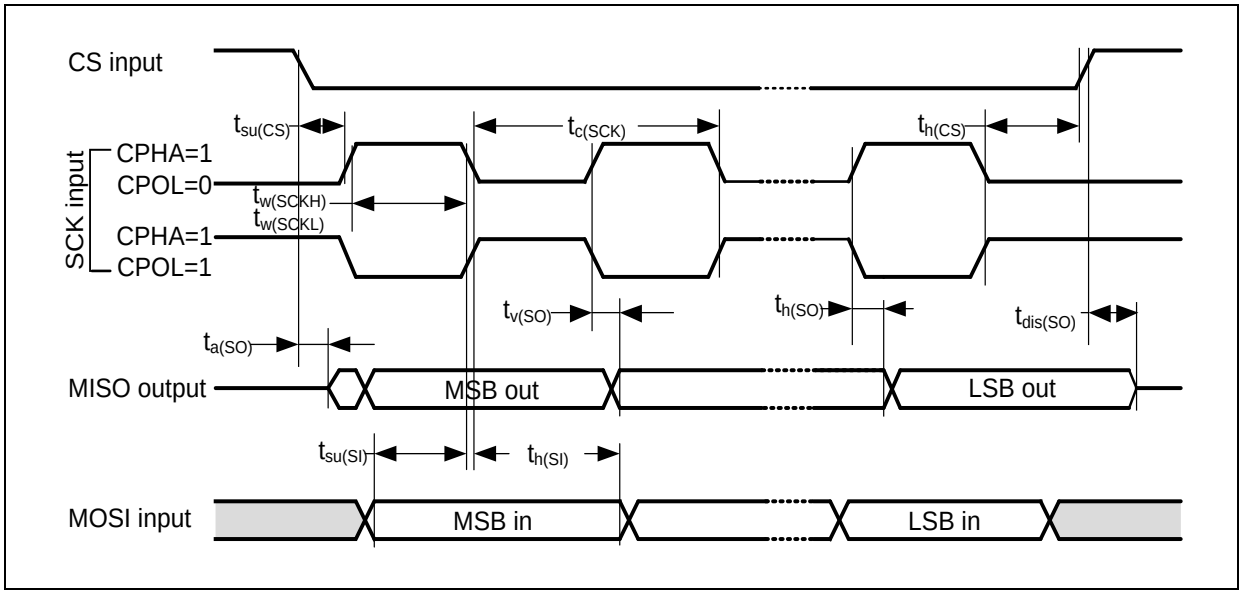
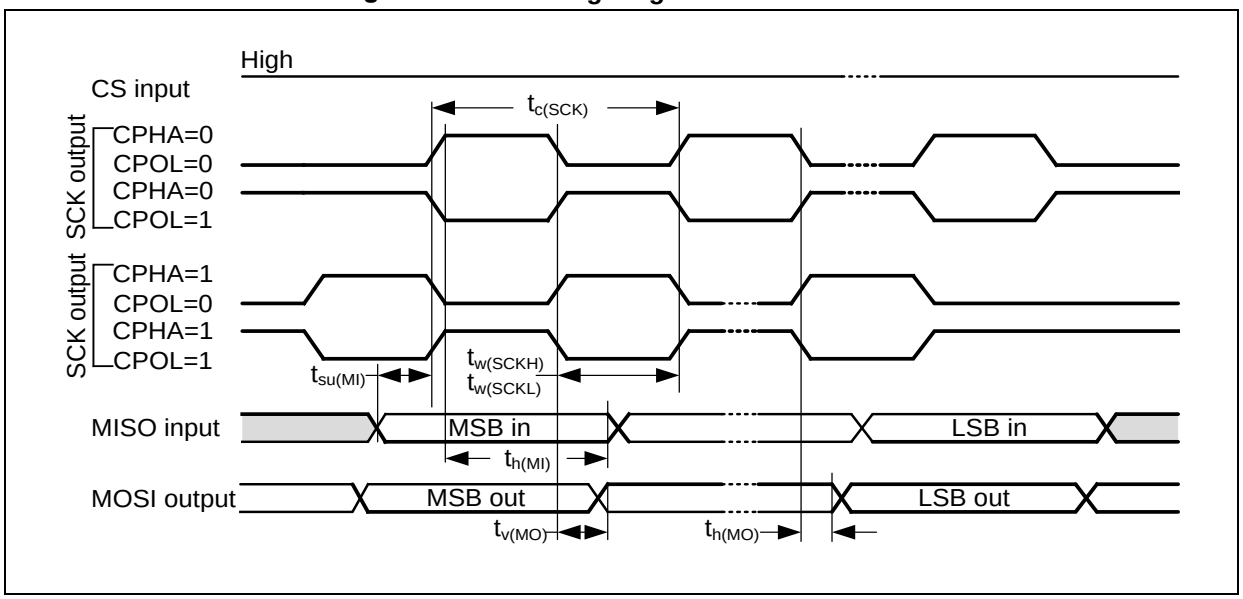


Figure 21. SPI timing diagram - master mode



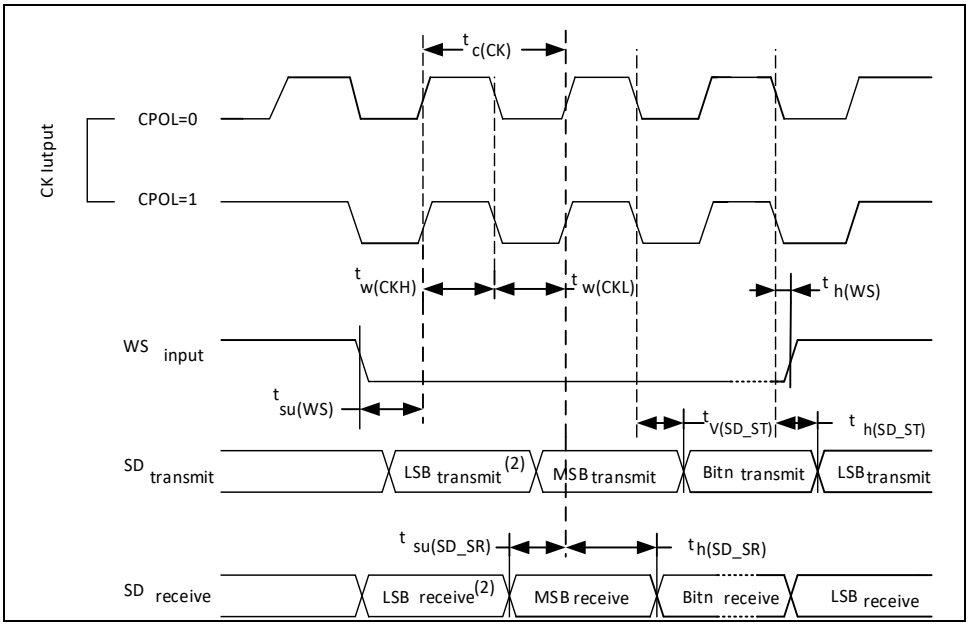
5.3.15 I²S characteristics

Table 39. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	0	4	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	4	
$t_{su(WS)}$(1)	WS setup time	Slave mode	9	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

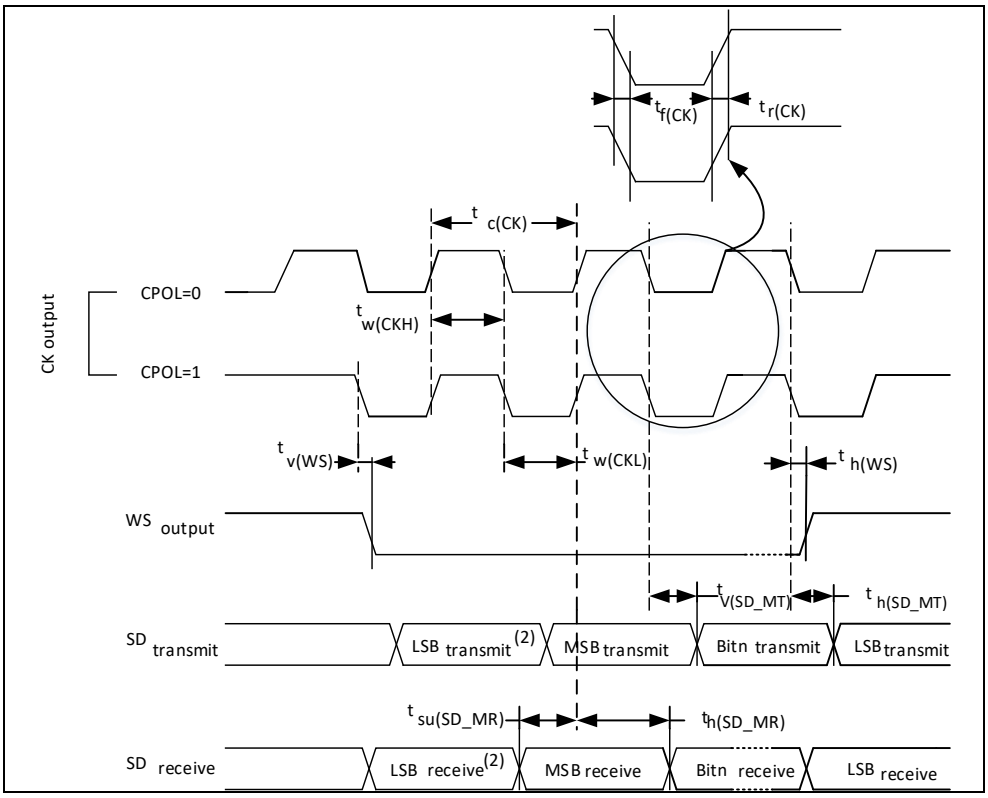
(1) Guaranteed by design, not tested in production.
(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 22. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 23. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

5.3.16 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not ”true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz) and fast mode (max. 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more complete information, please contact your local Artery sales office for technical support.

5.3.17 SDIO characteristics

Figure 24. SDIO high-speed mode

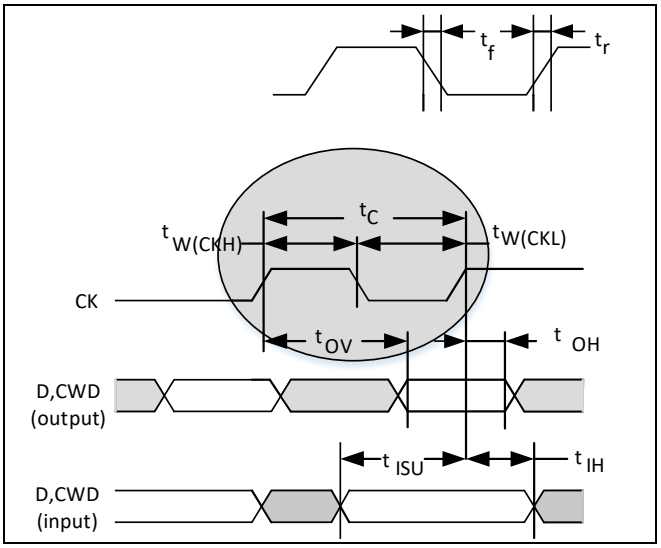


Figure 25. SD default mode

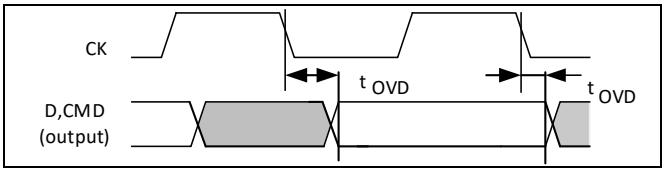


Table 40. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	48	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	-	32	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	-	30	-	
t_r	Clock rise time	-	-	4	
t_f	Clock fall time	-	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	-	2	-	ns
t_{IH}	Input hold time	-	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	-	-	6	ns
t_{OH}	Output hold time	-	0	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time	-	-	7	ns
t_{OHD}	Output hold default time	-	0.5	-	

5.3.18 OTGFS characteristics

Table 41. OTGFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	µs

(1) Guaranteed by design, not tested in production.

Table 42. OTGFS DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	OTGFS operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I (OTGFS_D+/D-)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PU}		OTGFS_D+ internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ
R_{PD}		OTGFS_D+/D- internal pull-up	V_{IN} = V_{DD}	15	19	25	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32F415 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by design, not tested in production.
(4) R_L is the load connected on the USB drivers.

Figure 26. OTGFS timings: definition of data signal rise and fall time

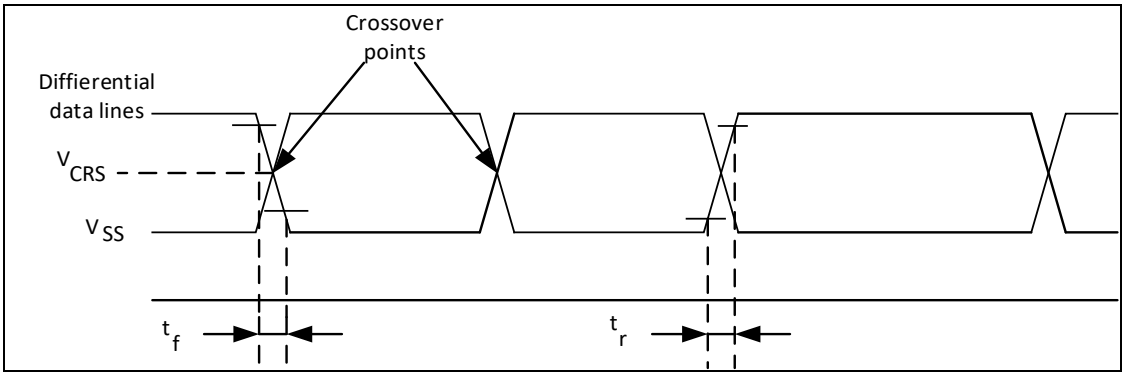


Table 43. OTGFS electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time(2)	C_L ≤ 50 pF	4	20	ns
t_f	Fall Time(2)	C_L ≤ 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 11*.

Note: It is recommended to perform a calibration after each power-up.

Table 44. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.6	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	560(1)	660	μA
f_{ADC}	ADC clock frequency		0.6	-	28	MHz
f_S(2)	Sampling rate		0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-}tied internally to ground))	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 45* and *Table 46* for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	15	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.14			μs
		-	172			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	ns
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14 ~ 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Obtained by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} is internally connected to V_{DDA} whereas V_{REF-} is internally connected to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 44*.

Table 45 and *Table 46* are used to define the maximum external impedance allowed for an error below 1 of LSB.

Table 45. R_{AIN} max for f_{ADC} = 14 MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.25
7.5	0.54	1.3
13.5	0.96	2.5
28.5	2.04	5.0
41.5	2.96	8.0
55.5	3.96	10.5
71.5	5.11	13.5
239.5	17.11	40

(1) Guaranteed by design.

Table 46. R_{AIN} max for f_{ADC} = 28 MHz

T_S (Cycle)	t_S (μs)	R_{AIN} max (kΩ)(1)
1.5	0.05	0.1
7.5	0.27	0.6
13.5	0.48	1.2
28.5	1.02	2.5
41.5	1.48	4.0
55.5	1.98	5.2
71.5	2.55	7.0
239.5	8.55	20

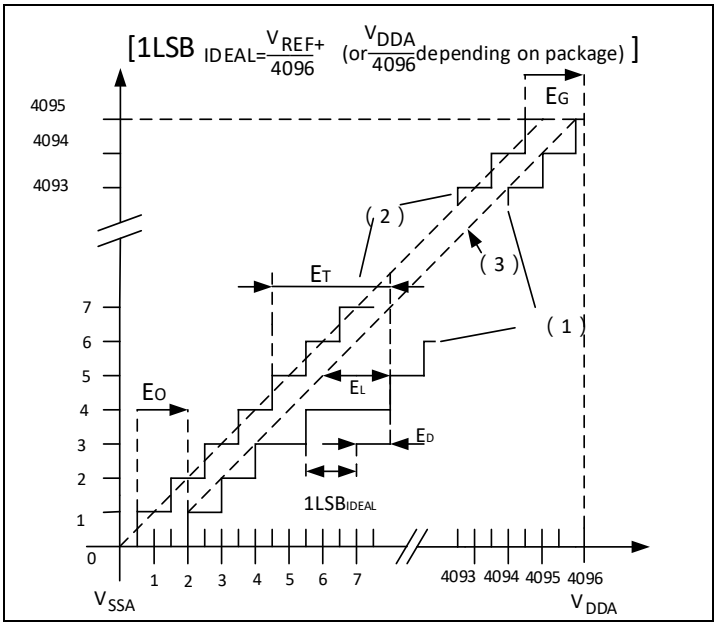
(1) Guaranteed by design.

Table 47. ADC accuracy(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C	±2	±3	LSB
EO	Offset error		±1	±1.6	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±0.6	±1	
EL	Integral linearity error		±1	±2	
ET	Total unadjusted error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.6 to 3.6 V, T_A = -40 ~ 105 °C	±2	±4	LSB
EO	Offset error		±1	±2	
EG	Gain error		±1.5	±3.5	
ED	Differential linearity error		±0.6	+1.5/-1	
EL	Integral linearity error		±1	±2	

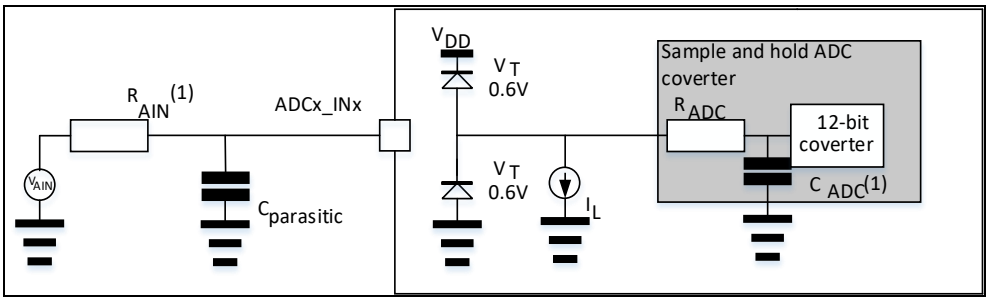
(1) ADC DC accuracy values are measured after internal calibration.
(2) Obtained by characterization results, not tested in production.

Figure 27. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 28. Typical connection diagram using the ADC



(1) Refer to *Table 44* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 7.* The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

5.3.20 Internal reference voltage (V_{INTRV}) characteristics

Table 48. Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs

(1) Obtained by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

5.3.21 Temperature sensor (V_{TS}) characteristics

Table 49. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±2	±5	ºC
Avg_Slope(1(2))	Average slope	-4.13	-4.34	-4.54	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	1.26	1.32	1.38	V
t_{START}(3)	Startup time	-	-	100	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	5.1	-	-	µs

(1) Obtained by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

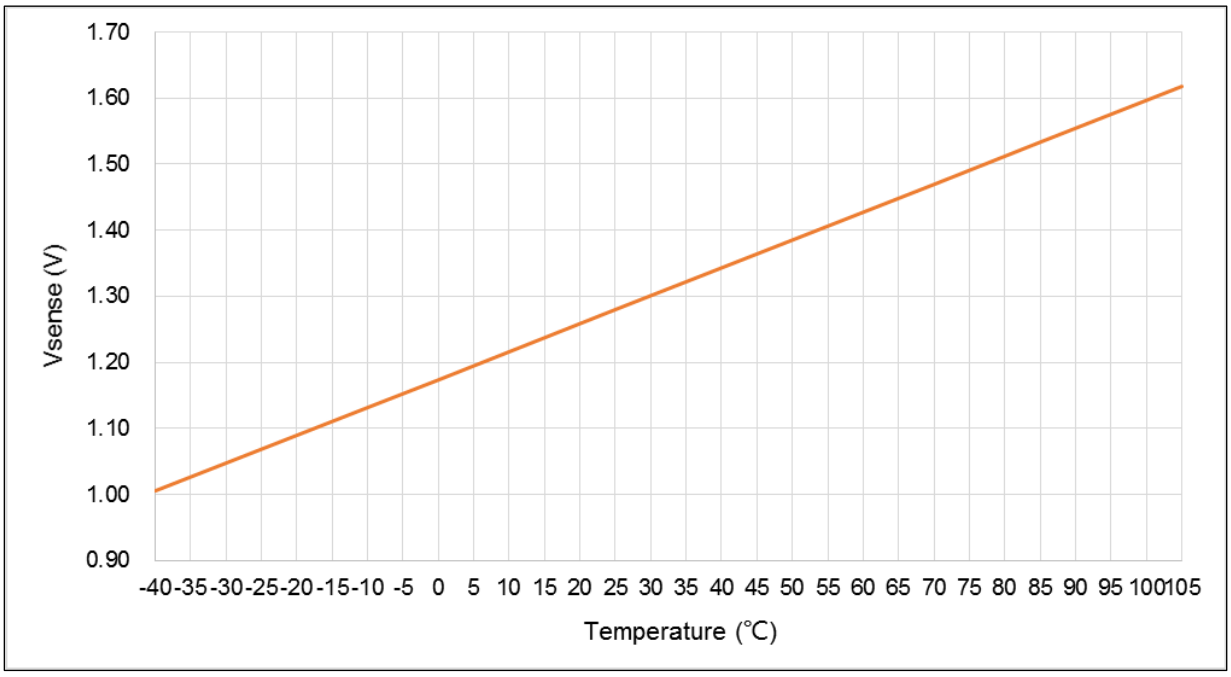
Temperature (in °C) = {(V_{25} - V_{TS}) / Avg_Slope} + 25.

Where,

V_{25} = V_{TS} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{TS} (given in mV/° C).

Figure 29. V_{TS} vs. temperature



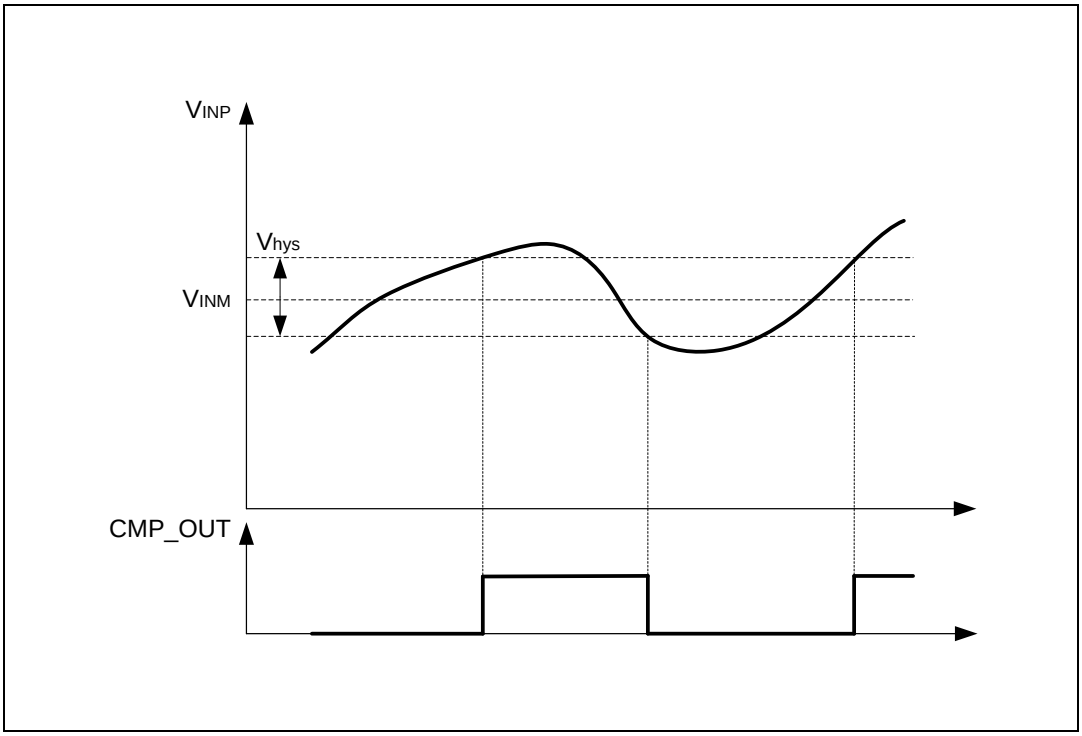
5.3.22 CMP characteristics

Table 50. CMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	单位
V_{DDA}	Analog supply voltage	-		2.6	-	3.6	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	V
t_{START}	Startup time	High speed mode		-	2.0	3.2	µs
		Low power mode		-	3.6	5.5	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	High speed mode		-	105	320	ns
		Low power mode		-	1.2	3	µs
V_{offset}	Offset voltage	-		-	±3	±10	mV
V_{hys}	Hysteresis	No hysteresis		-	0	-	mV
		High speed mode	Low hysteresis	40	65	100	
			Medium hysteresis	120	180	280	
			High hysteresis	200	320	450	
		Low power mode	Low hysteresis	15	25	35	
			Medium hysteresis	50	70	90	
			High hysteresis	90	120	160	
I_{DDA}	Current consumption	High speed mode		-	120	165	µA
		Low power mode		-	1.9	3.5	

(1) Obtained by characterization results, not tested in production.

Figure 30. CMP hysteresis



6 Package information

6.1 LQFP64 – 10 x 10 mm

Figure 31. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline

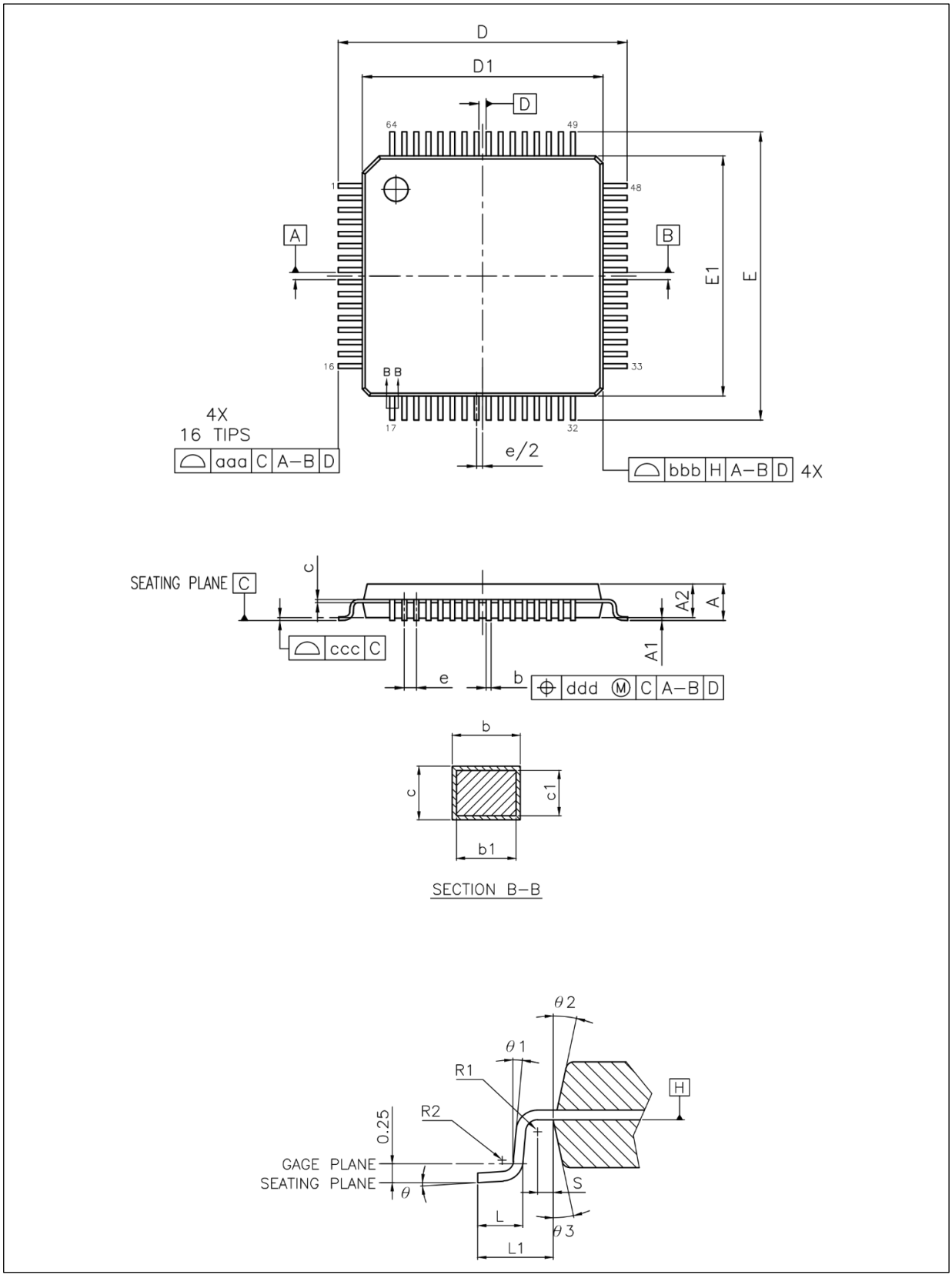


Table 51. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC.		
Θ	3.5° REF.		
L	0.45	0.60	0.75
L1	1.00 REF.		
ccc	0.08		

6.2 LQFP64 – 7 x 7 mm

Figure 32. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package outline

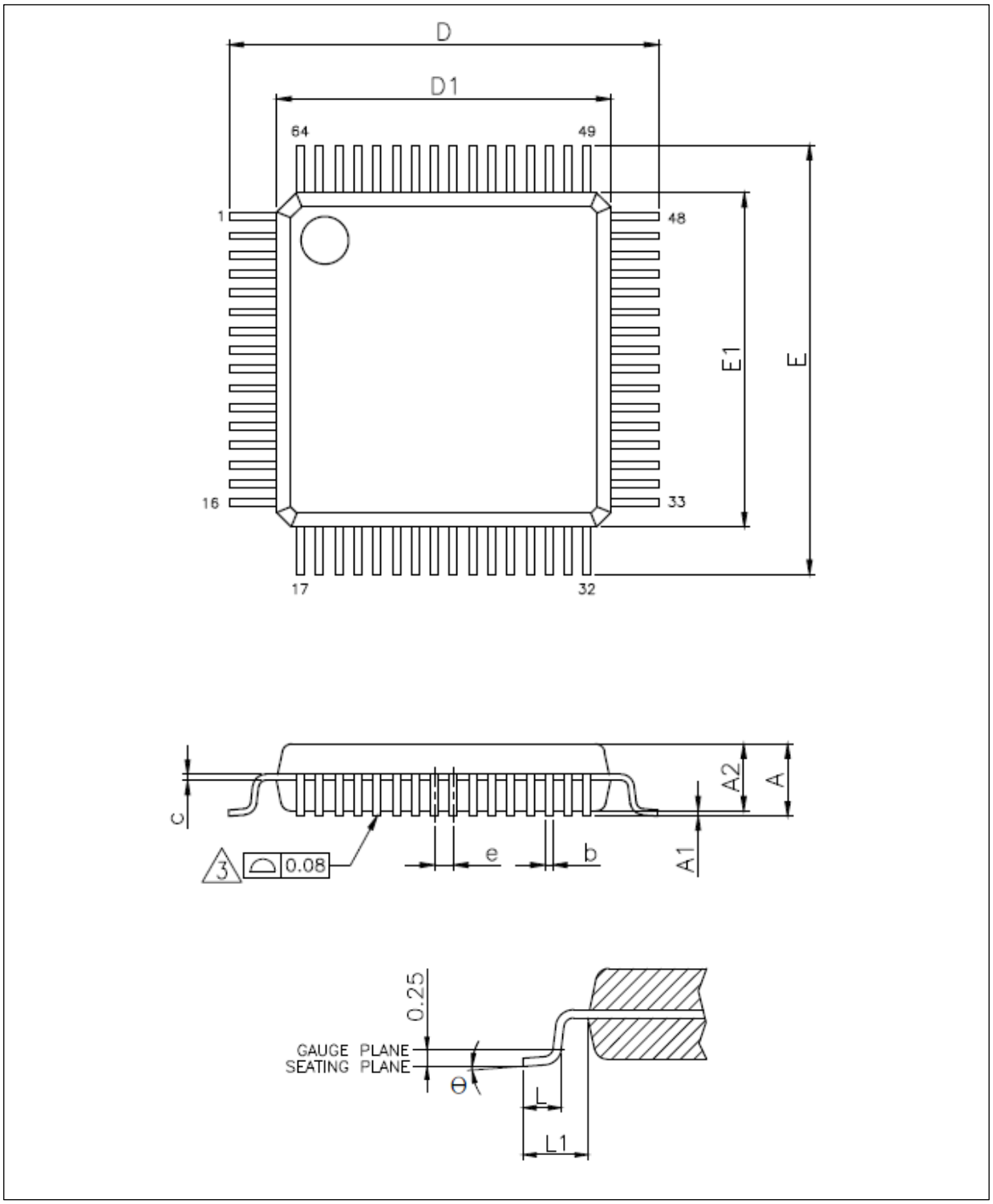


Table 52. LQFP64 – 7 x 7 mm 64 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

6.3 LQFP48 – 7 x 7 mm

Figure 33. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline

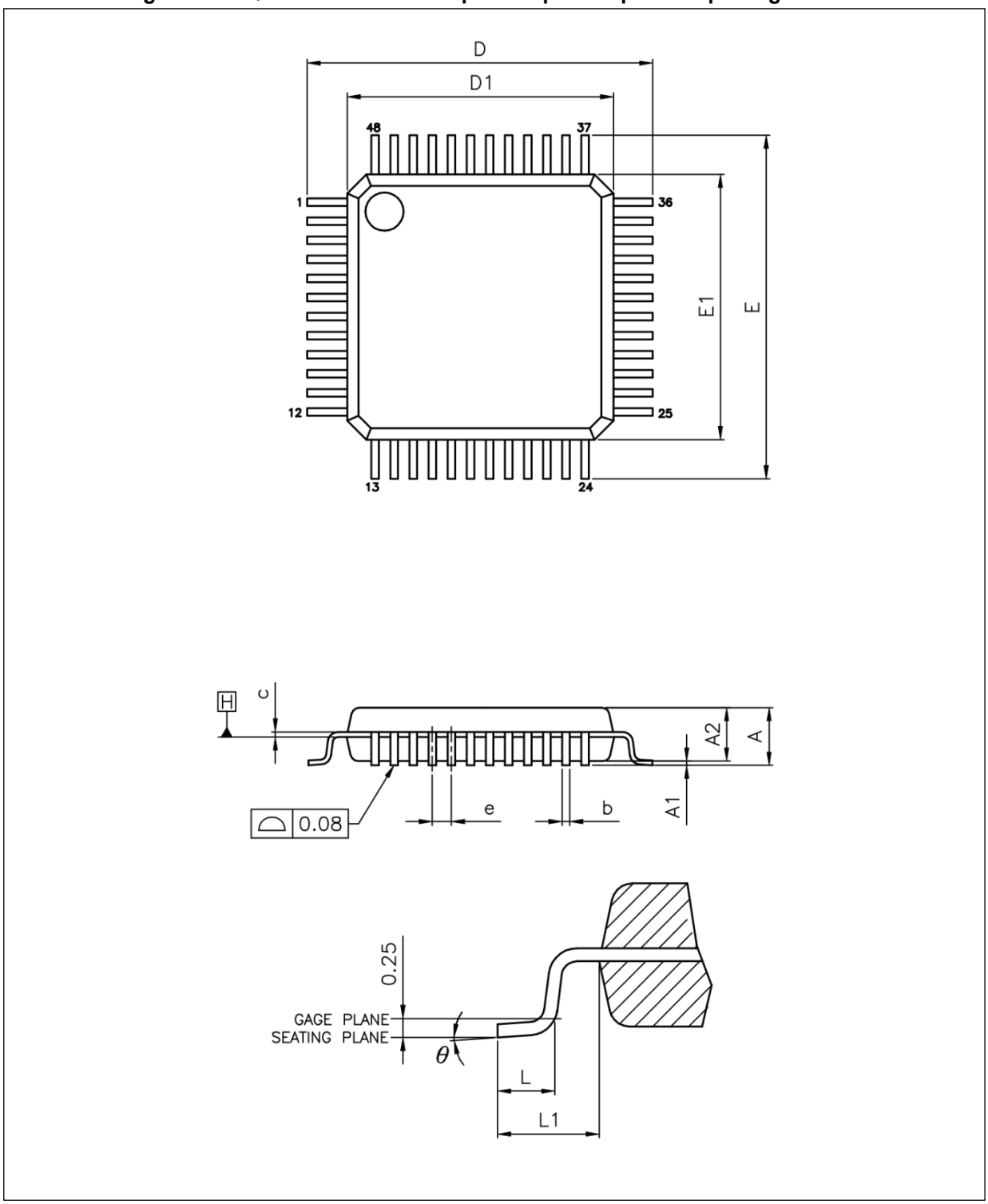


Table 53. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

6.4 QFN48 – 6 x 6 mm

Figure 34. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package outline

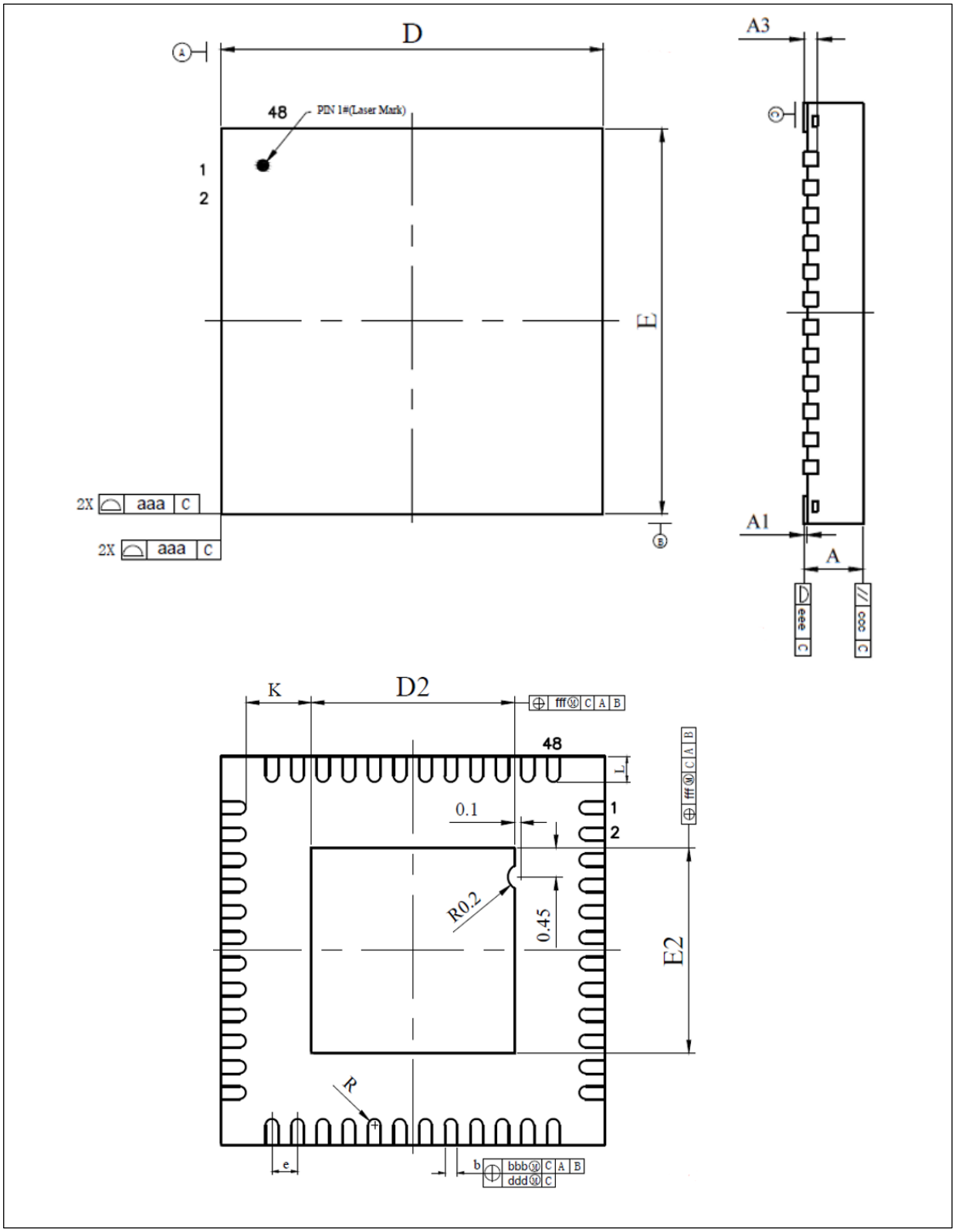


Table 54. QFN48 – 6 x 6 mm 48 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	3.07	3.17	3.27
E	5.90	6.00	6.10
E2	3.07	3.17	3.27
e	0.40 BSC.		
K	0.20	-	-
L	0.35	0.40	0.45

6.5 QFN32 – 4 x 4 mm

Figure 35. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline

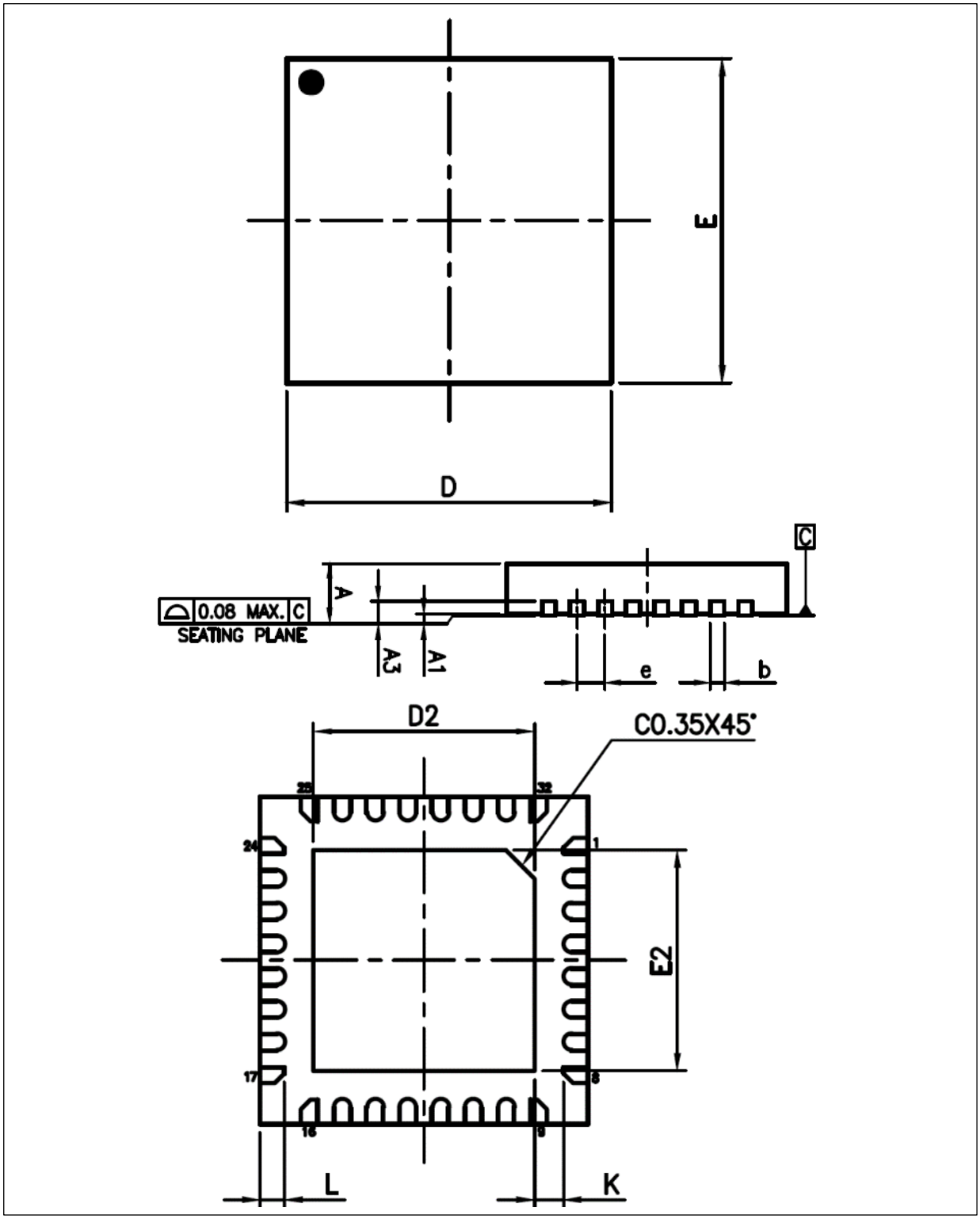


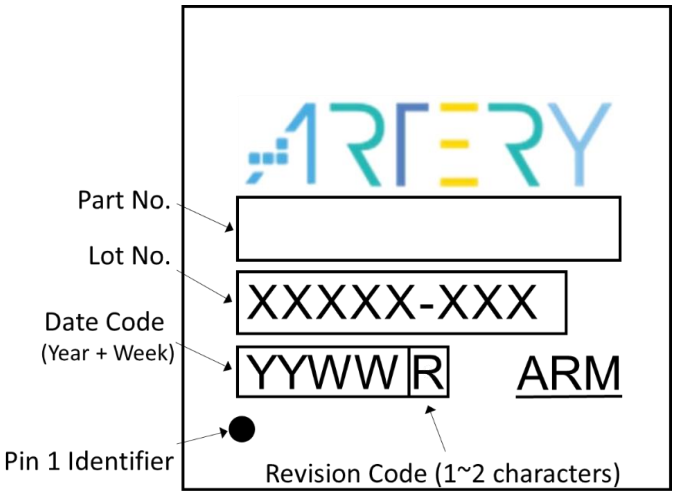
Table 55. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

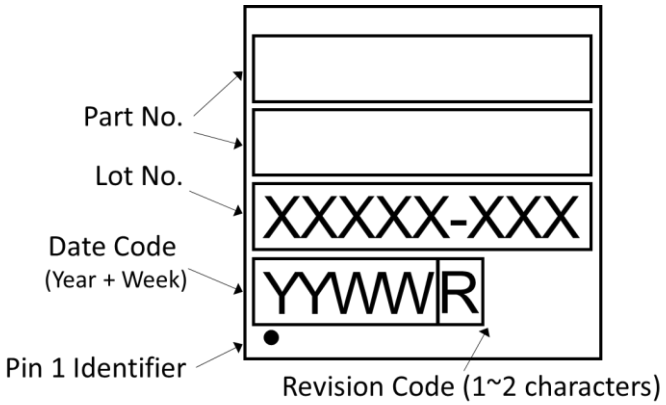
6.6 Device marking

Figure 36. Marking example

LQFP64, LQFP48, QFN48



QFN32



(1) Not In Scale.

6.7 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material of 1.6mm thickness. They are guaranteed by design, not tested in production.

Table 56. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 – 10 × 10 mm / 0.5 mm pitch	75.3	°C/W
	Thermal resistance junction-ambient LQFP64 – 7 × 7 mm / 0.4 mm pitch	80.4	
	Thermal resistance junction-ambient LQFP48 – 7 × 7 mm / 0.5 mm pitch	76.8	
	Thermal resistance junction-ambient QFN48 – 6 × 6 mm / 0.4 mm pitch	38.8	
	Thermal resistance junction-ambient QFN32 – 4 × 4 mm / 0.4 mm pitch	59.7	

7 Part numbering

Table 57. AT32F415 series part numbering

Examples: AT32 F 4 1 5 R C T 7 -7

Product family

AT32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex™-M4

Product series

1 = Value line

Product application

5 = OTG series

Pin count

R = 64 pins

C = 48 pins

K = 32 pins

Internal Flash memory size

C = 256 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

Package type

T = LQFP

U = QFN

Temperature range

7 = -40 °C to +105 °C

Package information

-7 = LQFP64 - 7 x 7 mm

-4 = QFN32 - 4 x 4 mm

Blank = other packages

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

8 Document revision history

Table 58. Document revision history

Date	Version	Change
2019.8.1	1.00	Initial release.
2019.10.11	1.01	1. Modified DMA2 as 7 channels 2. Modified USART/UART maximum communication rate 3. Added AT32F415CCU7 and AT32F415CBU7
2020.3.10	1.02	Added the note (9) of *Table 5* to describe the usage limitation of PA9
2020.6.5	1.03	Corrected a typo of PA8 in the note (9) of *Table 5*. It should be PA9
2020.8.7	1.04	Added the description in the note (3) of *Table 5* about devices having reduced peripheral counts
2020.10.14	1.05	1. Deleted CMP digital noise filter for malfunction 2. Corrected the start address of the system memory in *Figure 6* as 0x1FFF_AC00
2021.6.30	1.06	1. Crystal-less is no more supported at OTG device mode 2. Modified the description in the note (8) and (9) of *Table 5* 3. Added LQFP48 package mechanical D, D1, E, E1 Min. and Max. in *Table 53* 4. Modified QFN48 package mechanical D2, E2 in *Table 54*
2020.11.3	1.10	1. Added the description of note (9) of *Table 5* about exception starting from Silicon reversion code C 2. Added the description of the endpoint number in *2.14.7*
2022.2.14	2.00	1. Modified paragraph orders and descriptions of the whole document 2. Corrected LQFP64 7 x 7 mm package mechanical in *Table 52*
2022.6.6	2.0.1	1. Added max value and notes (T_A = 25 °C) in *Table 21* and *Table 22* 2. Added min and max values in D, D1, E and E1 lines of all package mechanic data tables. 3. Updated figures in *Section 3*
2023.10.17	2.02	1. Updated *Table 38* and *Table 39* 2. Added footnote (3) to *Table 33* 3. Added a paragraph of description to *Section 2.14.6 Controller area network (CAN)* 4. Update “IMPORTANT NOTICE” at the end of this file.

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