ARM®-based 32-bit Cortex®-M4F MCU+FPU with 256 to 1024 KB Flash, USB, CAN, 18 timers, 3 ADCs,16 communication interfaces

Feature

- **Core: ARM® 32-bit Cortex®-M4F CPU with FPU**
  - 200 MHz maximum frequency, with a memory protection unit (MPU)
  - Single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 256 to 1024 Kbytes of Flash instruction/data memory
  - SPIM interface: Extra interfacing up to 16 Mbytes of the external SPI Flash (as instruction/data memory)
  - Up to 96+128 Kbytes of SRAM
  - External memory controller (XMC) with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- **Clock, reset, and supply management**
  - 2.6 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4 to 25 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC (accuracy 1 % at T_A = 25 °C, 2.5 % at T_A = -40 to +85 °C)
  - Internal 40 kHz RC with calibration
  - 32 kHz oscillator for RTC with calibration
- **Low power**
  - Sleep, Stop, and Standby modes
- **3 x 12-bit, 0.5 µs A/D converters (up to 21 channels)**
  - Conversion range: 0 to 3.6V
  - Triple sample-and-hold capability
  - Temperature sensor
- **2 x 12-bit D/A converters**
- **DMA: 12-channel DMA controller**
  - Supported peripherals: timers, ADCs, DACs, SDIOs, I²Ss, SPIs, I²Cs, and USARTs
- **Debug mode**
  - Serial wire debug (SWD) and JTAG interfaces
  - Cortex®-M4F Embedded Trace Macrocell (ETM™)
- **Up to 112 fast I/O**
  - 37/51/80/112 multi-functional bi-directional I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- **Up to 18 timers**
  - Up to 8 x 16-bit timers + 2 x 32-bit timers, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Up to 3 x 16-bit motor control PWM advanced timers with dead-time generator and emergency stop
  - 2 x watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 x 16-bit basic timers to drive the DAC
- **Up to 16 communication interfaces**
  - Up to 3 x I²C interfaces (SMBus/PMBus)
  - Up to 5 x USARTs (ISO7816 interface, LIN, IrDA capability, modem control)
  - Up to 4 x SPIs (50 Mbit/s), all with I²S interface multiplexed
  - CAN interface (2.0B Active)
  - USB 2.0 full speed interface
  - Up to 2 x SDIO interfaces
- **CRC calculation unit, 96-bit unique ID**
- **Packages**
  - LQFP144 20 x 20 mm
  - LQFP100 14 x 14 mm
  - LQFP64 10 x 10 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm

Table 1. Device summary

Internal Flash	Part number
256 KBytes	AT32F403CCT6, AT32F403CCU6, AT32F403RCT6, AT32F403VCT6, AT32F403ZCT6
512 KBytes	AT32F403CET6, AT32F403CEU6, AT32F403RET6, AT32F403VET6, AT32F403ZET6
1024 KBytes	AT32F403CGT6, AT32F403CGU6, AT32F403RGT6, AT32F403VGT6, AT32F403ZGT6

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the AT32F403 microcontrollers.

The AT32F403 datasheet should be read in conjunction with the AT32F403 reference manual.

For information on programming, erasing, and protection of the internal Flash memory please also refer to the AT32F403 reference manual.

For information on the Cortex®-M4 core please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website at the following address:

http://infocenter.arm.com

2 Description

The AT32F403 incorporates the high-performance ARM® Cortex®-M4F 32-bit RISC core operating at 200 MHz. The Cortex®-M4F core features a Floating point unit (FPU) single precision which supports all ARM single-precision data processing instructions and data type. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F403 incorporates high-speed embedded memories (up to 1024 Kbytes of Flash memory, 96+128 Kbytes of SRAM), the extensive external SPI Flash (up to 16 Mbytes addressing capability), and enhanced I/Os and peripherals connected to two APB buses.

The AT32F403 offers three 12-bit ADC, eight general-purpose 16-bit timers plus two general-purpose 32-bit timers, and up to three PWM timers for motor control, as well as standard and advanced communication interfaces, up to three I^2Cs, four SPIs (all multiplexed as I^2Ss), two SDIOs, five USARTs, an USB, and a CAN.

The AT32F403 operates in the -40 to +85 °C temperature range, from a 2.6 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

These features make the AT32F403 suitable for a wide range of applications such as:

- Consumer
  - Camera holder/stabilizer
  - LED/Light control
  - Smart home application
  - Fingerprint recognition
  - 2D micro printer
  - Drone
- IoT
  - IoT sensor node/gateway
  - RF wireless module
- Industrial automation
  - Human machine interface (HMI)
  - Programmable logic controller
  - Robot controller
  - 3D printer
  - BMS
- Motor control
  - BLDC/PMSM motor control
  - Invertor
  - Servo motor control

2.1 Device overview

The AT32F403 offers devices in five different package types: from 48 pins to 144 pins. Depending on the different packages, the pin-to-pin is completely compatible among devices, and also the software and functionality. Only different sets of peripherals are included. The description below gives an overview of the complete range of peripherals proposed in different devices.

Table 2. AT32F403 features and peripheral counts

Part Number		AT32F403xxU6			AT32F403xxT6										
		CC	CE	CG	CC	CE	CG	RC	RE	RG	VC	VE	VG	ZC	ZE	ZG
CPU frequency (MHz)		200														
Int. Flash(1)(2)	ZW (KBytes)	256	256	256	256	256	256	256	256	256	256	256	256	256	256	256
	NZW (KBytes)	0	256	768	0	256	768	0	256	768	0	256	768	0	256	768
	Total (KBytes)	256	512	1024	256	512	1024	256	512	1024	256	512	1024	256	512	1024
SRAM (KBytes)		96 + 128(2)														
Timers	Advanced-control	2			2			2			2			3		
	32-bit general-purpose	2			2			2			2			2		
	16-bit general-purpose	8			8			8			8			8		
	Basic	2			2			2			2			2		
	SysTick	1			1			1			1			1		
	IWDG	1			1			1			1			1		
	WWDG	1			1			1			1			1		
	RTC	1			1			1			1			1		
Communication	I²C	3			3			3			3			3		
	SPI/I²S	3/3(3)			3/3(3)			3/3			4/4			4/4		
	USART+UART	3+0			3+0			3+2			3+2			3+2		
	SDIO	1(4)			1(4)			2			2			2		
	USB Device	1			1			1			1			1		
	CAN	1			1			1			1			1		
Analog	12-bit ADC numbers/channels	3														
		10			10			16			16			21		
	12-bit DAC numbers/channels	2														
		2			2			2			2			2		
GPIOs		37			37			51			80			112		
XMC		-			-			-			1(5)			1		
SPIM(6)		1 ch / up to 16 MB														
Operating temperatures		-40 to +85 °C														
Packages		QFN48 6 x 6 mm			LQFP48 7 x 7 mm			LQFP64 10 x 10 mm			LQFP100 14 x 14 mm			LQFP144 20 x 20 mm		

(1) ZW = zero wait-state, up to SYSCLK 200 MHz
NZW = non-zero wait-state
(2) The internal Flash supports extensive SRAM 224 KBytes. Take the AT32F403ZGT6 as an example, on which the Flash/SRAM can be configured into two options below:
- ZW: 256 KBytes, NZW: 768 KBytes, RAM: 96 KBytes;
- ZW: 128 KBytes, NZW: 896 KBytes, RAM: 224 KBytes.
(3) Only I²S1 exists MCK pin on LQFP48 and QFN48 packages.
(4) Only SDIO2 exists on LQFP48 and QFN48 packages, supporting maximum 4-bit (D0~D3) mode.

(5) For the LQFP100 package, only XMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
(6) SPIM = External SPI Flash memory extension (for both program execution and data storage) with encryption capability.

2.2 Overview

2.2.1 ARM® Cortex®-M4F with FPU core and DSP instruction set

The ARM Cortex®-M4F with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

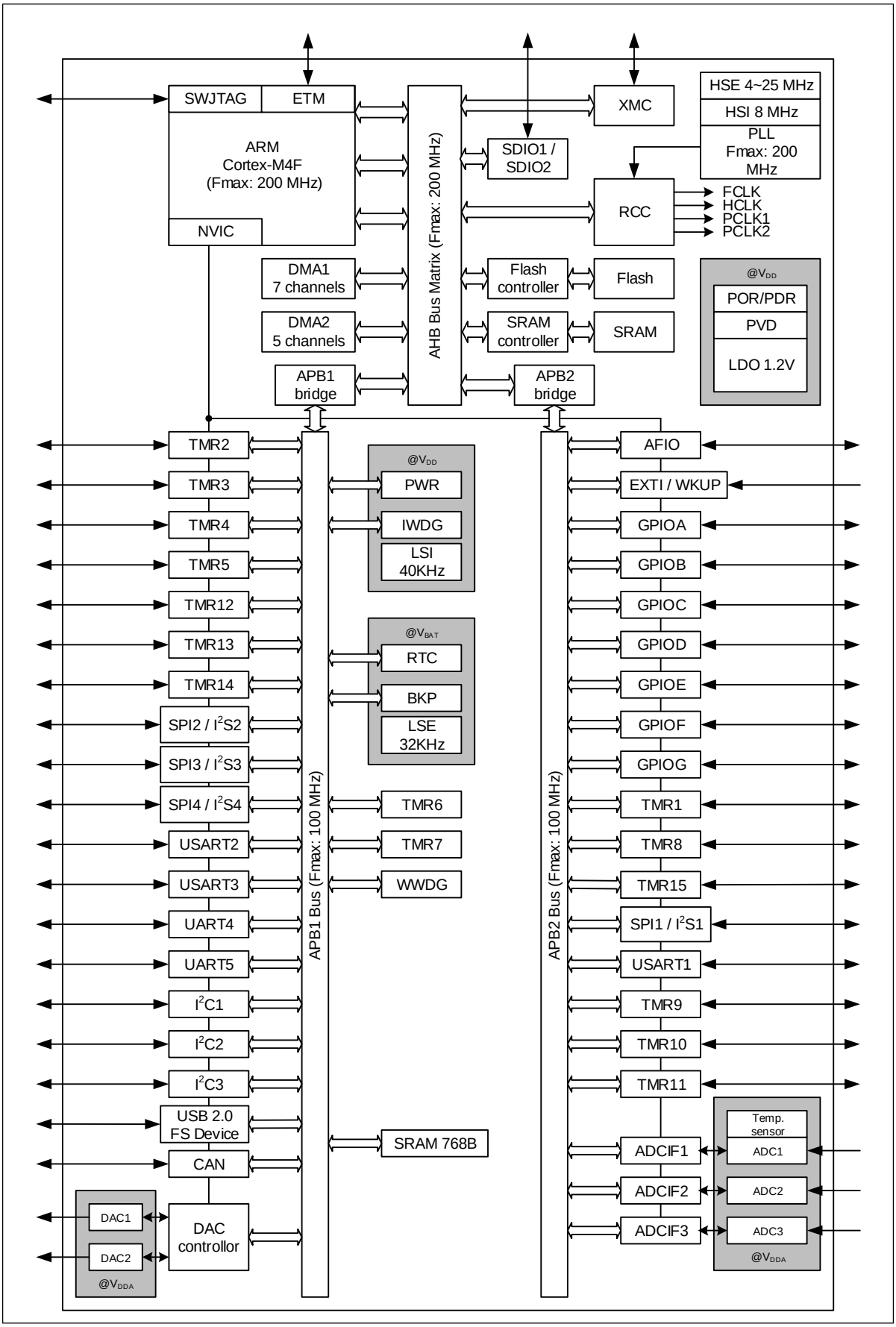
The ARM Cortex®-M4F with FPU 32-bit RISC processor features exceptional code efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the AT32F403 is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the AT32F403.

Note: Cortex®-M4F with FPU is binary compatible with Cortex®-M3.

Figure 1. AT32F403 block diagram



(1) Operating temperatures: -40 to +85 °C. Junction temperature reaches 105 °C.

2.2.2 MPU (memory protection unit)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.3 Flash memory

Up to 1024 Kbytes of embedded Flash is available for storing programs and data.

The AT32F403 provides extra interface called SPIM (SPI memory), which interfaces the external SPI Flash memory storing programs and data. With maximum 16 MBytes addressing capability, SPIM can be used as an extensive Flash memory Bank 3. SPIM additionally exists encryption to protect contents inside, enabling through the option bytes and determining the encryption area through a control register.

2.2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

2.2.5 Embedded SRAM

Up to 224 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.6 XMC (external memory controller)

The XMC is embedded in the AT32F403. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Function overview:

- The three XMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card

2.2.7 LCD parallel interface

The XMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.8 Nested vectored interrupt controller (NVIC)

The AT32F403 embed a nested vectored interrupt controller able to manage 16 priority levels and handle up to 68 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.9 External interrupt/event controller (EXTI)

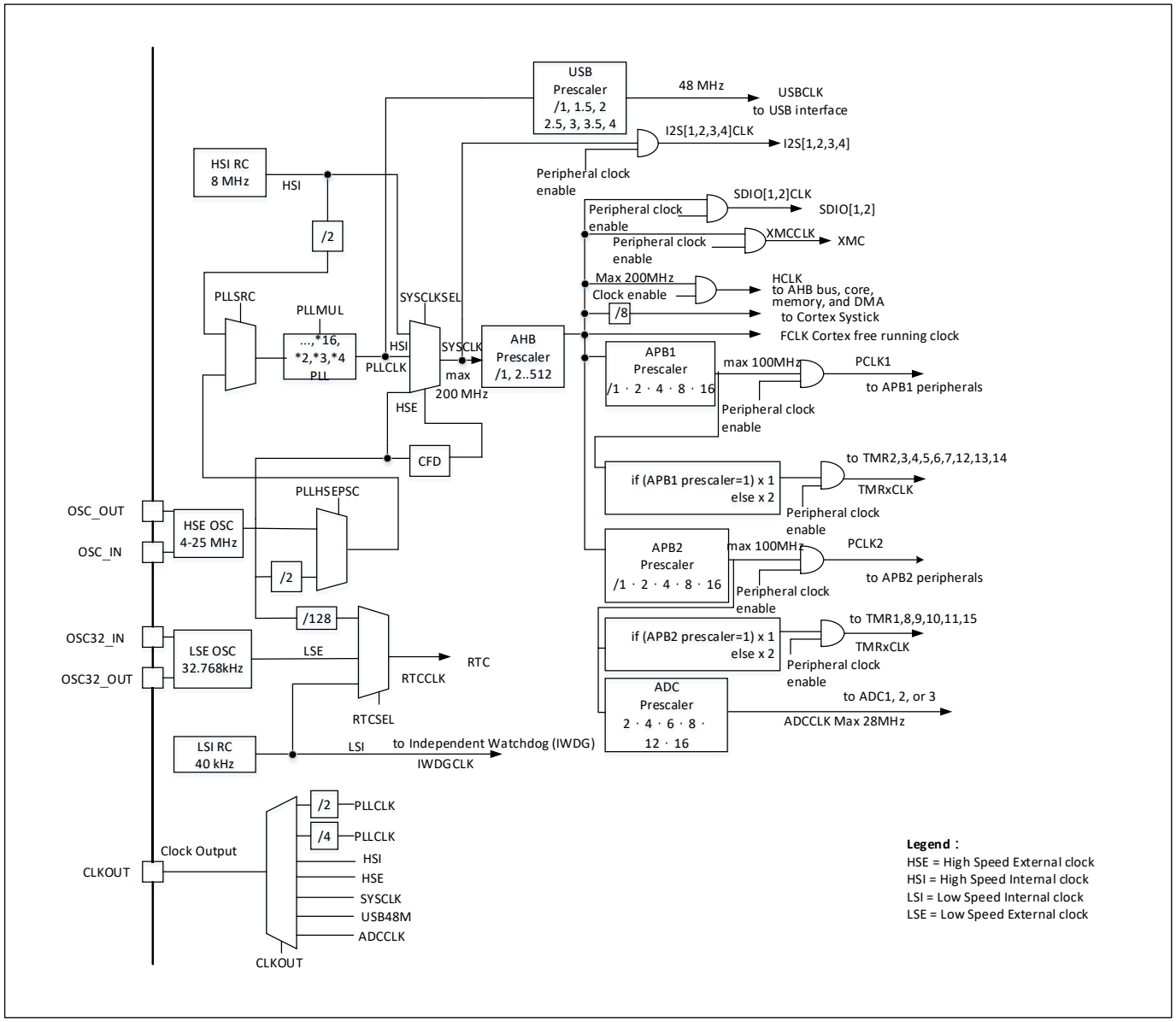
The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.2.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-25 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 200 MHz. The maximum allowed frequency of the APB domains are 100 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



(1) When using USB function, PLLCLK frequency must be 48 MHz, 72 MHz, 96 MHz, 120 MHz, 144 MHz, 168 MHz, or 192 MHz.

2.2.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash. For the AT32F403xG, user has an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. User can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is stored in system memory. It is used to reprogram the Flash memory through USART1, USART2, or USB. Because of the pin multiplex of USB and SPIM, the Flash memory Bank 3 cannot be reprogrammed through USB. *Table 3* provides the supporting interfaces of the Bootloader to different AT32F403 part numbers and pin configurations.

Table 3. The Bootloader supporting part numbers and pin configurations

Interface	Part number	Pin
USART1	All part numbers	PA9: USART1_TX PA10: USART1_RX
USART2	AT32F403ZGT6 and AT32F403VGT6	PD5: USART2_TX (remapped) PD6: USART2_RX (remapped)
	Part numbers except AT32F403ZGT6 and AT32F403VGT6	PA2: USART2_TX(1) PA3: USART2_RX(1)
USB	All part numbers	PA11: USB_DM PA12: USB_DP

(1) Note that pins used are not 5 V tolerant.

2.2.12 Power supply schemes

- V_{DD} = 2.6～3.6 V: external power supply for I/Os and the internal regulator provided externally through V_{DD} pins.
- V_{DDA} = 2.6～3.6 V: external analog power supplies for ADC and DAC. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 2.6～3.6 V: V_{BAT} must be connected to V_{DD}.

For more detail on how to connect power pins, refer to *Figure 11.*

2.2.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12* for the characteristic values of $V_{POR/PDR}$ and V_{PVD}.

2.2.14 Voltage regulator

The regulator has two operation modes: main (MR) and power down.

- Main mode (MR) is used in the nominal regulation mode (Run) and in the Stop mode
- Power down mode is used in Standby mode: the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption of the regulator (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.2.15 Low-power modes

The AT32F403 supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator is put in normal mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, or the USB wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.16 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic, and advanced-control timers TMRx, DAC, I^2S, SDIO, and ADC.

2.2.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied with V_{DD}. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator, or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using a divied-by-64 output of TAMPER pin to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.18 Timers and watchdogs

The AT32F403 devices include up to 3 advanced-control timers, up to 10 general-purpose timers, 2 basic timers, 2 watchdog timers, and a SysTick timer.

The table below compares the features of the advanced-control, general-purpose, and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TMR1, TMR8, TMR15	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TMR2, TMR5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR3, TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR9, TMR12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TMR10, TMR11, TMR13, TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TMR6, TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timers (TMR1, TMR8, and TMR15)

The three advanced-control timers (TMR1, TMR8, and TMR15) can each be seen a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR timers which have the same architecture. The advanced-control timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

General-purpose timers (TMRx)

There are 10 synchronizable general-purpose timers embedded in the AT32F403.

- **TMR2, TMR3, TMR4, and TMR5**

  The AT32F403 has 4 full- featured general-purpose timers: TMR2, TMR3, TMR4, and TMR5.The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload up/down counter and a 16-bit prescaler. They all feature four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs.

  The TMR2, TMR3, TMR4, and TMR5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers via the link feature for synchronization or event chaining. In debug mode, their counter can be frozen. Any of these general-purpose timers can be used to generate PWM outputs.

  The TMR2, TMR3, TMR4, and TMR5 are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TMR9 and TMR12**

  TMR9 and TMR12 are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TMR10, TMR11, TMR13, and TMR14**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channels for input capture/output compare, PWM, or one-pulse mode output.

They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

Basic timers (TMR6 and TMR7)

These two timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.19 I²C bus

Up to 3 I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.20 Universal synchronous/asynchronous receiver transmitters (USART)

The AT32F403 embeds 3 universal synchronous/asynchronous receiver transmitters (USART1, USART2, and USART3) and 2 universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability.

3 USARTs and 2 UARTs are able to communicate at speeds of up to 6.25 Mbit/s.

USART1, USART2, and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.2.21 Serial peripheral interface (SPI)

Up to four SPIs are able to communicate up to 50 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.2.22 Inter-integrated sound (I^2S)

Up to four standard I^2S interfaces (multiplexed with SPI) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.2.23 SDIO

Up to two SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different data bus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 50 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different data bus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.2.25 Universal serial bus (USB)

AT32F403 embeds a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL.

2.2.26 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked, if needed, in order to avoid spurious writing to the I/Os registers by following a specific sequence.

2.2.27 ADC (analog to digital converter)

Three 12-bit analog-to-digital converters are embedded into AT32F403 devices and they share up to 21 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hole
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced-control timers (TMR1, TMR8, and TMR15) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.2.28 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the AT32F403. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.29 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.6 V ≤ V_{DDA} ≤ 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.30 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.2.31 Embedded Trace Macrocell (ETM™)

The ARM® Embedded Trace Macrocell (ETM™) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the AT32F403 through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

3 Pinouts and pin descriptions

Figure 3. AT32F403 LQFP144 pinout

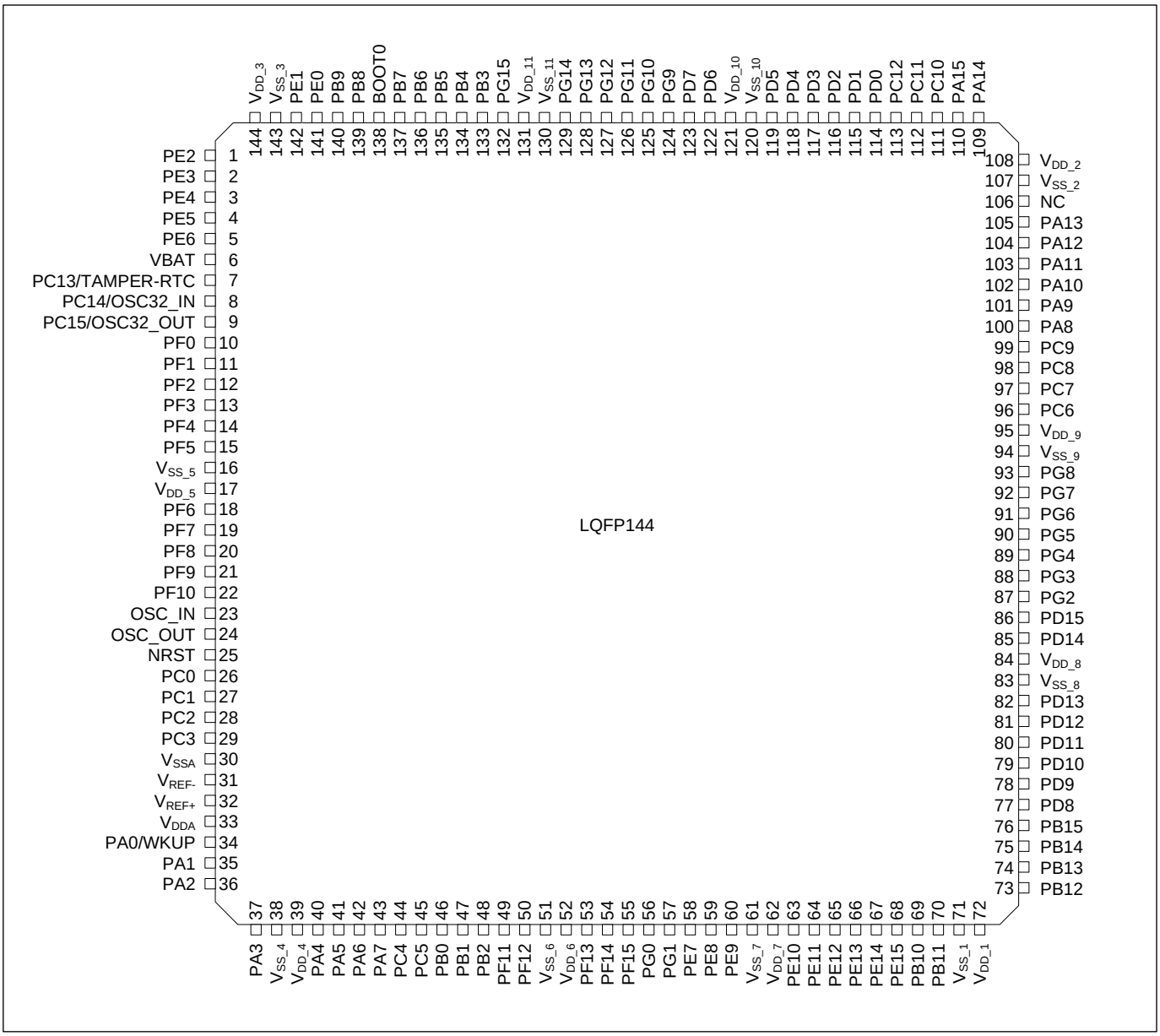


Figure 4. AT32F403 LQFP100 pinout

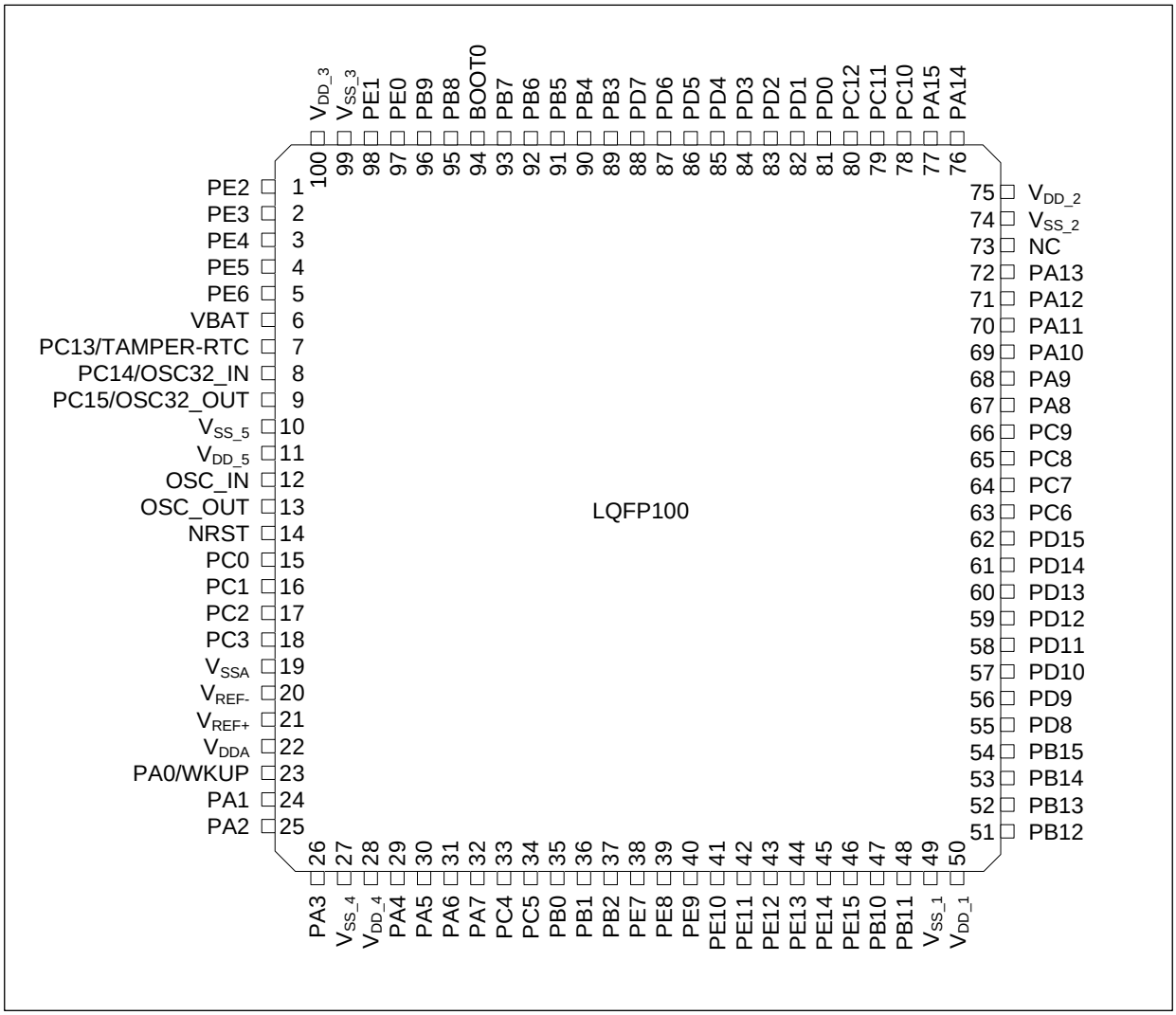


Figure 5. AT32F403 LQFP64 pinout

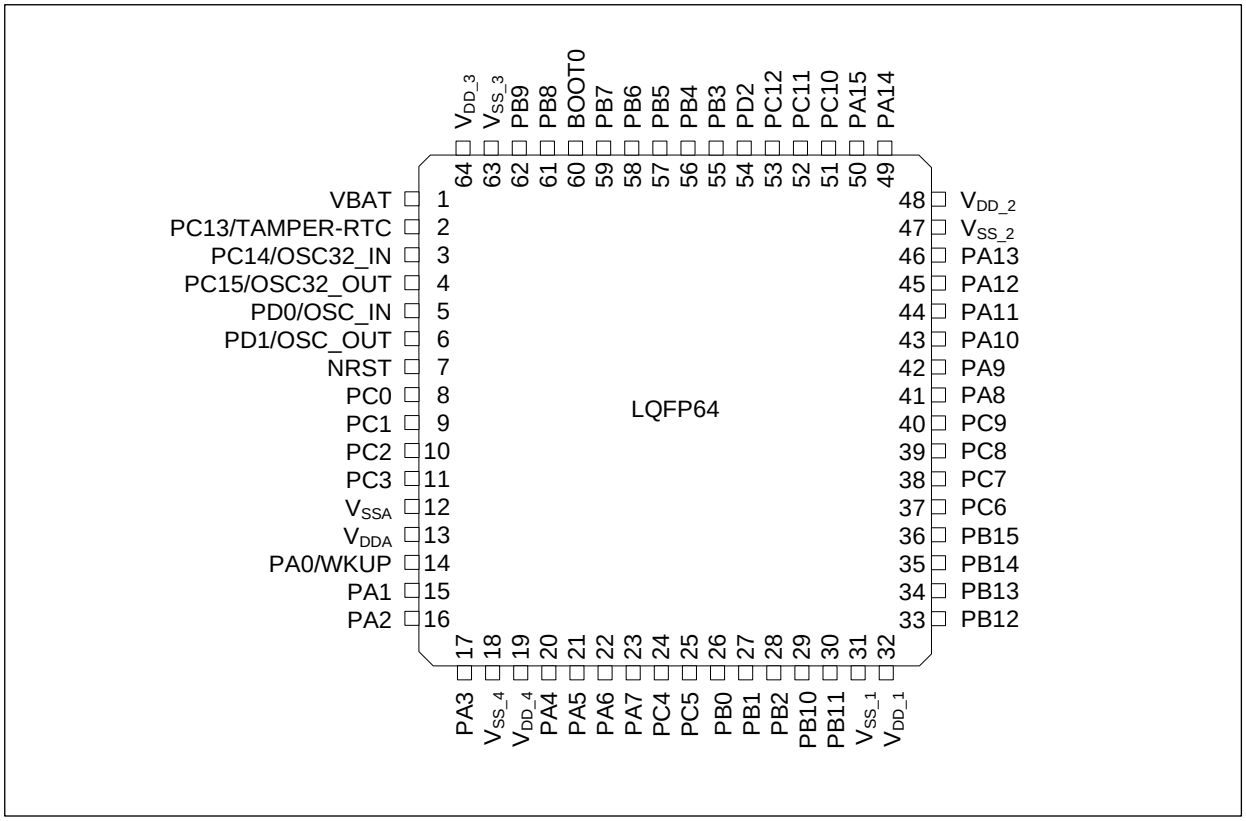


Figure 6. AT32F403 LQFP48 pinout

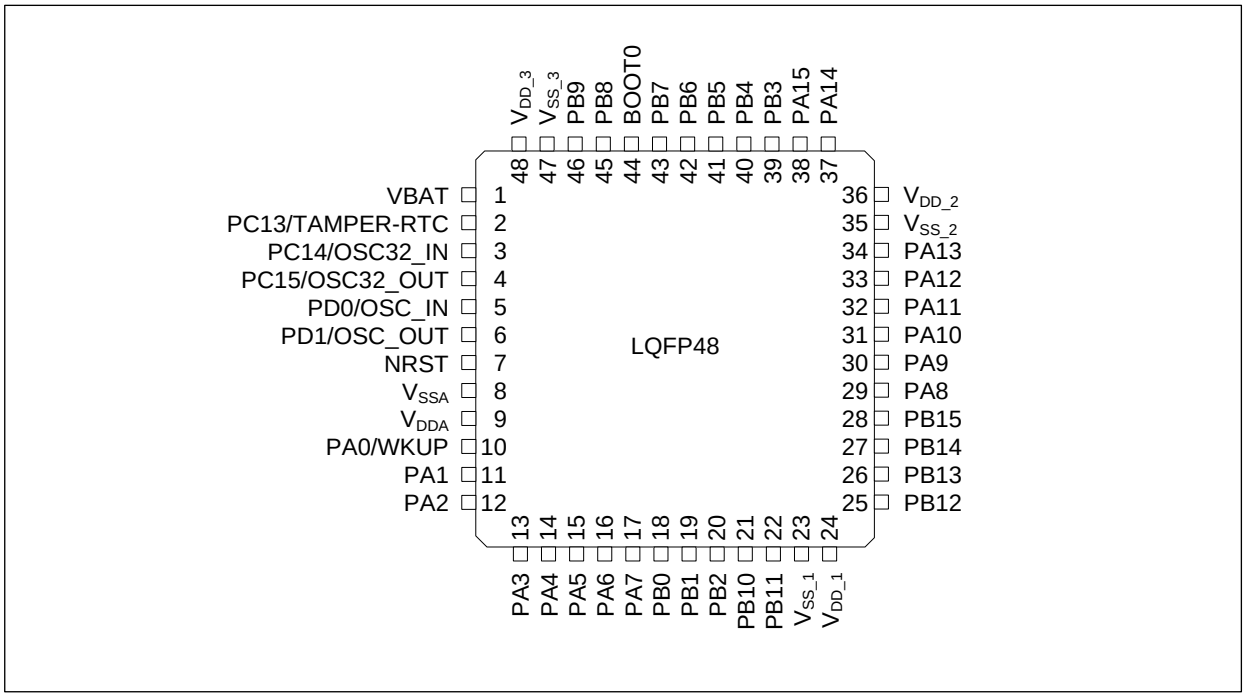
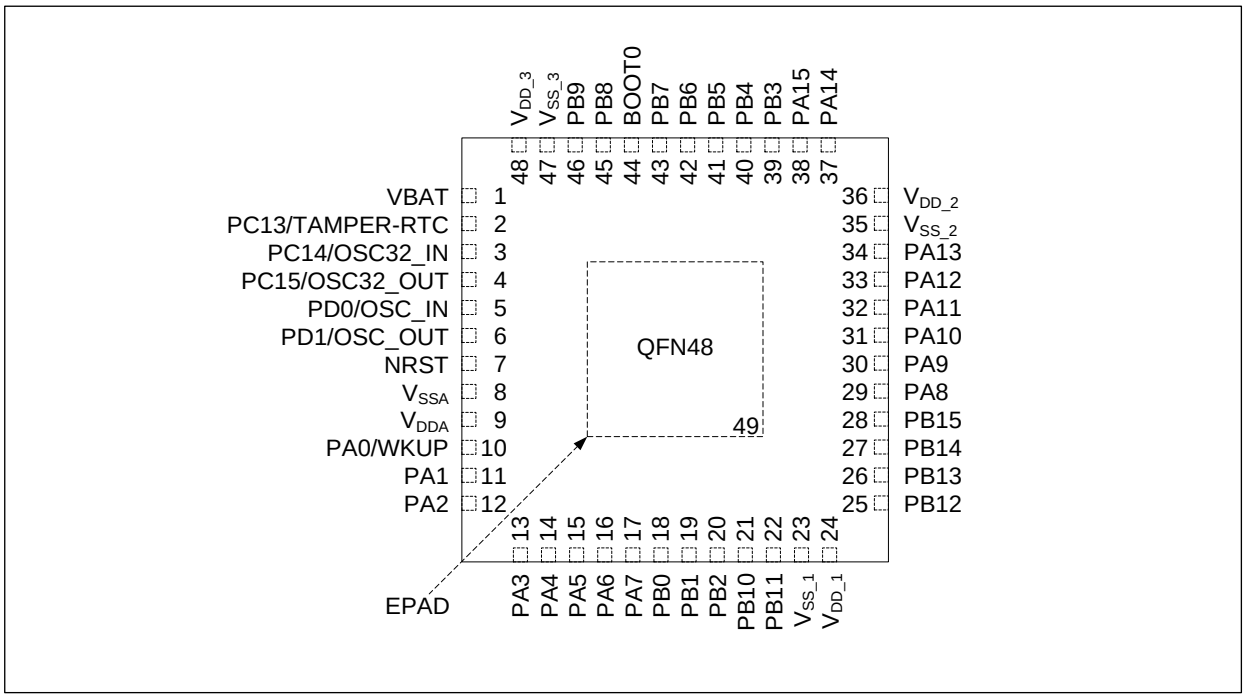


Figure 7. AT32F403 QFN48 pinout



The table below is the pin definition of the AT32F403. ”-” presents there is no such pinout on the related package. The multi-functions list follows priority from high to low. In principle, the analog signals have higher priority than the digital signals, and the digital output signals have higher priority than the digital input signals.

Table 5. AT32F403 series pin definitions

Pin number				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Alternate functions	
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					Default	Remap
-	-	1	1	PE2	I/O	FT	PE2	TRACECK / XMC_A23 / SPI4_SCK / I2S4_CK	-
-	-	2	2	PE3	I/O	FT	PE3	TRACED0 / XMC_A19	-
-	-	3	3	PE4	I/O	FT	PE4	TRACED1 / XMC_A20 / SPI4_NSS / I2S4_WS	-
-	-	4	4	PE5	I/O	FT	PE5	TRACED2 / XMC_A21 / SPI4_MISO	TMR9_CH1
-	-	5	5	PE6	I/O	FT	PE6	TRACED3 / XMC_A22 / SPI4_MOSI / I2S4_SD	TMR9_CH2
1	1	6	6	V_{BAT}(9)	S	-	V_{BAT}	-	-
2	2	7	7	PC13(4)	I/O	-	PC13(5)	TAMPER-RTC	-
3	3	8	8	PC14(4)	I/O	-	PC14(5)	OSC32_IN	-
4	4	9	9	PC15(4)	I/O	-	PC15(5)	OSC32_OUT	-
-	-	-	10	PF0	I/O	FT	PF0	XMC_A0 / TMR15_CH1	-
-	-	-	11	PF1	I/O	FT	PF1	XMC_A1 / TMR15_CH1N	-
-	-	-	12	PF2	I/O	FT	PF2	XMC_A2 / TMR15_CH2	-
-	-	-	13	PF3	I/O	FT	PF3	XMC_A3 / TMR15_CH2N	-
-	-	-	14	PF4	I/O	FT	PF4	XMC_A4 / TMR15_CH3	-
-	-	-	15	PF5	I/O	FT	PF5	XMC_A5 / TMR15_CH3N	-
-	-	10	16	V_{SS_5}	S	-	V_{SS_5}	-	-
-	-	11	17	V_{DD_5}	S	-	V_{DD_5}	-	-
-	-	-	18	PF6	I/O	-	PF6	ADC3_IN4 / XMC_NIORD / TMR15_CH4	TMR10_CH1
-	-	-	19	PF7	I/O	-	PF7	ADC3_IN5 / XMC_NREG / TMR15_ETR	TMR11_CH1
-	-	-	20	PF8	I/O	-	PF8	ADC3_IN6 / XMC_NIOWR / TMR15_BKIN	TMR13_CH1
-	-	-	21	PF9	I/O	-	PF9	ADC3_IN7 / XMC_CD	TMR14_CH1
-	-	-	22	PF10	I/O	-	PF10	ADC3_IN8 / XMC_INTR	-
-	-	12	23	OSC_IN	I	-	OSC_IN	-	-
-	-	13	24	OSC_OUT	O	-	OSC_OUT	-	-
5	5	-	-	PD0(6)	I/O	-	OSC_IN(6)	-	PD0(6)
6	6	-	-	PD1(6)	I/O	-	OSC_OUT(6)	-	PD1(6)
7	7	14	25	NRST	I/O	-	NRST	-	-
-	8	15	26	PC0	I/O	-	PC0	ADC123_IN10 / SDIO2_D0	-
-	9	16	27	PC1	I/O	-	PC1	ADC123_IN11 / SDIO2_D1	-

Pin number				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Alternate functions	
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					Default	Remap
-	10	17	28	PC2	I/O	-	PC2	ADC123_IN12 / SDIO2_D2	-
-	11	18	29	PC3	I/O	-	PC3	ADC123_IN13 / SDIO2_D3	-
8	12	19	30	V_{SSA}	S	-	V_{SSA}	-	-
-	-	20	31	V_{REF-}	S	-	V_{REF-}	-	-
-	-	21	32	V_{REF+}	S	-	V_{REF+}	-	-
9	13	22	33	V_{DDA}	S	-	V_{DDA}	-	-
10	14	23	34	PA0-WKUP	I/O	-	PA0	ADC123_IN0 / TMR2_CH1 / TMR5_CH1 / WKUP / USART2_CTS(7) / TMR2_ETR / TMR8_ETR	-
11	15	24	35	PA1	I/O	-	PA1	ADC123_IN1 / TMR2_CH2(7) / TMR5_CH2 / USART2_RTS(7)	-
12	16	25	36	PA2	I/O	-	PA2	ADC123_IN2 / TMR2_CH3(7) / TMR5_CH3 / TMR9_CH1 / USART2_TX(7)	SDIO2_CK
13	17	26	37	PA3	I/O	-	PA3	ADC123_IN3 / TMR2_CH4(7) / TMR5_CH4 / TMR9_CH2 / USART2_RX(7)	SDIO2_CMD
-	18	27	38	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	28	39	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	29	40	PA4	I/O	-	PA4	DAC_OUT1 / ADC12_IN4 / USART2_CK(7) / SPI1_NSS(7) / I2S1_WS / SDIO2_D4	SDIO2_D0
15	21	30	41	PA5	I/O	-	PA5	DAC_OUT2 / ADC12_IN5 / SPI1_SCK(7) / I2S1_CK / SDIO2_D5	SDIO2_D1
16	22	31	42	PA6	I/O	-	PA6	ADC12_IN6 / TMR3_CH1(7) / TMR13_CH1 / SPI1_MISO(7) / SDIO2_D6 / TMR8_BKIN	SDIO2_D2 / TMR1_BKIN
17	23	32	43	PA7	I/O	-	PA7	ADC12_IN7 / TMR3_CH2(7) / TMR8_CH1N / TMR14_CH1 / SPI1_MOSI(7) / I2S1_SD / SDIO2_D7	TMR1_CH1N / SDIO2_D3
-	24	33	44	PC4	I/O	-	PC4	ADC12_IN14 / SDIO2_CK	-
-	25	34	45	PC5	I/O	-	PC5	ADC12_IN15 / SDIO2_CMD	-
18	26	35	46	PB0	I/O	-	PB0	ADC12_IN8 / TMR3_CH3 / TMR8_CH2N / I2S1_MCK	TMR1_CH2N
19	27	36	47	PB1	I/O	-	PB1	ADC12_IN9 / TMR3_CH4(7) / TMR8_CH3N / SPIM_SCK	TMR1_CH3N
20	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
-	-	-	49	PF11	I/O	FT	PF11	XMC_NIOS16	-
-	-	-	50	PF12	I/O	FT	PF12	XMC_A6	-
-	-	-	51	V_{SS_6}	S	-	V_{SS_6}	-	-
-	-	-	52	V_{DD_6}	S	-	V_{DD_6}	-	-

Pin number				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Alternate functions	
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					Default	Remap
-	-	-	53	PF13	I/O	FT	PF13	XMC_A7	TMR15_CH4
-	-	-	54	PF14	I/O	FT	PF14	XMC_A8	TMR15_ETR
-	-	-	55	PF15	I/O	FT	PF15	XMC_A9	TMR15_BKIN
-	-	-	56	PG0	I/O	FT	PG0	XMC_A10	SPI1_MISO
-	-	-	57	PG1	I/O	FT	PG1	XMC_A11	SPI1_MOSI / I2S1_SD
-	-	38	58	PE7	I/O	FT	PE7	XMC_D4	TMR1_ETR
-	-	39	59	PE8	I/O	FT	PE8	XMC_D5	TMR1_CH1N
-	-	40	60	PE9	I/O	FT	PE9	XMC_D6	TMR1_CH1
-	-	-	61	V_{SS_7}	S	-	V_{SS_7}	-	-
-	-	-	62	V_{DD_7}	S	-	V_{DD_7}	-	-
-	-	41	63	PE10	I/O	FT	PE10	XMC_D7	TMR1_CH2N
-	-	42	64	PE11	I/O	FT	PE11	XMC_D8	TMR1_CH2 / SPI4_SCK / I2S4_CK
-	-	43	65	PE12	I/O	FT	PE12	XMC_D9	TMR1_CH3N / SPI4_NSS / I2S4_WS
-	-	44	66	PE13	I/O	FT	PE13	XMC_D10	TMR1_CH3 / SPI4_MISO
-	-	45	67	PE14	I/O	FT	PE14	XMC_D11	TMR1_CH4 / SPI4_MOSI / I2S4_SD
-	-	46	68	PE15	I/O	FT	PE15	XMC_D12	TMR1_BKIN
21	29	47	69	PB10	I/O	FT	PB10	USART3_TX(7) / I2C2_SCL	TMR2_CH3
22	30	48	70	PB11	I/O	FT	PB11	USART3_RX(7) / I2C2_SDA	TMR2_CH4
23	31	49	71	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	50	72	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	51	73	PB12	I/O	FT	PB12	USART3_CK(7) / I2C2_SMBA / SPI2_NSS / I2S2_WS / TMR1_BKIN(7)	-
26	34	52	74	PB13	I/O	FT	PB13	TMR1_CH1N / SPI2_SCK / I2S2_CK / USART3_CTS(7)	-
27	35	53	75	PB14	I/O	FT	PB14	TMR1_CH2N / TMR12_CH1 / USART3_RTS(7) / SPI2_MISO	-
28	36	54	76	PB15	I/O	FT	PB15	TMR1_CH3N(7) / TMR12_CH2 / SPI2_MOSI / I2S2_SD	-
-	-	55	77	PD8	I/O	FT	PD8	XMC_D13	USART3_TX
-	-	56	78	PD9	I/O	FT	PD9	XMC_D14	USART3_RX
-	-	57	79	PD10	I/O	FT	PD10	XMC_D15	USART3_CK
-	-	58	80	PD11	I/O	FT	PD11	XMC_A16	USART3_CTS
-	-	59	81	PD12	I/O	FT	PD12	XMC_A17	TMR4_CH1 / USART3_RTS
-	-	60	82	PD13	I/O	FT	PD13	XMC_A18	TMR4_CH2

Pin number				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Alternate functions	
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					Default	Remap
-	-	-	83	V_{SS_8}	S	-	V_{SS_8}	-	-
-	-	-	84	V_{DD_8}	S	-	V_{DD_8}	-	-
-	-	61	85	PD14	I/O	FT	PD14	XMC_D0	TMR4_CH3
-	-	62	86	PD15	I/O	FT	PD15	XMC_D1	TMR4_CH4
-	-	-	87	PG2	I/O	FT	PG2	XMC_A12	TMR15_CH1
-	-	-	88	PG3	I/O	FT	PG3	XMC_A13	TMR15_CH1N
-	-	-	89	PG4	I/O	FT	PG4	XMC_A14	TMR15_CH2
-	-	-	90	PG5	I/O	FT	PG5	XMC_A15	TMR15_CH2N
-	-	-	91	PG6	I/O	FT	PG6	XMC_INT2	TMR15_CH3
-	-	-	92	PG7	I/O	FT	PG7	XMC_INT3	TMR15_CH3N
-	-	-	93	PG8	I/O	FT	PG8	-	-
-	-	-	94	V_{SS_9}	S	-	V_{SS_9}	-	-
-	-	-	95	V_{DD_9}	S	-	V_{DD_9}	-	-
-	37	63	96	PC6	I/O	FT	PC6	TMR8_CH1 / I2S2_MCK / SDIO1_D6	TMR3_CH1
-	38	64	97	PC7	I/O	FT	PC7	TMR8_CH2 / I2S3_MCK / SDIO1_D7	TMR3_CH2
-	39	65	98	PC8	I/O	FT	PC8	TMR8_CH3 / SDIO1_D0 / I2S4_MCK	TMR3_CH3
-	40	66	99	PC9	I/O	FT	PC9	TMR8_CH4 / SDIO1_D1 / I2C3_SDA	TMR3_CH4
29	41	67	100	PA8	I/O	FT	PA8	TMR1_CH1(7) / CLKOUT / USART1_CK / I2C3_SCL / SPIM_NSS	-
30	42	68	101	PA9	I/O	FT	PA9	TMR1_CH2(7) / USART1_TX(7) / I2C3_SMBA	-
31	43	69	102	PA10	I/O	FT	PA10	TMR1_CH3(7) / USART1_RX(7)	-
32	44	70	103	PA11	I/O	-	PA11	USB_DM(8) / TMR1_CH4(7) / SPIM_IO0(8) / USART1_CTS / CAN_RX(7)	-
33	45	71	104	PA12	I/O	-	PA12	USB_DP(8) / CAN_TX(7) / USART1_RTS / SPIM_IO1(8) / TMR1_ETR(7)	-
34	46	72	105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	-	73	106	Not connected					
35	47	74	107	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	75	108	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	76	109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
38	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS / I2S3_WS	PA15 / TMR2_CH1 / SPI1_NSS / I2S1_WS / TMR2_ETR

Pin number				Pin name	Type[1]	IO level[2]	Main function[3] (after reset)	Alternate functions	
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					Default	Remap
-	51	78	111	PC10	I/O	FT	PC10	UART4_TX / SDIO1_D2	USART3_TX
-	52	79	112	PC11	I/O	FT	PC11	UART4_RX / SDIO1_D3	USART3_RX
-	53	80	113	PC12	I/O	FT	PC12	UART5_TX / SDIO1_CK	USART3_CK
-	-	81	114	PD0	I/O	FT	PD0	XMC_D2	CAN_RX
-	-	82	115	PD1	I/O	FT	PD1	XMC_D3	CAN_TX
-	54	83	116	PD2	I/O	FT	PD2	SDIO1_CMD / UART5_RX / TMR3_ETR	-
-	-	84	117	PD3	I/O	FT	PD3	XMC_CLK	USART2_CTS
-	-	85	118	PD4	I/O	FT	PD4	XMC_NOE	USART2_RTS
-	-	86	119	PD5	I/O	FT	PD5	XMC_NWE	USART2_TX
-	-	-	120	V_{SS_10}	S	-	V_{SS_10}	-	-
-	-	-	121	V_{DD_10}	S	-	V_{DD_10}	-	-
-	-	87	122	PD6	I/O	FT	PD6	XMC_NWAIT	USART2_RX
-	-	88	123	PD7	I/O	FT	PD7	XMC_NCE2 / XMC_NE1	USART2_CK
-	-	-	124	PG9	I/O	FT	PG9	XMC_NCE3 / XMC_NE2	-
-	-	-	125	PG10	I/O	FT	PG10	XMC_NCE4_1 / XMC_NE3	-
-	-	-	126	PG11	I/O	FT	PG11	XMC_NCE4_2	-
-	-	-	127	PG12	I/O	FT	PG12	XMC_NE4	-
-	-	-	128	PG13	I/O	FT	PG13	XMC_A24	-
-	-	-	129	PG14	I/O	FT	PG14	XMC_A25	-
-	-	-	130	V_{SS_11}	S	-	V_{SS_11}	-	-
-	-	-	131	V_{DD_11}	S	-	V_{DD_11}	-	-
-	-	-	132	PG15	I/O	FT	PG15	-	-
39	55	89	133	PB3	I/O	FT	JTDO	SPI3_SCK / I2S3_CK	PB3 / TRACESWO / TMR2_CH2 / SPI1_SCK / I2S1_CK
40	56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TMR3_CH1 / SPI1_MISO / I2C3_SDA
41	57	91	135	PB5	I/O	-	PB5	I2C1_SMBA / SPI3_MOSI / I2S3_SD	TMR3_CH2 / SPI1_MOSI / I2S1_SD
42	58	92	136	PB6	I/O	FT	PB6	TMR4_CH1[7] / I2C1_SCL[7] / SPIM_IO3	USART1_TX
43	59	93	137	PB7	I/O	FT	PB7	TMR4_CH2[7] / I2C1_SDA[7] / XMC_NADV / SPIM_IO2	USART1_RX
44	60	94	138	BOOT0	I	-	BOOT0	-	-
45	61	95	139	PB8	I/O	FT	PB8	TMR4_CH3[7] / TMR10_CH1 / SDIO1_D4	CAN_RX / I2C1_SCL
46	62	96	140	PB9	I/O	FT	PB9	TMR4_CH4[7] / TMR11_CH1 / SDIO1_D5	CAN_TX / I2C1_SDA
-	-	97	141	PE0	I/O	FT	PE0	XMC_NBL0 / TMR4_ETR	-

Pin number				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Alternate functions	
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					Default	Remap
-	-	98	142	PE1	I/O	FT	PE1	XMC_NBL1	-
47	63	99	143	V_{SS_3}	S	-	V_{SS_3}	-	-
48	64	100	144	V_{DD_3}	S	-	V_{DD_3}	-	-
-/49	-	-	-	EPAD	S	-	V_{SS}	-	-

(1) I = input, O = output, S = supply.

(2) FT = 5 V tolerant.

(3) Function availability depends on the chosen device.

(4) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the normal sourcing/sinking strength should be used with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

(5) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the AT32F403 reference manual.

(6) For the LQFP64, LQFP48, and QFN48 packages, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, the functionality of PD0 and PD1 can be remapped by software on these pins. However, for the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the AT32F403 reference manual.

(7) This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the AT32F403 reference manual.

(8) SPIM and USB interfaces cannot be used simultaneously because they are multi-functions with PA11 and PA12.

(9) V_{BAT} pin must be connected with V_{DD}. AT32F403 does not support individual V_{BAT} power supplying.

Table 6. XMC pin definition

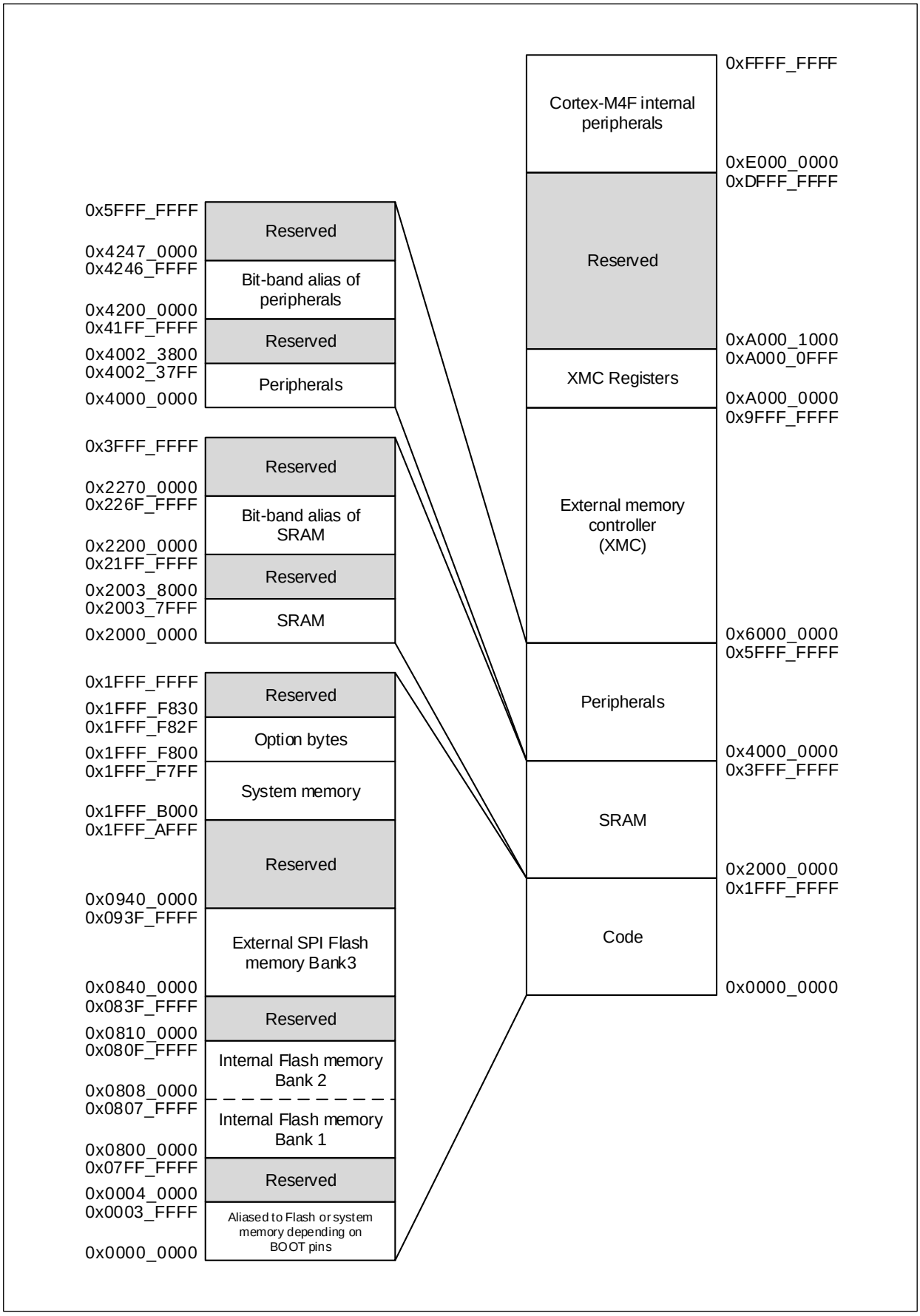
Pins	XMC					LQFP100[1]
	CF	CF / IDE	NOR / PSRAM / SRAM	NOR / PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes

Pins	XMC					LQFP100(1)
	CF	CF / IDE	NOR / PSRAM / SRAM	NOR / PSRAM Mux	NAND 16 bit	
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18	-	Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

(1) Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

Figure 8. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production with an ambient temperature at T_A = 25 °C and T_A = T_A max.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V. They are given only as design guidelines and are not tested.

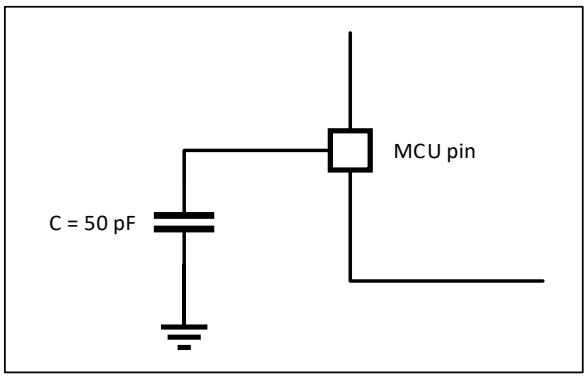
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

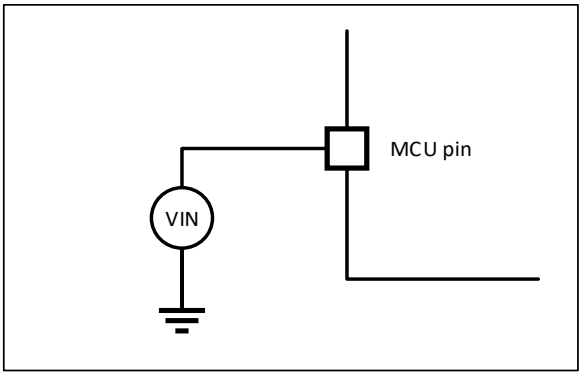
Figure 9. Pin loading conditions



5.1.5 Pin input voltage

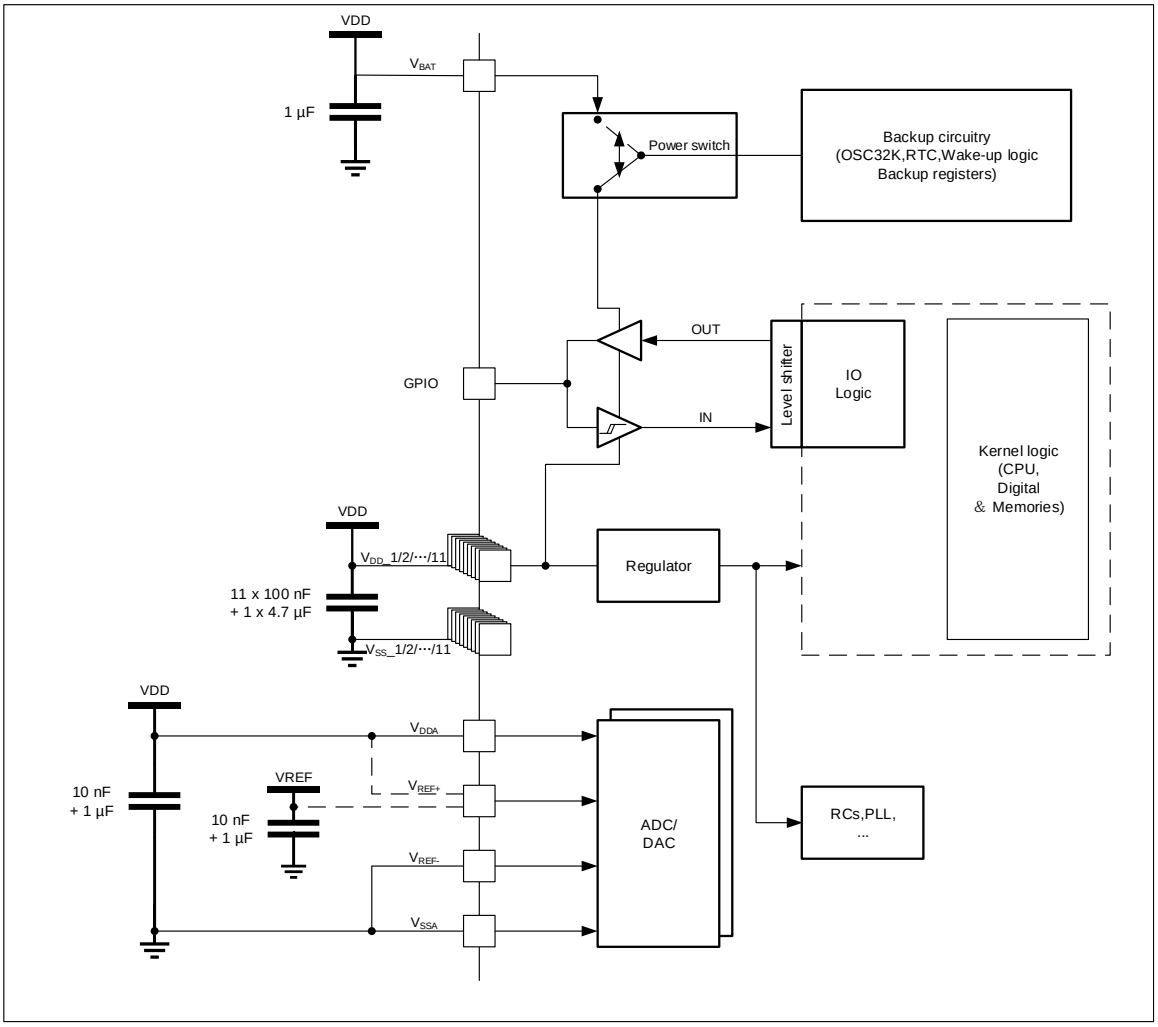
The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



5.1.6 Power supply scheme

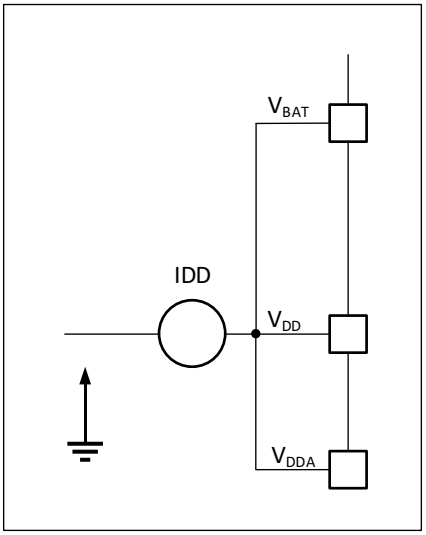
Figure 11. Power supply scheme



Caution: In this figure, the 4.7µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7*, *Table 8*, and *Table 9* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin (2)	V_{SS}-0.3	6.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins (2)	-	50	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
(2) V_{REF-} included.

Table 8. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) (1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) (1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	105	

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Bank 3 not used	0	200	MHz
		Bank 3 used	0	120	
f_{PCLK1}	Internal APB1 clock frequency	-	0	100	
f_{PCLK2}	Internal APB2 clock frequency	-	0	100	
V_{DD}	Standard operating voltage	-	2.6	3.6	V
V_{DDA}(1)	Analog operating voltage	Must be the same potential as V_{DD}(1)	2.6	3.6	V
V_{BAT}	Backup operating voltage	Must be connected with V_{DD}	2.6	3.6	V
P_D	Power dissipation: T_A = 85 °C	LQFP144	-	413	mW
		LQFP100	-	380	
		LQFP64	-	358	
		LQFP48	-	314	
		QFN48	-	733	
T_A	Ambient temperature	-	-40	85	°C

(1) It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Operating conditions at power-up / power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in *Table 10*.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	180	ms/V
	V_{DD} fall time rate		20	∞	μs/V

5.3.3 Embedded reset and power control block characteristics

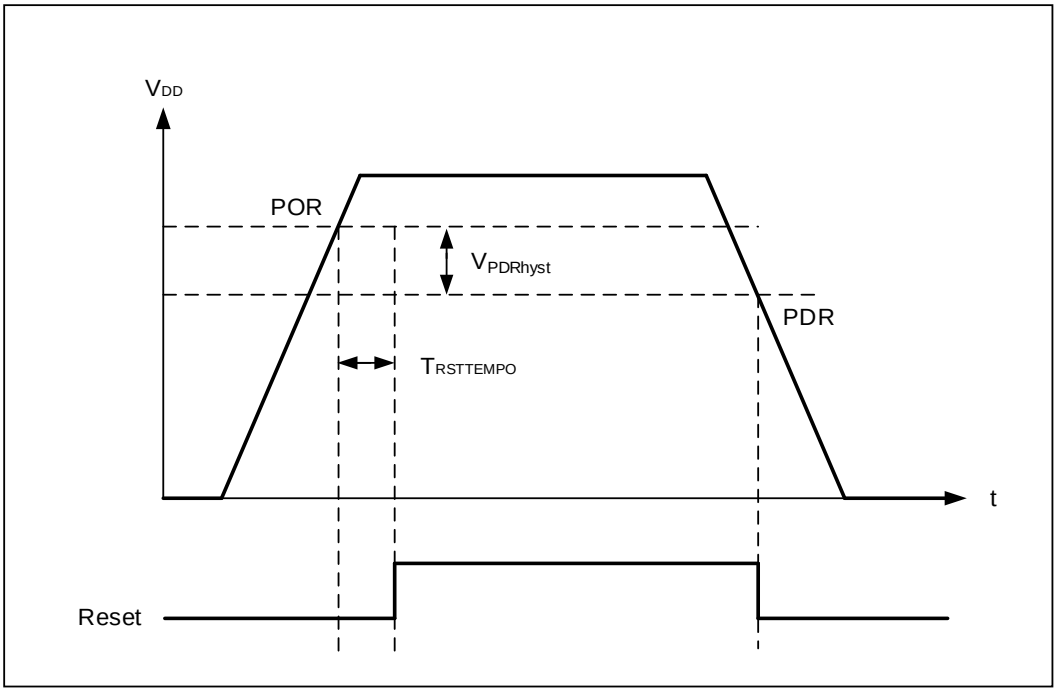
The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0] = 001 (rising edge)(1)	2.19	2.28	2.37	V
		PLS[2:0] = 001 (falling edge)(1)	2.09	2.18	2.27	V
		PLS[2:0] = 010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0] = 010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0] = 011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0] = 011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0] = 100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0] = 100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0] = 101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0] = 101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0] = 110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0] = 110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0] = 111 (rising edge)	2.76	2.88	3	V
		PLS[2:0] = 111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.85(3)	2.0	2.2	V
		Rising edge	2.03	2.16	2.35	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	160	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	-	20	-	ms

(1) PLS[2:0] = 001 may be not available for its voltage detector level may be lower than $V_{POR/PDR}$.
(2) Guaranteed by design, not tested in production.
(3) The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

Figure 13. Power on reset/power down reset waveform



5.3.4 Embedded reference voltage

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 13. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
T_{Coeff}(2)	Temperature coefficient	-	-	-	120	ppm/°C

(1) Shortest sampling time can be determined in the application by multiple iterations.
(2) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, and executed binary code.

The current consumption is measured as described in *Figure 12*.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling
- When the peripherals are enabled:
  - $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$ if $f_{HCLK} > 100$ MHz
  - $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$ if $f_{HCLK} \leq 100$ MHz
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 14. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled (2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	200 MHz	76.1	38.6	mA
			144 MHz	55.5	28.3	
			100 MHz	45.4	20.6	
			72 MHz	33.7	15.8	
			48 MHz	23.1	11.1	
			36 MHz	17.7	8.80	
			24 MHz	12.4	6.51	
			16 MHz	8.94	4.99	
			8 MHz	4.96	3.00	
			4 MHz	3.30	2.31	
			2 MHz	2.47	1.94	
			1 MHz	2.06	1.81	
			500 kHz	1.85	1.71	
			125 kHz	1.70	1.66	
		Running on high speed internal RC (HSI)	200 MHz	76.0	38.5	mA
			144 MHz	55.3	28.1	
			100 MHz	45.3	20.4	
			72 MHz	33.5	15.6	
			48 MHz	22.9	10.9	
			36 MHz	17.5	8.57	
			24 MHz	12.2	6.27	
			16 MHz	8.70	4.73	
			8 MHz	4.71	2.75	
			4 MHz	3.05	2.07	
			2 MHz	2.21	1.73	
			1 MHz	1.80	1.56	
			500 kHz	1.59	1.47	
			125 kHz	1.44	1.41	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(2) Add an additional power consumption of 0.4 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADCx_CTRL2 register).
(3) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Table 15. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled (2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	200 MHz	64.0	15.6	mA
			144 MHz	46.7	11.8	
			100 MHz	33.0	8.74	
			72 MHz	24.7	7.24	
			48 MHz	17.1	5.46	
			36 MHz	13.3	4.58	
			24 MHz	9.46	3.71	
			16 MHz	6.95	3.13	
			8 MHz	3.97	2.08	
			4 MHz	2.81	1.86	
			2 MHz	2.23	1.76	
			1 MHz	1.94	1.70	
			500 kHz	1.79	1.67	
			125 kHz	1.68	1.65	
		Running on high speed internal RC (HSI)	200 MHz	63.9	15.3	mA
			144 MHz	46.6	11.5	
			100 MHz	32.8	8.51	
			72 MHz	24.5	6.99	
			48 MHz	16.9	5.21	
			36 MHz	13.0	4.33	
			24 MHz	9.22	3.45	
			16 MHz	6.70	2.87	
			8 MHz	3.72	1.82	
			4 MHz	2.55	1.60	
			2 MHz	1.97	1.50	
			1 MHz	1.68	1.44	
			500 kHz	1.53	1.42	
			125 kHz	1.42	1.40	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(2) Add an additional power consumption of 0.4 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADCx_CTRL2 register).
(3) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling
- When the peripherals are enabled:
  - $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$ if $f_{HCLK} > 100$ MHz
  - $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$ if $f_{HCLK} \leq 100$ MHz

The parameters given in *Table 16* and *Table 17* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 16. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	200 MHz	83.5	mA
			144 MHz	62.5	
			100 MHz	52.4	
			72 MHz	40.4	
			48 MHz	29.9	
			36 MHz	24.3	
			24 MHz	18.9	
			16 MHz	15.4	
			8 MHz	11.3	
		External clock(2), all peripherals disabled	200 MHz	45.2	mA
			144 MHz	34.8	
			100 MHz	27.1	
			72 MHz	22.2	
			48 MHz	17.5	
			36 MHz	15.2	
			24 MHz	12.8	
			16 MHz	11.5	
			8 MHz	9.26	

(1) Guaranteed by characterization results, not tested in production.
(2) External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 17. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	200 MHz	71.3	mA
			144 MHz	53.7	
			100 MHz	39.9	
			72 MHz	31.4	
			48 MHz	23.7	
			36 MHz	19.8	
			24 MHz	16.0	
			16 MHz	13.4	
			8 MHz	10.4	
		External clock(2), all peripherals disabled	200 MHz	22.0	mA
			144 MHz	18.1	
			100 MHz	15.2	
			72 MHz	13.5	
			48 MHz	11.8	
			36 MHz	10.9	
			24 MHz	10.0	
			16 MHz	9.72	
			8 MHz	8.38	

(1) Guaranteed by characterization results, not tested in production.
(2) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Table 18. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max	Unit
			V_{DD}/V_{BAT} = 2.6 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	940	1000	9000	µA
	Supply current in Standby mode	Low-speed oscillator and RTC OFF	7.7	10.4	17.5(2)	µA
		Low-speed oscillator and RTC ON	8.4	11.9	18.7(2)	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 14. Typical current consumption in Stop mode versus temperature at different V_{DD}

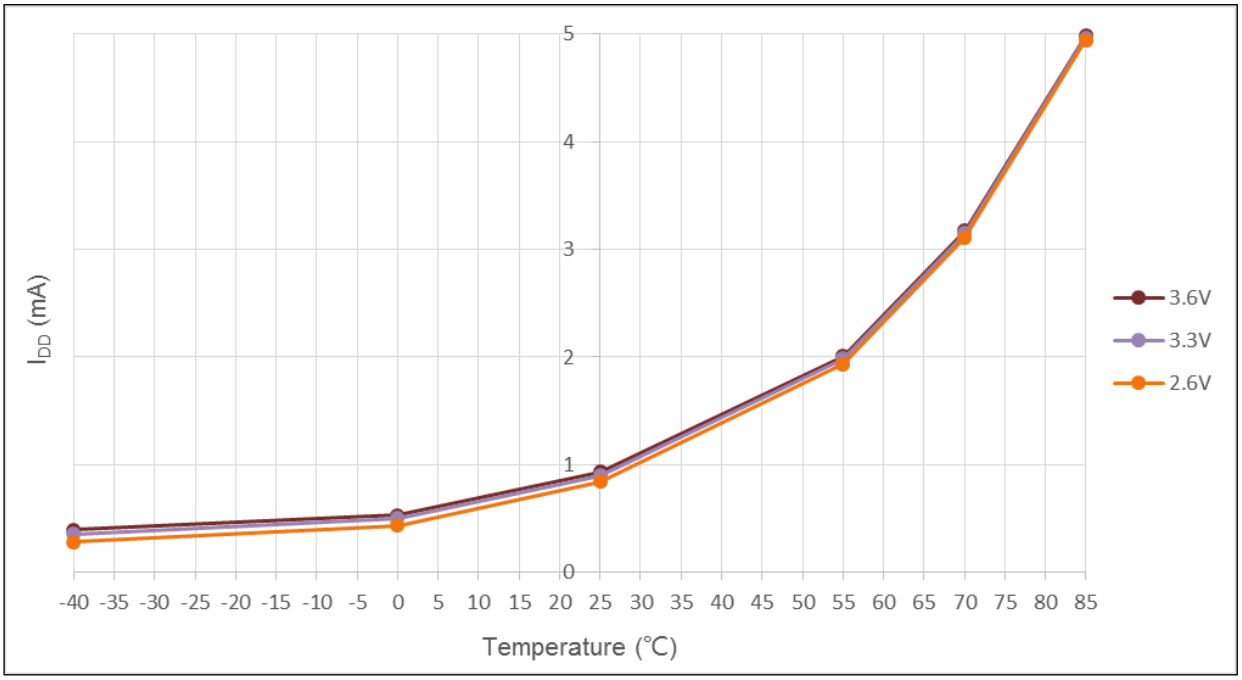
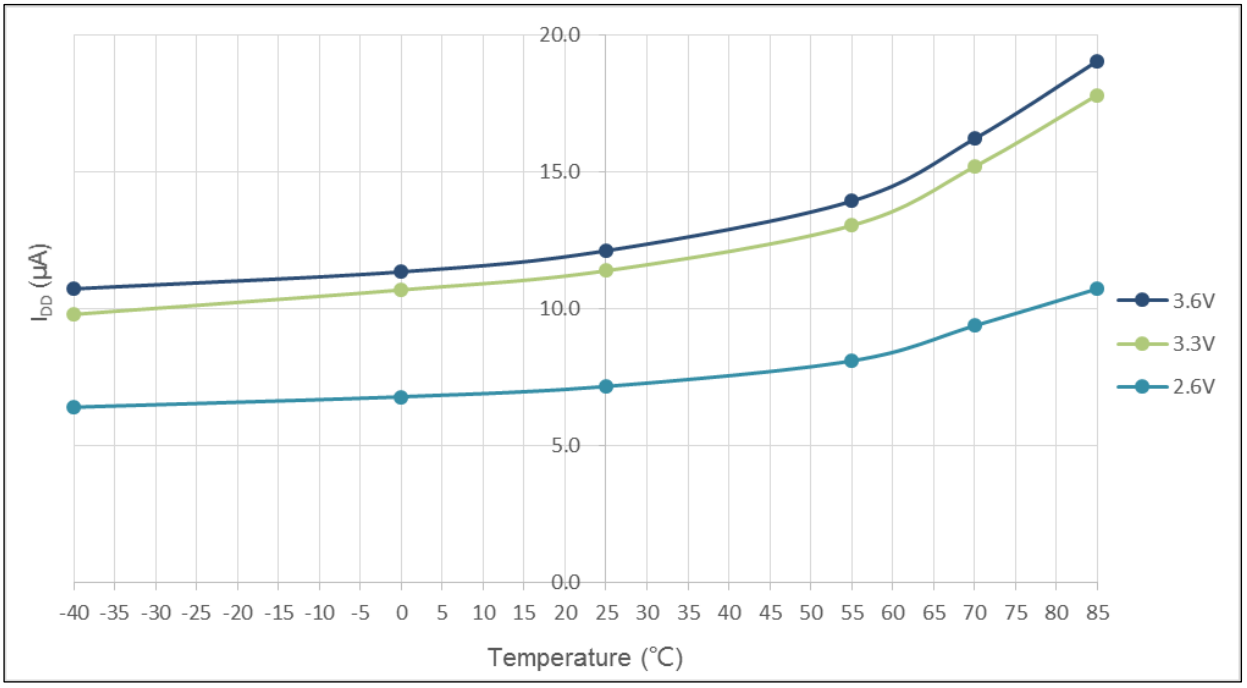


Figure 15. Typical current consumption in Standby mode versus temperature at different V_{DD}



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 19. Peripheral current consumption

Peripheral		Typ	Unit
AHB (up to 200 MHz)	DMA1	8.60	μA/MHz
	DMA2	9.17	
	XMC	26.9	
	CRC	1.55	
	SDIO1	19.2	
	SDIO2	19.4	
APB1 (up to 100 MHz)	TMR2	5.92	
	TMR3	4.54	
	TMR4	4.40	
	TMR5	6.06	
	TMR6	0.78	
	TMR7	0.80	
	TMR12	3.28	
	TMR13	2.81	
	TMR14	2.84	
	SPI2/I²S2	2.53	
	SPI3/I²S3	2.52	
	SPI4/I²S4	2.61	
	USART2	2.70	
	USART3	2.73	
	UART4	2.70	
	UART5	2.54	
	I²C1	2.42	
	I²C2	2.43	
	I²C3	2.44	
	USB	6.56	
	CAN	4.82	
	DAC(1)	2.55	
	WWDG	0.44	
	PWR	0.54	
	BKP	31.9	

Peripheral		Typ	Unit
APB2 (up to 100 MHz)	AFIO	0.92	μA/MHz
	GPIOA	0.99	
	GPIOB	0.97	
	GPIOC	0.99	
	GPIOD	0.94	
	GPIOE	1.02	
	GPIOF	1.02	
	GPIOG	1.02	
	SPI1/I^2S1	2.65	
	USART1	2.52	
	TMR1	5.28	
	TMR8	5.36	
	TMR9	3.40	
	TMR10	2.90	
	TMR11	2.80	
	TMR15	5.18	
	ADC1(2)	6.43	
	ADC2(2)	5.91	
	ADC3(2)	5.95	

(1) When DAC_OUT1 or DAC_OUT2 is enabled, a current consumption equal to 0.8 mA must be added.
(2) When ADON bit in the ADCx_CTRL2 register is set to 1, a current consumption of analog part equal to 0.4 mA must be added for each ADC.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

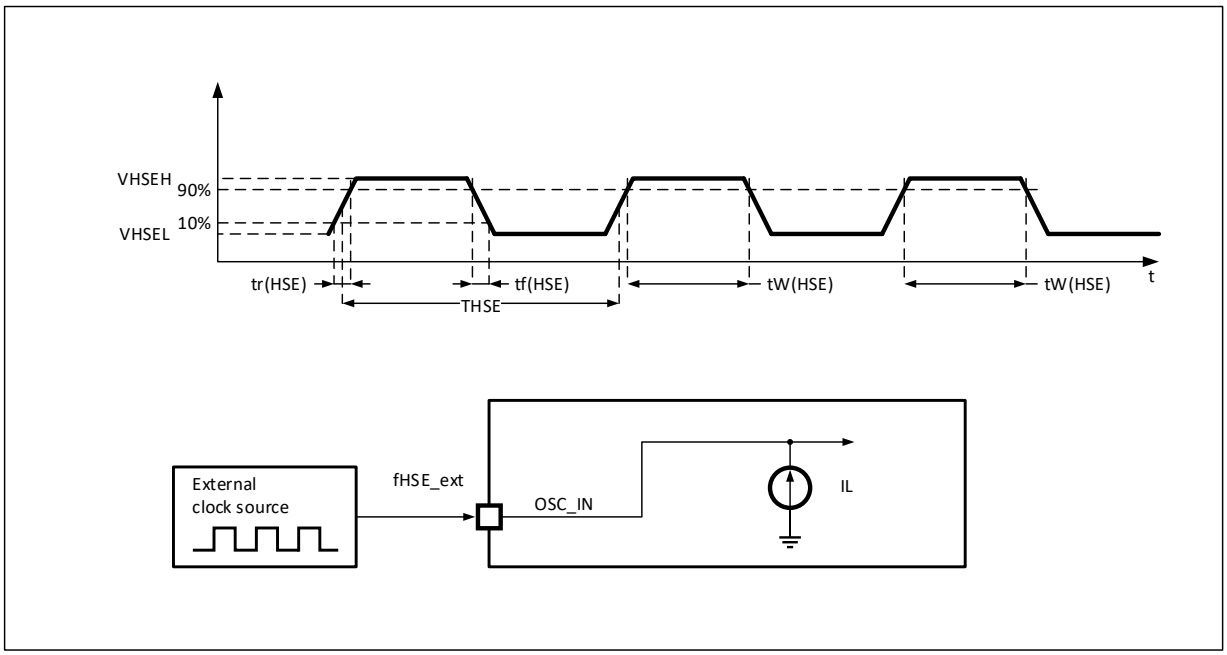
The characteristics given in the table below result from tests performed using a high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 16. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

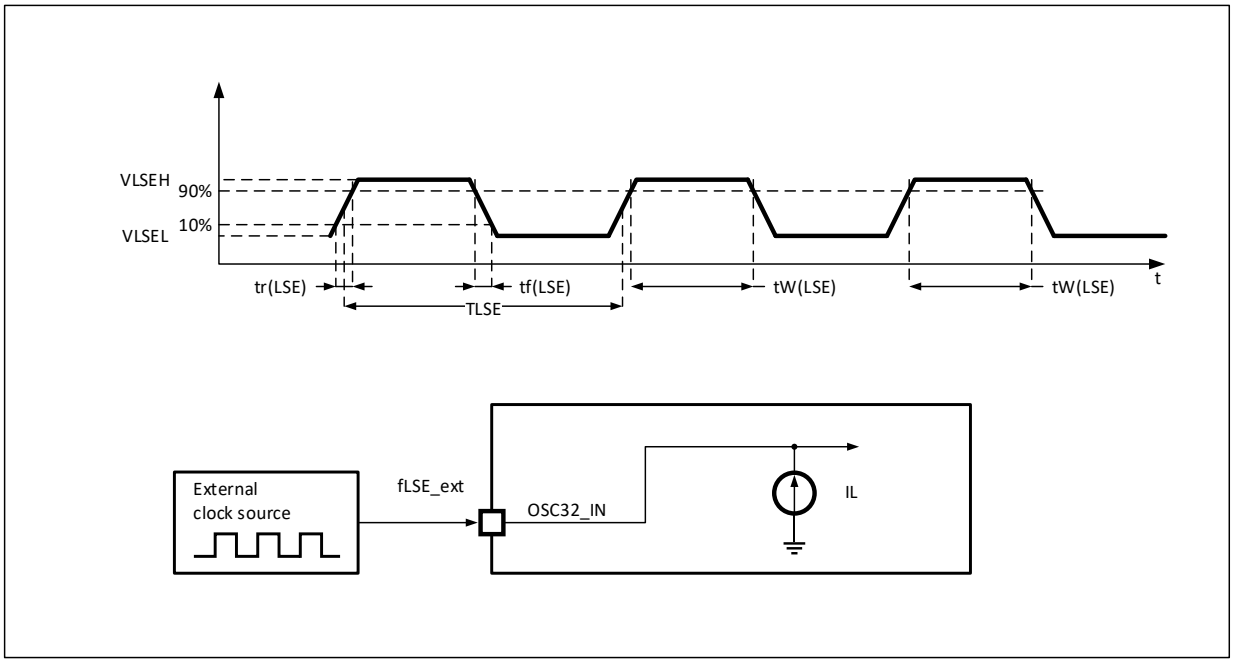
The characteristics given in the table below result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	+60/-1	μA

(1) Guaranteed by design, not tested in production.

Figure 17. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

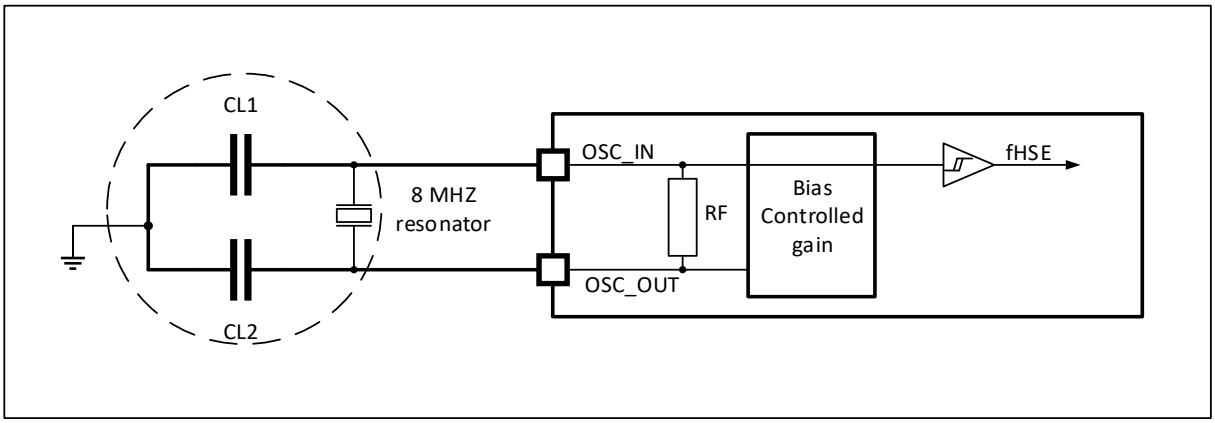
Table 22. HSE 4-25 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

(1) Resonator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1}和C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 18. Typical application with an 8 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

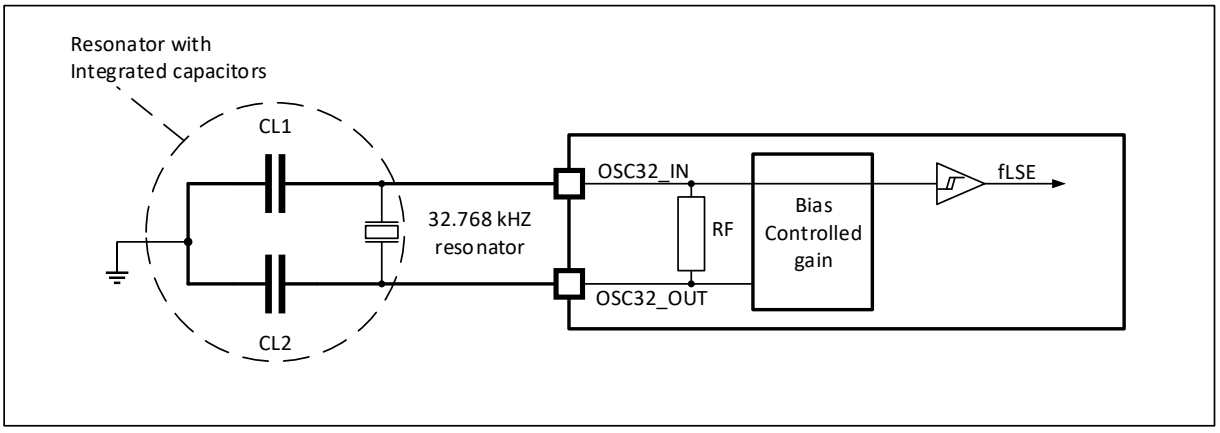
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SU(LSE)}$	Startup time	V_{DD} is stabilized	T_A = -40 °C	-	150	-	ms
			T_A = 25 °C	-	200	-	
			T_A = 85 °C	-	250	-	

(1) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 19. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

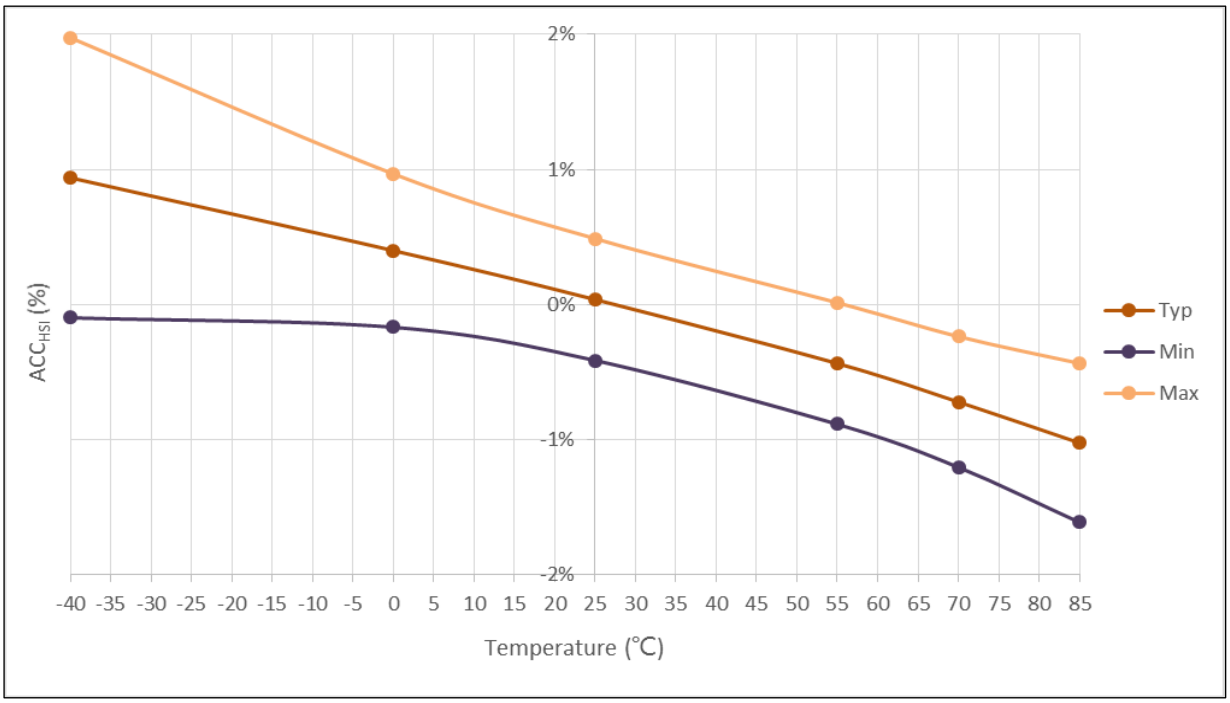
High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CTRL register		-	-	1(2)	%
		Factory-calibrated(3)	T_A = -40 ~ 85 °C	-2.5	-	2.5	%
			T_A = 0 ~ 70 °C	-1.5	-	1.5	%
			T_A = 25 °C	-1	-	1	%
$t_{SU(HSI)}$(3)	HSI oscillator startup time	-		-	-	5	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-		-	100	120	µA

(1) V_{DD} = 3.3 V, T_A = -40~85 °C, unless otherwise specified.
(2) Guaranteed by design, not tested in production.
(3) Guaranteed by characterization results, not tested in production.

Figure 20. HSI oscillator frequency accuracy versus temperature



Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	-	30	40	60	kHz

(1) V_{DD} = 3.3 V, T_A = -40 to 85 °C, unless otherwise specified.
(2) Guaranteed by characterization results, not tested in production.

5.3.8 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with an 8 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	3.3	μs
t_{WUSTOP}(1)	Wakeup from Stop mode	280	μs
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	150	ms

(1) The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.9 PLL characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 27. PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	200	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by characterization results, not tested in production.
(2) Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.10 Memory characteristics

The characteristics in *Table 28* are given at T_A = 25 °C and V_{DD} = 3.3 V.

Table 28. Internal Flash memory characteristics

Symbol	Parameter	Conditions	Typ					Unit
			f_{HCLK}					
			200	144	72	48	8	MHz
T_{PROG}	Programming time	-	30					µs
t_{ERASE}	Page (2 KB) erase time	-	40					ms
t_{ME}	Mass erase time	AT32F403xC	5					s
		AT32F403xE	10					
		AT32F403xG	20					
I_{DD}	Supply current	Programming mode	42.4	32.6	18.3	14.8	6.9	mA
		Erase mode	52.5	40.4	24.4	19.2	9.9	

Table 29. Internal Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 85 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 85 °C	20	-	-	years

(1) Guaranteed by design, not tested in production.

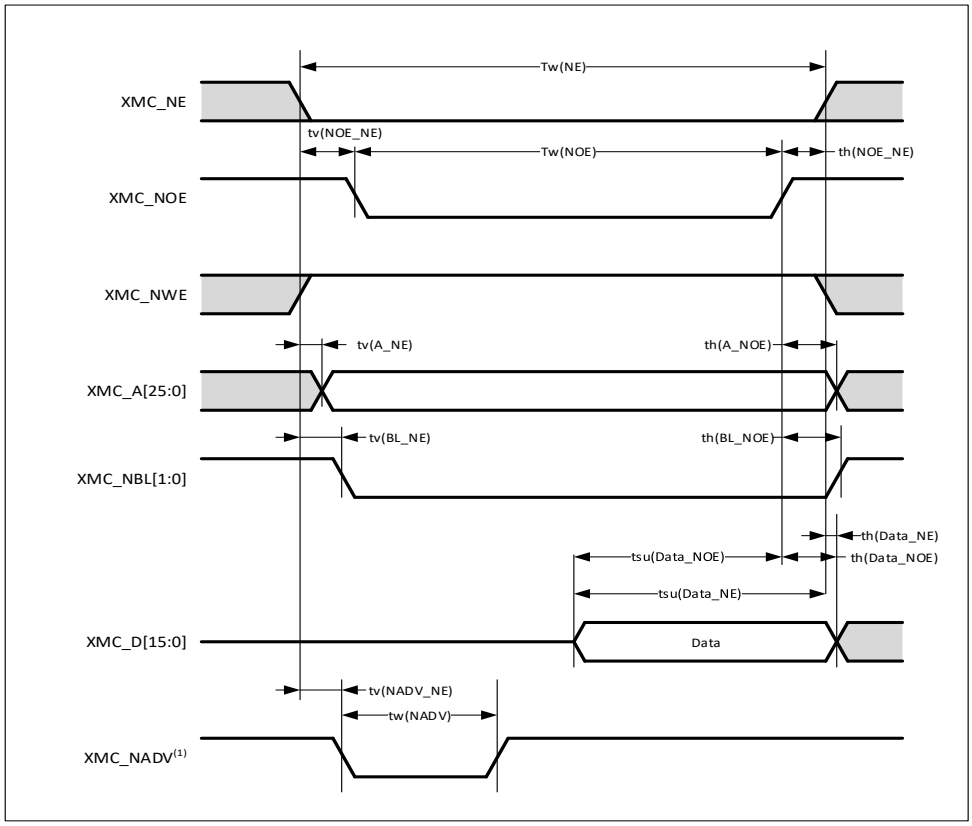
5.3.11 XMC characteristics

Asynchronous waveforms and timings

Figure 21 through *Figure 24* represent asynchronous waveforms and *Table 30* through *Table 33* provide the corresponding timings. The results shown in these tables are obtained with the following XMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



(1) Mode 2/B, C and D only. In Mode 1, XMC_NADV is not used.

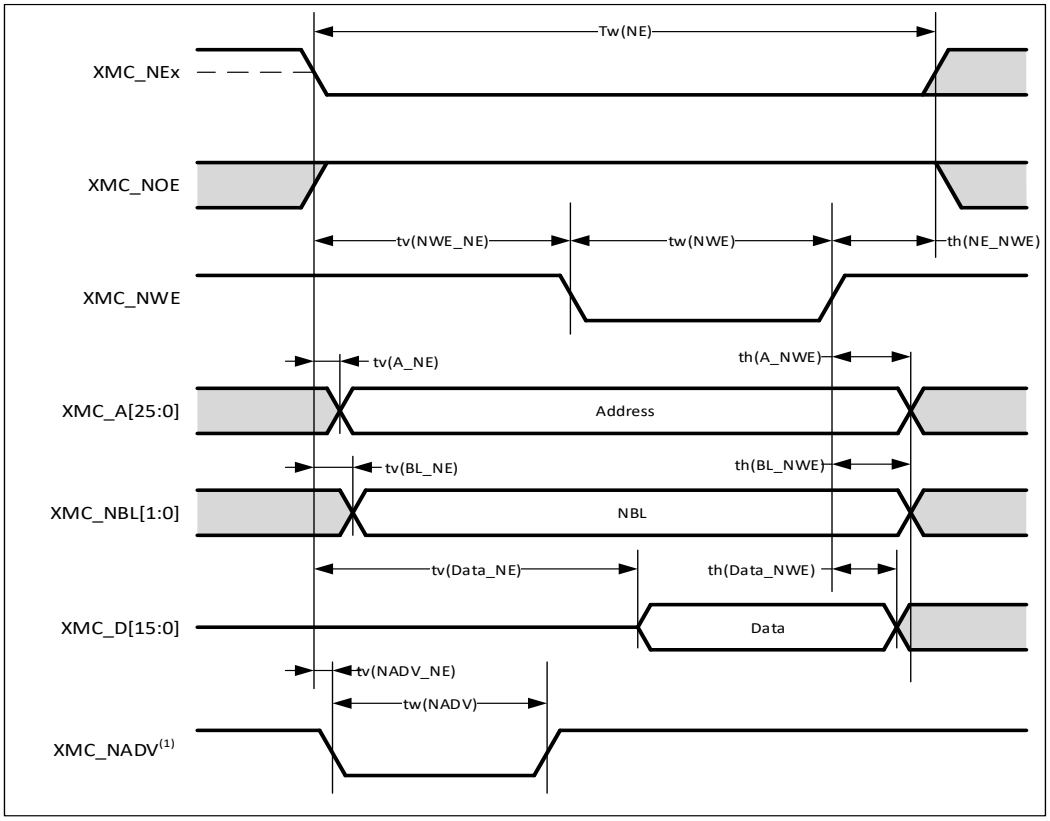
Table 30. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$5t_{HCLK}$ - 1.5	$5t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	XMC_NEx low to XMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	XMC_NOE low time	$5t_{HCLK}$ - 1.5	$5t_{HCLK}$ + 1.5	ns
$t_{h(NE\_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1.5	-	ns
$t_{v(A\_NE)}$	XMC_NEx low to XMC_A valid	-	7	ns
$t_{h(A\_NOE)}$	Address hold time after XMC_NOE high	2.5	-	ns
$t_{v(BL\_NE)}$	XMC_NEx low to XMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	XMC_BL hold time after XMC_NOE high	2.5	-	ns
$t_{su(Data\_NE)}$	Data to XMC_NEx high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{su(Data\_NOE)}$	Data to XMC_NOEx high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NOE)}$	Data hold time after XMC_NOE high	0	-	ns

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after XMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	XMC_NEx low to XMC_NADV low	-	5	ns
$t_{w(NADV)}$	XMC_NADV low time	-	t_{HCLK} + 1.5	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



(1) Mode 2/B, C and D only. In Mode 1, XMC_NADV is not used.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$3t_{HCLK}$ - 1	$3t_{HCLK}$ + 2	ns
$t_{v(NWE\_NE)}$	XMC_NEx low to XMC_NWE low	t_{HCLK} - 0.5	t_{HCLK} + 1.5	ns
$t_{w(NWE)}$	XMC_NWE low time	t_{HCLK} - 0.5	t_{HCLK} + 1.5	ns
$t_{h(NE\_NWE)}$	XMC_NWE high to XMC_NE high hold time	t_{HCLK}	-	ns
$t_{v(A\_NE)}$	XMC_NEx low to XMC_A valid	-	7.5	ns
$t_{h(A\_NWE)}$	Address hold time after XMC_NWE high	t_{HCLK} + 2	-	ns
$t_{v(BL\_NE)}$	XMC_NEx low to XMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	XMC_BL hold time after XMC_NWE high	t_{HCLK} - 0.5	-	ns
$t_{v(Data\_NE)}$	XMC_NEx low to Data valid	-	t_{HCLK} + 7	ns
$t_{h(Data\_NWE)}$	Data hold time after XMC_NWE high	t_{HCLK} + 3	-	ns
$t_{v(NADV\_NE)}$	XMC_NEx low to XMC_NADV low	-	5.5	ns
$t_{w(NADV)}$	XMC_NADV low time	-	t_{HCLK} + 1.5	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Figure 23. Asynchronous multiplexed PSRAM/NOR read waveforms

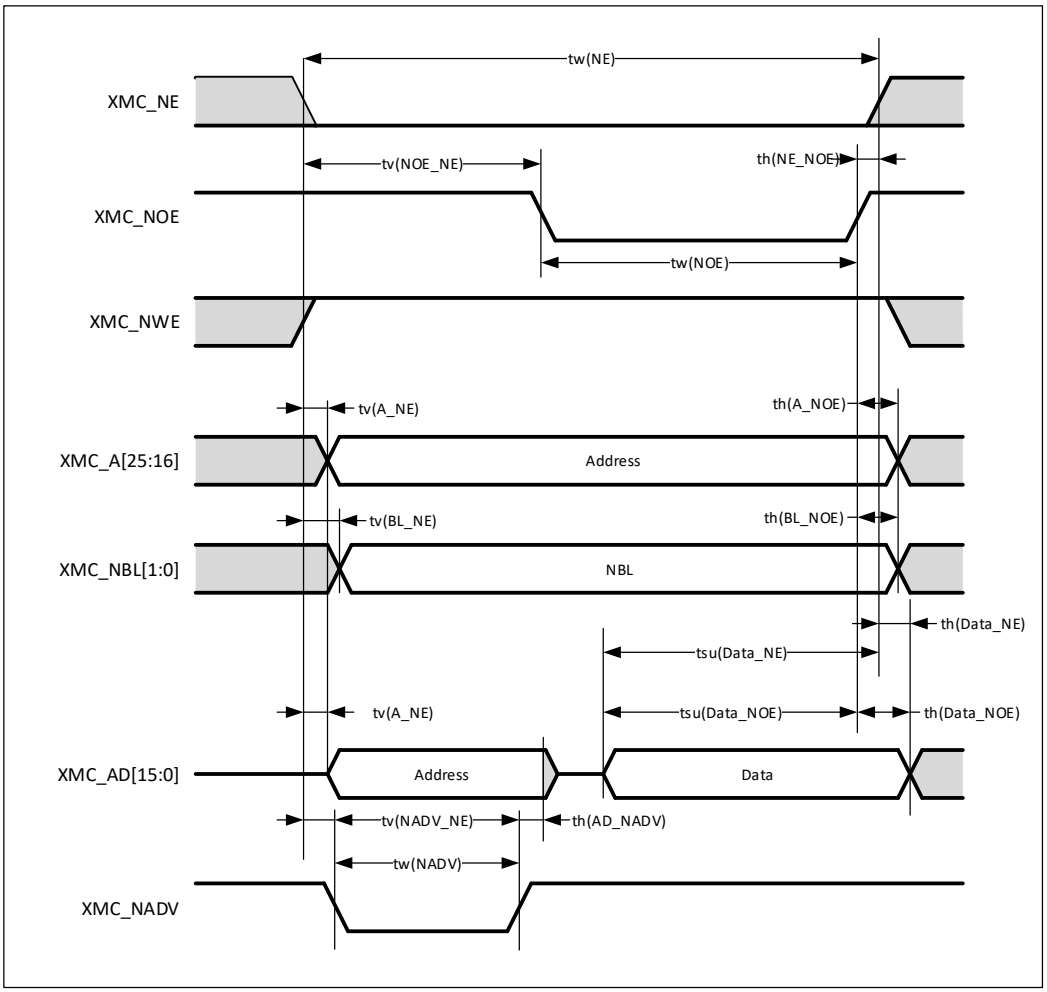


Table 32. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$7t_{HCLK}$ - 2	$7t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	XMC_NEx low to XMC_NOE low	$3t_{HCLK}$ - 0.5	$3t_{HCLK}$ + 1.5	ns
$t_{w(NOE)}$	XMC_NOE low time	$4t_{HCLK}$ - 1	$4t_{HCLK}$ + 2	ns
$t_{h(NE\_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1	-	ns
$t_{v(A\_NE)}$	XMC_NEx low to XMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	XMC_NEx low to XMC_NADV low	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	XMC_AD (address) valid hold time after XMC_NADV high	t_{HCLK} + 3	-	ns
$t_{h(A\_NOE)}$	Address hold time after XMC_NOE high	t_{HCLK} + 3	-	ns
$t_{h(BL\_NOE)}$	XMC_BL hold time after XMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	XMC_NEx low to XMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to XMC_NEx high setup time	$2t_{HCLK}$ + 24	-	ns
$t_{su(Data\_NOE)}$	Data to XMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NE)}$	Data hold time after XMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after XMC_NOE high	0	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Figure 24. Asynchronous multiplexed PSRAM/NOR write waveforms

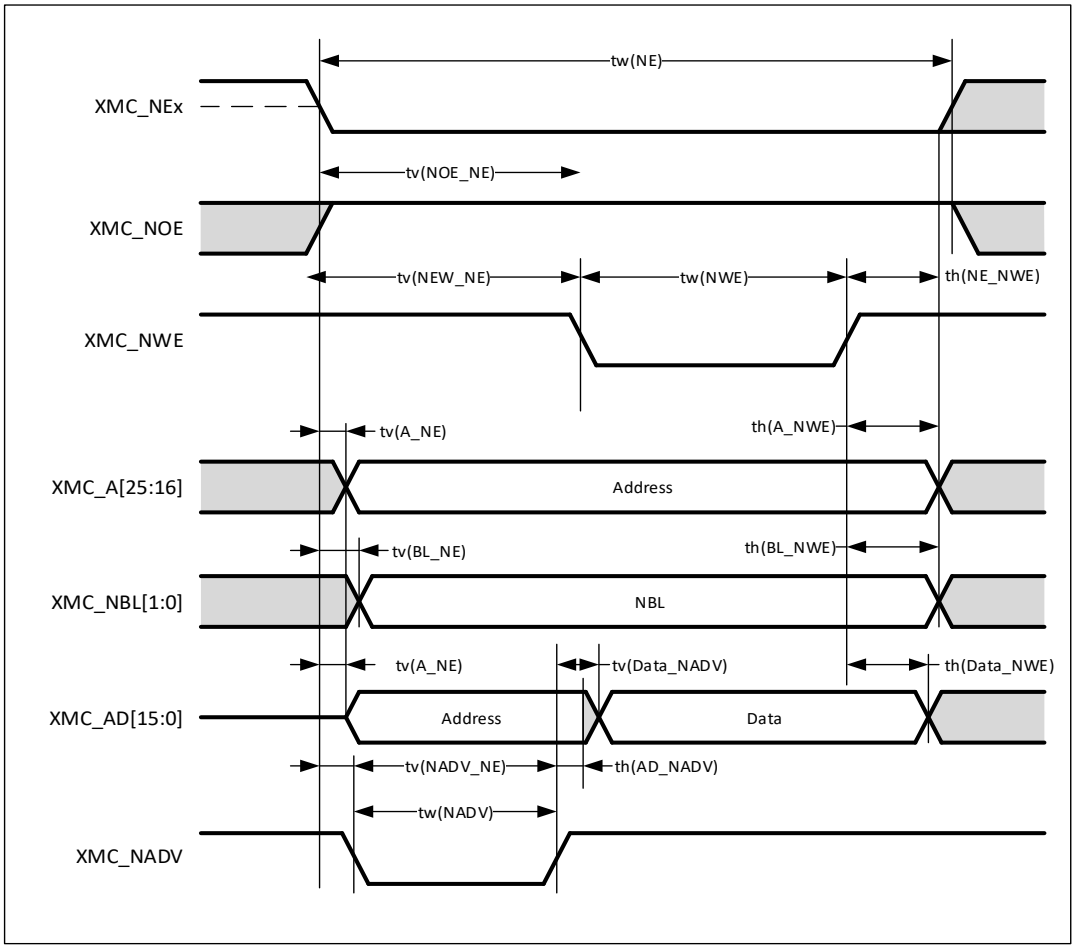


Table 33. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$5t_{HCLK}$ - 1	$5t_{HCLK}$ + 2	ns
$t_{v(NWE\_NE)}$	XMC_NEx low to XMC_NWE low	$2t_{HCLK}$	$2t_{HCLK}$ + 1	ns
$t_{w(NWE)}$	XMC_NWE low time	$2t_{HCLK}$ - 1	$2t_{HCLK}$ + 2	ns
$t_{h(NE\_NWE)}$	XMC_NWE high to XMC_NE high hold time	t_{HCLK} - 1	-	ns
$t_{v(A\_NE)}$	XMC_NEx low to XMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	XMC_NEx low to XMC_NADV low	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1	t_{HCLK} + 1	ns
$t_{h(AD\_NADV)}$	XMC_AD (address) valid hold time after XMC_NADV high	t_{HCLK} - 3	-	ns
$t_{h(A\_NWE)}$	Address hold time after XMC_NWE high	$4t_{HCLK}$ + 2.5	-	ns
$t_{v(BL\_NE)}$	XMC_NEx low to XMC_BL valid	-	1.6	ns
$t_{h(BL\_NWE)}$	XMC_BL hold time after XMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{v(Data\_NADV)}$	XMC_NADV high to Data valid	-	t_{HCLK} + 1.5	ns
$t_{h(Data\_NWE)}$	Data hold time after XMC_NWE high	t_{HCLK} - 5	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 25 through *Figure 28* represent synchronous waveforms and *Table 34* through *Table 37* provide the corresponding timings. The results shown in these tables are obtained with the following XMC configuration:

- BurstAccessMode = XMC_BurstAccessMode_Enable;
- MemoryType = XMC_MemoryType_CRAM;
- WriteBurst = XMC_WriteBurst_Enable;
- CLKPrescale = 1; (Note: CLKPrescale is CLKPSC bit in XMC_BK1TMGx register. Refer to the AT32F403 reference manual.)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM (Note: DataLatency is DATLAT bit in XMC_BK1TMGx register. Refer to the AT32F403 reference manual.)

Figure 25. Synchronous multiplexed NOR/PSRAM read timings

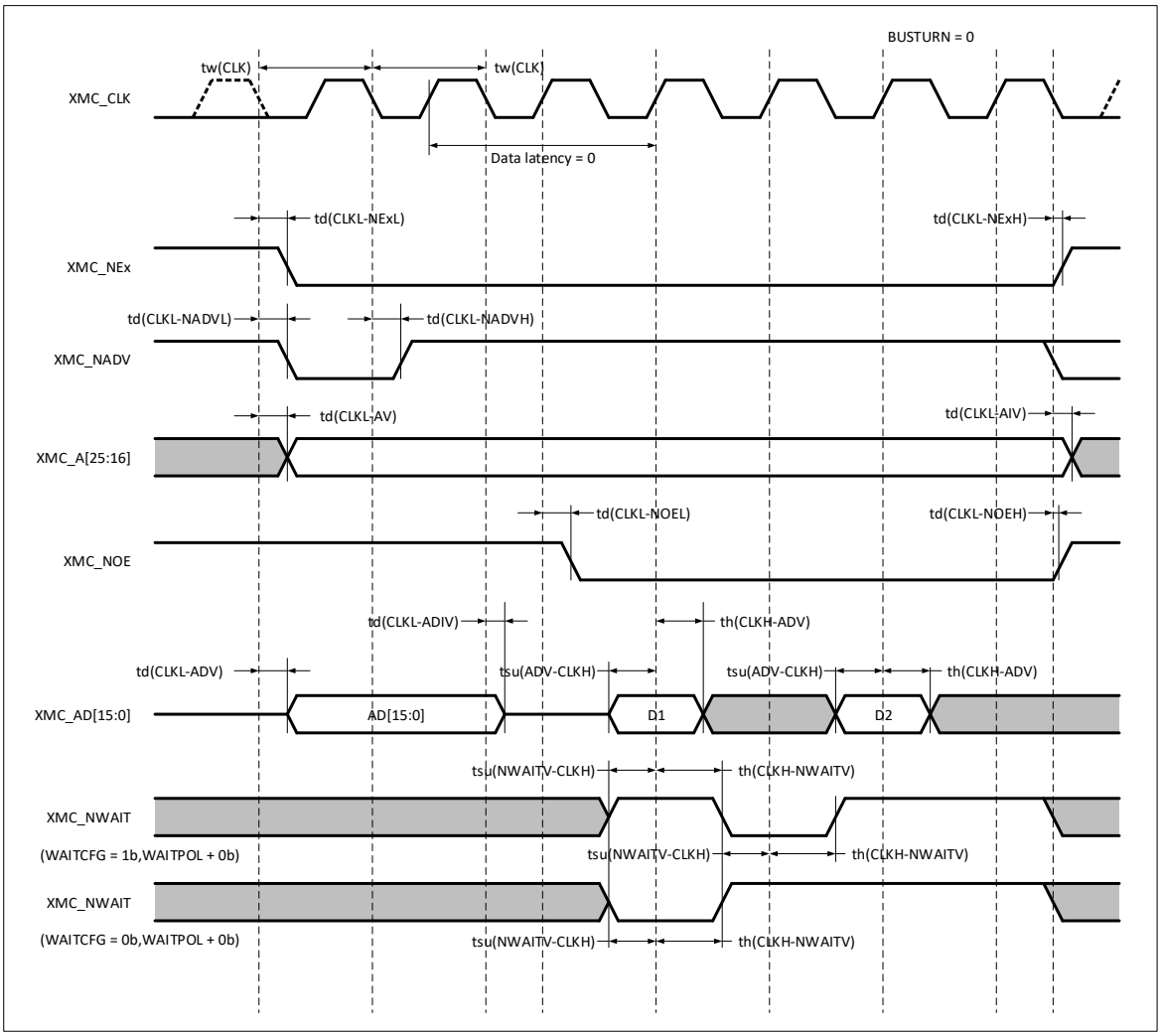


Table 34. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NexL)}$	XMC_CLK low to XMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKH-NexH)}$	XMC_CLK low to XMC_NEx high (x = 0...2)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKH-AIV)}$	XMC_CLK low to XMC_Ax invalid (x = 16...25)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NOEL)}$	XMC_CLK low to XMC_NOE low		t_{HCLK} + 1	ns
$t_{d(CLKH-NOEH)}$	XMC_CLK low to XMC_NOE high	t_{HCLK} + 0.5	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	XMC_A/D[15:0] valid data before XMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	XMC_A/D[15:0] valid data after XMC_CLK high	t_{HCLK} - 10	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	6	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Figure 26. Synchronous multiplexed PSRAM write timings

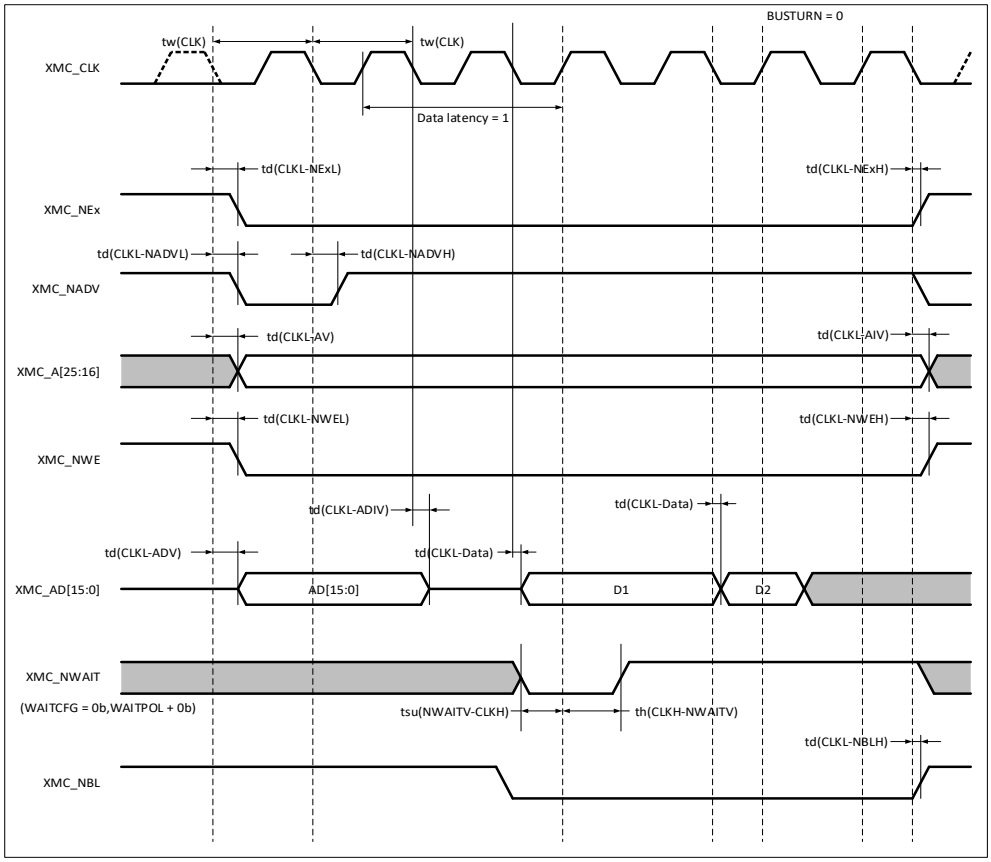


Table 35. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NexL)}$	XMC_CLK low to XMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKH-NexH)}$	XMC_CLK low to XMC_NEx high (x = 0...2)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKH-AIV)}$	XMC_CLK low to XMC_Ax invalid (x = 16...25)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKH-NWEH)}$	XMC_CLK low to XMC_NWE high	t_{HCLK} + 1	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	XMC_A/D[15:0] valid after XMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	XMC_CLK low to XMC_NBL high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid before XMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	XMC_NWAIT valid after XMC_CLK high	1	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Figure 27. Synchronous non-multiplexed NOR/PSRAM read timings

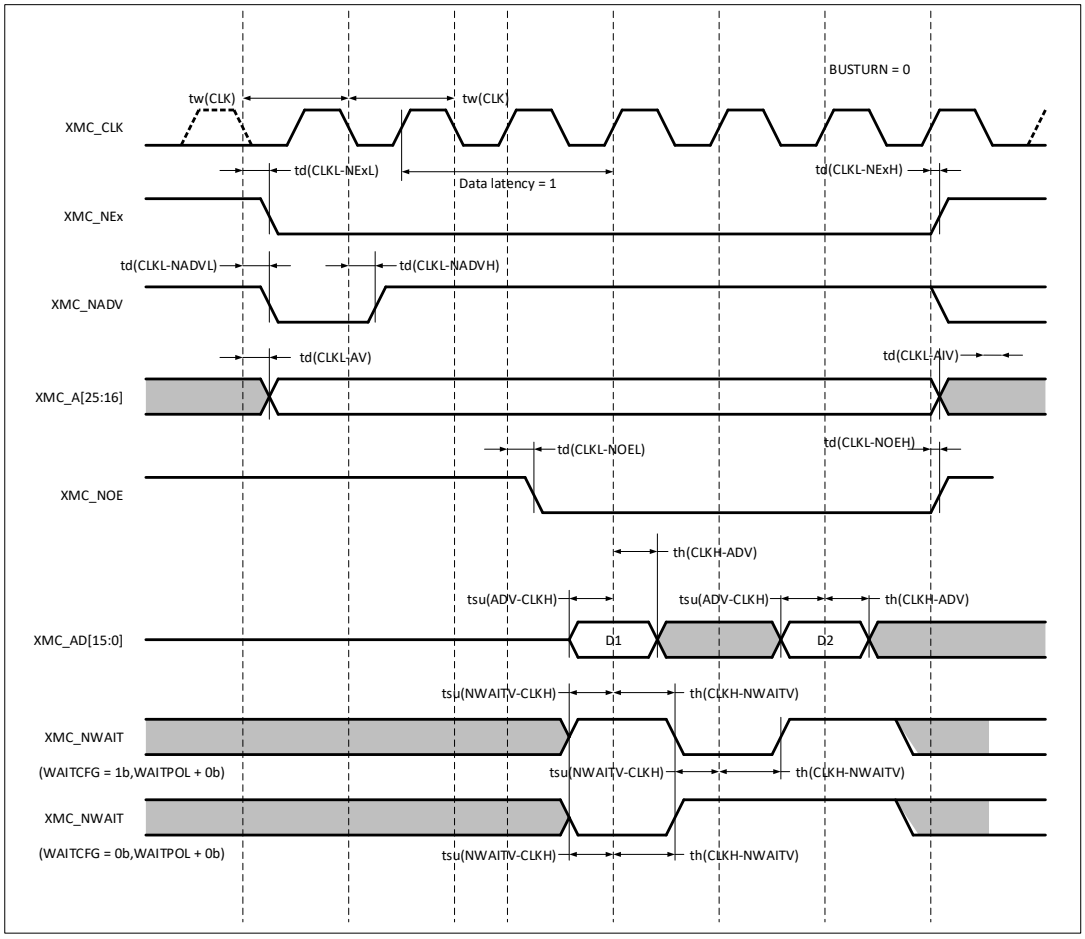


Table 36. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NexL)}$	XMC_CLK low to XMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKH-NexH)}$	XMC_CLK low to XMC_NEx high (x = 0...2)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKH-AIV)}$	XMC_CLK low to XMC_Ax invalid (x = 0...25)	t_{HCLK} + 4	-	ns
$t_{d(CLKL-NOEL)}$	XMC_CLK low to XMC_NOE low	-	t_{HCLK} + 1.5	ns
$t_{d(CLKH-NOEH)}$	XMC_CLK low to XMC_NOE high	t_{HCLK} + 1.5	-	ns
$t_{su(DV-CLKH)}$	XMC_D[15:0] valid data before XMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	XMC_D[15:0] valid data after XMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	2	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

Figure 28. Synchronous non-multiplexed PSRAM write timings

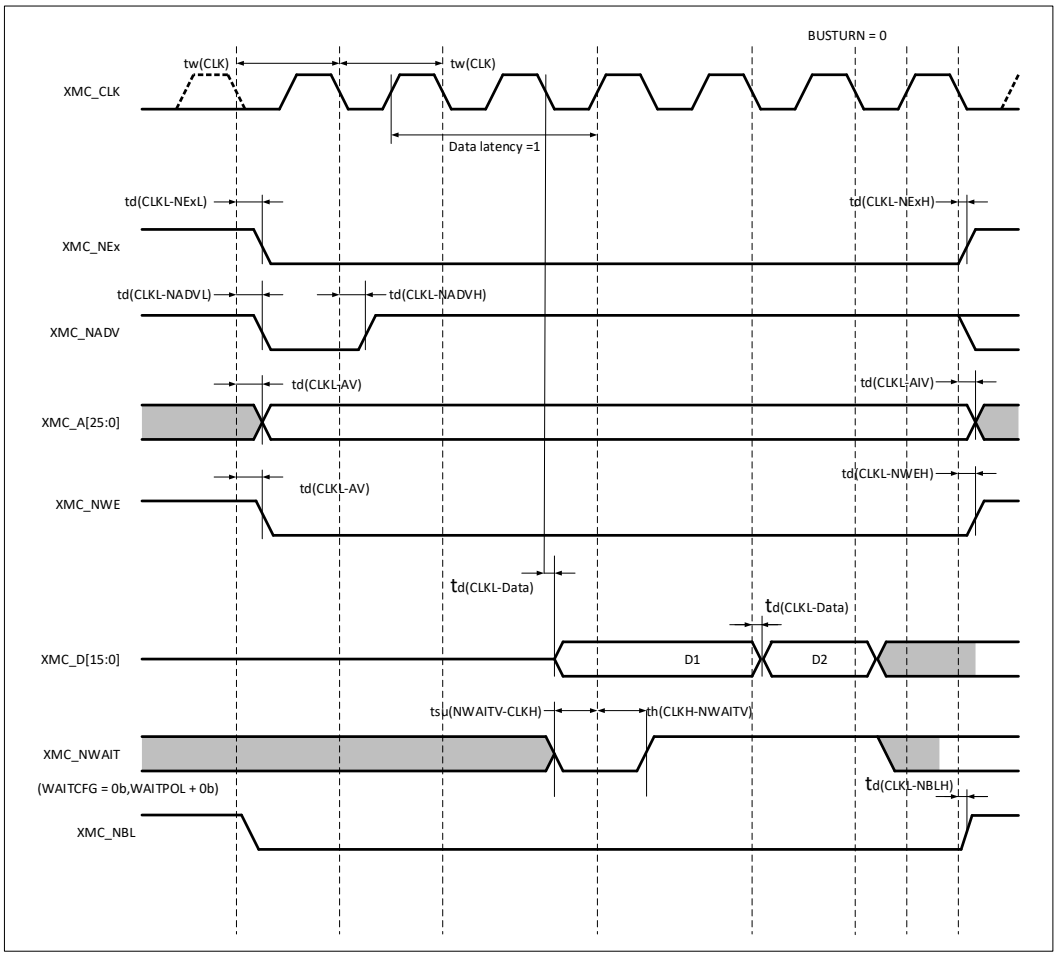


Table 37. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NexL)}$	XMC_CLK low to XMC_NEx low (x = 0...2)	-	2	ns
$t_{d(CLKH-NexH)}$	XMC_CLK low to XMC_NEx high (x = 0...2)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKH-AIV)}$	XMC_CLK low to XMC_Ax invalid (x = 16...25)	t_{HCLK} + 2	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKH-NWEH)}$	XMC_CLK low to XMC_NWE high	t_{HCLK} + 1	-	ns
$t_{d(CLKL-Data)}$	XMC_D[15:0] valid data after XMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	XMC_CLK low to XMC_NBL high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid before XMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	XMC_NWAIT valid after XMC_CLK high	1	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

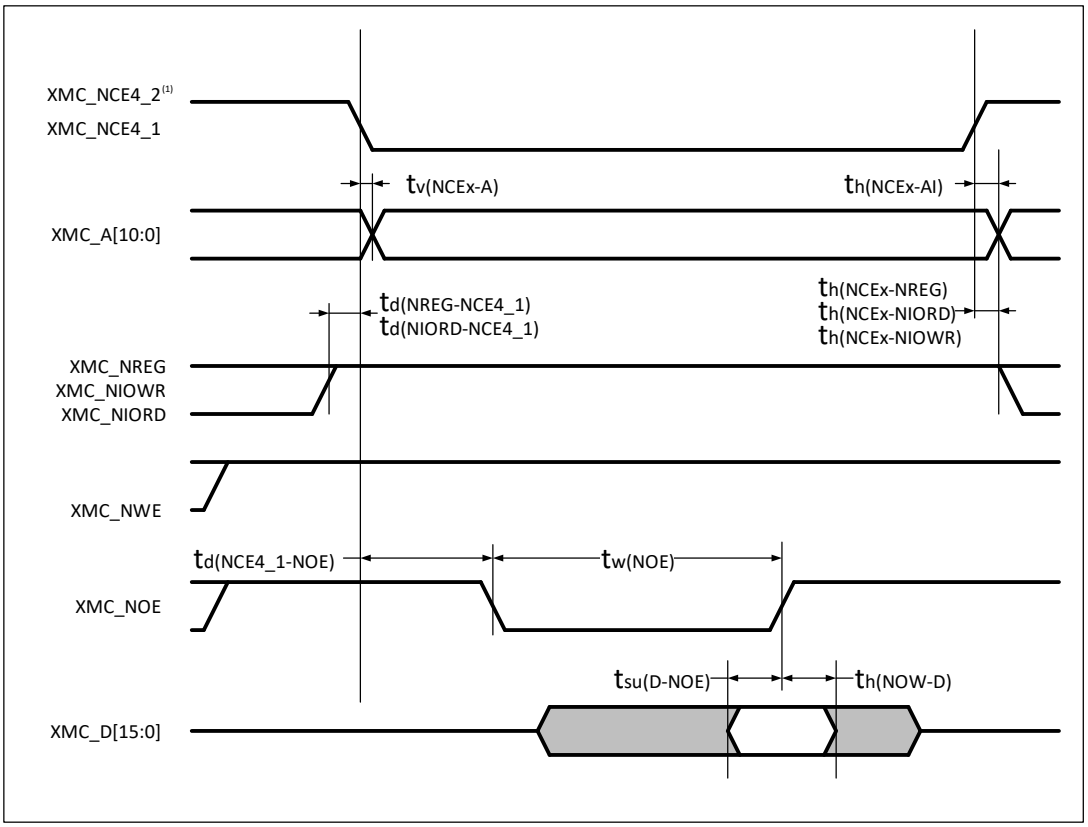
PC Card/CompactFlash controller waveforms and timings

Figure 29 through *Figure 34* represent synchronous waveforms and *Table 38* provides the corresponding timings. The results shown in this table are obtained with the following XMC configuration:

- COM.XMC_SetupTime = 0x04; (Note: STP in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_WaitSetupTime = 0x07; (Note: OP in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_HoldSetupTime = 0x04; (Note: HLD in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_HiZSetupTime = 0x00; (Note: WRSTP in XMC_BKxTMGMEM, x = 2…4)
- ATT.XMC_SetupTime = 0x04; (Note: STP in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_WaitSetupTime = 0x07; (Note: OP in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_HoldSetupTime = 0x04; (Note: HLD in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_HiZSetupTime = 0x00; (Note: WRSTP in XMC_BKxTMGATT, x = 2…4)
- IO.XMC_SetupTime = 0x04; (Note: STP in XMC_BKxTMGIO, x = 4)
- IO.XMC_WaitSetupTime = 0x07; (Note: OP in XMC_BKxTMGIO, x = 4)
- IO.XMC_HoldSetupTime = 0x04; (Note: HLD in XMC_BKxTMGIO, x = 4)
- IO.XMC_HiZSetupTime = 0x00; (Note: WRSTP in XMC_BKxTMGIO, x = 4)
- DLYCRSetupTime = 0; (Note: DLYCR in XMC_BKxCTRL)
- DLYARSetupTime = 0; (Note: DLYAR in XMC_BKxCTRL)

Note: Refer to the AT32F403 reference manual about the description of registers above (XMC_BKXTMGMEMx, XMC_BKxTMGATT, XMC_BKxTMGIO, and XMC_BKxCTRL).

Figure 29. PC Card/CompactFlash controller waveforms for common memory read access



(1) XMC_NCE4_2 remains high (inactive during 8-bit access).

Figure 30. PC Card/CompactFlash controller waveforms for common memory write access

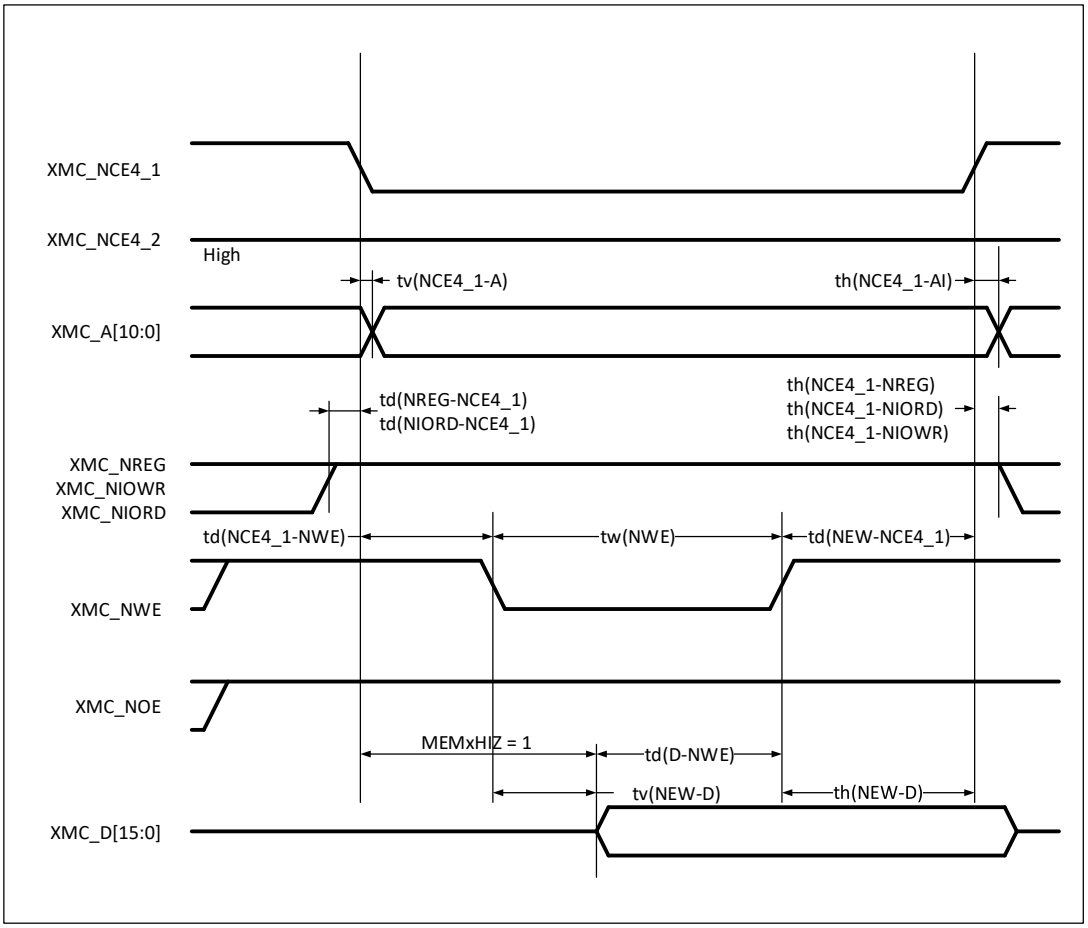
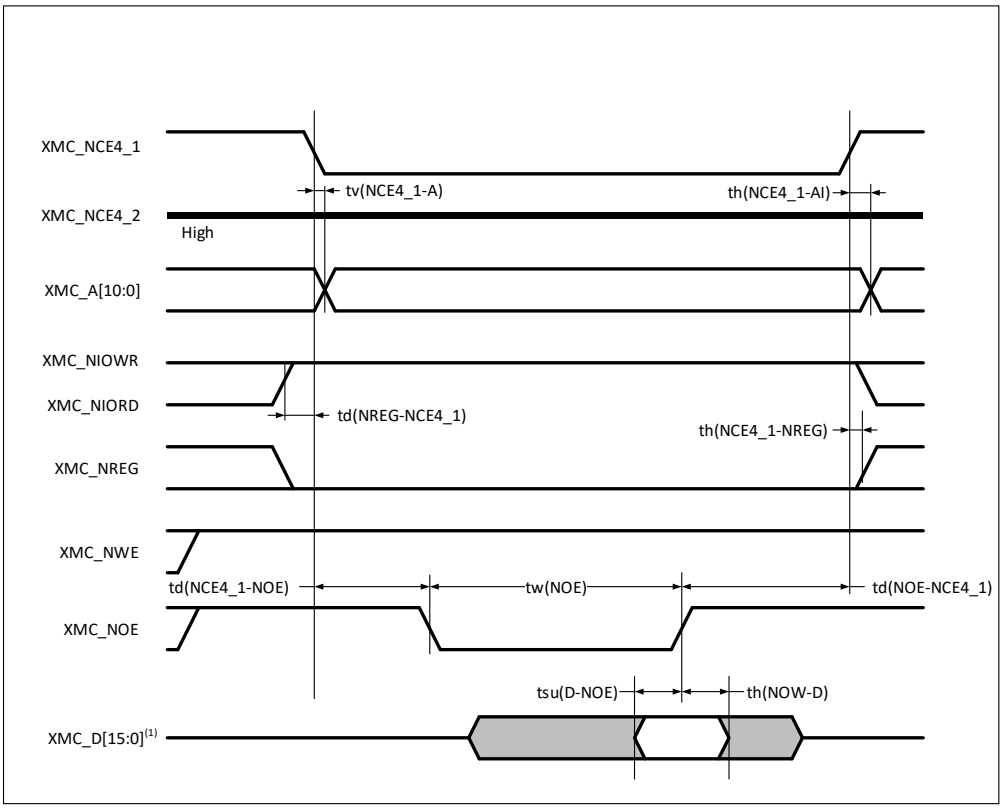
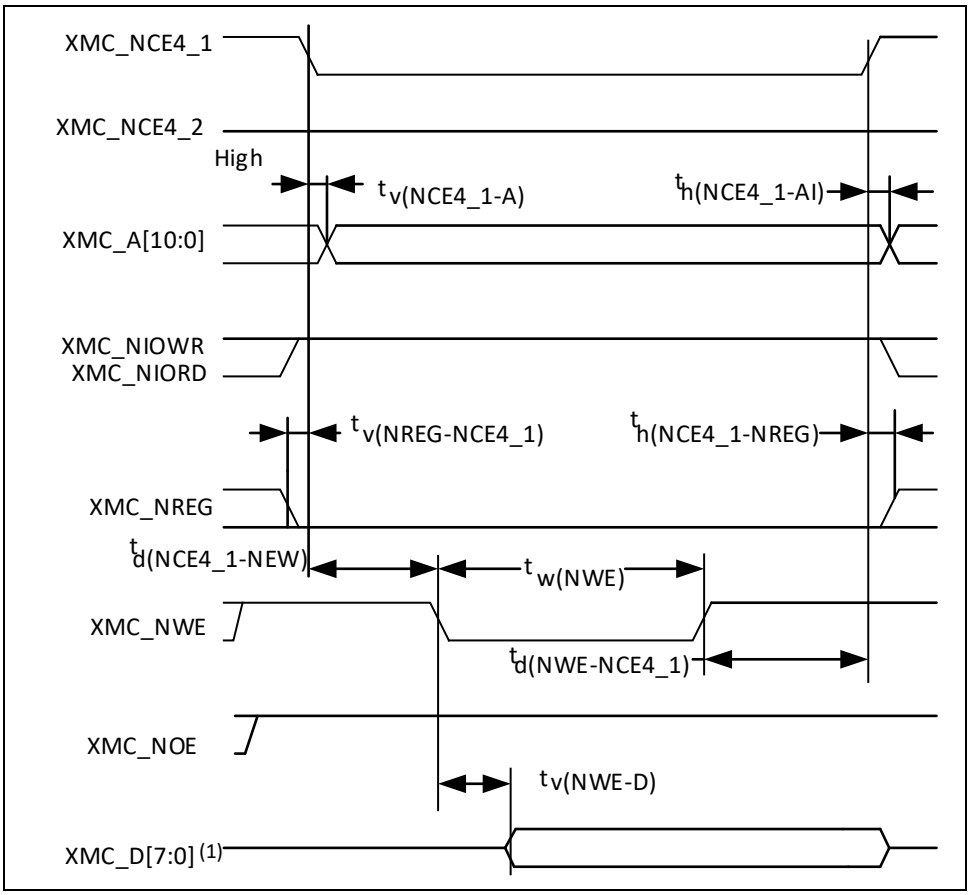


Figure 31. PC Card/CompactFlash controller waveforms for attribute memory read access



(1) Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 32. PC Card/CompactFlash controller waveforms for attribute memory write access



(1) Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 33. PC Card/CompactFlash controller waveforms for I/O space read access

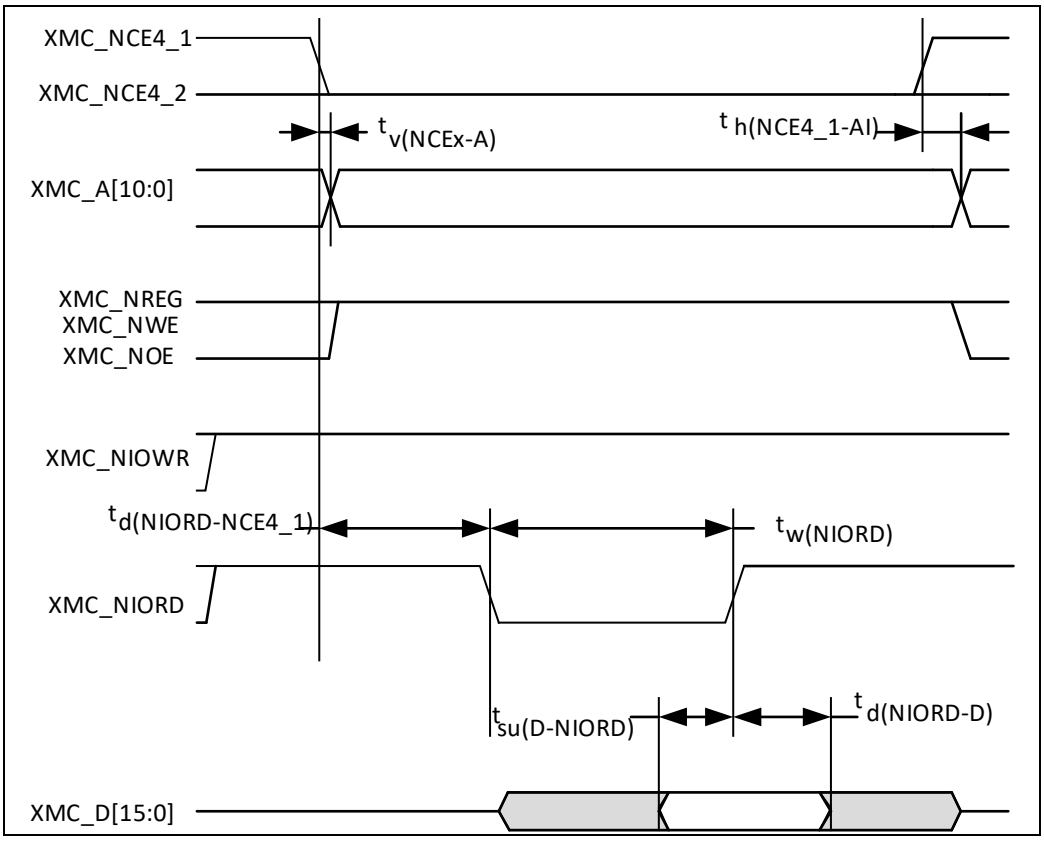


Figure 34. PC Card/CompactFlash controller waveforms for I/O space write access

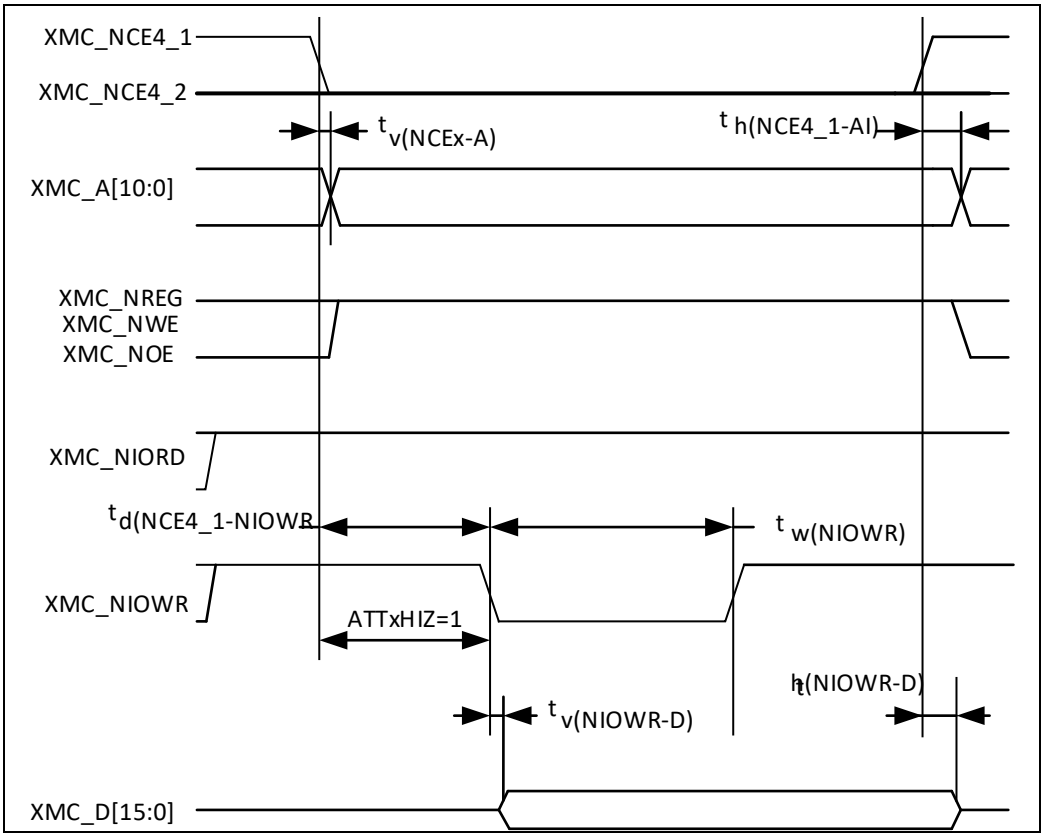


Table 38. Switching characteristics for PC Card/CF read and write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$ $t_{v(NCE4\_1-A)}$	XMC_NCEx low (x = 4_1/4_2) to XMC_Ay valid (y = 0...10) XMC_NCE4_1 low (x = 4_1/4_2) to XMC_Ay valid (y = 0...10)	-	0	ns
$t_{h(NCEx-AI)}$ $t_{h(NCE4\_1-AI)}$	XMC_NCEx high (x = 4_1/4_2) to XMC_Ax invalid (x = 0...10) XMC_NCE4_1 high (x = 4_1/4_2) to XMC_Ax invalid (x = 0...10)	2.5	-	ns
$t_{d(NREG-NCEx)}$ $t_{d(NREG-NCE4\_1)}$	XMC_NCEx low to XMC_NREG valid XMC_NCE4_1 low to XMC_NREG valid	-	5	ns
$t_{h(NCEx-NREG)}$ $t_{h(NCE4\_1-NREG)}$	XMC_NCEx high to XMC_NREG invalid XMC_NCE4_1 high to XMC_NREG invalid	t_{HCLK} + 3	-	ns
$t_{d(NCE4\_1-NOE)}$	XMC_NCE4_1 low to XMC_NOE low	-	$5t_{HCLK}$ + 2	ns
$t_{w(NOE)}$	XMC_NOE low width	$8t_{HCLK}$ - 1.5	$8t_{HCLK}$ + 1	ns
$t_{d(NOE-NCE4\_1)}$	XMC_NOE high to XMC_NCE4_1 high	$5t_{HCLK}$ + 2	-	ns
$t_{su(D-NOE)}$	XMC_D[15:0] valid data before XMC_NOE high	25	-	ns
$t_{h(NOE-D)}$	XMC_D[15:0] valid data after XMC_NOE high	15	-	ns
$t_{w(NWE)}$	XMC_NWE low width	$8t_{HCLK}$ - 1	$8t_{HCLK}$ + 2	ns
$t_{d(NWE-NCE4\_1)}$	XMC_NWE high to XMC_NCE4_1 high	$5t_{HCLK}$ + 2	-	ns
$t_{d(NCE4\_1-NWE)}$	XMC_NCE4_1 low to XMC_NWE low	-	$5t_{HCLK}$ + 1.5	ns
$t_{v(NWE-D)}$	XMC_NWE low to XMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	XMC_NWE high to XMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(D-NWE)}$	XMC_D[15:0] valid before XMC_NWE high	$13t_{HCLK}$	-	ns
$t_{w(NIOWR)}$	XMC_NIOWR low width	$8t_{HCLK}$ + 3	-	ns
$t_{v(NIOWR-D)}$	XMC_NIOWR low to XMC_D[15:0] valid	-	$5t_{HCLK}$ + 1	ns
$t_{h(NIOWR-D)}$	XMC_NIOWR high to XMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	XMC_NCE4_1 low to XMC_NIOWR valid	-	$5t_{HCLK}$ + 3	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	XMC_NCEx high to XMC_NIOWR invalid XMC_NCE4_1 high to XMC_NIOWR invalid	$5t_{HCLK}$ - 5	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	XMC_NCEx low to XMC_NIORD valid XMC_NCE4_1 low to XMC_NIORD valid	-	$5t_{HCLK}$ + 2.5	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	XMC_NCEx high to XMC_NIORD invalid XMC_NCE4_1 high to XMC_NIORD invalid	$5t_{HCLK}$ - 5	-	ns
$t_{su(D-NIORD)}$	XMC_D[15:0] valid before XMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	XMC_D[15:0] valid after XMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	XMC_NIORD low width	$8t_{HCLK}$ + 2	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 35 through *Figure 38* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following XMC configuration:

- COM.XMC_SetupTime = 0x01; (Note: STP in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_WaitSetupTime = 0x03; (Note: OP in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_HoldSetupTime = 0x02; (Note: HLD in XMC_BKxTMGMEM, x = 2…4)
- COM.XMC_HiZSetupTime = 0x01; (Note: WRSTP in XMC_BKxTMGMEM, x = 2…4)
- ATT.XMC_SetupTime = 0x01; (Note: STP in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_WaitSetupTime = 0x03; (Note: OP in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_HoldSetupTime = 0x02; (Note: HLD in XMC_BKxTMGATT, x = 2…4)
- ATT.XMC_HiZSetupTime = 0x01; (Note: WRSTP in XMC_BKxTMGATT, x = 2…4)
- Bank = XMC_Bank_NAND;
- MemoryDataWidth = XMC_MemoryDataWidth_16b; (Note: Memory data width = 16 bits)
- ECC = XMC_ECC_Enable; (Note: enable ECC calculation)
- ECCPageSize = XMC_ECCPageSize_512Bytes; (Note: ECC page size = 512 Bytes)
- DLYCRSetupTime = 0; (Note: DLYCR in XMC_BKxCTRL)
- DLYARSetupTime = 0; (Note: DLYAR in XMC_BKxCTRL)

Figure 35. NAND controller waveforms for read access

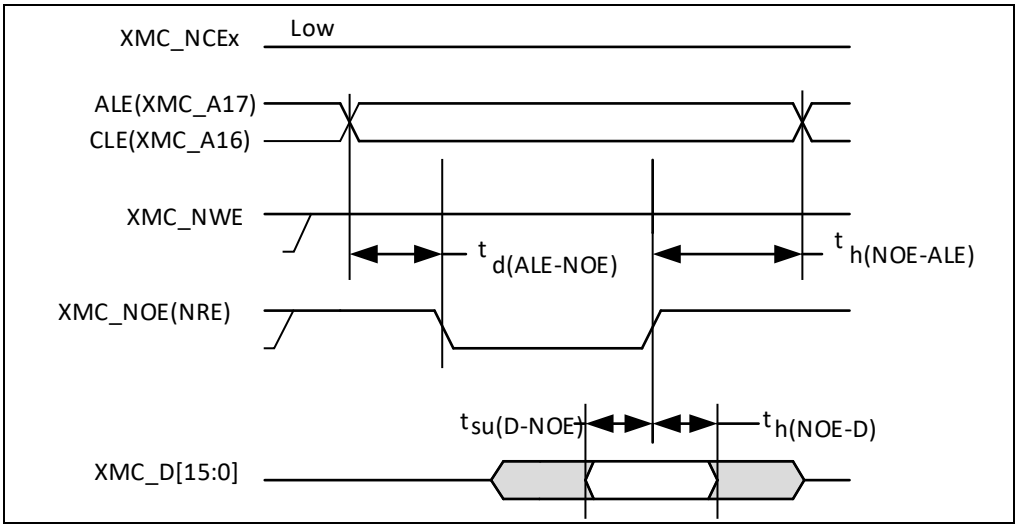


Figure 36. NAND controller waveforms for write access

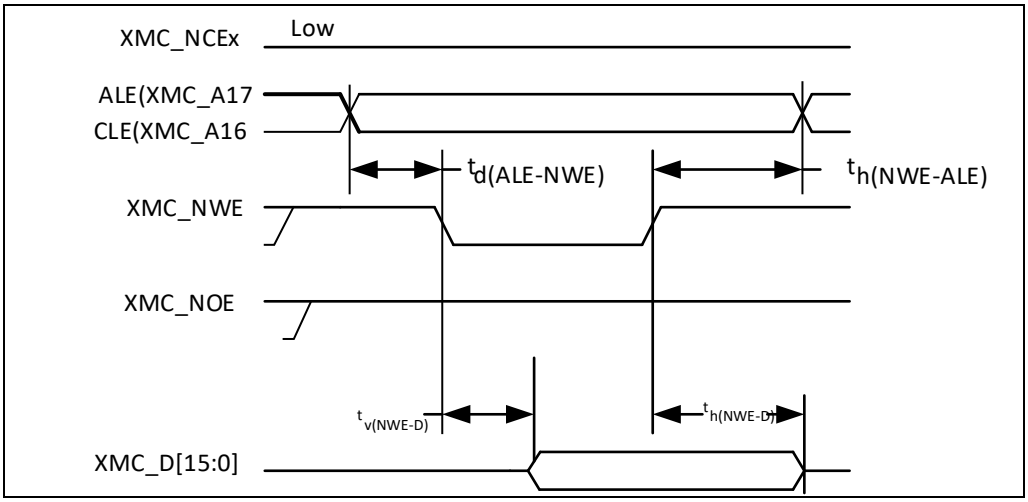


Figure 37. NAND controller waveforms for common memory read access

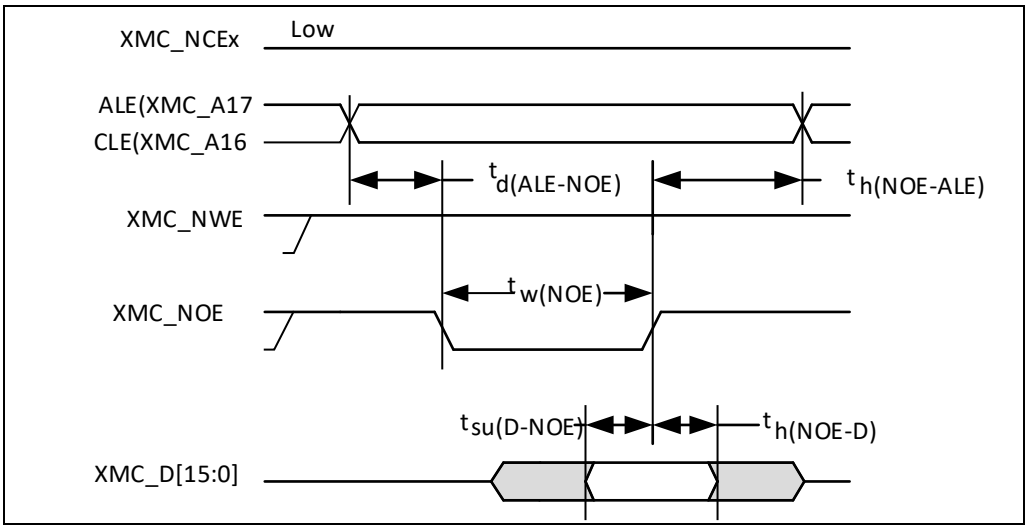


Figure 38. NAND controller waveforms for common memory write access

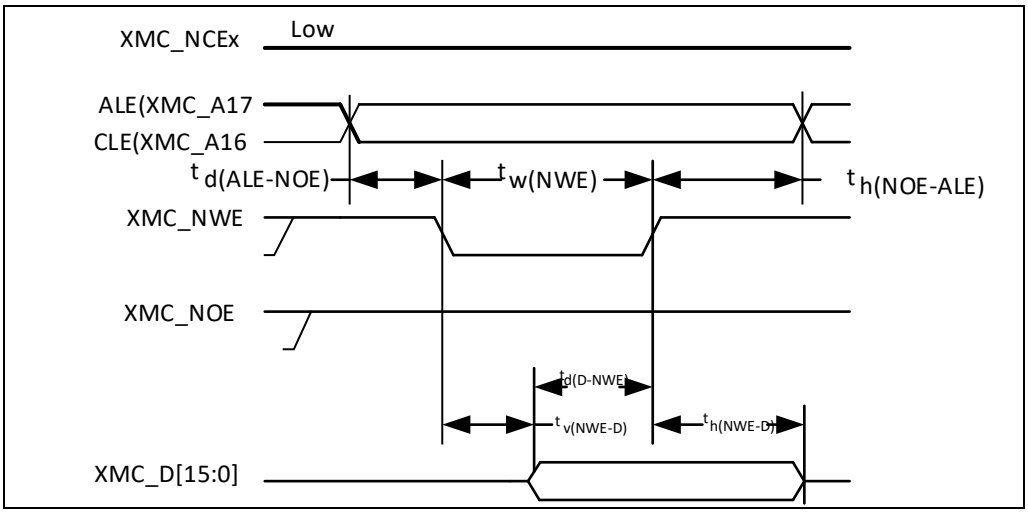


Table 39. Switching characteristics for NAND Flash read and write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$(2)	XMC_D[15:0] valid before XMC_NWE high	$6T_{HCLK}$ + 12	-	ns
$t_{w(NOE)}$(2)	XMC_NWE low width	$4T_{HCLK}$ - 1.5	$4T_{HCLK}$ + 1.5	ns
$t_{su(D-NOE)}$(2)	XMC_D[15:0] valid data before XMC_NOE high	25	-	ns
$t_{h(NOE-D)}$(2)	XMC_D[15:0] valid data after XMC_NOE high	14	-	ns
$t_{w(NWE)}$(2)	XMC_NWE low width	$4T_{HCLK}$ - 1	$4T_{HCLK}$ + 2.5	ns
$t_{v(NWE-D)}$(2)	XMC_NWE low to XMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$(2)	XMC_NWE high to XMC_D[15:0] invalid	$10T_{HCLK}$ + 4	-	ns
$t_{d(ALE-NWE)}$(3)	XMC_ALE valid before XMC_NWE low	-	$3T_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$(3)	XMC_NWE high to XMC_ALE invalid	$3T_{HCLK}$ + 4.5	-	ns
$t_{d(ALE-NOE)}$(3)	XMC_ALE valid before XMC_NOE low	-	$3T_{HCLK}$ + 2	ns
$t_{h(NOE-ALE)}$(3)	XMC_NWE high to XMC_ALE invalid	$3T_{HCLK}$ + 4.5	-	ns

(1) C_L = 15 pF
(2) Guaranteed by characterization results, not tested in production.
(3) Guaranteed by design, not tested in production.

5.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 40. EMS characteristics

Symb	Parameter	Conditions	Level/Class
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 200 MHz conforms to IEC 61000-4-4	4A (4kV)

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

5.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JS-001-2017/JS-002-2014 standard.

Table 41. ESD absolute maximum ratings

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2014	III	1000	

(1) Guaranteed by characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on 6 parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 42. Electrical sensitivities

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +85 °C, conforming to EIA/JESD78E	II level A (200 mA)

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symb	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O(1) input low level voltage	-	–0.3	-	0.28 * V_{DD} + 0.1	V
V_{IH}	Standard I/O input high level voltage	-	0.31 * V_{DD} + 0.8	-	V_{DD} + 0.3	V
	I/O FT(1) input high level voltage			-	5.5	V
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)	-	-	mV
I_{lkg}	Input leakage current(4)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os(5)	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5V$ I/O FT	-	-	±10	
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	60	80	100	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)(6)	$V_{IN} = V_{DD}$	70	90	120	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

(1) FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
(2) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(3) With a minimum of 100 mV.
(4) Leakage could be higher than max if negative current is injected on adjacent pins.
(5) Each of PA11 and PA12 has a weak pull-down resistor 330 kΩ which is permanently enabled.
(6) The pull-down resistor of BOOT0 exists permanently.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 8*).
- The sum of the currents sunk by all I/Os on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 8*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
MDEx[1:0] = 11 (maximum sourcing/sinking stregth)					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 45 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
MDEx[1:0] = 01 (large sourcing/sinking stregth)					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 20 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
MDEx[1:0] = 10 (normal sourcing/sinking stregth)					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 10 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Unless otherwise specified, the parameters given below are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in *Table 10*.

Table 45. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
t_{EXTIpw}	Pulse width of external	10	-	V

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

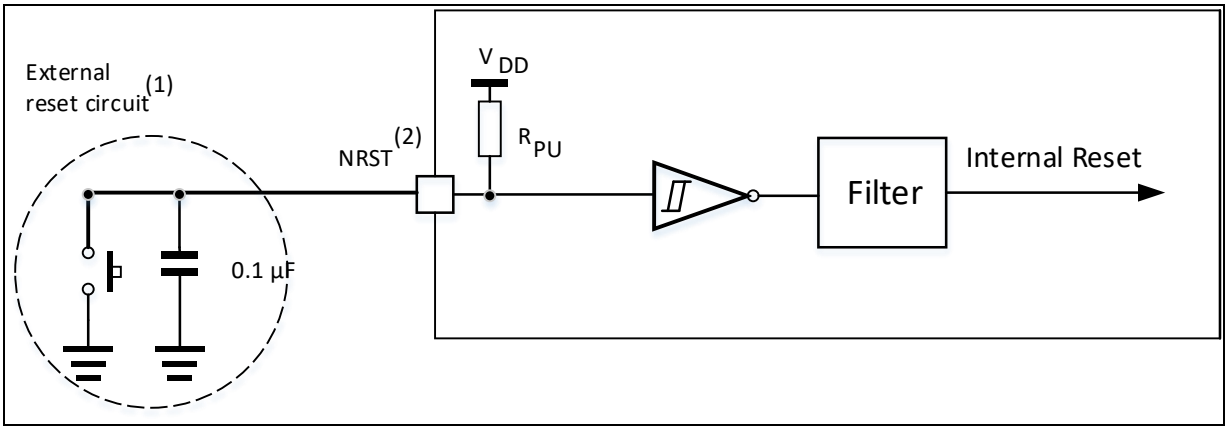
Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 46. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	370	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	33.3	μs
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	66.7	-	-	μs

(1) Guaranteed by design.

Figure 39. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the V_{IL} (NRST) max level specified in unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 46*. Otherwise the reset will not be taken into account by the device.

5.3.16 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to *5.3.14 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TMRx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 100 MHz	10	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz
		$f_{TMRxCLK}$ = 100 MHz	0	50	MHz

(1) TMRx is used as a general term to refer to the TMR1 to TMR15.

5.3.17 Communications interfaces

I²C interface characteristics

The AT32F403 I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL mapped to are not ”true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in the table below. Refer also to *5.3.14 I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 48. I²C characteristics

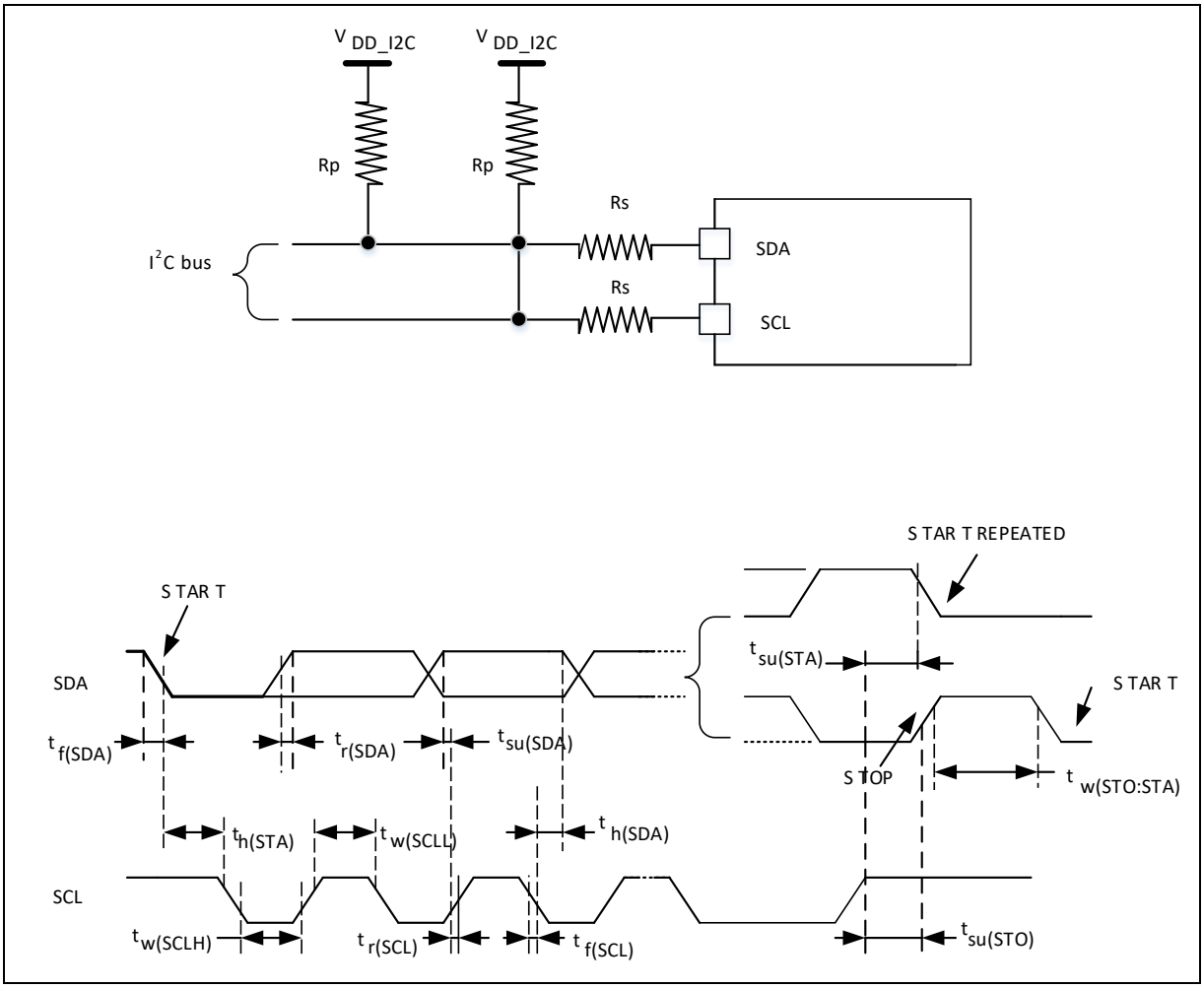
Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

(1) Guaranteed by design, not tested in production.

(2) f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve the fast mode I²C frequencies.

(3) The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.

Figure 40. I²C bus AC waveforms and measurement circuit(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. SCL frequency (f_{PCLK1} = 36 MHz, V_{DD} = 3.3 V)(1)(2)

f_{SCL}(kHz)	I2C_CLKCTRL value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

(1) R_P = External pull-up resistance, f_{SCL} = I²C speed.
(2) For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI-I²S and SPIM characteristics

Unless otherwise specified, the parameters given in *Table 50* for SPI and SPIM or in *Table 51* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *5.3.14 I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 50. SPI and SPIM characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	SPI1~4 master mode	-	50	MHz
		SPI1~4 slave mode	-	$f_{PCLK}/2$(4)	
		SPIM	-	60	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 100 MHz, prescaler = 4	15	25	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{su(SI)}$(1)		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{h(SI)}$(1)		Slave mode	4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

(1) Guaranteed by characterization results, not tested in production.
(2) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(3) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.
(4) When SPI1~4 operate in full-duplex mode with accessing through DMA, f_{HCLK} must be 8 timers of f_{SCK}.

Figure 41. SPI timing diagram - slave mode and CPHA = 0

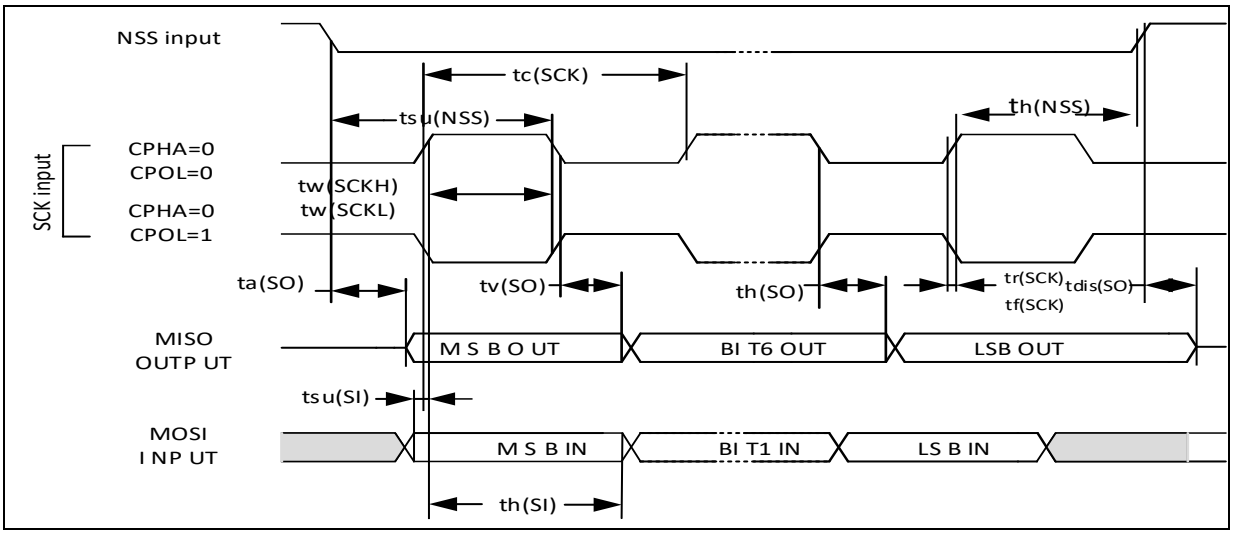
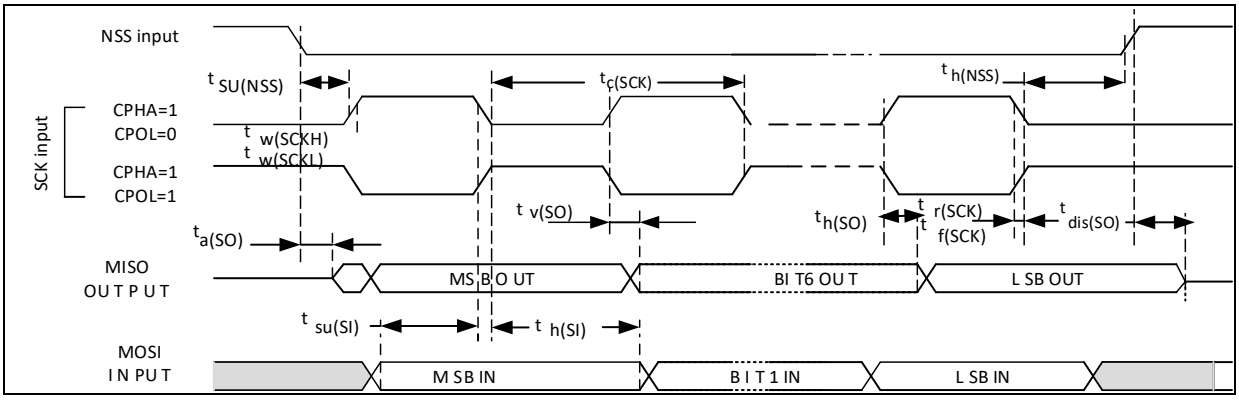
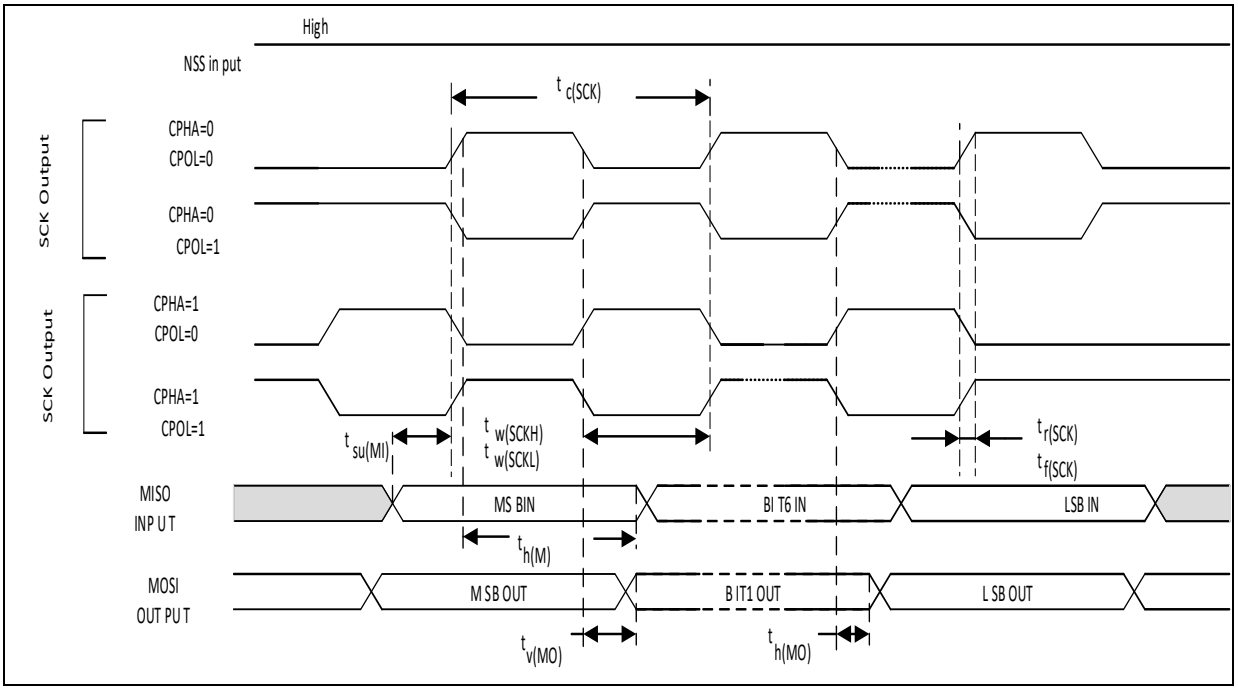


Figure 42. SPI timing diagram - slave mode and CPHA = 1(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 43. SPI timing diagram - master mode(1)



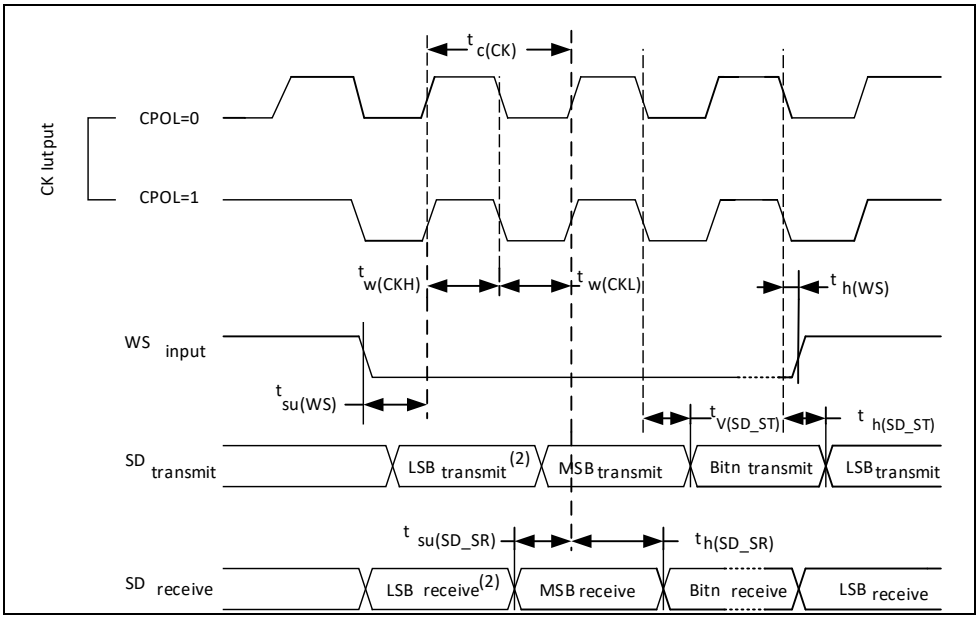
(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 51. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I²S clock frequency	Master mode (data: 16 bits, audio frequency = 48 kHz)	1.522	1.525	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 50 pF	-	8	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	3	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	2	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	4	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{w(CKH)}$(1)	CK high and low time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz	312.5	-	
$t_{w(CKL)}$(1)			345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6.5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	18	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	11	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

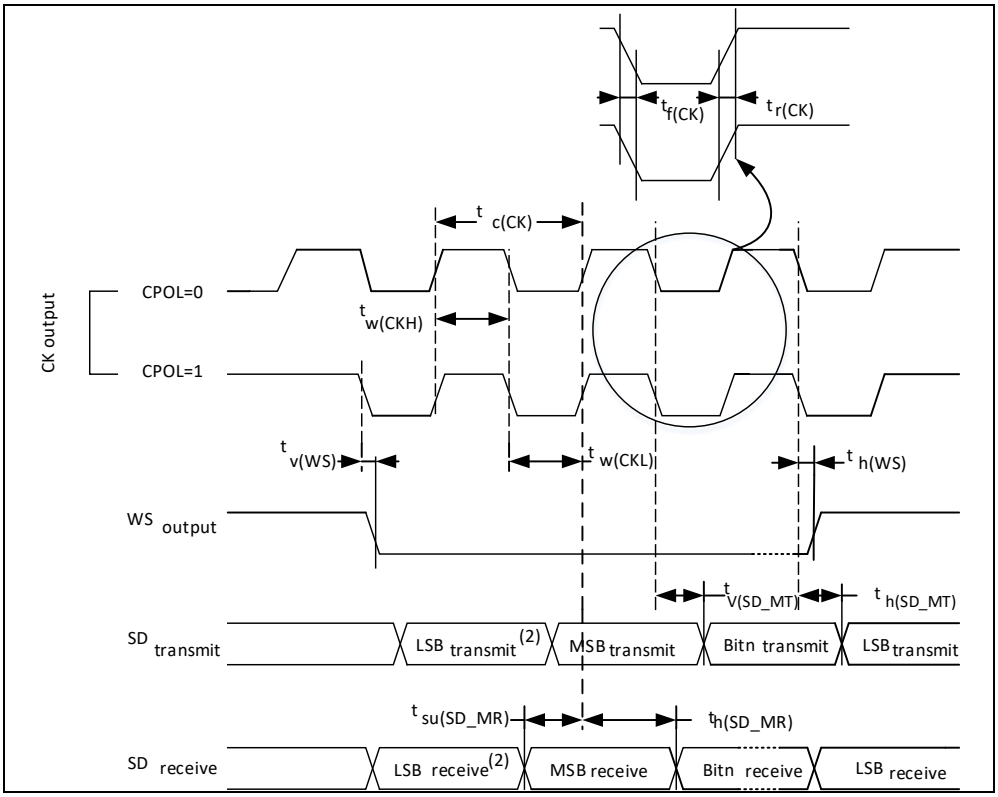
(1) Guaranteed by design and/or characterization results.
(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 44. I²S slave timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 45. I²S master timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *5.3.14 I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 46. SDIO high-speed mode

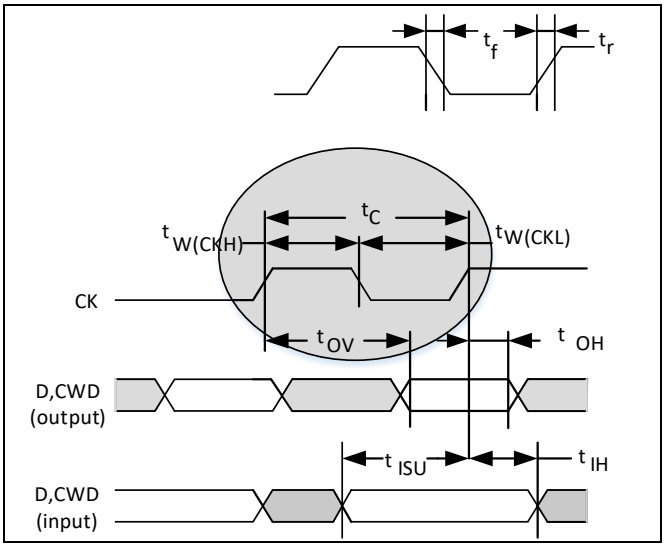


Figure 47. SD default mode

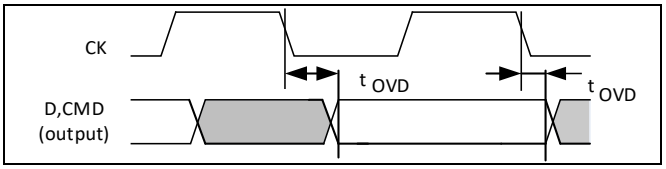


Table 52. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \le 30$ pF	0	48	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	$C_L \le 30$ pF	32	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	$C_L \le 30$ pF	30	-	
t_r	Clock rise time	$C_L \le 30$ pF	-	4	
t_f	Clock fall time	$C_L \le 30$ pF	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \le 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \le 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \le 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \le 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \le 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \le 30$ pF	0.5	-	

(1) Refer to SDIO_CLKCTRL, the SDIO clock control register to control the CK output.

USB characteristics

Table 53. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 54. USB DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	USB operating voltage	-	3.0(2)		3.6	V
	V_{DI}(3)	Differential input sensitivity	I (USB_DP, USB_DM)	0.2		-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8		2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3		2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8		3.6	
R_{PU}		USB_DP internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32F403 USB functionality is ensured down to 2.6 V but not the full USB electrical characteristics which are degraded in the 2.6 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by characterization results, not tested in production.
(4) R_L is the load connected on the USB drivers.

Figure 48. USB timings: definition of data signal rise and fall time

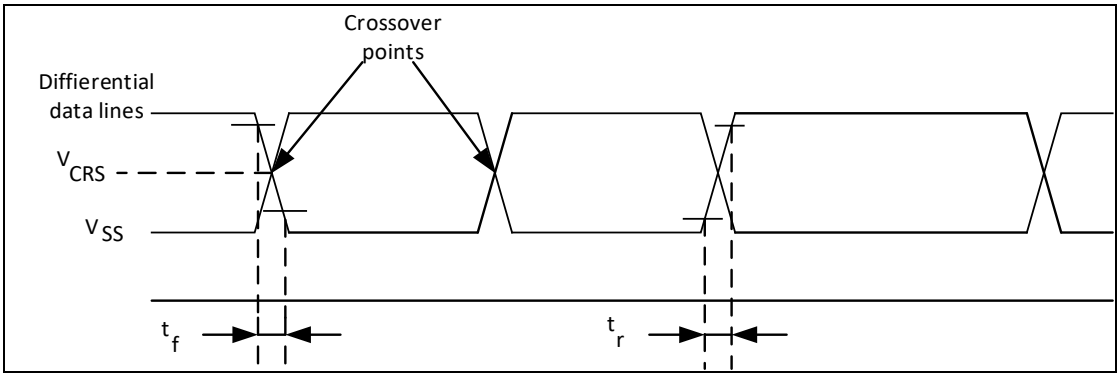


Table 55. USB full-speed electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time (2)	C_L ≤ 50 pF	4	20	ns
t_f	Fall Time (2)	C_L ≤ 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.18 CAN (controller area network) interface

Refer to *5.3.14 I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

Table 56. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.6	-	3.6	V
V_{REF+}	Positive reference voltage(3)	-	2.6	-	V_{DDA}	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	520(1)	600	μA
I_{VREF}	Current on the V_{REF+} input pin(3)	-	-	280(1)	350	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(2)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground))	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table* 57 and *Table* 58 for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	15	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	11.1			μs
		-	312			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	μs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Chapter 3 Pinouts and pin descriptions* for further details.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 56*.

Table 57 and *Table 58* are used to determine the maximum external impedance allowed for an error below 1/4 of LSB.

Table 57. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.2
7.5	0.54	1.0
13.5	0.96	2.0
28.5	2.04	4.2
41.5	2.96	6.0
55.5	3.96	8.5
71.5	5.11	11
239.5	17.11	32

(1) Guaranteed by design.

Table 58. R_{AIN} max for f_{ADC} = 28 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	0.4
13.5	0.48	0.9
28.5	1.02	2.1
41.5	1.48	3.0
55.5	1.98	4.0
71.5	2.55	5.0
239.5	8.55	19

(1) Guaranteed by design.

Table 59. ADC accuracy (V_{DDA} = 3.0 to 3.6 V, V_{REF+} = V_{DDA}, T_A = 25 °C)(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz,	±2	±3	LSB
EO	Offset error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ,	±0.8	±1.5	
EG	Gain error	V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C	±0.5	±1.5	
ED	Differential linearity error	Measurements made after ADC calibration	+1.5/-0.5	+2/-1	
EL	Integral linearity error	V_{REF+} = V_{DDA}	±1.8	±2.5	

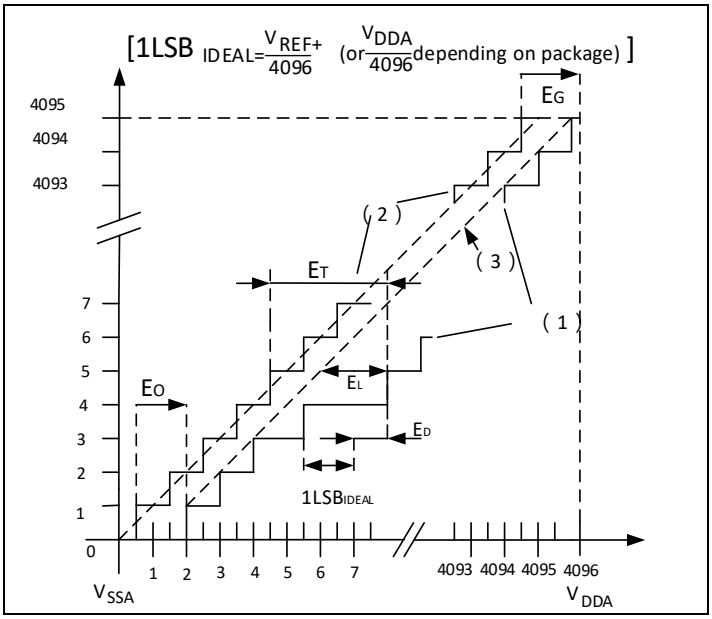
(1) ADC DC accuracy values are measured after internal calibration.
(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
(3) Guaranteed by characterization results, not tested in production.

Table 60. ADC accuracy (V_{DDA} = 2.6 to 3.6 V, T_A = -40 to +85 °C)(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz,	±2.5	±4	LSB
EO	Offset error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ,	±1	±1.5	
EG	Gain error	V_{DDA} = 2.6 to 3.6 V	±1	±1.5	
ED	Differential linearity error	Measurements made after ADC calibration	+2/-0.5	+3/-1	
EL	Integral linearity error		±2	±3.5	

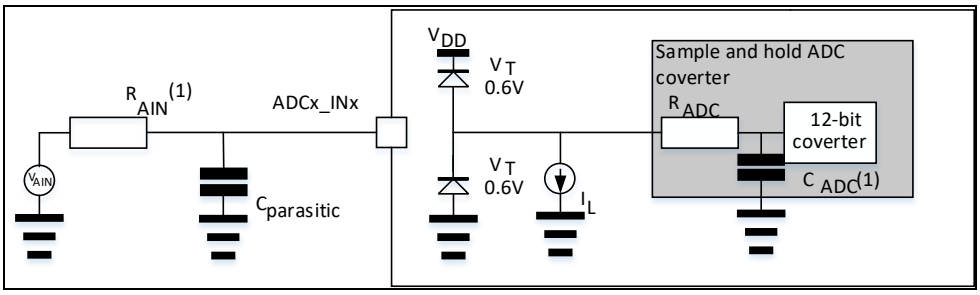
(1) ADC DC accuracy values are measured after internal calibration.
(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
(3) Guaranteed by characterization results, not tested in production.

Figure 49. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 50. Typical connection diagram using the ADC



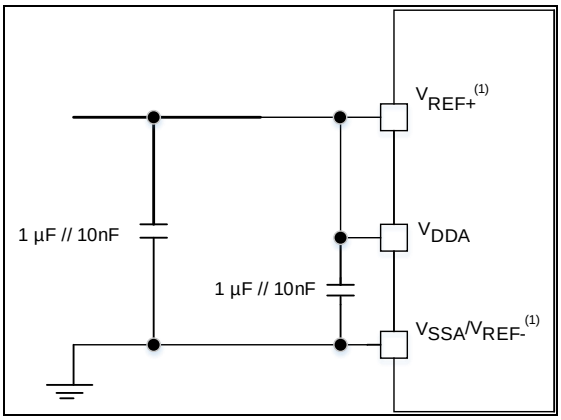
(1) Refer to *Table 56* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*.depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip. If HSE is enabled while ADC uses any input channel of ADC3_IN4 to 8 or ADC123_IN10 to 13, following PCB layout guide line below benefits to isolate the high frequency interference from HSE emitting to ADC input signals nearby.

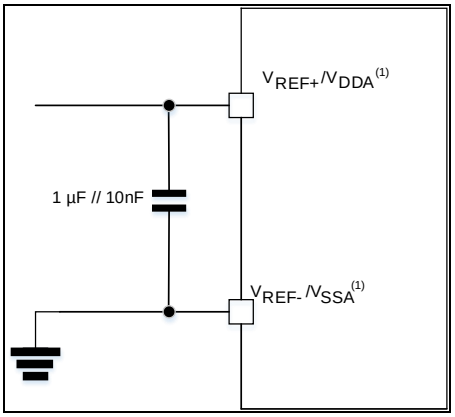
- Use different PCB layers to route ADC_IN signal apart from HSE path
- Do not route ADC_IN signals and HSE path parallel

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



(1) V_{REF+} and V_{REF-} inputs are available only on 144-pin and 100-pin package.

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



(1) V_{REF+} and V_{REF-} inputs are available only on 144-pin and 100-pin package

5.3.20 DAC electrical specifications

Table 61. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.6	-	3.6	V	-
V_{REF+}(3)	Reference supply voltage	2.6	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	13.2	16	kΩ	-
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON)
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output DAC_OUT excursion of the DAC
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{REF+} - 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	1.5	2.5	mV	It gives the maximum output DAC_OUT excursion of the DAC
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} - 1.5 mV	V	
I_{VREF}(3)	DAC DC current consumption in quiescent mode (Standby mode)	-	320	350	μA	With no load, worst case at V_{REF+} = 3.6 V
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	-	520	700	μA	With no load, worst case at V_{REF+} = 3.6 V
DNL(2)	Differential non linearity (difference between two consecutive code-1LSB)	-	±0.5	±1	LSB	Give for the DAC in 12-bit
INL(2)	Integral non linearity (difference between measured value at Code I and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	±1	±2.5	LSB	Give for the DAC in 12-bit
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	±6	±18	mV	-
		-	±5	±20	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(2)	Gain error	-	±0.1	±0.2	%	Give for the DAC in 12-bit
$t_{SETTLING}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	1.5	4	μs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1 LSB)	-	-	1	MS/s	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)	-	-	4	µs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ input code between lowest and highest possible ones
PSRR+(1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	-	-45	dB	No R_{LOAD}, C_{LOAD} ≤ 50 pF

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.
(3) V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Chapter 3 Pinouts and pin descriptions* for further details.

5.3.21 Temperature sensor characteristics

Table 62. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	-	±5	ºC
Avg_Slope(1(2))	Average slope	-4.06	-4.23	-4.39	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	1.16	1.26	1.36	V
t_{START}(3)	Startup time	-	-	100	µs
T_{S_temp}(3)(4)	ADC sampling time when reading the temperature	-	-	17.1	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.
(4) Shortest sampling time can be determined in the application by multiple iterations.

Obtain the temperature using the following formula:

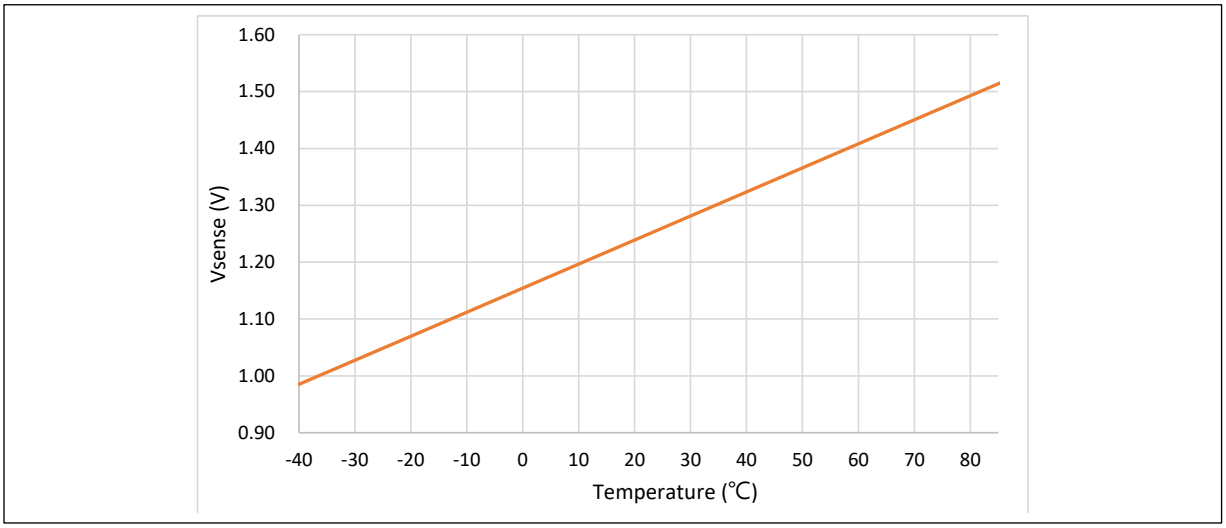
Temperature (in °C) = {(V_{25} - V_{SENSE}) / Avg_Slope} + 25.

Where,

V_{25} = V_{SENSE} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{SENSE} (given in mV/° C).

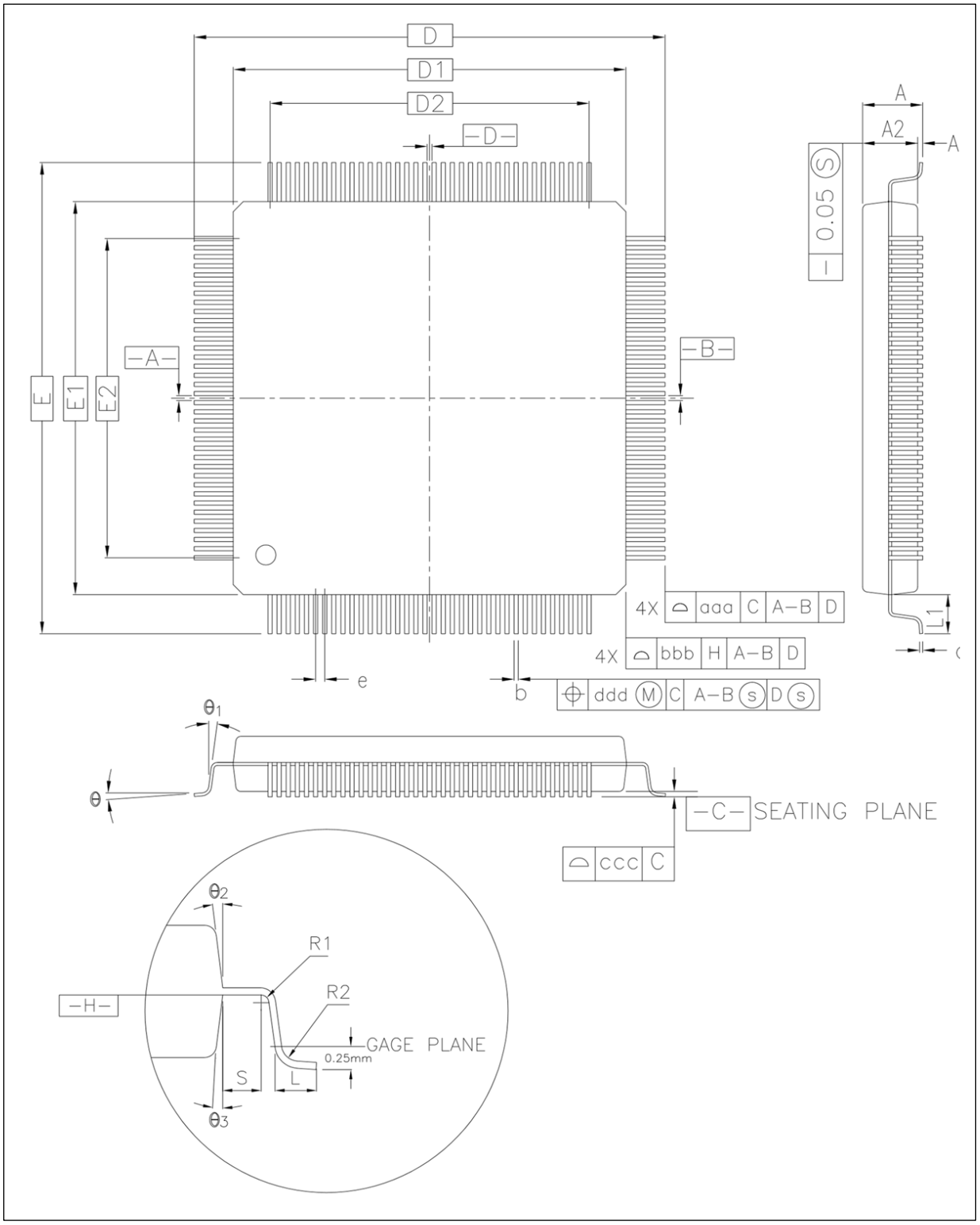
Figure 53. V_{SENSE} versus temperature



6 Package information

6.1 LQFP144 package information

Figure 54. LQFP144 – 20 x 20 mm 144 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 63. LQFP144 – 20 x 20 mm 144 pin low-profile quad flat package mechanical data

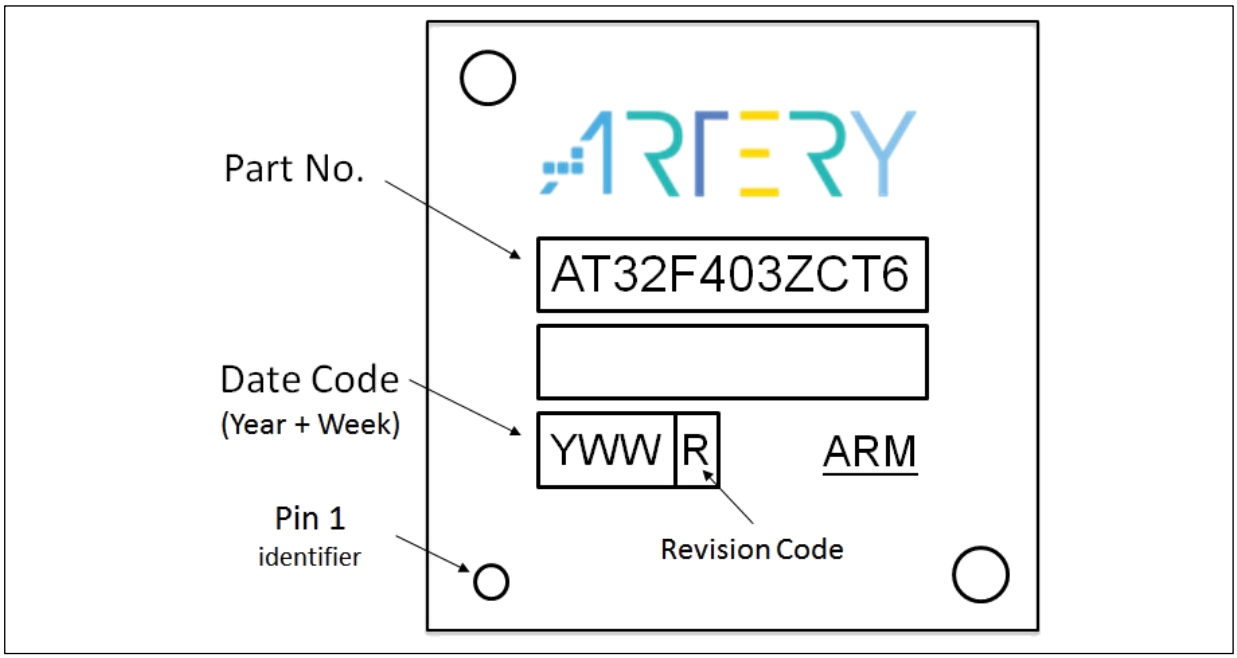
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.09	-	0.20	0.004	-	0.008
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
D2	17.50			0.689		
E	22.00 BSC.			0.866 BSC.		
E1	20.00 BSC.			0.787 BSC.		
E2	17.50			0.689		
e	0.50 BSC.			0.020 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
θ	0°	3.5°	7°	0°	3.5°	7°
ccc	0.08			0.003		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP144

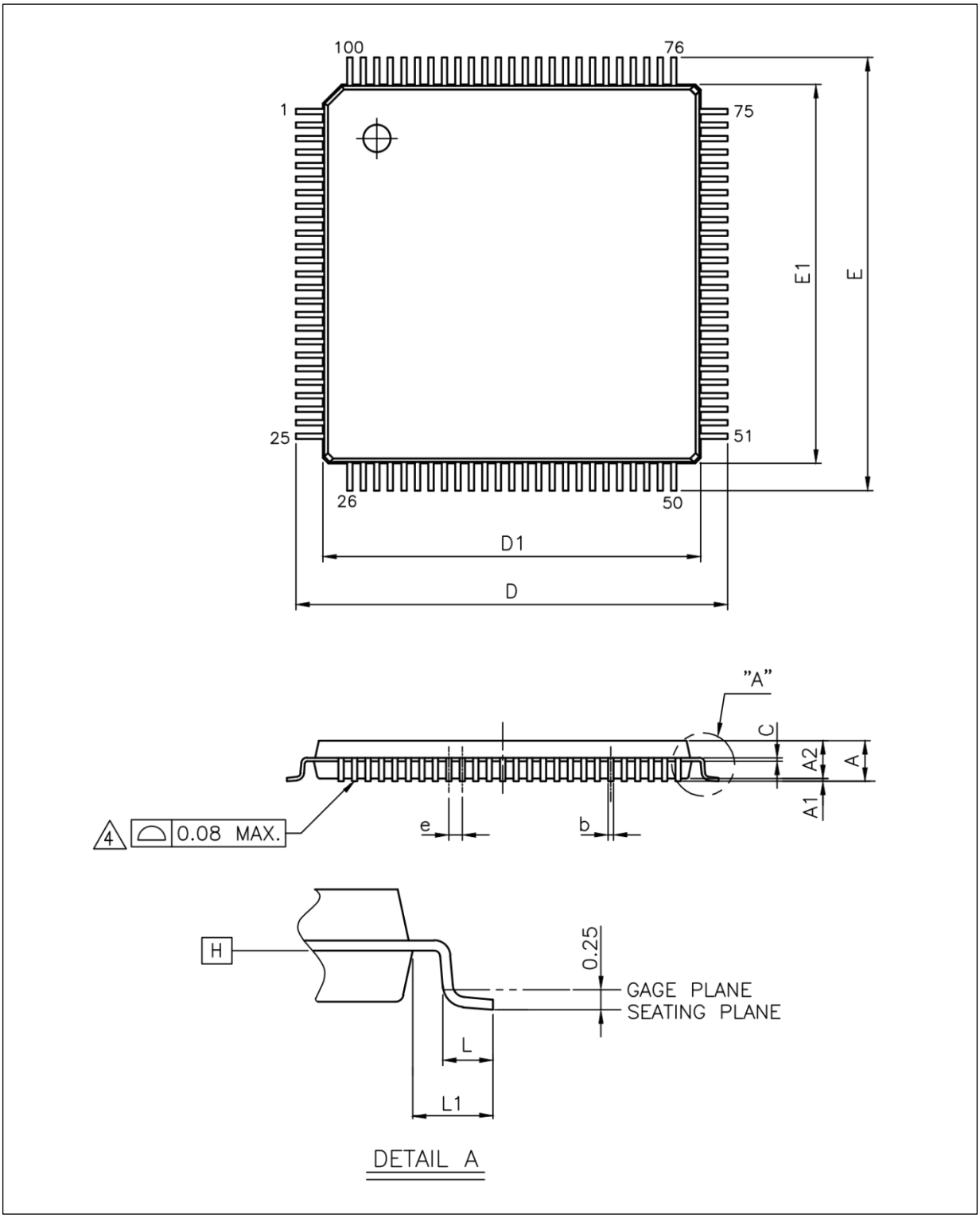
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 55. LQFP144 marking example (package top view)



6.2 LQFP100 package information

Figure 56. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 64. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package mechanical data

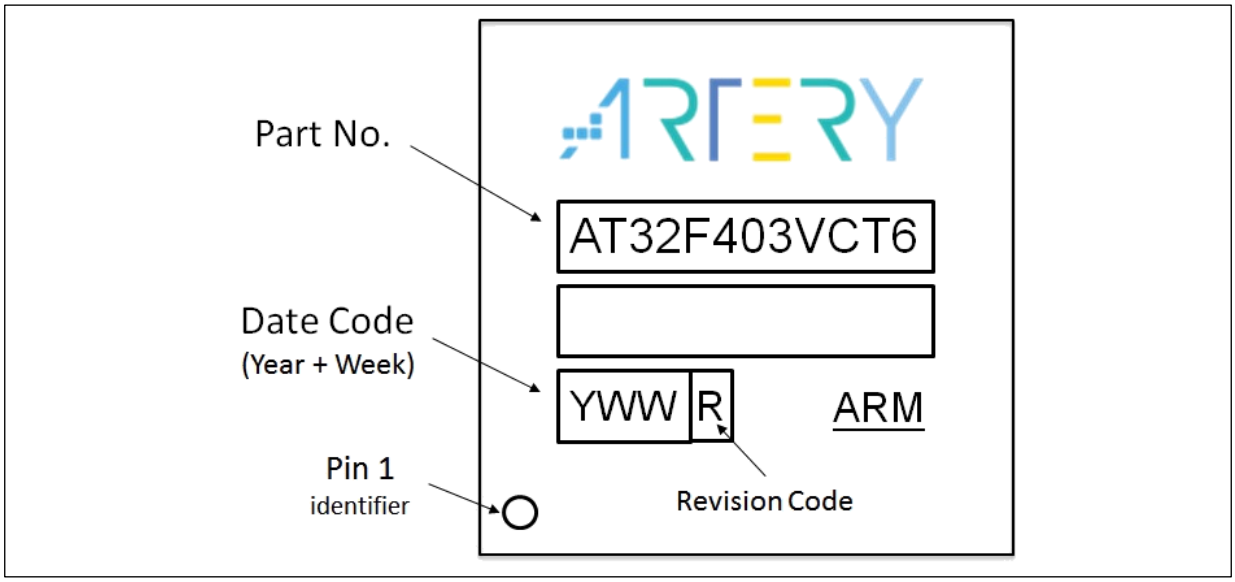
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.26	0.007	0.008	0.010
c	0.10	0.127	0.20	0.004	0.005	0.008
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
e	0.50 BSC.			0.020 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP100

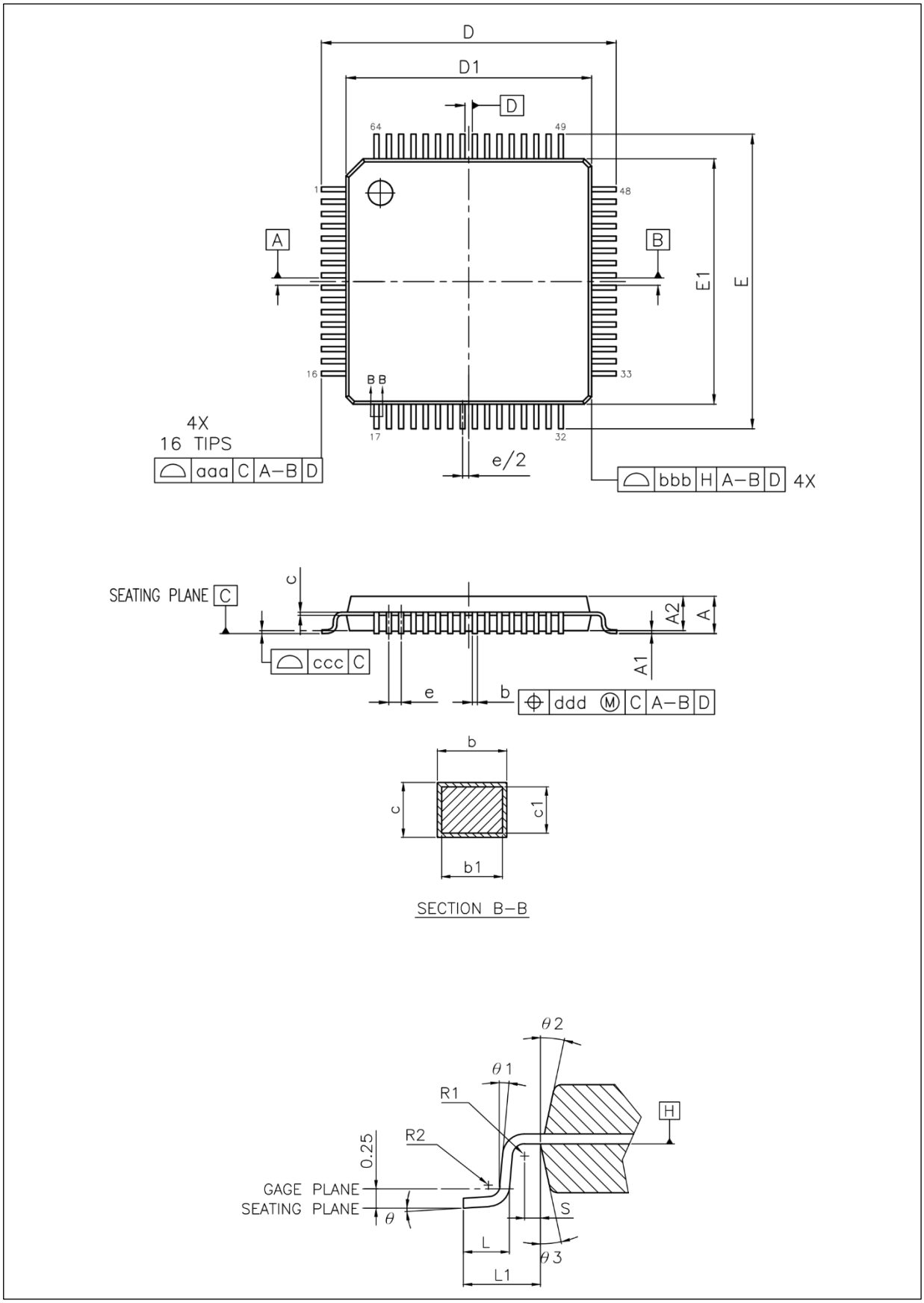
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 57. LQFP100 marking example (package top view)



6.3 LQFP64 package information

Figure 58. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 65. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

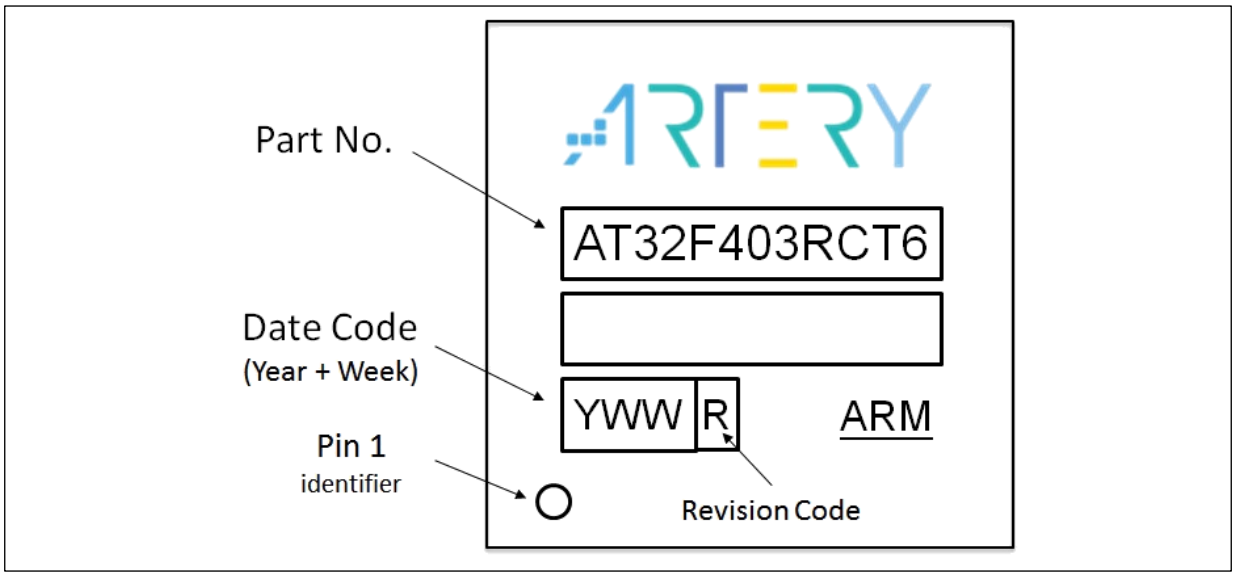
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.09	-	0.20	0.004	-	0.008
D	11.75	12.00	12.25	0.463	0.472	0.482
D1	9.90	10.00	10.10	0.390	0.394	0.398
E	11.75	12.00	12.25	0.463	0.472	0.482
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	0.50 BSC.			0.020 BSC.		
Θ	3.5° REF.			3.5° REF.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
ccc	0.08			0.003		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP64

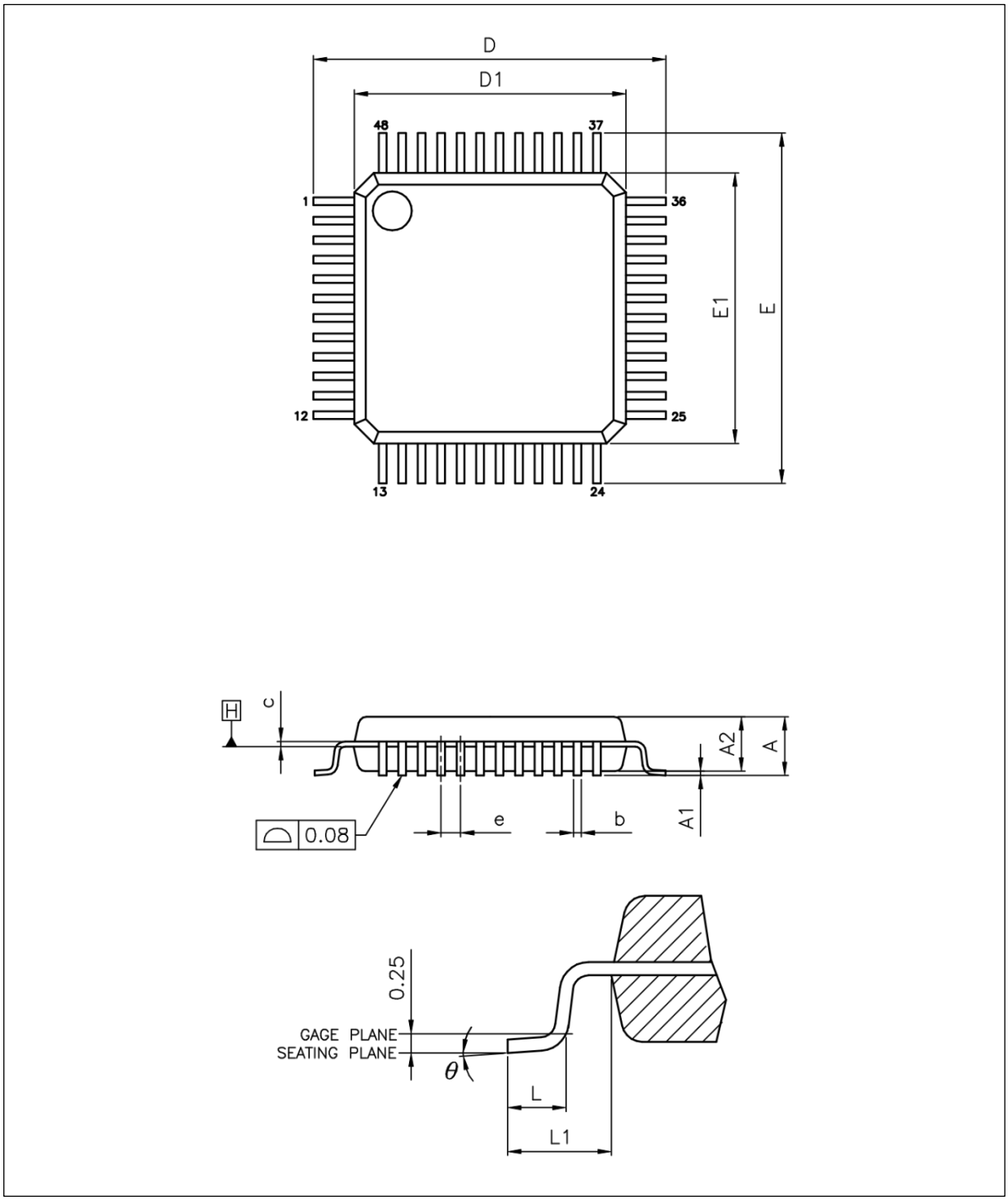
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 59. LQFP64 marking example (package top view)



6.4 LQFP48 package information

Figure 60. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 66. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

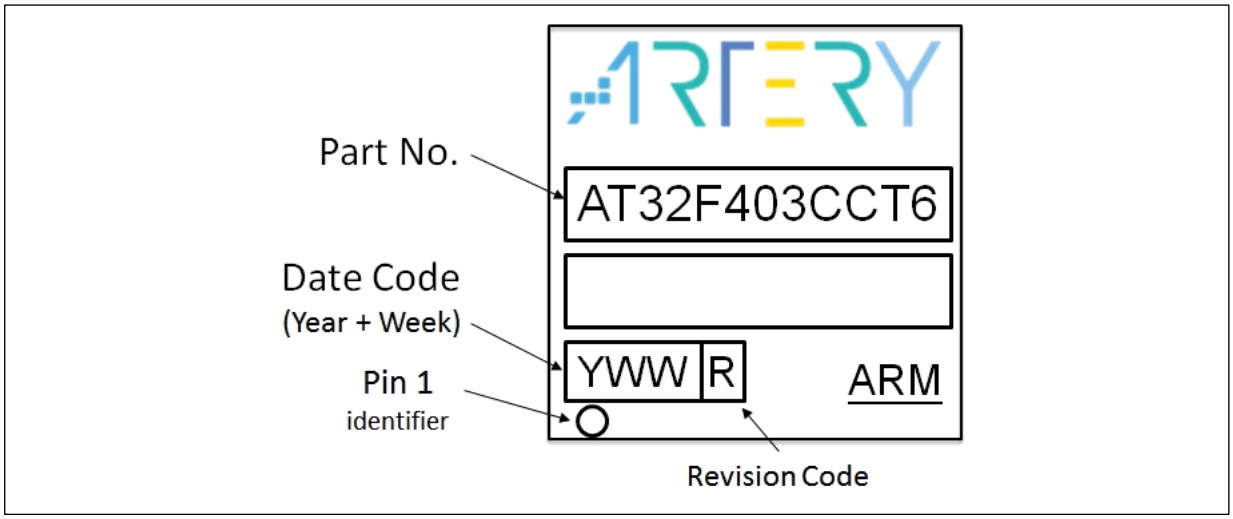
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	-	0.20	0.004	-	0.008
D	9.00 BSC			0.345 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.345 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC.			0.020 BSC.		
Θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP48

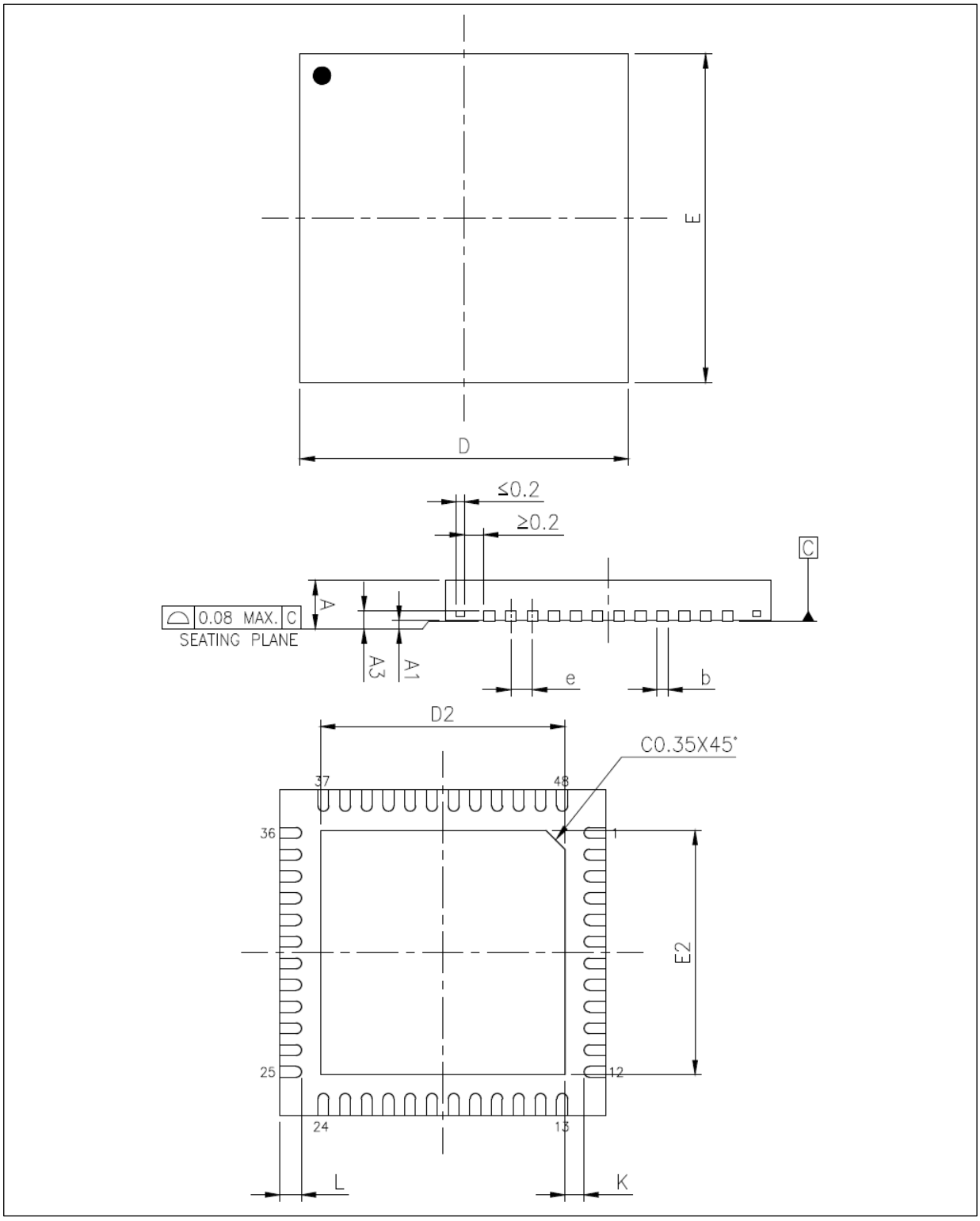
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 61. LQFP48 marking example (package top view)



6.5 QFN48 package information

Figure 62. QFN48 – 6 x 6 mm 48 pin fine-pitch quad flat package outline



(1) Drawing is not in scale.

Table 67. QFN48 – 6 x 6 mm 48 pin fine-pitch quad flat package mechanical data

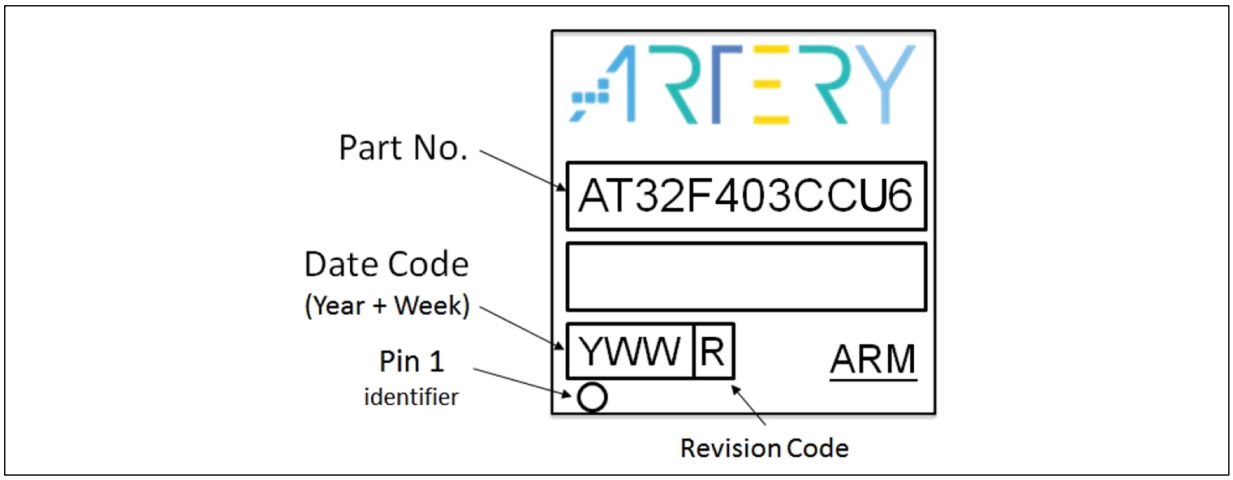
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 BSC.			0.236 BSC.		
D2	4.45	4.50	4.55	0.175	0.177	0.179
E	6.00 BSC.			0.236 BSC.		
E2	4.45	4.50	4.55	0.175	0.177	0.179
e	0.40 BSC.			0.016 BSC.		
K	0.20	-	-	0.008	-	-
L	0.35	0.40	0.45	0.014	0.016	0.018

(1) Values in inches are converted from mm and rounded to 3 decimal digits.
(2) Topside view.

Device marking for QFN48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 63. QFN48 marking example (package top view)



6.6 Thermal characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 10*. The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_j max = T_a max + (P_d max \times \Theta_{JA})$$

Where:

- $T_a$max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_d$max is the sum of P_{INT}max and $P_{I/O}$max ($P_d max = P_{INT} max + P_{I/O} max$),
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins where:

$$P_{I/O} max = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 68. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP144 – 20 × 20 mm / 0.5 mm pitch	48.4	°C/W
	Thermal resistance junction-ambient LQFP100 – 14 × 14 mm / 0.5 mm pitch	52.7	
	Thermal resistance junction-ambient LQFP64 – 10 × 10 mm / 0.5 mm pitch	55.8	
	Thermal resistance junction-ambient LQFP48 – 7 × 7 mm / 0.5 mm pitch	63.6	
	Thermal resistance junction-ambient QFN48 – 6 × 6 mm / 0.4 mm pitch	27.3	

7 Part numbering

Table 69. AT32F403 ordering information scheme

Example: AT32 F 4 0 3 R C T 6

Product family

AT32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4+FPU

Product series

0 = Main Stream

Product application

3 = CAN + USB series

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Z = 144 pins

Internal Flash memory size

C = 256 KBytes of the internal Flash memory

E = 512 KBytes of the internal Flash memory

G = 1 MBytes of the internal Flash memory

Package

T = LQFP

U = QFN

Temperature range

6 = -40 °C to +85 °C

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Artery sales office.

8 Revision history

Table 70. Document revision history

Date	Version	Change
2018.3.19	1.00	Initial release.
2018.6.16	1.01	1. Added *Table 3* to describe the Bootloader supporting part numbers and pin configurations 2. Added *Figure 14* and *Figure 15* to describe the typical current consumption in Stop and Standby modes versus temperature 3. Added *Figure 20* to describe the HSI oscillator frequency accuracy versus temperature 4. Added more description about the PCB layout guide line of ADC_IN signals when HSE is enabled
2018.10.3	1.02	1. Corrected *Table 28* the mass erase time 2. Modified *Table 41* $V_{ESD(HBM)}$ and *Table 42* values 3. Added *Table 54* the value of USB_DP internal pull-up
2019.1.18	1.03	1. Modified the max frequency of HSE crystal/resonator as 25 MHz 2. Added *Figure 13.* Power on reset/power down reset waveform 3. Modified *Table 13* the max of temperature coefficient 4. Deleted *Table 56* R_{ADC} and added *Table 57* and *Table 58* 5. Modified *Table 62* the max of linearity with temperature and startup time; added note (2) to describe the application notice 6. Added *Table 2* note (5) to describe XMC limitation on LQFP100
2019.4.16	1.04	Modified MDEx[1:0] descriptions of *Table 44*
2019.8.6	1.05	*Table 2* added dimemsions of each packages
2020.2.18	1.06	1. Added *Table 45* 2. Modified the priority of PA7, PB10, PB11, PB8 and PB9 in *Table 5*

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