Features

- Single 3.0V - 3.6V or 2.7V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
- 33 MHz Max Clock Frequency
- Byte Program Operation
- Page Program Operation
  - 2048 Pages (256 Bytes/Page) Main Memory
  - Single Cycle Reprogram Capability (Page Erase and Program)
- Supports Optional Page and Block (2 KB or 4 KB) Erase Operations
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Hardware Data Protection Feature for the Top 64 KB of Memory
- Low Power Dissipation
  - 4 mA Active Read Current Typical
  - 2 µA CMOS Standby Current Typical
- 5.0V-tolerant Inputs: SI, SCK, $\overline{CS}$, and $\overline{WP}$ Pins
- 100,000 Program/Erase Cycles Typical
- Data Retention – 20 years

4-megabit 3.0-volt Only or 2.7-volt Only Serial Firmware DataFlash®

AT26DF041

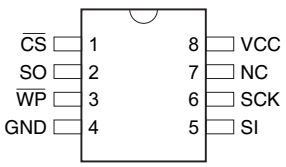
1. Description

The AT26DF041 is a 3.0-volt or 2.7-volt only, serial interface Flash memory ideally suited for a wide variety of program code- and data-storage applications. Its 4,194,304 bits of memory are organized as 2048 pages of 256 bytes each. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash® uses an SPI serial interface to sequentially access its data. The DataFlash supports SPI mode 0 and mode 3. The simple serial interface facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential. To allow for simple in-system reprogrammability, the AT26DF041 does not require high input voltages for programming. The device operates from a single power supply, 3.0V to 3.6V or 2.7V to 3.6V, for both the program and read operations. The AT26DF041 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

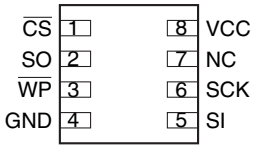
Table 1-1. Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
$\overline{WP}$	Hardware Write Protect Pin

8-SOIC



8-MLF Top View

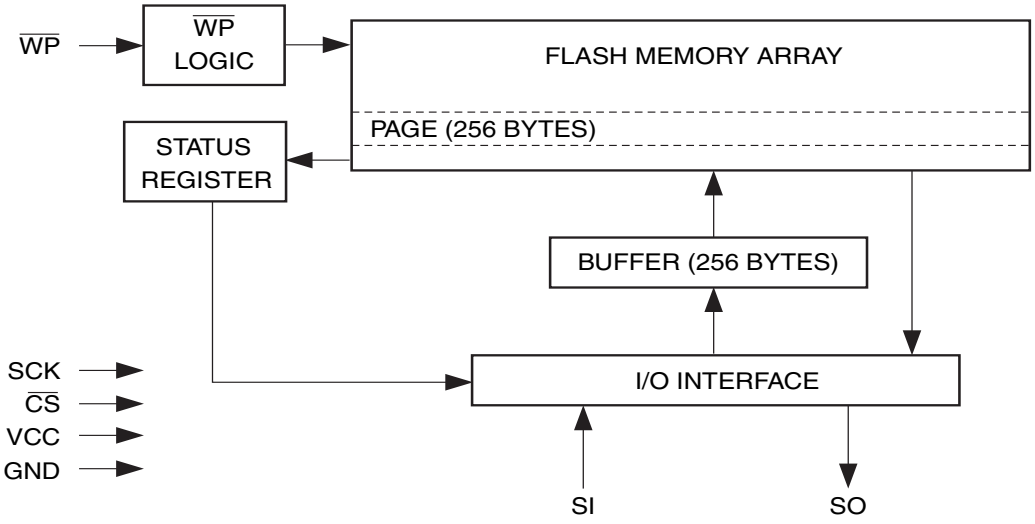


3495B–DFLSH–8/05

To allow for simple in-system reprogrammability, the AT26DF041 does not require high input voltages for programming. The device operates from a single power supply, 3.0V to 3.6V or 2.7V to 3.6V, for both the program and read operations. The AT26DF041 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All program and erase cycles are self-timed, and no separate erase cycle is required when using the Page Program with Auto-Erase feature.

2. Block Diagram



3. Memory Array

To provide optimal flexibility, the memory array of the AT26DF041 is divided into three levels of granularity comprising of sectors, blocks, and pages. The Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur either on a byte basis or on a page-by-page basis; however, the optional erase operations can be performed at the block or page level.

4. Memory Architecture Diagram

Block Erase Detail

Block Address Range	4KB Block Erase (20h Command)	Internal Sector Architecture	2KB Block Erase (50h Command)	Block Address Range
7FFFFh – 7F000h	4KB	Sector 5	2KB	7FFFFh – 7F800h
		Sector 4 (62KB)	2KB	7F7FFh – 7F000h
7EFFFh – 7E000h	4KB		2KB	7EFFFh – 7E800h
			2KB	7E7FFh – 7E000h
7DFFFh – 7D000h	4KB		2KB	7DFFFh – 7D800h
			2KB	7D7FFh – 7D000h
	⋮		⋮	
71FFFh – 71000h	4KB		2KB	71FFFh – 71800h
			2KB	717FFh – 71000h
70FFFh – 70000h	4KB		2KB	70FFFh – 70800h
			2KB	707FFh – 70000h
6FFFFh – 6F000h	4KB	Sector 3 (64KB)	2KB	6FFFFh – 6F800h
			2KB	6F7FFh – 6F000h
6EFFFh – 6E000h	4KB		2KB	6EFFFh – 6E800h
			2KB	6E7FFh – 6E000h
	⋮		⋮	
61FFFh – 61000h	4KB		2KB	61FFFh – 61800h
			2KB	617FFh – 61000h
60FFFh – 60000h	4KB		2KB	60FFFh – 60800h
			2KB	607FFh – 60000h
5FFFFh – 5F000h	4KB	Sector 2 (128KB)	2KB	5FFFFh – 5F800h
			2KB	5F7FFh – 5F000h
5EFFFh – 5E000h	4KB		2KB	5EFFFh – 5E800h
			2KB	5E7FFh – 5E000h
	⋮		⋮	
41FFFh – 41000h	4KB		2KB	41FFFh – 41800h
			2KB	417FFh – 41000h
40FFFh – 40000h	4KB		2KB	40FFFh – 40800h
			2KB	407FFh – 40000h
3FFFFh – 3F000h	4KB	Sector 1 (128KB)	2KB	3FFFFh – 3F800h
			2KB	3F7FFh – 3F000h
3EFFFh – 3E000h	4KB		2KB	3EFFFh – 3E800h
			2KB	3E7FFh – 3E000h
	⋮		⋮	
21FFFh – 21000h	4KB		2KB	21FFFh – 21800h
			2KB	217FFh – 21000h
20FFFh – 20000h	4KB		2KB	20FFFh – 20800h
			2KB	207FFh – 20000h
1FFFFh – 1F000h	4KB	Sector 0 (128KB)	2KB	1FFFFh – 1F800h
			2KB	1F7FFh – 1F000h
1EFFFh – 1E000h	4KB		2KB	1EFFFh – 1E800h
			2KB	1E7FFh – 1E000h
	⋮		⋮	
01FFFh – 01000h	4KB		2KB	01FFFh – 01800h
			2KB	017FFh – 01000h
00FFFh – 00000h	4KB		2KB	00FFFh – 00800h
			2KB	007FFh – 00000h

Page Erase Detail

4KB Block Erase (20h Command)	2KB Block Erase (50h Command)	256 Byte Page Erase (81h Command)	Page Address Range
4KB	2KB	256 Bytes	7FFFFh – 7FF00h
		256 Bytes	7FEFFh – 7FE00h
		256 Bytes	7FDFFh – 7FD00h
		256 Bytes	7FCFFh – 7FC00h
		256 Bytes	7FBFFh – 7FB00h
		256 Bytes	7FAFFh – 7FA00h
		256 Bytes	7F9FFh – 7F900h
		256 Bytes	7F8FFh – 7F800h
	2KB	256 Bytes	7F7FFh – 7F700h
		256 Bytes	7F6FFh – 7F600h
		256 Bytes	7F5FFh – 7F500h
		256 Bytes	7F4FFh – 7F400h
		256 Bytes	7F3FFh – 7F300h
		256 Bytes	7F2FFh – 7F200h
		256 Bytes	7F1FFh – 7F100h
		256 Bytes	7F0FFh – 7F000h
⋮	⋮	⋮	
4KB	2KB	256 Bytes	00FFFh – 00F00h
		256 Bytes	00EFFh – 00E00h
		256 Bytes	00DFFh – 00D00h
		256 Bytes	00CFFh – 00C00h
		256 Bytes	00BFFh – 00B00h
		256 Bytes	00AFFh – 00A00h
		256 Bytes	009FFh – 00900h
		256 Bytes	008FFh – 00800h
	2KB	256 Bytes	007FFh – 00700h
		256 Bytes	006FFh – 00600h
		256 Bytes	005FFh – 00500h
		256 Bytes	004FFh – 00400h
		256 Bytes	003FFh – 00300h
		256 Bytes	002FFh – 00200h
		256 Bytes	001FFh – 00100h
		256 Bytes	000FFh – 00000h

5. Device Operation

The device operation is controlled by instructions from a host processor. The list of instructions and their associated opcodes are contained in Tables 1 through 3. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (serial input) pin. All instructions, addresses and data are transferred with the most significant bit (MSB) first.

Main memory addressing is referenced using the terminology A23 - A0.

5.1 Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two data buffers.

5.1.1 Continuous Array Read

The Continuous Array Read command can be used to sequentially read a continuous stream of data from the device by simply providing a clock signal once the initial starting address has been specified. The device incorporates an internal address counter that automatically increments on every clock cycle.

Two opcodes, 0BH and 03H, can be used for the Continuous Array Read command. The use of each opcode depends on the maximum SCK frequency that will be used to read data from the device. The 0BH opcode can be used at any SCK frequency up to the maximum specified by f_{CAR1}. The 03H opcode can be used for lower frequency read operations up to the maximum specified by f_{CAR2}.

To perform a Continuous Array Read, the $\overline{CS}$ pin must first be asserted and the appropriate opcode must be clocked in. After the opcode has been clocked in, three address bytes (24 bits representing A23 - A0) must be clocked in to specify the starting address location of the first byte to read within the memory array. Since the upper address limit of the device is 07FFFFh, the first five address bits (A23 - A19) will be ignored. If the 0BH opcode is used, one don't care byte must also be clocked in after the three address bytes.

After the three address bytes (and the one don't care byte if using opcode 0BH) have been clocked in, additional pulses on the SCK pin will result in serial data being output on the SO (serial output) pin. The data is always output with the most-significant bit (MSB) of a byte first. When the last bit of the memory array has been read, the device will continue reading back at the beginning of the array (000000h). No delays will be incurred when wrapping around from the end of the array to the beginning of the array.

Deasserting the $\overline{CS}$ pin (a low-to-high transition) will terminate the read operation and put the SO pin into a high-impedance state. The Continuous Array Read command bypasses both data buffers and leaves the contents of the buffers unchanged.

5.1.2 Status Register Read

The status register can be used to determine the device's Ready/Busy status or the device density. To read the status register, an opcode of 05H must be loaded into the device. After the last bit of the opcode is shifted in, the eight bits of the status register, starting with the MSB (bit 7), will be shifted out on the SO pin during the next eight clock cycles. After bit 0 of the status register has been shifted out, the sequence will repeat itself (as long as $\overline{CS}$ remains low

and SCK is being toggled) starting again with bit 7. The data in the status register is constantly updated, so each repeating sequence will output new data.

Table 5-1. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	0	1	1	1	X	$\overline{\text{RDY}}$/BUSY

Ready/Busy status is indicated using bit 0 of the status register. If bit 0 is a 0, then the device is not busy and is ready to accept the next command. If bit 0 is a 1, then the device is in a busy state. The user can continuously poll bit 0 of the status register by stopping SCK at a low level once bit 0 has been output. The status of bit 0 will continue to be output on the SO pin, and once the device is no longer busy, the state of SO will change from 1 to 0. There are five operations which can cause the device to be in a busy state: Page Erase, Block Erase, Byte Program, Page Program, and Page Program with Auto-Erase.

The device density is indicated using bits 5, 4, 3 and 2 of the status register. For the AT26DF041, the four bits are 0, 1, 1 and 1. The decimal value of these four binary bits does not equate to the device density; the four bits represent a combinational code relating to differing densities of Serial DataFlash devices, allowing a total of 16 different density configurations.

Bits 7, 6, and 1 of the status register will contain undefined data.

5.2 Program and Erase Commands

5.2.1 Byte Program

The Byte Program command can be used to program a single byte of data into a previously erased memory location. An erased memory location is one that has all eight bits set to the logical “1” state (a byte value of FFH).

The perform a Byte Program operation, an opcode of 02H must be clocked into the device followed by the 24-bit address sequence denoting which byte location to program. Since the upper address limit of the device is 07FFFFh, address bits A23 - A19 are ignored. After all address bits have been shifted in, the device will take the one byte of data from the SI pin and store it in the internal buffer. If more than one byte of data is clocked in, then only the last byte of data sent will be stored in the buffer.

When the $\overline{\text{CS}}$ pin is deasserted (low-to-high transition), the device will take the one byte stored in the internal buffer and program it into the main memory array at the location specified by A18 - A0. The programming of the byte is internally self-timed and should take place in a maximum time of t_{BP}. During this time, the status register will indicate that the device is busy.

5.2.2 Page Program

An entire previously erased page in the main memory can be programmed by using the Page Program command. Data is first shifted into the internal buffer and then programmed into the specified page in main memory. To start the operation, an opcode of 11H must be clocked into the device followed by the 24-bit address sequence. Address bits A23 - A19 are ignored since the upper address limit of the device is 07FFFFh. After all address bits have been shifted in, the device will take data from the SI pin and store it in the buffer starting at the first byte location specified by A7 - A0. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{\text{CS}}$ pin, the device will program the data stored in the buffer into the specified page in the main memory. It is nec-

essary that the page in the main memory has been previously erased. The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the status register will indicate that the device is busy.

Successive page programming operations without doing a page erase are not recommended. In other words, changing bytes within a page from a “1” to a “0” during multiple page programming operations without erasing that page is not recommended.

5.2.3 Page Program with Auto-Erase

This operation functions similarly to the Page Program command except that the device will automatically erase the addressed page in the main memory before it programs the page, thereby eliminating the need to pre-erase the page or a block of memory. To initiate the operation, the 8-bit opcode of 82H must be clocked into the device followed by the 24-bit address sequence (A23 - A0). Since the upper address limit of the device is 07FFFFh, the five most significant bits (A23 - A19) are ignored. After all address bits are shifted in, the device will take data from the SI pin and store it in the internal buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into the specified page in the main memory. Both the erase and the programming of the page are internally self-timed and should take place in a maximum of time t_{EP}. During this time, the status register will indicate that the part is busy.

Because of the single page erase granularity, care must be taken to preserve data integrity within the memory array when using the Page Program with Auto-Erase command. If multiple pages of data within a sector are modified in a random fashion numerous times while certain pages within the same sector are never modified or modified infrequently, then the system must ensure that each page within the sector is updated/rewritten, or “refreshed”, at least once within every 10,000 cumulative page erase operations to that sector. For example, if the first six pages of a sector are used to store static data and the remaining pages are used to store changing data, then the first six pages of the sector must be “refreshed” within 10,000 cumulative page erase operations to that sector. The pages used to store the changing data do not need to be “refreshed” provided that the pages are updated sequentially or in such a fashion that guarantees that each page is rewritten on a fairly even basis.

5.2.4 Page Erase

The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Page Program or Byte Program commands to be utilized at a later time. To perform a Page Erase, an opcode of 81H must be loaded into the device followed by the 24-bit address sequence. Address bits A23 - A19 are ignored since the upper address limit of the device is 07FFFFh. In addition, address bits A7 - A0 are ignored since a full page of data is being erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register will indicate that the part is busy.

Because of the single page erase granularity, care must be taken to preserve data integrity within the memory array when using the Page Erase command. If multiple pages of data within a sector are modified in a random fashion numerous times while certain pages within the same sector are never modified or modified infrequently, then the system must ensure that each page within the sector is updated/rewritten, or “refreshed”, at least once within every 10,000 cumulative page erase operations to that sector. For example, if the first six pages of a sector are used to store static data and the remaining pages are used to store changing data,

then the first six pages of the sector must be “refreshed” within 10,000 cumulative page erase operations to that sector. The pages used to store the changing data do not need to be “refreshed” provided that the pages are updated sequentially or in such a fashion that guarantees that each page is rewritten on a fairly even basis.

5.2.5 Block Erase (2 Kbytes)

A block of 2 Kbytes (eight pages) can be erased at one time allowing the Page Program or Byte Program commands to be utilized to reduce programming times when writing large amounts of data to the device. To perform a 2 KB Block Erase, an opcode of 50H must be loaded into the device, followed by the 24-bit address sequence. As stated previously, address bits A23 - A19 are ignored. In addition, address bits A10 - A0 are ignored since a full block of eight pages is being erased, but any address within the block can be used. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages to 1s. The erase operation is internally self-timed and should take place in a maximum time of t_{BE1}. During this time, the status register will indicate that the part is busy.

5.2.6 Block Erase (4 Kbytes)

A block of 4 Kbytes (16 pages) can be erased at one time allowing the Page Program or Byte Program commands to be utilized to reduce programming times when writing large amounts of data to the device. To perform a 4 KB Block Erase, an opcode of 20H must be clocked into the device followed by the 24 bit address sequence (A23 - A0), of which address bits A23 - A19 are ignored since the upper address limit of the device is 07FFFFh. In addition, address bits A11 - A0 are ignored since a full block of 16 pages is being erased; however, any address within the block can be used to specify which block to erase. When the $\overline{CS}$ pin is deasserted, the device will erase the selected block of 16 pages to logical 1s. The erase operation is internally self-timed and should take place in a maximum of time of t_{BE2}. During this time, the status register will indicate that the device is busy.

6. Manufacturer and Device ID Read

This instruction allows the user to read the Manufacturer ID, Device ID, and Extended Device Information. A 1-byte opcode, 9FH, must be clocked into the device while the $\overline{CS}$ pin is low. After the opcode is clocked in, the Manufacturer ID, 2 bytes of Device ID and Extended Device Information will be clocked out on the SO pin. The fourth byte of the sequence output is the Extended Device Information String Length byte. This byte is used to signify how many bytes of Extended Device Information will be output. Reading the Extended Device Information String Length (byte 4) and any subsequent information is optional.

6.1 Manufacturer and Device ID Information

6.1.1 Byte 1 – Manufacturer ID

Hex Value	JEDEC Assigned Code							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FH	0	0	0	1	1	1	1	1

Manufacturer ID	1FH = Atmel

6.1.2 Byte 2 – Device ID (Part 1)

Hex Value	Family Code			Density Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
44H	0	1	0	0	0	1	0	0

Family Code	010 = AT26xxx Series
Density Code	00100 = 4-Mbit

6.1.3 Byte 3 – Device ID (Part 2)

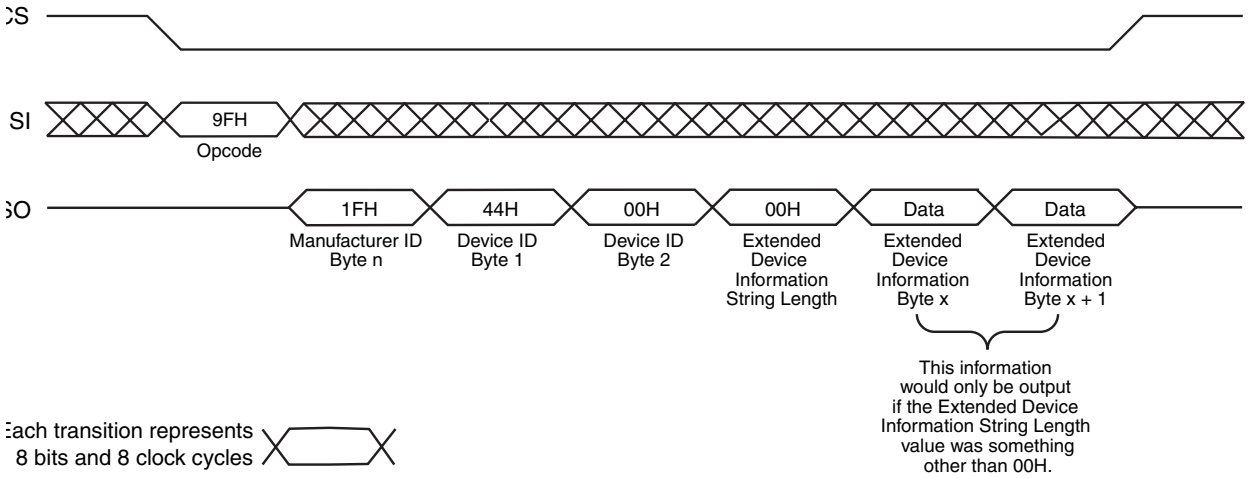
Hex Value	MLC Code			Product Version Code				
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

MLC Code	000 = 1-bit/cell Technology
Product Version	00000 = Initial version

6.1.4 Byte 4 – Extended Device Information String Length

Hex Value	Byte Count							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	0	0	0	0	0	0	0	0

Byte Count	00H = 0 Bytes of Information



Note: Based on JEDEC publication 106 (JEP106), Manufacturer ID data can be comprised of any number of bytes. Some manufacturers may have Manufacturer ID codes that are two, three or even four bytes long with the first byte(s) in the sequence being 7FH. A system should detect code 7FH as a “Continuation Code” and continue to read Manufacturer ID bytes. The first non-7FH byte would signify the last byte of Manufacturer ID data. For Atmel (and some other manufacturers), the Manufacturer ID data is comprised of only one byte.

7. Pin Descriptions

7.1 Serial Input (SI)

The SI pin is an input-only pin and is used to shift data into the device. The SI pin is used for all data input including opcodes and address sequences.

7.2 Serial Output (SO)

The SO pin is an output-only pin and is used to shift data out from the device.

7.3 Serial Clock (SCK)

The SCK pin is an input-only pin and is used to control the flow of data to and from the DataFlash. Data is always clocked into the device on the rising edge of SCK and clocked out of the device on the falling edge of SCK.

7.4 Chip Select ($\overline{CS}$)

The DataFlash is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted on the SI pin, and the SO pin will remain in a high-impedance state. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition on the $\overline{CS}$ pin is required to end an operation.

7.5 Write Protect ($\overline{WP}$)

If the $\overline{WP}$ pin is held low, the top 256 pages (64K-bytes of address locations 07FFFFh to 070000h) of the main memory cannot be reprogrammed. The only way to reprogram the top 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. If this pin and feature are not utilized it is recommended that the $\overline{WP}$ pin be driven high externally.

8. Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI Mode 3. In addition, the SO pin will be in a high-impedance state, and a high-to-low transition on the $\overline{CS}$ pin will be required to start a valid instruction. The SPI mode will be automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state. After power is applied and V_{CC} is at the minimum datasheet value, the system should wait 20 ms before an operational mode is started.

Table 8-1. Read Commands

Command	Opcode		Address Bytes	Dummy Bytes	Data Bytes
Continuous Array Read	0BH	0000 1011	3	1	1+
Continuous Array Read (Low Frequency)	03H	0000 0011	3	0	1+
Status Register Read	05H	0000 0101	0	0	1+
Manufacturer and Device ID Read	9FH	1001 1111	0	0	1+

Table 8-2. Erase and Program Commands

Command	Opcode		Address Bytes	Dummy Bytes	Data Bytes
Page Erase	81H	1000 0001	3	0	0
Block Erase (2 KB)	50H	0101 0000	3	0	0
Block Erase (4 KB)	20H	0010 0000	3	0	0
Byte Program	02H	0000 0010	3	0	1
Page Program	11H	0001 0001	3	0	256
Page Program with Auto-Erase	82H	1000 0010	3	0	256

Notes: 1. Address bits A23 - A19 are don't care bits because the upper address limit of the device is 07FFFFh.
Address bits A7 - A0 are don't care for the Page Erase Command.
Address bits A10 - A0 are don't care for the 2 KB Block Erase Command.
Address bits A11 - A0 are don't care for the 4 KB Block Erase Command.

9. Electrical Specifications

Table 9-1. Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9-2. DC and AC Operating Range

		AT26DF041
Operating Temperature (Case)	Ind.	-40°C to 85°C
V_{CC} Power Supply[1]		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified datasheet value, the system should wait 20 ms before an operational mode is started.

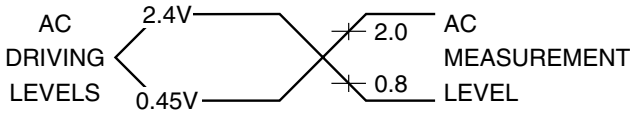
Table 9-3. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{WP}$ = V_{CC}, all inputs at CMOS levels		2	10	µA
I_{CC1}	Active Current, Read Operation	f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		8	15	mA
		f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		15	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

Table 9-4. AC Characteristics

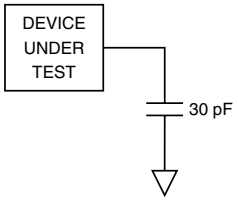
Symbol	Parameter	AT26DF041				Units
		2.7V V_{cc}		3.0V V_{cc}		
		Min	Max	Min	Max	
f_{SCK}	SCK Frequency		25		33	MHz
f_{CAR1}	SCK Frequency for Continuous Array Read		25		33	MHz
f_{CAR2}	SCK Frequency for Continuous Array Read (Low Frequency)		20		20	MHz
t_{WH}	SCK High Time	18		13		ns
t_{WL}	SCK Low Time	18		13		ns
t_{CS}	Minimum $\overline{CS}$ High Time	100		100		ns
t_{CSS}	$\overline{CS}$ Setup Time	20		20		ns
t_{CSH}	$\overline{CS}$ Hold Time	20		20		ns
t_{SU}	Data In Setup Time	5		3		ns
t_{H}	Data In Hold Time	5		3		ns
t_{HO}	Output Hold Time	0		0		ns
t_{DIS}	Output Disable Time		12		10	ns
t_{V}	Output Valid		15		11	ns
t_{EP}	Page Erase and Programming Time		12		12	ms
t_{BP}	Byte Program Time		30		30	µs
t_{P}	Page Programming Time		5		5	ms
t_{PE}	Page Erase Time		8		8	ms
t_{BE1}	Block Erase (2 KB) Time		10		10	ms
t_{BE2}	Block Erase (4 KB) Time		12		12	ms

10. Input Test Waveforms and Measurement Levels



t_R, t_F < 3 ns (10% to 90%)

11. Output Test Load



12. AC Waveforms

Two different timing diagrams are shown below. Waveform 1 shows timing that is compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3. The setup and hold times for the SI signal are referenced to the low-to-high transition on the SCK signal.

Figure 12-1. Waveform 1 – SPI Mode 0

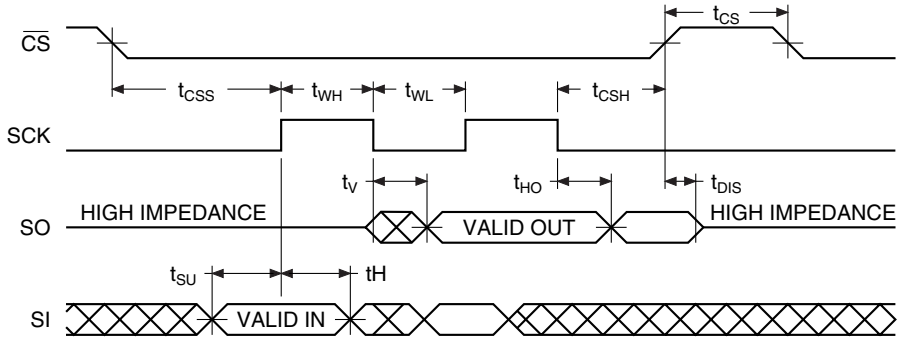


Figure 12-2. Waveform 2 – SPI Mode 3

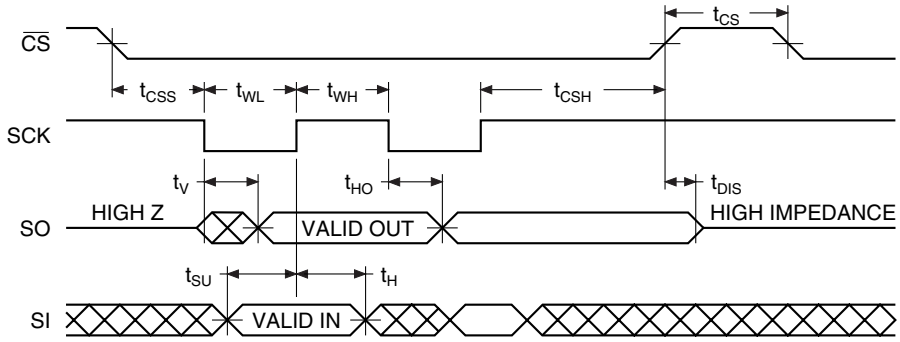
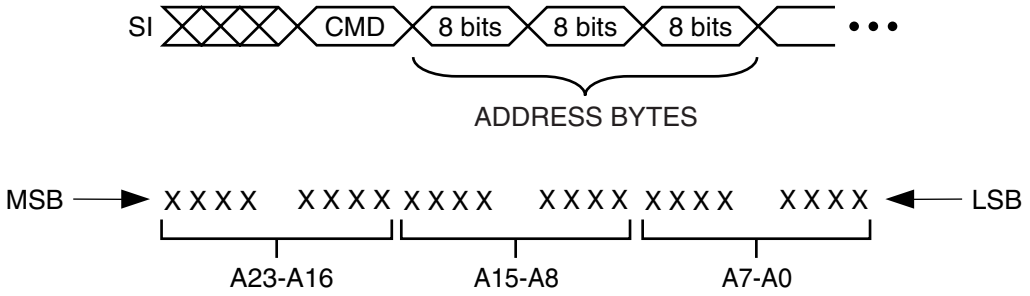


Figure 12-3. Command Sequence for Read/Write Operations (except Status Register Read)



13. Write Operations

The following waveforms illustrate the various write sequences available.

Figure 13-1. Byte Program

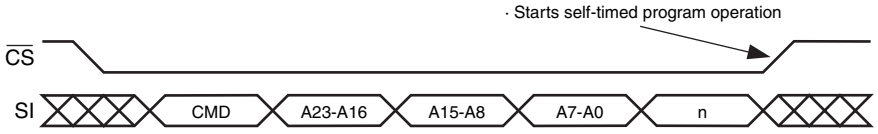
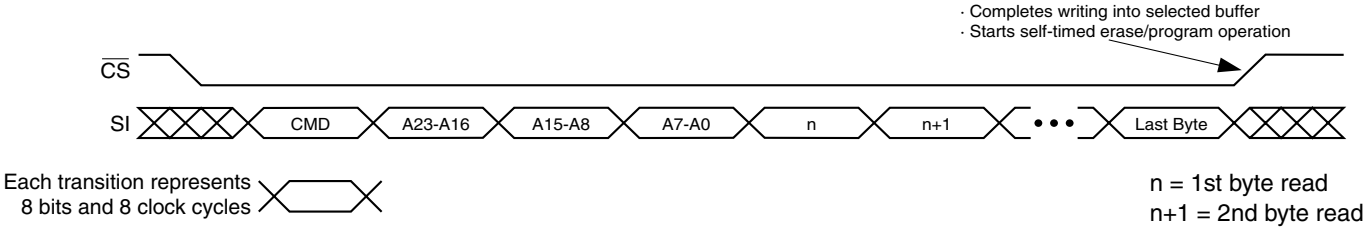


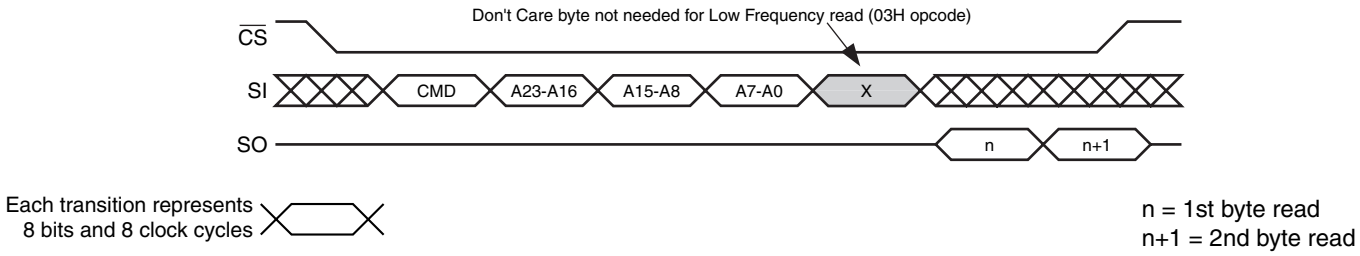
Figure 13-2. Page Program



14. Read Operations

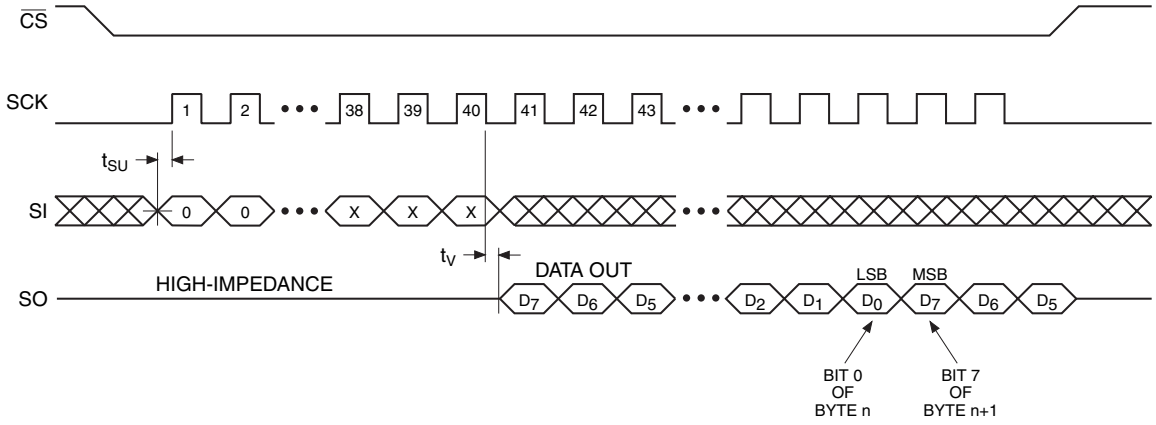
The following waveform illustrates the read sequence available.

Figure 14-1. Continuous Array Read

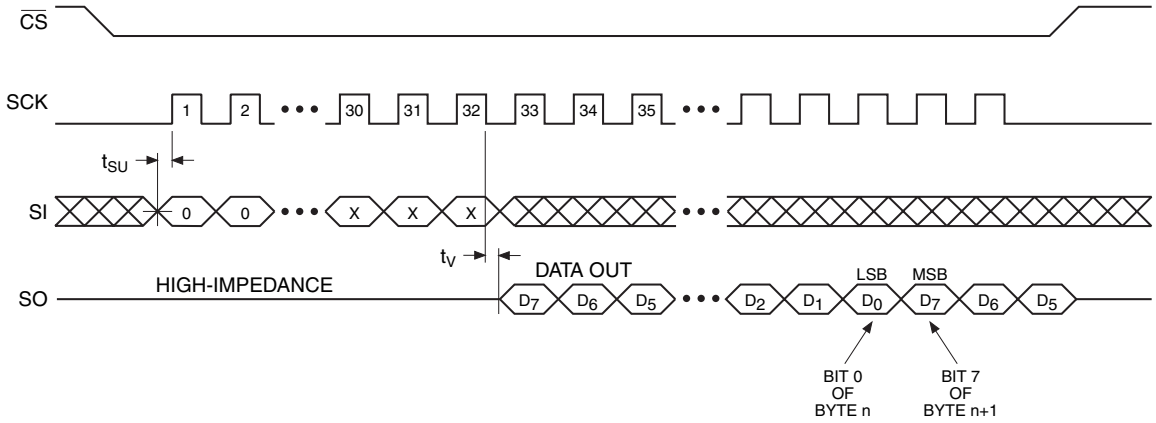


15. Detailed Bit-level Read Timing – SPI Mode 0

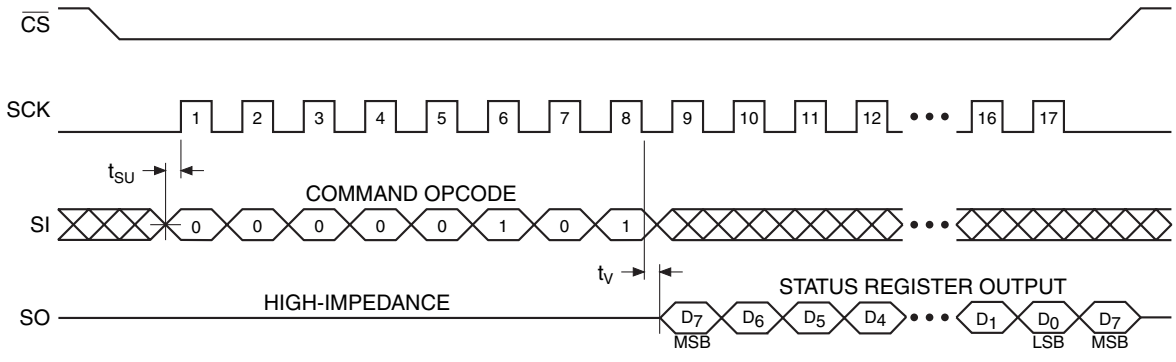
15.1 Continuous Array Read (Opcode 0BH)



15.2 Continuous Array Read (Low Frequency: Opcode 03H)

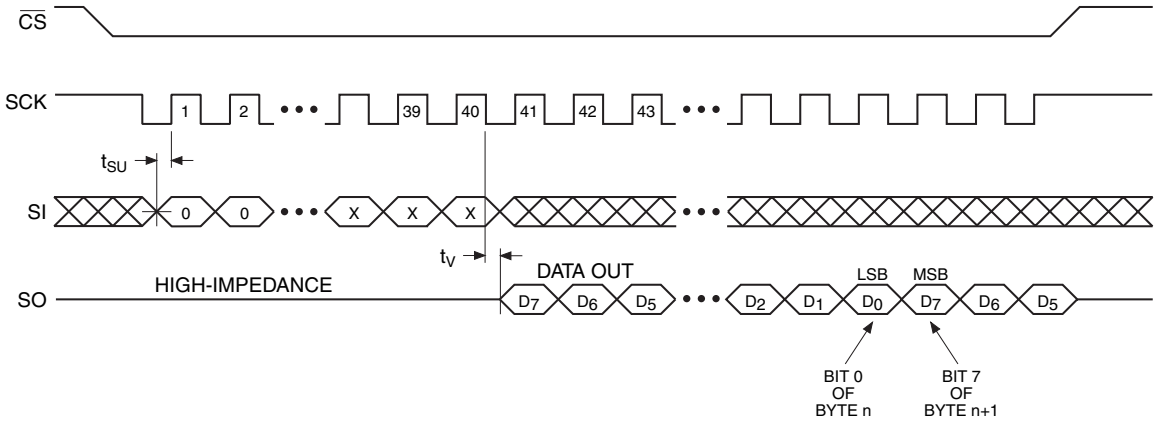


15.3 Status Register Read (Opcode: 05H)

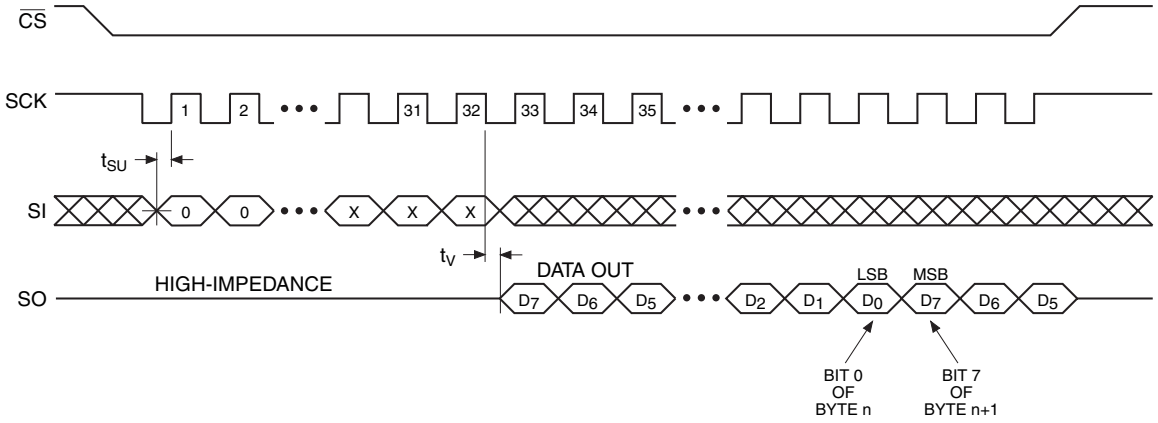


16. Detailed Bit-level Read Timing – SPI Mode 3

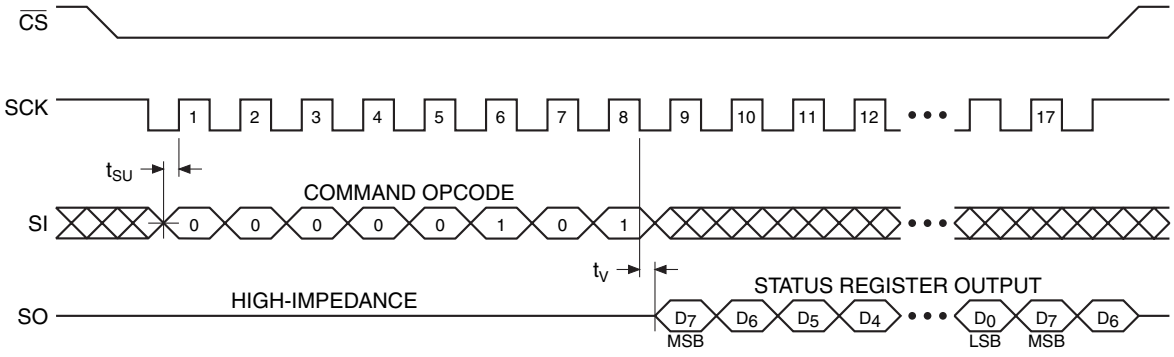
16.1 Continuous Array Read (Opcode 0BH)



16.2 Continuous Array Read (Low Frequency: Opcode 03H)



16.3 Status Register Read (Opcode: 05H)



17. Ordering Information

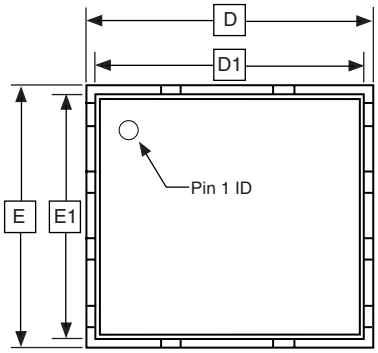
17.1 Green Packages (Pb/Halide-free/RoHS Compliant)

f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
33	15	0.01	AT26DF041-MU AT26DF041-SU	8M1-A 8S2	Industrial (-40°C to 85°C)

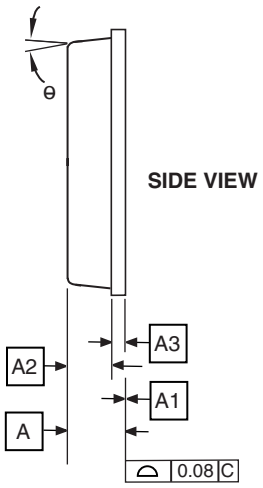
Package Type	
8M1-A	8-contact, 5 mm x 6 mm Very Thin Micro Lead-Frame Package (MLF)
8S2	8-lead, 0.209" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)

18. Packaging Information

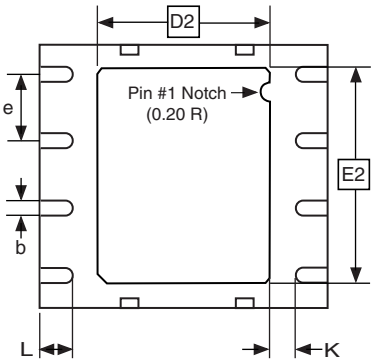
18.1 8M1-A – MLF



TOP VIEW



SIDE VIEW



BOTTOM VIEW

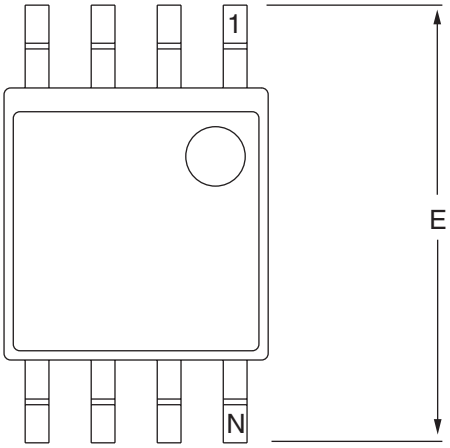
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.85	1.00	
A1	–	–	0.05	
A2		0.65 TYP		
A3		0.20 TYP		
b	0.35	0.40	0.48	
D		6.00 TYP		
D1		5.75 TYP		
D2	3.20	3.40	3.60	
E		5.00 TYP		
E1		4.75 TYP		
E2	3.80	4.00	4.20	
e		1.27		
L	0.50	0.60	0.75	
θ			12°	
K		1.30 REF		

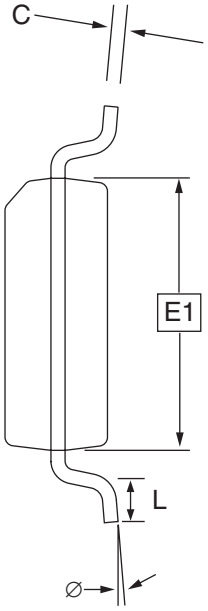
12/6/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8M1-A,** 8-lead, 6 x 5 x 1.00 mm Body, Very Thin Dual Flat Package No Lead (MLF)	8M1-A	A

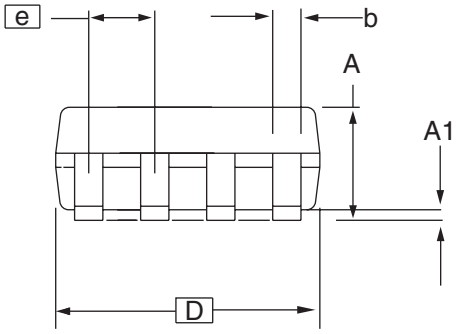
18.2 8S2 – EIAJ SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
∅	0°		8°	
e	1.27 BSC			4

Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b and C apply to pb/Sn solder plated terminal. The standard thickness of the solder layer shall be 0.010 +0.010/–0.005 mm.

10/7/03

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8S2**, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	**DRAWING NO.** 8S2	**REV.** C

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