Feature

- 2.6V to 5.5V Supply Voltage Operating Range.
- 1.2MHz Fixed Switching Frequency.
- Current-Mode PWM Step-Up Regulator
  Main High-Power Output up to 15V
  Typical ± 1% Accuracy
  Built-In N-MOS, $R_{ds(on)} \fallingdotseq 0.25\Omega$ (Typ.)
  Current-Limit Comparator
- Negative Charge-Pump Output Voltage Down to –30 V.
- Positive Charge-Pump Output Voltage Up to 30 V.
- Internal Power-On Sequencing , Soft-Start.
- Thermal Protection , Short Circuit Protection.
- 1uA Shutdown Current.
- 1.5mA Quiescent Current.
- 16-pin TSSOP Package.

Application

- TFT-LCD Notebook Display
- TFT-LCD Desktop Monitor Panels.
- Car Navigation Systems.

Description

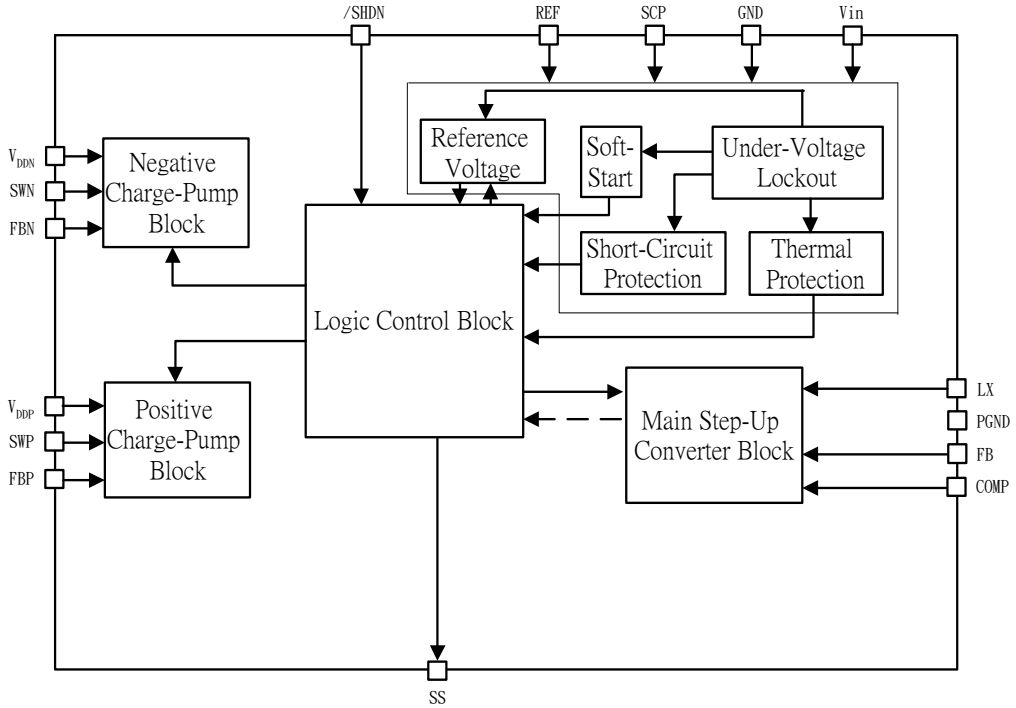
The AT1731A DC-DC converter supply a compact and small power supply solution to provide the regulated voltages required by thin film transistor (TFT) LCD display. A built-in power sequence control.

The main step-up DC-DC converter is a high-Frequency 1.2 MHz current-mode PWM regulator with a built-in 0.25Ω N-MOS that allows the use of ultra-small inductors and ceramic capacitor to generate an externally set output voltage up to 15V. It provides fast transient response to pulsed loads while operating with efficiencies over 85%.

The two built-in charge-pump regulators are used to generate the TFT gate-on and gate-off supplies and can adjust gate-on and gate-off output voltage with external resistive divider between gate-off/on output voltage and ground.

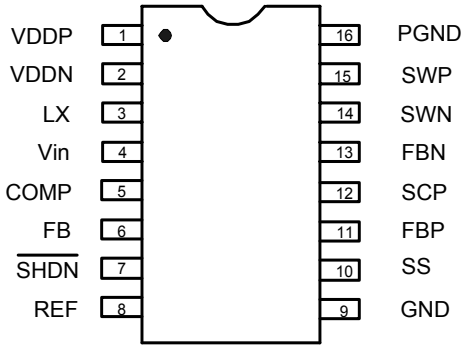
AT1731A is available in TSSOP- 16 package.

Block Diagram



Aimtron reserves the right without notice to change this circuitry and specifications.

Pin Configurations



Ordering Information

Part Number	Package	Marking
AT1731AP	TSSOP-16	□□□□□□ Date Code
AT1731AP_GRE	TSSOP-16 , Green	□□□□□□ , Date code with one bottom line

□□□□□□: Date Code

**For more marking information, contact our sales representative directly*

Pin Description

Pin N0.	Symbol	I / O	Description
1	VDDP	P	Positive Charge-Pump Driver Supply Voltage. Bypass to power ground with 0.1uF capacitor.
2	VDDN	P	Negative Charge-Pump Driver Supply Voltage. Bypass to power ground with 0.1uF capacitor.
3	LX	I	Main Step-up Regulator N-MOS Drain. Place output diode and inductor.
4	Vin	P	Input voltage pin of the device .Vin may range from 2.6V to 5.5V
5	COMP	O	Compensation pin for the main step-up converter. A series RC is connected to this pin.
6	FB	I	Main Step-Up Regulator Feedback Input. Connect a resistive divider from main output to FB to analog ground.
7	/SHDN	I	Active-low shutdown control input. Pull SHDN low to force the controller into shutdown. If unused, connect SHDN to Vin for normal operation.
8	REF	O	Internal Reference Output. External load capability up to 50uA.
9	GND	P	Analog Ground.
10	SS	I	Soft-start input. The capacitor connected to this pin to sets the current-limited start time.
11	FBP	I	Positive Charge-Pump Regulator Feedback Input. Connect a resistive divider from the positive charge-pump output to FBP to analog ground.
12	SCP	I	Short Circuit Protection.
13	FBN	I	Negative Charge-Pump Regulator Feedback Input. Connect a resistive divider from the negative charge-pump output to FBN to the reference.
14	SWN	O	Negative Charge-Pump Driver Output. Output high level is VDDN and low level is PGND.
15	SWP	O	Positive Charge-Pump Driver Output. Output high level is VDDP and low level is PGND.
16	PGND	P	Power Ground.

Absolute Maximum Ratings *1

Parameter		Rated Value	unit
Vin , SHDN , SS Voltage		+6	V
LX , SWP , SWN Voltage		+18	V
COMP, REF, FB, FBN, FBP voltage		Vin + 0.3	V
Quiescent Current		2.5	mA
Continuous power dissipation (TSSOP-16,Ta=+70^{O}C)		650	mW
Junction Temperature		150	℃
Lead Temperature (Soldering 10 sec)		260	℃
Storage Temperature		-40~150	℃
ESD Susceptibility *2	HBM	2	KV
	MM	200	V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operation Conditions

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power supply voltage	Vcc	2.6	—	5.5	V
Operating temperature	Top	-30	+25	+85	℃

Electrical Characteristics

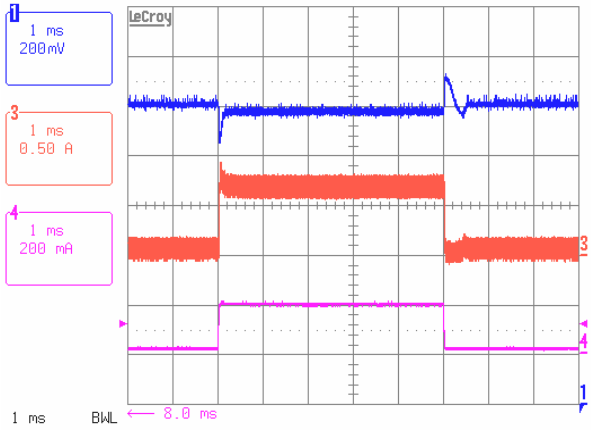
(Vin=3.0V, SHDN=Vin, VDDP=VDDN=10V, Ta=+25℃, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max	Units
Input operating voltage	Vin		2.6	—	5.5	V
Input under-voltage threshold	V_{UVLO}	Vin Rising	2.45	2.5	2.55	V
Vin UVLO hysteresis			—	120	—	mV
Vin Quiescent Current	Iin	V_{FB}=V_{FBP}=1.23V, V_{FBN}= - 0.2V		1	1.5	mA
Vin Shutdown Current	I_{SHDN}	SHDN=GND		1	10	uA
VDDP Quiescent Current	I_{VDDP}	V_{FBP}=1.5V		0.5	0.8	mA
VDDP Shutdown Current		SHDN=GND, VDDP=15V		1	10	uA
VDDN Quiescent Current	I_{VDDN}	V_{FBN}= - 0.2V		0.5	0.8	mA
VDDN Shutdown Current		SHDN=GND, VDDN=15V		1	10	uA
Main Step-Up Converter						
Main Output Voltage Range	V_{MAIN}		Vin		15	V
Feedback Regulation voltage	V_{FB}	Ta=+25℃	1.21	1.23	1.24	V
FB Input Bias Current	I_{FB}	V_{FB}=1.23V	-50	—	50	nA
Operating Frequency	f_{OSC}	Ta=+25℃	1.1	1.2	1.3	MHz
Oscillator Maximum Duty Cycle			80	85	90	%
Load Regulation		0 mA<I_{LX}<300 mA		0.2		%
Line Regulation		2.6V < Vin < 5.5V		0.1		%/V
Trans-conductance				317		us
LX Switch On-Resistance	$R_{LX-DS(ON)}$	I_{LX}=300mA		0.25	0.5	Ω
LX Leakage Current	I_{LX}	V_{LX}=15V		0.1	20	uA
LX Current Limit	I_{LIM}	Vin=3.3V	2.0	2.2	2.5	A
Maximum RMS LX Current				1.87		A
Soft-Start — Current	Iss			2		uA
Soft-Start — Reset switch resistance	R_{SS}			100		Ω
Short- circuit Capacitor charge current			-	1.0	-	uA
Negative Charge-Pump						
VDDN Input Supply Range	V_{DDN}		Vin		15	V
Operating Frequency	f_{CHN}		0.5 x f_{OSC}			Hz
FBN Feedback Regulation Voltage	V_{FBN}		-50	0	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN}=0V	-50		+50	nA
P-ch On-Resistance	$R_{PCH-DS(ON)}$			5	10	Ω
N-ch On-Resistance	$R_{NCH-DS(ON)}$	V_{FBN}=+50mV		2	4	Ω
		V_{FBN}=-50mV	20			KΩ
Maximum RMS SWN Current				50		mA
Positive Charge-Pump						
VDDP Input Supply Range	V_{DDP}		Vin		15	V
Operating Frequency	f_{CHP}		0.5 x f_{OSC}		Hz	
FBP Feedback Regulation Voltage	V_{FBP}		1.21	1.23	1.24	V
FBP Input Bias Current	I_{FBP}	V_{FBP}=1.23V	-50		+50	nA
P-ch On-Resistance	$R_{PCH-DS(}$			5	10	Ω

	ON)					
N-ch On-Resistance	$R_{NCH-DS(ON)}$	V_{FBP}=1.2V		2	4	Ω
		V_{FBP}=1.24V	20			KΩ
Maximum RMS SWP Current				30		mA
Reference						
Reference Voltage	V_{REF}	-2uA <I_{REF} <50uA	1.21	1.23	1.24	V
Reference Under-voltage Threshold			0.9	1.06	1.16	V
Logic Signals						
SHDN input low voltage		0.4V hysteresis			0.9	V
SHDN input high voltage			2.1			V
SHDN input current	I_{SHDN}			0.01	1	uA
Thermal Shutdown				160		℃

Typical Operating Characteristics

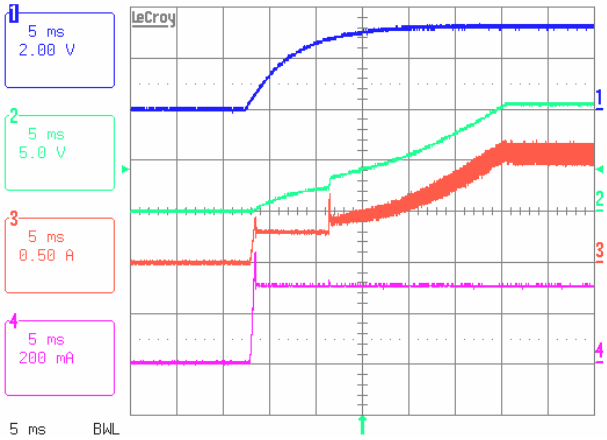
Load-Transient Response Vin=3.3V, Vmain=10V



CH1:V_{MAIN}, CH3:I_{LX}, CH4:I_{MAIN}

I_{MAIN}=200mA to 2mA

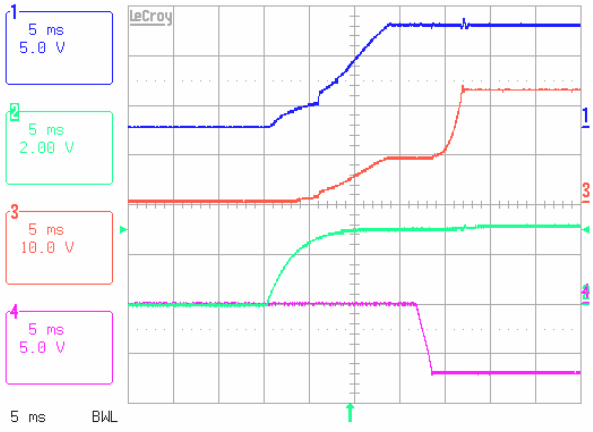
Main Boost Step-Up waveform with Load



CH1:SHDN, Ch2:V_{MAIN}, CH3:I_{LX}, CH4:I_{MAIN}

I_{MAIN}=300mA

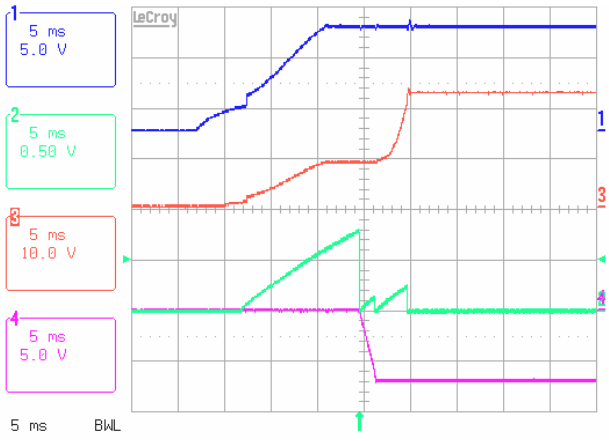
Power-Up Sequence



CH1: V_{MAIN}, Ch2: V_{POS}, CH3: SHDN, CH4:V_{NEG}

I_{MAIN}=300mA,I_{NEG}=20mA,I_{POS}=20mA

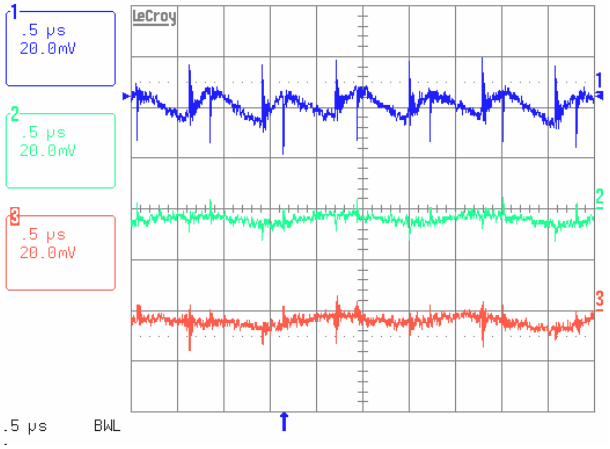
Power-Up Sequence



CH1:V_{MAIN}, CH2: Soft-Start, CH3: V_{POS}, Ch4: V_{NEG}

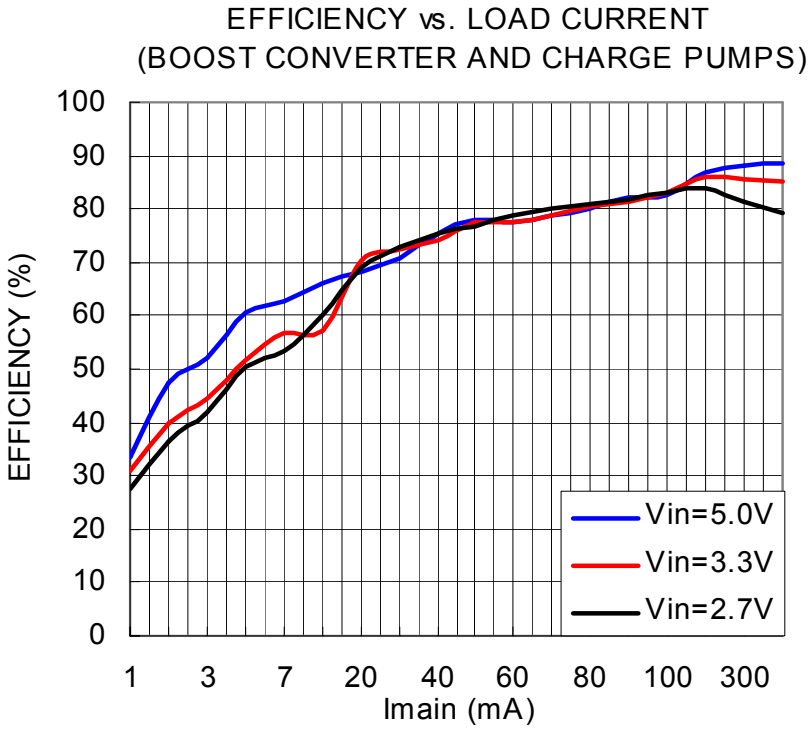
I_{MAIN}=300mA,I_{NEG}=20mA,I_{POS}=20mA

Ripple Waveform

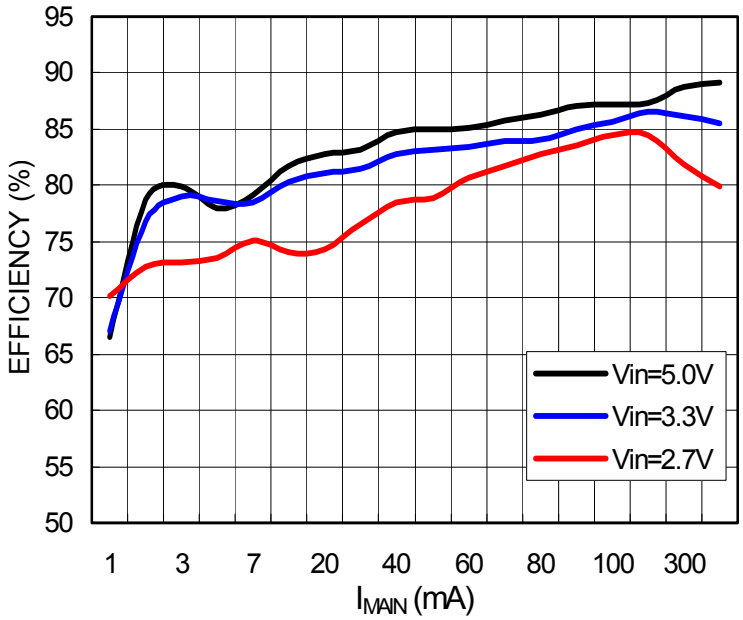


CH1:V_{MAIN}, CH2:V_{POS}, CH3:V_{NEG},

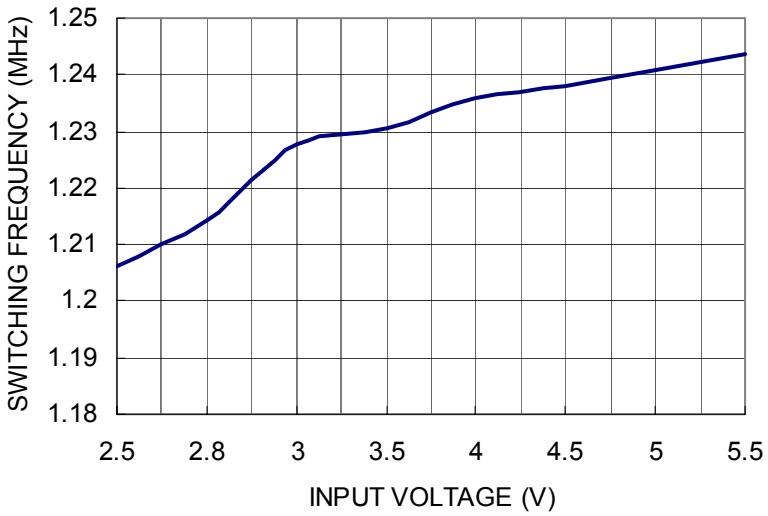
I_{MAIN}=300mA, I_{NEG}=20mA,I_{POS}=20mA



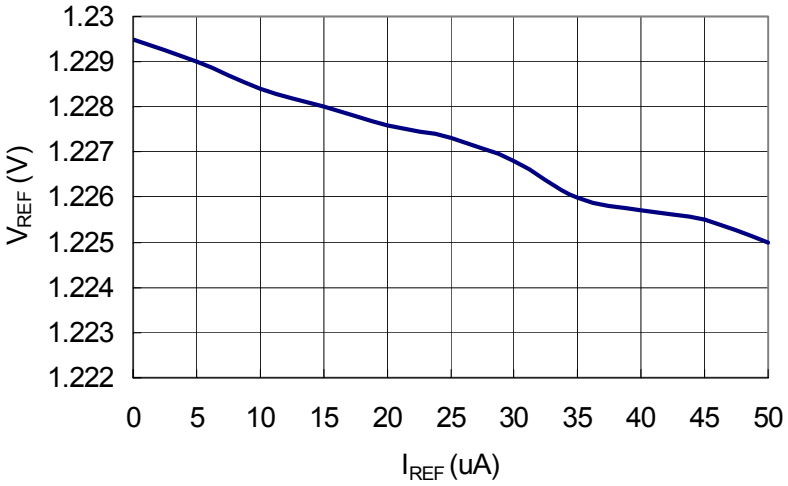
MAIN STEP-UP
CONVERTER EFFICIENCY vs. LOAD CURRENT
(BOOST ONLY)



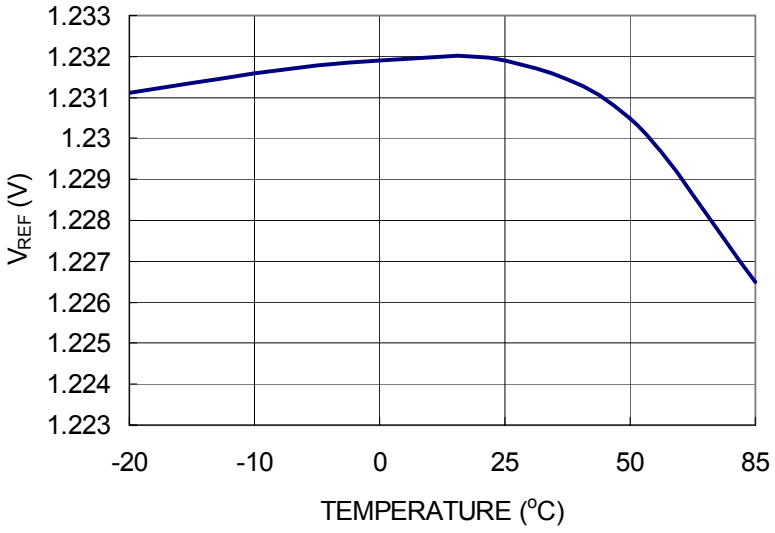
SWITCHING FREQUENCY vs. INPUT VOLTAGE

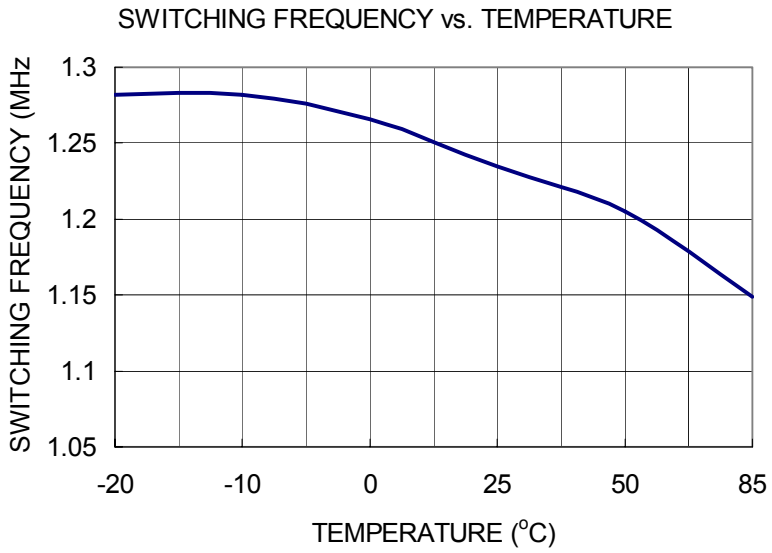


REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



REFERENCE VOLTAGE vs. TEMPERATURE




SWITCHING FREQUENCY vs. TEMPERATURE
SWITCHING FREQUENCY (MHz
1.3
1.25
1.2
1.15
1.1
1.05
-20
-10
0
25
50
85
TEMPERATURE (°C)

Typical Application Circuit

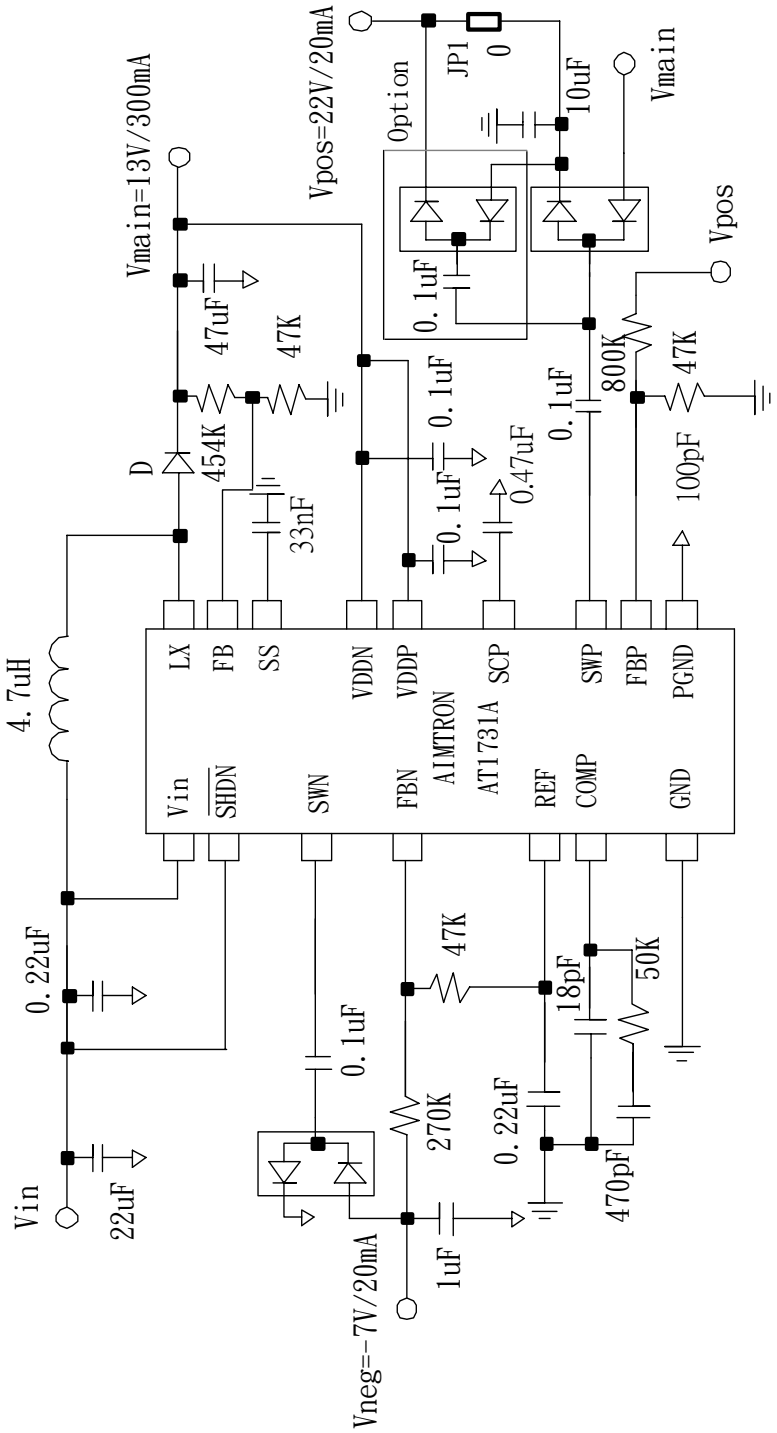


Figure 1. Standard Application Circuit

Function Description

The AT1731A is a multiple-output DC-DC converter IC which is designed primarily for use in thin-film transistor (TFT) liquid crystal display (LCD) applications. It features a PWM step-up converter operating with a fixed switching frequency of 1.2 MHz and uses internal N-MOS to provide maximum efficiency . The output voltage of the main step-up converter can be set from Vin to 15V with external resistive divider. A pair of charge-pump independently regulate a positive output VDDP and a negative output VDDN for TFT gate-on and gate-off supplies. AT1731A also consists of a precision 1.23V reference that sources up to 50uA, logic shutdown , current-limited , soft-start, power-up sequencing , thermal shutdown and active low.

Main Boost converter

The boost converter operates in fast transient response , current-mode PWM and a constant frequency of 1.2 MHz , allowing the use of smaller external inductor and output capacitors. Depending on duty cycle of each switching cycle can regulate output voltage.

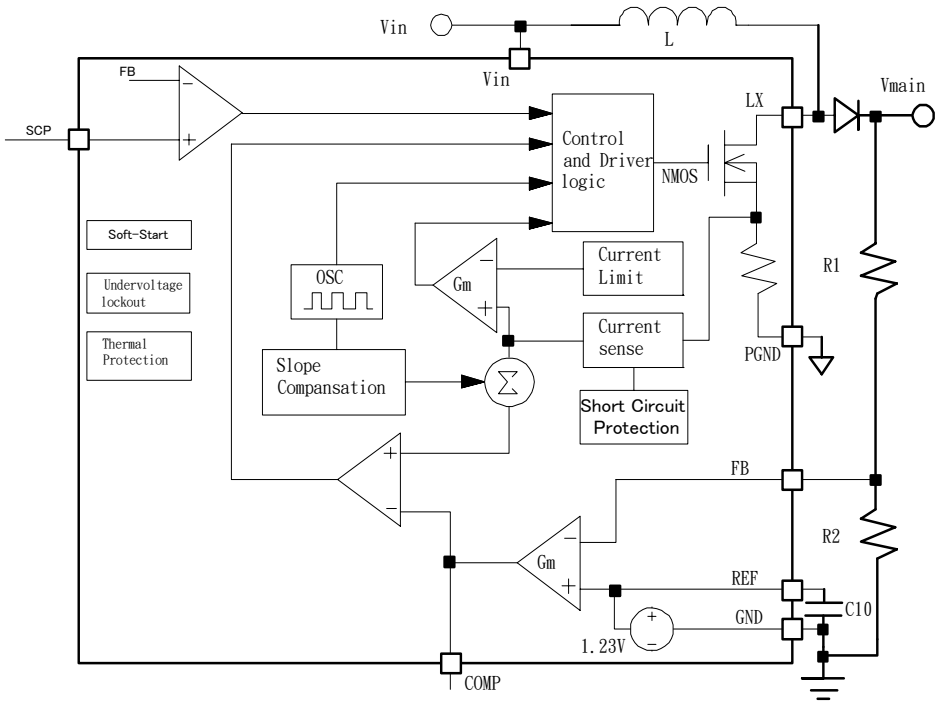


Figure 2 Main Step-Up Converter block Diagram

Figure 2 shows main step-up converter block diagram. On the rising edge of the internal clock , the control and driver logic block sets internal flip-flop when the output voltage is too low, which turns on the N-MOS . The external inductor current ramps up linearly , storing energy in a magnetic filed. Once peak current of inductor over trans-conductance output level , the N-MOS turns off, the flip-flop resets, and external schottky diode turns on . This

forces the current through the inductor to ramp back down , transferring the energy stored in the magnetic field to the output capacitor and load. To add higher flexibility to the selection of external component values, the device uses external loop compensation.

Negative Charge-Pump Regulator

Negative charge-pump contains internal P-channel and N-channel MOSFETs to perform the power transfer. The internal MOSFETs switch at a constant 600kHz (0.5x f_{OSC}). The charge-pump inverts the supply voltage (VDDN) and provides a regulated negative output voltage. Figure 3 shows charge-pump block diagram. During the first half-cycle, the P-channel MOSFET turns on and flying capacitor C_{CPN} charges to V_{DDN} minus a diode drop. During the second half-cycle, the P-channel MOSFET turns off, and the N-channel MOSFET turns on, level shifting C_{CPN}. This connects C_{CPN} in parallel with the reservoir capacitor C_{NEG}. If the voltage across C_{NEG} minus a diode drop is lower than the voltage across C_{CPN}, charge flows from C_{CPN} to C_{NEG} until the diode turns off. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

Positive Charge-Pump Regulator

Positive charge-pump also contains internal P-channel and N-channel MOSFETs to perform the power transfer. The internal MOSFETs switch at a constant 600kHz (0.5x f_{OSC}). The charge-pump inverts the doubles supply voltage (VDDP) and provides a regulated positive output voltage. During the first half-cycle, the N-channel MOSFET turns on and flying capacitor C_{CPP} charges to V_{DDP} minus a diode drop. During the second half-cycle, the N-channel MOSFET turns off, and the P-channel MOSFET turns on, level shifting C_{CPP} by V_{DDP} volts. This connects C_{CPP} in series with the reservoir capacitor C_{POS}. If the voltage across C_{POS} plus a diode drop is lower than the level shifted flying capacitor voltage (V_{CPP}+V_{DDP}), charge flows from C_{CPP} to C_{POS} until the diode turns off. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

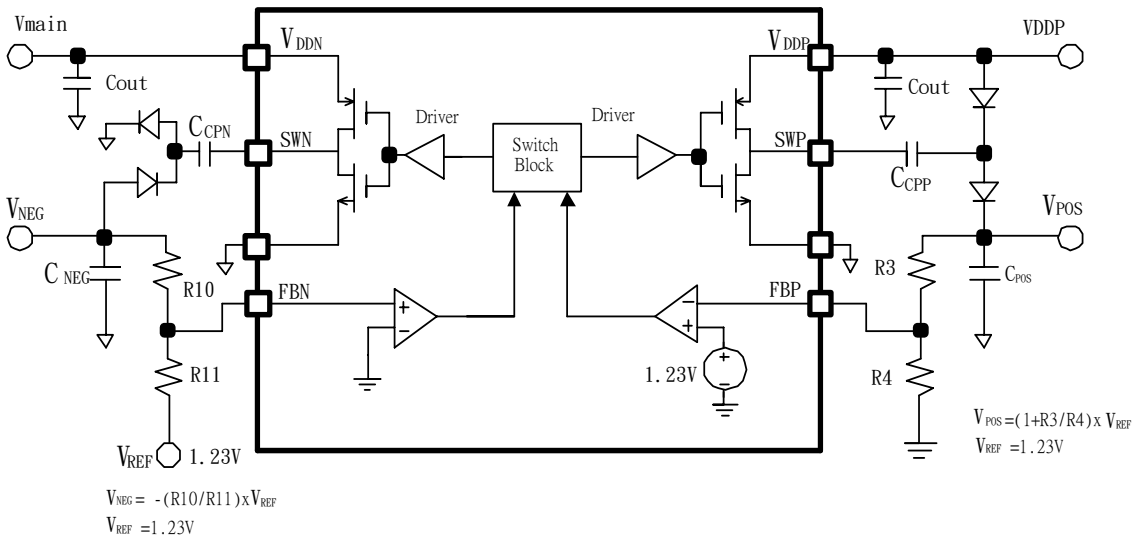


Figure 3 Charge-Pump Block Diagram

Shutdown

The AT1731A shuts down to reduce the supply current to 1uA when SHDN is low. In this mode, the internal reference , error amplifier , comparators, and biasing circuitry turn off while the N-channel MOSFET is turned off. The boost converter's output is connected to Vin normally. Do not leave SHDN pin floating. A logic-level transition on SHDN clears the fault latch.

Power-Up Sequencing

The AT1731A goes through start-up sequence after power-up or exiting shutdown. First, the reference power-up, then the main DC-DC step-up converter powers up with soft-start enable. Once the main DC-DC step-up converter reaches regulation , the negative charge pump turns on. When the negative charge pump output voltage reaches approximately 90% of its nominal value (V_{FBN}<110mV) , then the positive charge pump starts up. Finally, when the positive output voltage reaches 100% of its nominal value (V_{FBP}>1.1V) .The power-up sequence is completed, see figure 4.

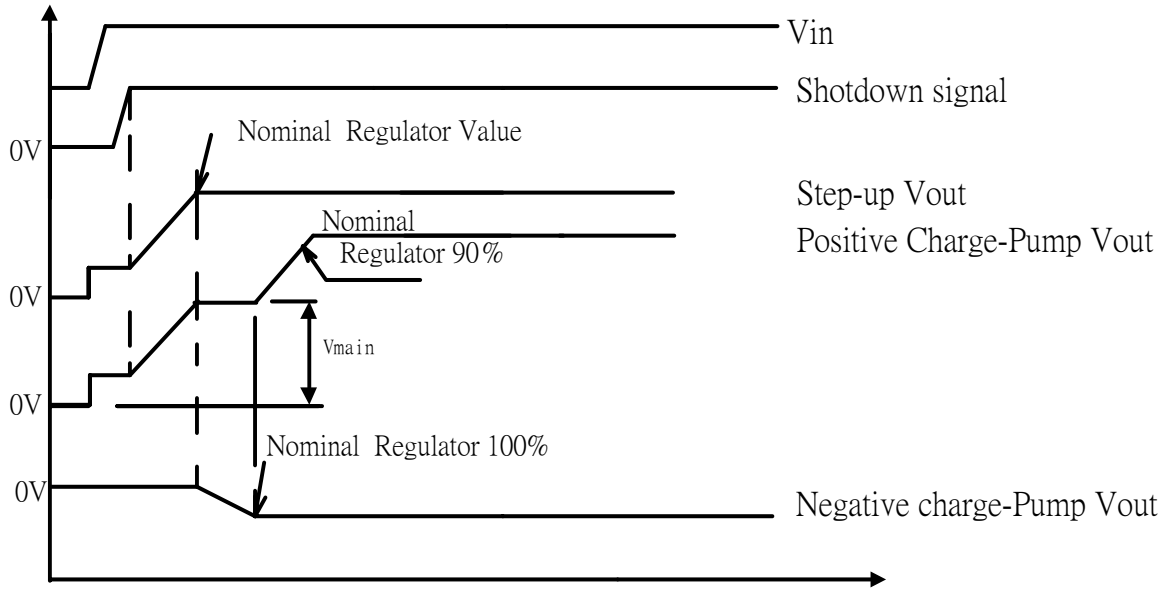


Figure 4 Power Sequence

Soft-Start

Soft-start allows a gradual increase of the internal current-limit level for the main step-up converter during power-up to reduce input surge currents. As the internal 2uA current source charges the external soft-start capacitor, the peak N-MOS current is limited by the voltage on the capacitor. For the dual charge pumps , soft-start is achieved by in-turn controlling the

rising rate of output voltage.

Short-Circuit Protection

If feedback voltage of the main regulator falls below 0.8V, positive charge-pump falls below 1.1V and negative charge-pump falls below 130mV , the built-in constant current will charge external capacitor C_{SCP} . If V_{SCP} reaches 0.8V ,the ready pin goes high impedance and all outputs shut down.; however , the reference remains active. When short- circuit problem is to eliminate, toggle shutdown or cycle the input voltage to clear the fault latch .

Voltage Reference

The voltage at REF is nominally 1.23V. The reference can source up to 50uA with good regulation. Connect a 0.22uF bypass capacitor between REF and GND.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the AT1731A. When the junction temperature exceeds Tj=160 ℃, a thermal sensor activates the thermal protection, which shuts down the IC, allowing the IC to cool. Once the device cools down by 15 ℃, IC will automatically recover normal operation. For continuous operation , do not exceed the absolute maximum junction-temperature rating of Tj=150 ℃.

Power dissipation consideration

The AT1731A maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of any airflow. The power dissipation in the device depends on the operating conditions of each regulator.

The step-up converter dissipates power across the internal N-MOS as the controller ramps up the inductor current. In continuous condition, the power dissipated internally can be approximated by :

$$P_{MAIN-boost} = [(\frac{I_{MAIN} \times V_{MAIN}}{V_{in}})^2 + \frac{1}{12}(\frac{V_{in} \times D}{f_{OSC} \times L})^2] \times R_{DS(ON)} \times D$$

where

I_{MAIN} : It includes the primary load current and the input supply current for the charge-pumps.

The charge-pumps provide regulated output voltages by dissipating power in the low-side N-MOS, so they could be modeled as linear regulators followed by unregulated charge-pumps. Therefore, their power dissipation is similar to a linear regulator :

$$P_{NEG} = I_{NEG} \times [(V_{DDN} - 2 \times V_{DIODE}) \times N - V_{NEG-OUT}]$$

$$P_{POS} = I_{POS} \times [(V_{DDP} - 2 \times V_{DIODE}) \times N - V_{POS-OUT}]$$

Where
N : It is the number of charge-pump stages.
V_{DIODE} : diodes' forward voltage
To find the total power dissipated in the device, the power dissipated by each regulator and the buffer must be added together :

$$P_{total} = P_{MAIN-boost} + P_{NEG} + P_{POS}$$

The maximum allowed power dissipation is around 650 mW (16-pin TSSOP)

$$P_{MAX} = \frac{(T_{j(MAX)} - T_A)}{\theta_{JB} + \theta_{BA}}$$

Where :
T_j - T_A : It is the temperature difference between the IC's junction and the surrounding air.
Θ_{JB} : the thermal resistance of the package to the board
Θ_{BA} : the thermal resistance from the PCB to the surrounding air.

Applications Information

External components of main boost converter can be designed by performing simple calculations. It need to follow regulation by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once L is know, choose the diode and capacitors.

Boost inductor

Inductor selection depends on input voltage, output voltage , maximum current , switching frequency and availability of inductor values. The following boost circuit equations are useful in choosing the inductor values based on the application. They allow the trading of peak current and inductor value while allowing for consideration of component availability and cost.

The peak inductor current is given by:

$$I_{Lpeak} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_{MAIN}}{1-D}$$

where:

$\triangle I_L$ is the inductor peak-to-peak current ripple and is decided by:

$$\Delta I_L = \frac{V_{in}}{L} \times \frac{D}{f_{OSC}}$$

D is the MOSFET turn on ratio and is decided by:

$$D = \frac{V_O - V_{in}}{V_O}$$

f_{OSC} is the switching frequency.

The inductor should be chosen to be able to handle this current and inductor saturation current rating should be greater than I_{PEAK}.

Diode selection

The output diode has average current of I_{MAIN}, and peak current the same as the inductor's peak current and a voltage rating at least 1.5 times the main output voltage. Schottky diode is recommended and it should be able to handle those current.

Feedback Resistor Network

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency . The maximum value of the resistor network is limited by the

feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 200kΩ is recommended. The boost converter output voltage is determined by the following relationship:

$$V_{MAIN} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

where V_{REF} =1.23V as specified.

Output Capacitor

The AT1731A is specially compensated to be stable with capacitors which have a worst- case minimum value of 10uF at the particular V_{MAIN} being set. Output ripple voltage requirements also determine the minimum value and type of capacitors. Output ripple voltage consists of two components the voltage drop caused by the switching current through the ESR of the output capacitor and the charging and discharging of the output capacitor:

$$V_{RIPPLE} = I_{LPEAK} \times ESR + \frac{V_{MAIN} - V_{in}}{V_{MAIN}} \times \frac{I_{MAIN}}{C_{OUT} \times f_{OSC}}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging or discharging of the output capacitor.

Compensation

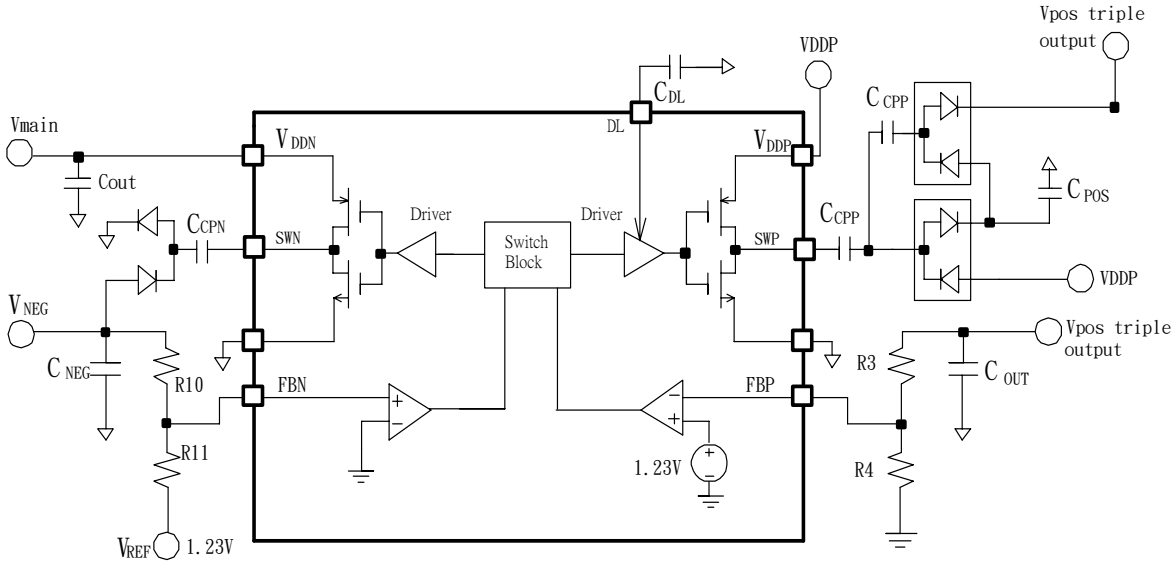
The Main step-up loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is connected to the output of the internal trans-conductance error amplifier. The compensation capacitor adjusts the low frequency gain , and the series resistor value adjusts the high frequency gain. The following formula calculates at what frequency the resistor increases the high frequency gain.

$$f_Z = \frac{1}{2 \times \pi \times C_C \times R_C}$$

If the device operates over the entire input voltage range from 2.7V to 5.5V, a larger compensation capacitor up to 18pF is recommended. For a good load transient where no oscillation should occur, 50 KΩ is recommended for R_C resistor.

Positive and Negative Charge Pump

The AT1731 contains two independent charge pump. The regulation of both the negative and positive charge pumps is generated by the internal comparator that senses the output voltage and compares it with and internal reference. The switching frequency of the charge pumps is set to $0.5xf_{OSC}$. The pumps use pulse width modulation to adjust the pump period, depending on the load present.



Negative and Positive charge pump function diagram

Negative Charge Pump Design Consideration

For a single stage charge pump, the maximum V_{NEG} output is determined by the following equation:

$$V_{NEG(MAX)} \geq I_{NEG} \times 2 \times (R_{SWNn(ON)} + R_{SWNP(ON)}) + 2 \times V_{DIODE} - I_{NEG} \times \frac{1}{0.5 \times f_{OSC} \times C_{CPN}}$$

$$- I_{NEG} \times \frac{1}{0.5 \times f_{OSC} \times C_{NEG}} - V_{DDN}$$

where:

$R_{SWNN(ON)}$ and $R_{SWNP(ON)}$ resistance values depend on the V_{DDN} voltage levels.

Positive Charge Pump Design consideration

For two stage charge pumps, the maximum V_{POS} output is determined by the following equation:

$$V_{POS(MAX)} \leq 2 \times V_{DDP} - I_{POS} \times 2 \times (R_{SWPN(ON)} + R_{SWPP(ON)}) - 2 \times V_{DIODE} - I_{POS} \times \frac{1}{0.5 \times f_{OSC} \times C_{CPP}} -$$

$$I_{POS} \times \frac{1}{0.5 \times f_{OSC} \times C_{POS}} + V_{DDP} - (2 \times V_{DIODE} + I_{POS} \times \frac{1}{0.5 \times f_{OSC} \times C_{CPP}} + I_{POS} \times \frac{1}{0.5 \times f_{OSC} \times C_{OUT}})$$

where:

$R_{SWPP(ON)}$ and $R_{SWPN(ON)}$ resistance values depend on the V_{DDP} voltage levels.

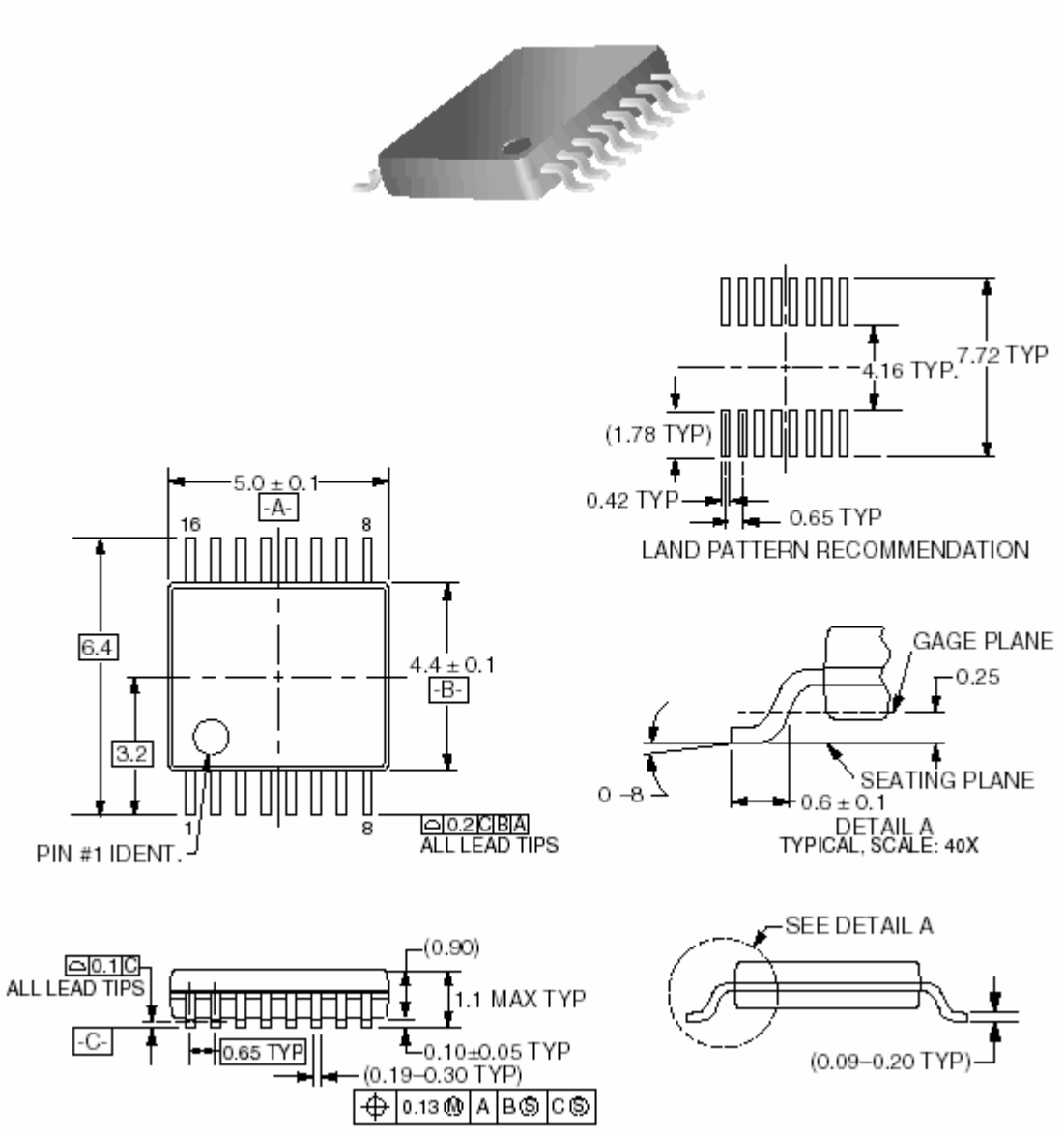
PCB layout guidelines

Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

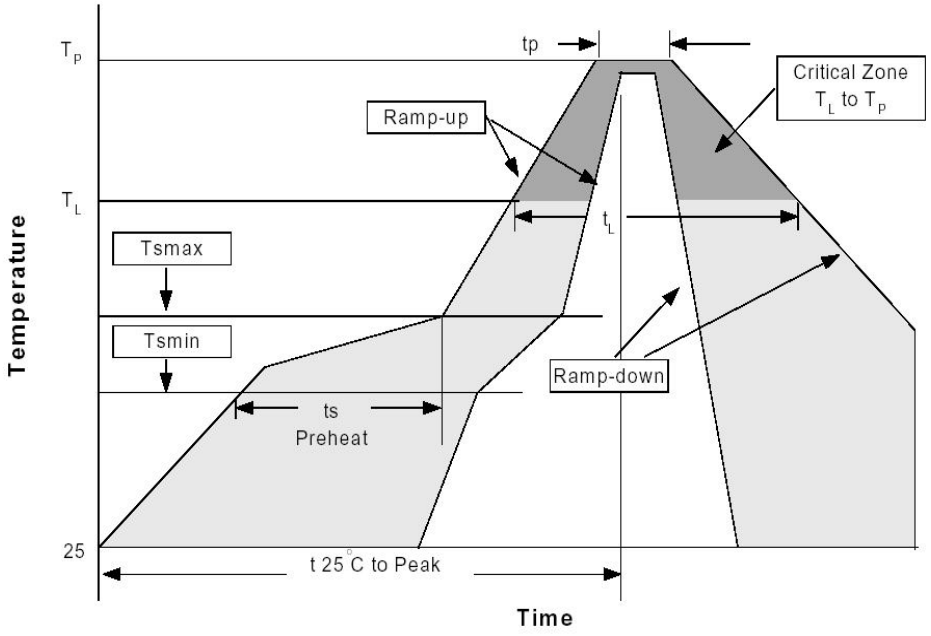
- Please the boost converter diode and inductor close to the LX pin and no via.
- Please ceramic bypass capacitors near the charge-pump input pin.
- Locate all feedback resistive dividers as close to their respective feedback pins as possible.
- Separate GND and PGND areas connected at only one point under the IC.
- Use wide traces and trace length is short as possible.

Package Outline TSSOP-16Pin

Unit: mm



Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm^3**	**Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3**	**Small Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3**
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	 100°C 150°C 60-120 seconds		 150°C 200°C 60-180 seconds	
Tsmax to T_L -Ramp-up Rate			3°C/second max.	
Time maintained above: -Temperature (T_L) -Time (t_L)	 183°C 60-150 seconds		 217°C 60-150 seconds	
Peak Temperature(T_P)	225+0/-5°C	240+0/-5°C	245+0/-5°C	250+0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		3°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

***All temperatures refer to topside of the package, measured on the package body surface.**