AT121

Micro-Power Voltage Detector With Delay Circuit
(External Delay Time Setting)

Immense Advance Tech.

FEATURES

- High Accuracy：± 2%
- Low Power Consumption：1.0μA(TYP.) at V_{IN}=2.0V
- Detect Voltage Range：1.2V ~ 5V in 0.05V step
- Operating Voltage Range：1V ~ 6V
- Detect Voltage Temperature Characteristics：±100ppm/℃
- Output Configuration：N-channel open drain or CMOS
- Packages：SOT-25, SOT-343, SOT-89, TO-92

DESCRIPTION

The AT121 series are highly accurate and ultra low power consumption voltage detectors. It offers internally fixed threshold levels with 0.05V per step range from 1.2V to 5V. A time delay circuit can be accomplished with the addition of an external capacitor. Both CMOS and N-channel open drain output configuration are available.

APPLICATION

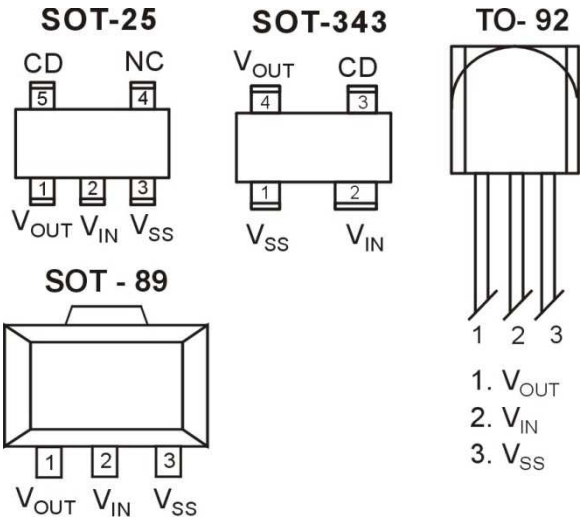
- Microprocessor Reset Circuitry
- Memory Battery Back-up Circuits
- Power-on Reset Circuits
- Power Failure Detection
- System Battery Life and Charge Voltage Monitors
- Delay Circuitry

ORDER INFORMATION

AT 121- X X.X KE R

- IAT
- Circuit Type
- Output Configuration:
  - C = CMOS
  - (Output “Active Low”)
  - M = N-ch open drain
  - (Output “Active High”)
  - N = N-ch open drain
- Output Voltage: X.X=1.3V to 5V
- KE: SOT-25
  KM4: SOT-343
  KG: SOT-89
  TD: TO-92
- Shipping:
  - R: Tape & Reel
  - T: Tube

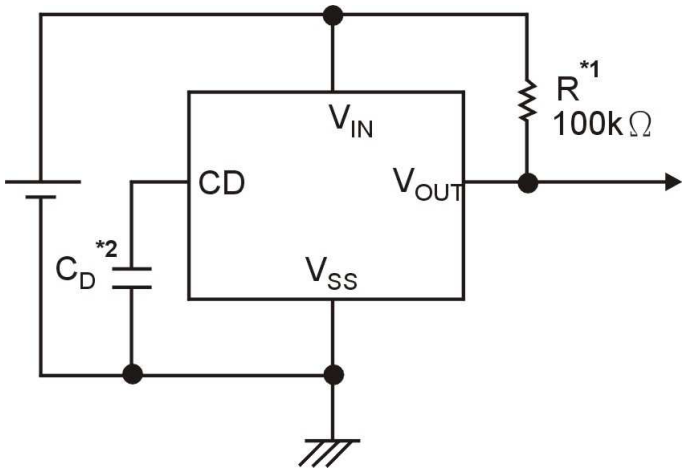
PIN CONFIGURATIONS (TOP VIEW)



PIN DESCRIPTIONS

Pin Name	Pin Description
V_{IN}	Supply Voltage Input
V_{SS}	Ground
V_{OUT}	Output
CD	Connect pin for delay capacitor
NC	No Connection

TYPICAL APPLICATION CIRCUITS

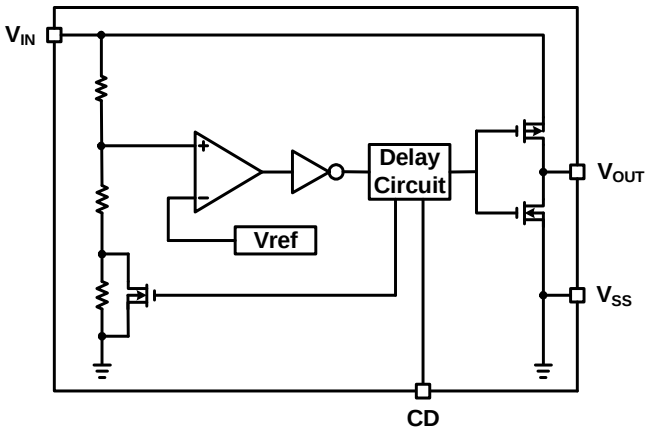


***1.** R is unnecessary for CMOS output products.

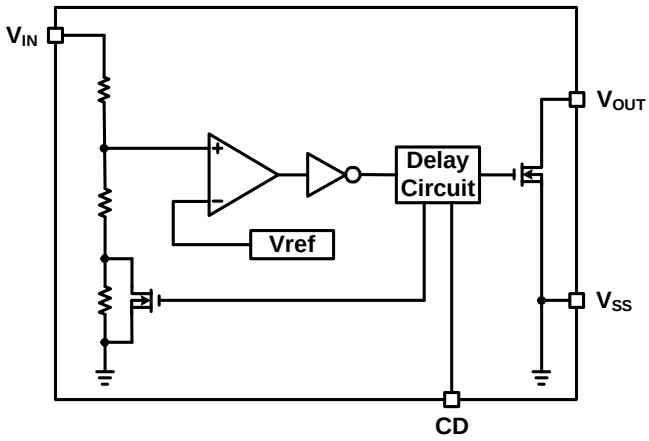
***2.** The delay capacitor (C_D) should be connected directly between the CD pin and to the V_{SS} pin.

BLOCK DIAGRAM

(1) CMOS Output



(2) N-ch Open Drain Output



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Max Value	Unit
Input Voltage		V_{IN}	7	V
Output Current		I_{OUT}	50	mA
Output Voltage	CMOS	V_{OUT}	V_{SS}-0.3 to V_{IN} + 0.3	V
	N-ch open drain		V_{SS}-0.3 to 6	V
Power Dissipation	SOT-25	P_D	150	mW
	SOT-343		250	
	SOT-89		640	
	TO-92		625	
Operating Temperature Range		T_{OPR}	-40 to +85	℃
Storage Temperature Range		T_{STG}	-40 to +125	℃

ELECTRICAL CHARACTERISTICS

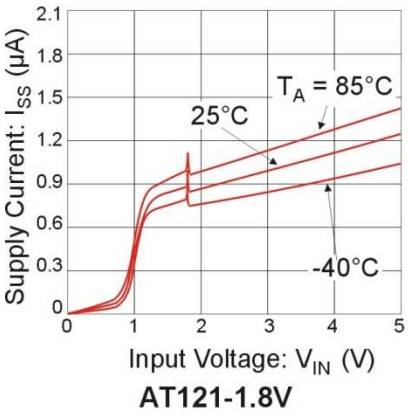
T_A=25℃, unless otherwise specified

Function Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Detect Voltage	V_{DF}		V_{DF} X0.98	V_{DF}	V_{DF} X1.02	V
Hysteresis Range	V_{HYS}		V_{DF} X0.02	V_{DF} X0.05	V_{DF} X0.08	V
Supply Current	I_{SS}	V_{IN} =1.5V	-	0.9	2.6	μA
		V_{IN} =2.0V	-	1.0	3.0	
		V_{IN} =3.0V	-	1.3	3.4	
		V_{IN} =4.0V	-	1.6	3.8	
		V_{IN} =5.0V	-	2.0	4.2	
Operating Voltage	V_{IN}	V_{DF}=1.2V to 5.0V	1	-	6	V
Output Current	I_{OUT}	N-ch V_{DS}=0.5V V_{IN} =1.0V V_{IN} =2.0V V_{IN} =3.0V V_{IN} =4.0V V_{IN} =5.0V	 1.0 3.0 5.0 6.0 7.0	 2.2 7.7 10.1 11.5 13.0		mA
		P-ch V_{DS}=2.1V V_{IN} =3V (with CMOS output)		-10.0	-2.0	
Detect voltage Temperature Characteristics		-40℃ ≤T_{OP}≤ 85℃		100		ppm/℃
Transient Delay Time (V_{DR} → V_{OUT} inversion) (Note 1)	T_{DLY}	C_D=4.7nF	9	12	15	ms

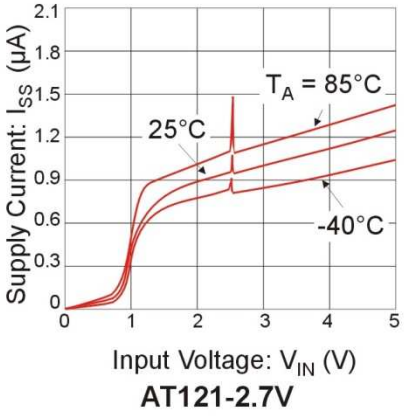
Note 1: V_{DR} = V_{DF} + V_{HYS}

TYPICAL OPERATING CHARACTERISTICS

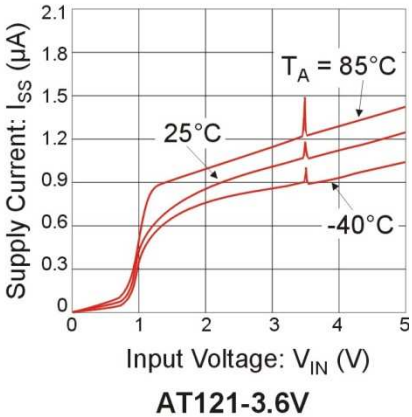
(1) Supply Current vs. Input Voltage



AT121-1.8V

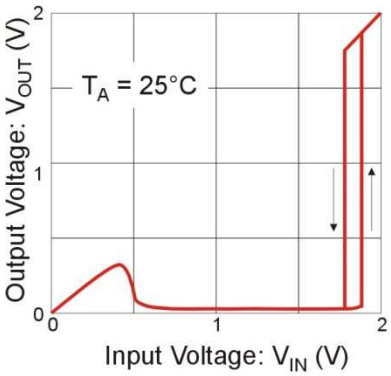


AT121-2.7V

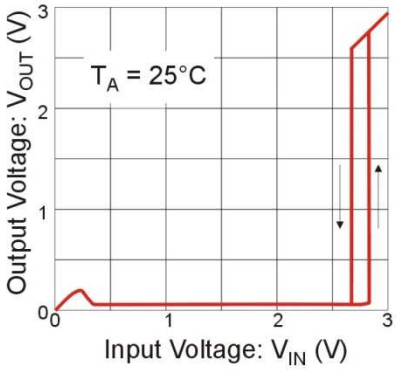


AT121-3.6V

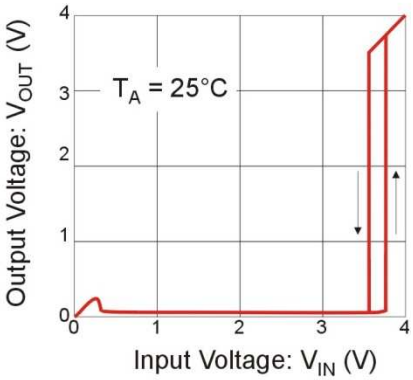
(2) Output Voltage vs. Input Voltage



AT121-1.8V



AT121-2.7V



AT121-3.6V

APPLICATION INFORMATION

OPERATION

- CMOS output

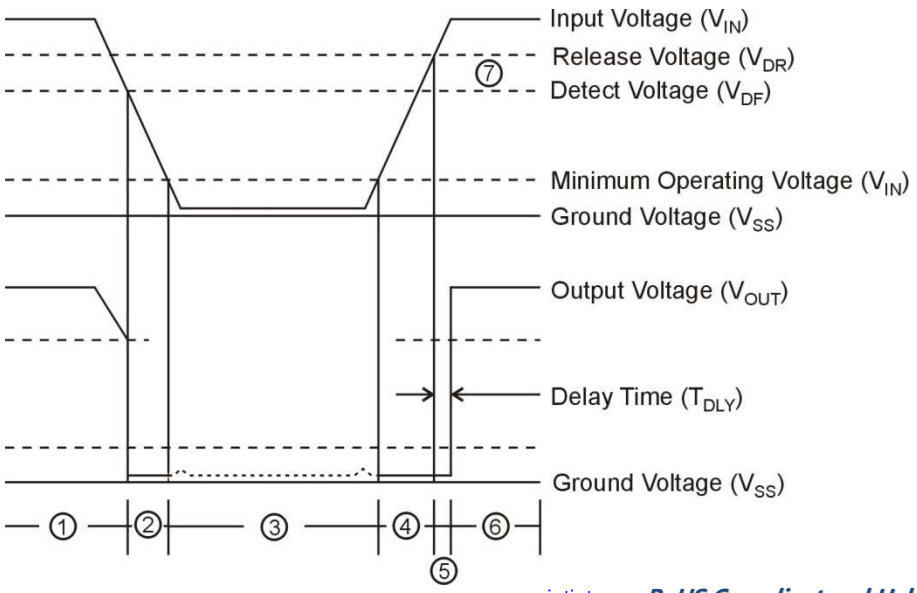
1. As an early state, the input voltage pin is applied sufficiently high voltage to the release voltage and the delay capacitance (CD) is charged to the input pin voltage. While the input pin voltage (V_{IN}) starts dropping to reach the detect voltage (V_{DF}) ($V_{IN} > V_{DF}$), the output voltage (V_{OUT}) keeps the “High” level ($=V_{IN}$).

   Note that high impedance exists at V_{OUT} with the N-channel open drain configuration. If the pin is pulled up, V_{OUT} will be equal to the pull up voltage.
2. When V_{IN} falls below V_{DF}, V_{OUT} will be equal to the ground voltage (V_{SS}) level (detect state). Note that this also applies to N-channel open drain configurations.
3. When V_{IN} falls to a level below that of the minimum operating voltage (V_{MIN}) output will become unstable.
4. When V_{IN} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), V_{OUT} will be equal to V_{SS} until V_{IN} reaches the V_{DR} level.
5. Although V_{IN} will rise to a level higher than V_{DR}, V_{OUT} maintains ground voltage level via the delay circuit.
6. Following transient delay time, V_{IN} will be output at V_{OUT}. Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.
7. The difference between V_{DR} and V_{DF} represents the hysteresis range.

Notes:

1. Propagation delay time (T_{DLY}) represents the time it takes for V_{IN} to appear at V_{OUT} once the said voltage has exceeded the V_{DR} level.

- Timing Chart



APPLICATION INFORMATION (CONTINUED)

- Delay Circuit

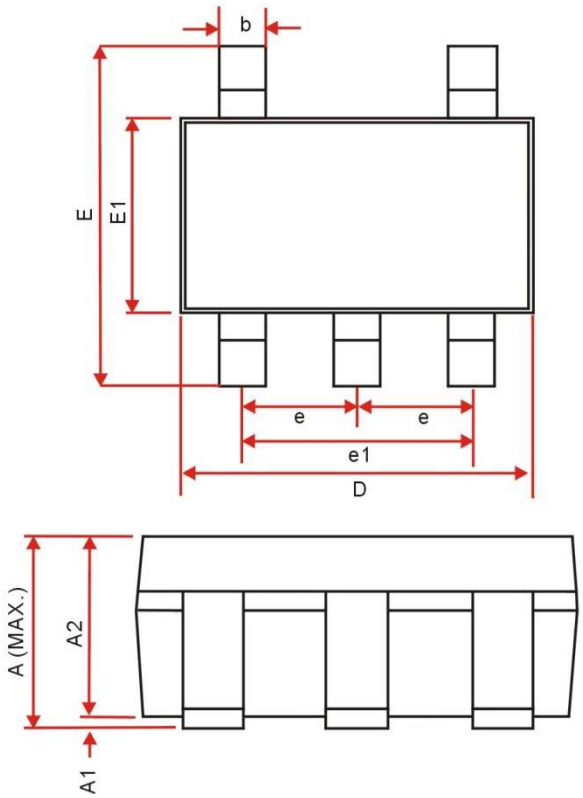
  The delay circuit delays the output signal from the time at which the power voltage (V_{IN}) exceeds the release voltage (V_{DR}) when V_{IN} is turned on. The output signal is not delayed when the V_{IN} goes below the detection voltage (V_{DF}). The delay time (T_{DLY}) is determined by the time constant of the built-in constant current and the attached external capacitor (C_D), and calculated from the following equation.

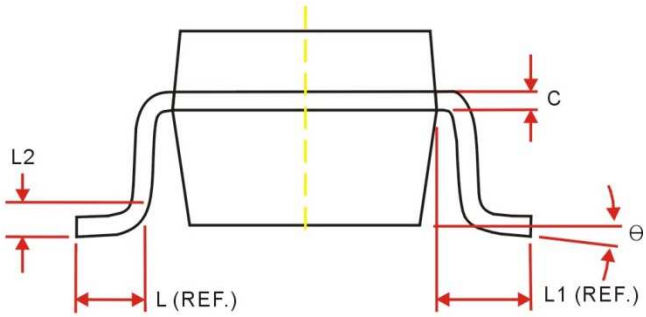
  T_{DLY} (ms) = Delay coefficient x C_D (nF)

  Delay coefficient of CMOS output products (25℃): M in. 1.91，Typ= 2.55，Max= 3.19。

PACKAGE OUTLINE DIMENSIONS

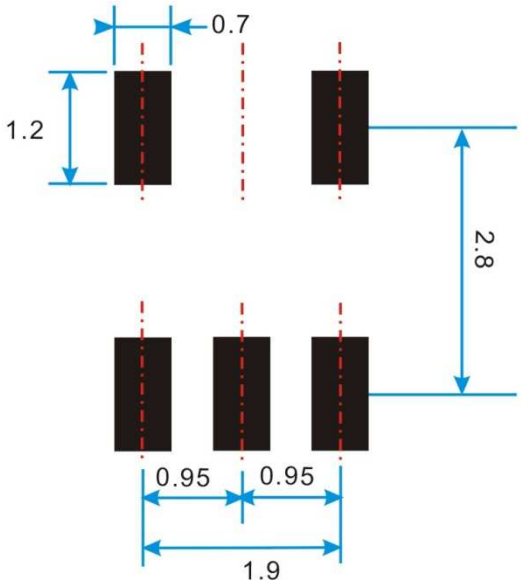
SOT-25 PACKAGE OUTLINE DIMENSIONS





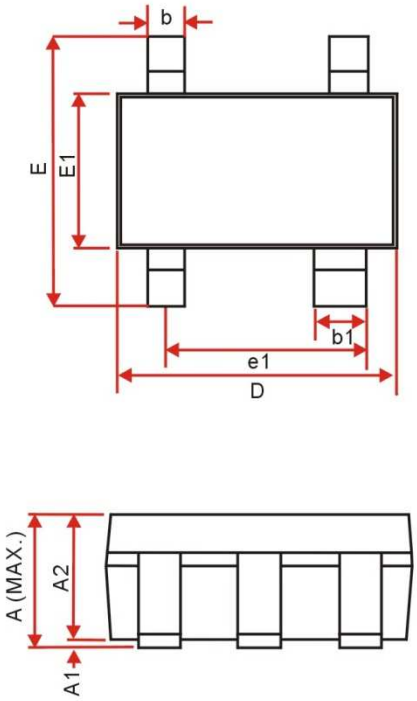
Symbol	Dimensions In Millimeters	
	Min	Max
A	1.45 MAX.	
A1	0	0.15
A2	0.90	1.30
C	0.08	0.22
D	2.90 BSC.	
E	2.80 BSC.	
E1	1.60 BSC.	
L	0.30	0.60
L1	0.60BSC.	
L2	0.25BSC.	
Θ	0°	10°
b	0.30	0.50
e	0.95BSC.	
e1	1.90BSC.	

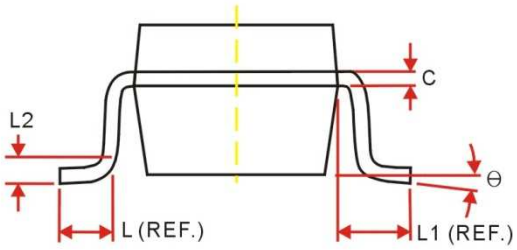
SOT-25 PACKAGE FOOTPRINT (mm)



PACKAGE OUTLINE DIMENSIONS

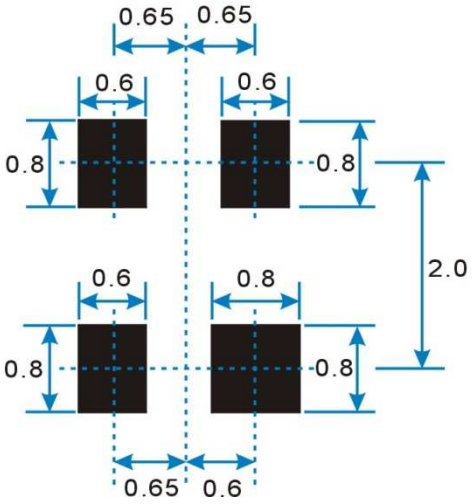
SOT-343 PACKAGE OUTLINE DIMENSIONS



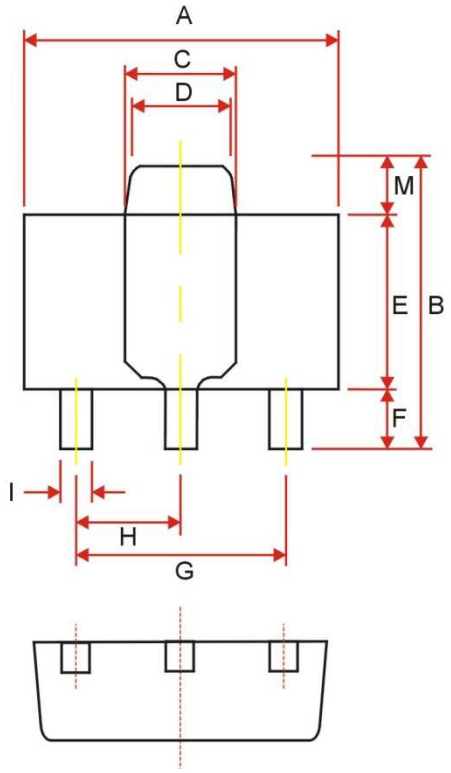


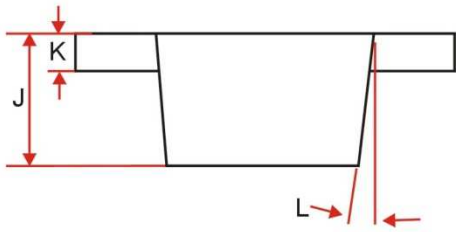
Symbol	Dimensions In Millimeters	
	Min	Max
A	1.10 MAX.	
A1	0	0.10
A2	0.70	1.00
C	0.08	0.22
D	2.10 BSC.	
E	2.30 BSC.	
E1	1.30 BSC.	
L	0.26	0.46
L1	0.525REF.	
L2	0.20BSC.	
Θ	0°	8°
b	0.15	0.35
b1	0.30	0.50
e1	1.30BSC.	

SOT-343 PACKAGE FOOTPRINT (mm)



PACKAGE OUTLINE DIMENSIONS
SOT-89 PACKAGE OUTLINE DIMENSIONS

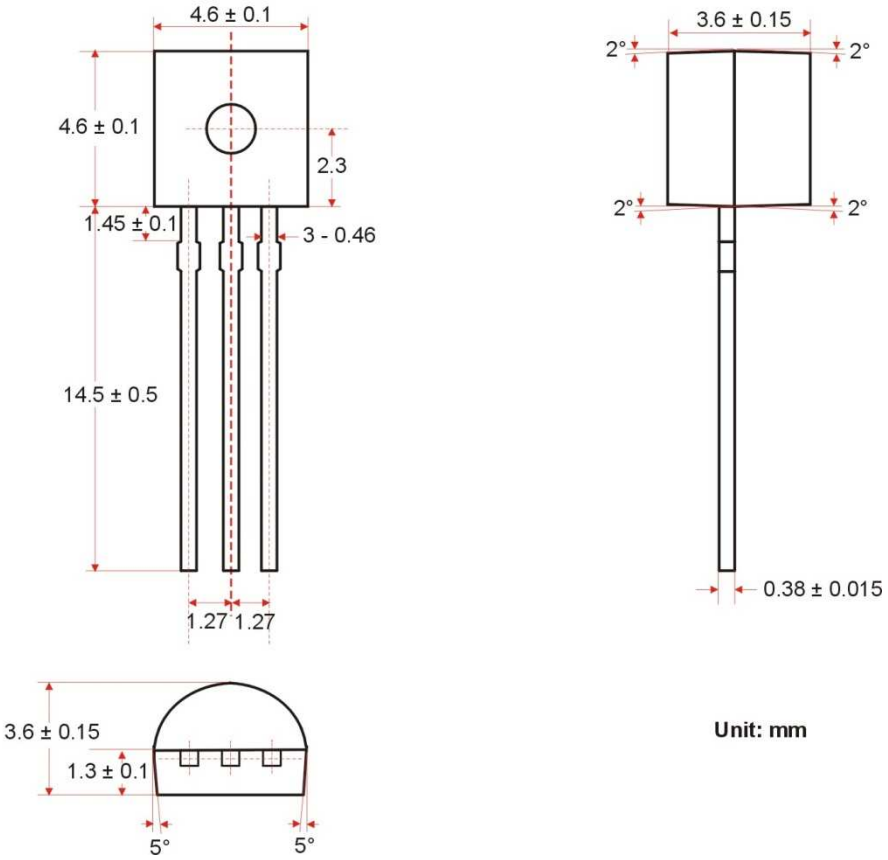




REF.	Dimensions In Millimeters	
	Min	Max
A	4.40	4.60
B	3.94	4.25
C	1.50	1.70
D	1.30	1.50
E	2.29	2.60
F	0.89	1.20
G	3.00 REF.	
H	1.50 REF.	
I	0.40	0.56
J	1.40	1.60
K	0.35	0.44
L	5°TYP.	
M	0.70 REF.	

PACKAGE OUTLINE DIMENSIONS

TO-92 PACKAGE OUTLINE DIMENSIONS



Unit: mm

Note :

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