rev 2.0

DDR 24-Bit to 48-Bit Registered Buffer

Features

- Differential clock signals.
- Supports SSTL_2 class II specifications on inputs and outputs.
- Low voltage operation.
  - V_{DD} = 2.3V to 2.7V.
- Available in 114 ball BGA package. Industrial temperature range also available.

Product Description

The 24-Bit to 48-Bit ASM4SSTVF32852 is a universal bus driver designed for 2.3V to 2.7V V_{DD} operation and SSTL_2 I/O levels except for the LVCMOS RESETB input.

Data flow from D to Q is controlled by the differential clock (CLK/CLKB) and a control signal (RESETB). The positive edge of CLK is used to trigger the data flow, and CLKB is used to maintain sufficient noise margins, whereas the RESETB, an LVCMOS asynchronous signal is intended for use at the time of power-up only.

The ASM4SSTVF32852 supports a low power standby mode of operation. A logic “Low” level at RESETB, assures that all internal registers and outputs (Q) are reset to a logic “Low” state, and that all input receivers, data (D) buffers, and clock (CLK/CLKB) are switched off. Please note that RESETB must always be supported with a LVCMOS levels at a valid logic state since VREF may not be stable during power-up.

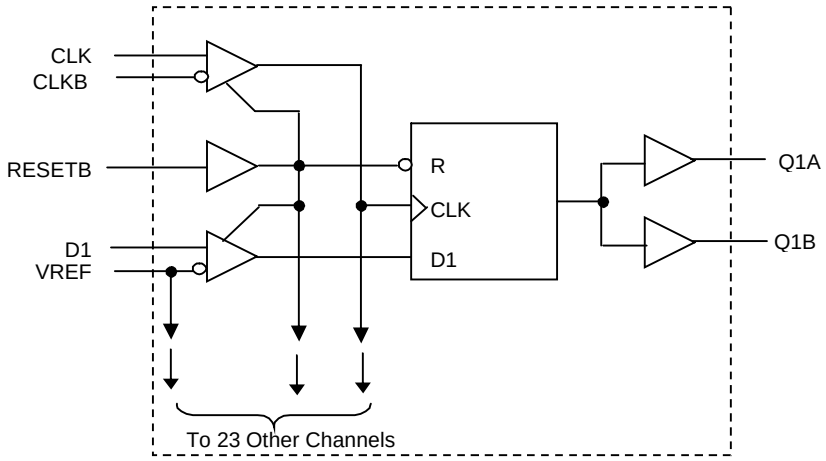
To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESETB must be held at a logic “Low” level during power-up.

In the DDR DIMM application, RESETB is specified to be asynchronous with respect to CLK/CLKB. Therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby state, the register will be cleared and the outputs will be driven to a logic “Low” level quickly relative to the time to disable the differential input receivers. This ensures there are no “glitches” on any output. However, when coming out of low power standby state, the register will become active quickly relative to the time taken to enable the differential input receivers. When the data inputs are at a logic level “Low” and the clock is stable during the “Low-to-High” transition of RESETB until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic “Low” level.

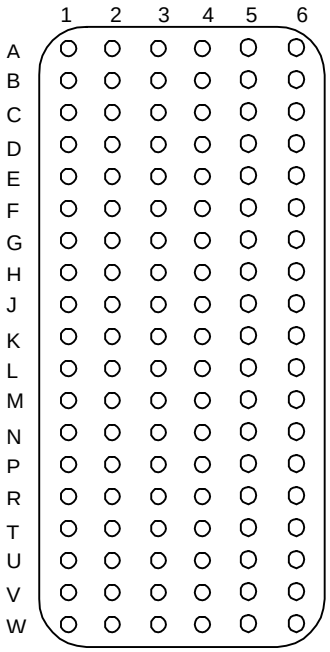
Applications

- DDR Memory Modules.
- Provides complete DDR DIMM logic solution with ASM5CVF857, ASM4SSTVF16857 and ASM4SSTVF16859.
- SSTL_2 compatible data registers.

Block Diagram



Pin Configurations



114-Pin Ball BGA

Pin Description

Pin #	Pin Name	Type	Description
R1, P1, N1, N2, M1, L2, L1, K1, K2, J2, J1, H1, G1, G2, F1, F2, E1, D1, D2, C1, C2, B1, A1, A2	Q (24:1)A	O	Data output.
R6, P6, N6,N5,M6, L5, L6, K6, K5, J5, J6, H6, G6, G5, F6, F5, E6, D6, D5, C6, C5, B6, A6, A5	Q (24:1)B	O	Data output.
E2, B3, D3, G3, J3, L3, M3, P3, B4, D4, G4, J4, L4, M4, P4, E5	GND	P	Ground.
B2, M2, P2, C3, E3, F3, H3, K3, N3, C4, E4, F4, H4, K4, N4, B5, M5, P5	VDDQ	P	Output supply voltage, 2,5V nominal.
W4, V4, U4, W5, W6, V5, T4, V6, U6, U5, T6, T5, W3, V3, U3, W2, W1, V2, T3, V1, U1, U2, T1, T2	D(24:1)	I	Data input.
A3	CLK	I	Positive master clock input.
A4	CLKB	I	Negative master clock input.
H2, H5, R2, R5	VDD	P	Core supply voltage, 2.5V nominal.
R3	RESETB	I	Reset (Active Low).
R4	VREF	I	Input reference, 1.25V nominal.

Pin Configuration Assignments

	1	2	3	4	5	6
A	Q2A	Q1A	CLK	CLKB	Q1B	Q2B
B	Q3A	VDDQ	GND	GND	VDDQ	Q3B
C	Q5A	Q4A	VDDQ	VDDQ	Q4B	Q5B
D	Q7A	Q6A	GND	GND	Q6B	Q7B
E	Q8A	GND	VDDQ	VDDQ	GND	Q8B
F	Q10A	Q9A	VDDQ	VDDQ	Q9B	Q10B
G	Q12A	Q11A	GND	GND	Q11B	Q12B
H	Q13A	VDD	VDDQ	VDDQ	VDD	Q13B
J	Q14A	Q15A	GND	GND	Q15B	Q14B
K	Q17A	Q16A	VDDQ	VDDQ	Q16B	Q17B
L	Q18A	Q19A	GND	GND	Q19B	Q18B
M	Q20A	VDDQ	GND	GND	VDDQ	Q20B
N	Q22A	Q21A	VDDQ	VDDQ	Q21B	Q22B
P	Q23A	VDDQ	GND	GND	VDDQ	Q23B
R	Q24A	VDD	RESETB	VREF	VDD	Q24B
T	D2	D1	D6	D18	D13	D14
U	D4	D3	D10	D22	D15	D16
V	D5	D7	D11	D23	D19	D17
W	D8	D9	D12	D24	D21	D20

Truth Table[1]

Inputs				Q Outputs
RESET#	CLK	CLK#	D	Q
L	X or floating	X or floating	X or floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0 [2]

Note: 1. H=High signal level, L=Low signal level, ↑= transition from low to high, ↓= transition from high to low, X = don't care 2. Output level before the indicated steady state input conditions were established.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	+150	°C
Supply Voltage	-0.5	3.6	V
Input Voltage[1]	-0.5	V_{DD} + 0.5	V
Output Voltage[1,2]	-0.5	V_{DD} + 0.5	V
Input Clamp Current	± 50		mA
Output Clamp Current	±50		mA
Continuous Output Current	±50		mA
VDD, VDDQ or GND current/pin	100		mA
Package Thermal Impedance[3]	55		°C/W

Note:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level $V_0 > V_{DDQ.}$
3. The package thermal impedance is calculated in accordance with JESD 51.
These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.

Recommended Operating Conditions

Guaranteed by design. Not 100% tested in production.

Parameter	Description		Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage		2.3	2.5	2.7	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input voltage		0		V_{DDQ}	V
$V_{IH(DC)}$	DC input high voltage	Data Inputs	V_{REF} + 0.15			V
$V_{IH(AC)}$	AC input high voltage		V_{REF} + 0.31			V
$V_{IL(DC)}$	DC input low voltage				V_{REF} - 0.15	V
$V_{IL(AC)}$	AC input low voltage				V_{REF} - 0.31	V
V_{IH}	Input high voltage level	RESETB	1.7			V
V_{IL}	Input low voltage level				0.7	V
V_{ICR}	Common mode input range	CLK	0.97		1.53	V
V_{ID}	Differential input voltage	CLKB	0.36			V
V_{IX}	Cross-point voltage of differential clock pair		(V_{DDQ}/2) - 0.2		(V_{DDQ}/2) +0.2	V
I_{OH}	High-level output current				-19	mA
I_{OI}	Low-level output current				19	mA
T_A	Operating free-air temperature		0		70	°C

DC Electrical Characteristics

T_A = 0°C to 70°C, V_{DD} = 2.5 ± 0.2V, and V_{DDQ} = 2.5±0.2V (unless otherwise stated)
Guaranteed by design. Not 100% production tested.

Symbol	Parameter	Test conditions		V_{DDQ}	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.3 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.3 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -16 mA		2.3 V	2.05			V
V_{OL}		I_{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.3 V			0.20	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.5V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}				40		mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle				35		µA/clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle; One data input switching at half clock frequency, 50% duty cycle				7		µA/clock MHz/data input
r_{OH}	Output high	I_{OH} = -20 mA		2.3 V to 2.7 V		12		Ω
r_{OL}	Output low	I_{OL} = 20 mA		2.3 V to 2.7 V		10		Ω
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.5 V			4	Ω
C_i	Data inputs	$V_I = V_{REF}$ ± 350 mV, V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV		2.5 V	2.5		3.5	pF
	CLK & CLKB			2.5 V	2.5		3.5	pF

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted).

Symbol	Parameters		V_{DD} = 2.5V±0.2V		Unit
			Min	Max	
f_{CLOCK}	Clock frequency			200	MHz
T_{PD}	Clock to output time		1.9	2.7	ns
T_{RST}	Reset to output time			4.5	ns
t_S	Setup time, fast slew rate [2,4]	Data before CLK↑, CLKB↓	0.5		ns
	Setup time, slow slew rate [3,4]		0.7		ns
t_h	Hold time, fast slew rate [2,4]	Data after CLK↑, CLKB↓	0.3		ns
	Hold time, slow slew rate [3,4]		0.5		ns
t_{SL}	Output slew rate		1	4	V/ns

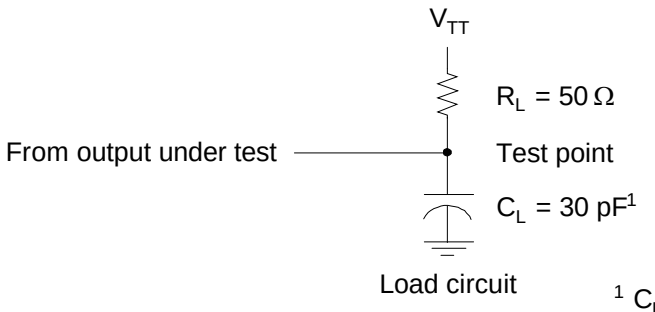
Note:
1. Guaranteed by design, not 100% tested in production.
2. For data signal input slew rate >= 1V/ns
3. For data signal input slew rate >= 0.5 V/ns and < 1V/ns
4. CLK,CLKB signals input slew rates are >=1V/ns

Switching Characteristics

(Over recommended operating free-air temperature range unless otherwise noted.)

Symbol	From (input)	To (output)	V_{DD} = 2.5 V ± 0.2 V			Units
			Min	Typ	Max	
f_{max}			200	–	–	MHz
t_{PD}	CLK, CLKB	Q	1.9		2.7	ns
t_{phl}	RESETB	Q	–	–	4.5	ns

Parameter Measurement Information (V_{DD} = 2.5 V ± 0.2V)



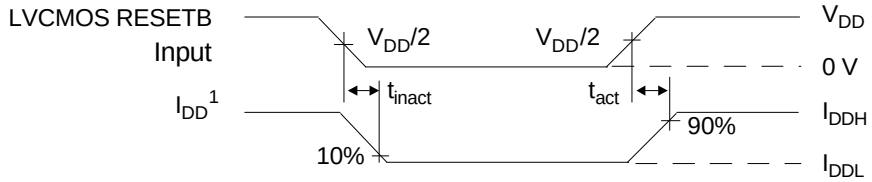
[1] C_L includes probe and jig capacitance.

Voltage and Current Waveforms

In the following waveforms, note that all input pulses are supplied by generators having the following characteristics:

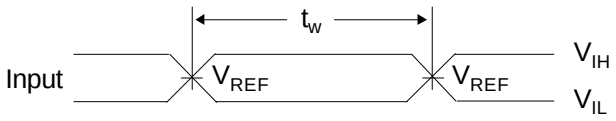
- PRR ≤ 10 MHz, Z_o = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).
- The outputs are measured one at a time with one transition per measurement.
- $V_{TT} = V_{REF} = V_{DDQ}/2$.
- $V_{IH} = V_{REF}$ + 310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
- $V_{IL} = V_{REF}$ - 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
- t_{PLH} and t_{PHL} are the same as t_{pd}.

Input active and inactive times

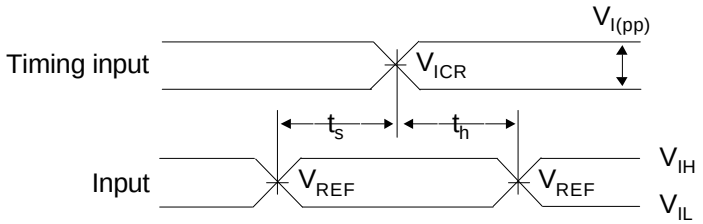


[1] I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

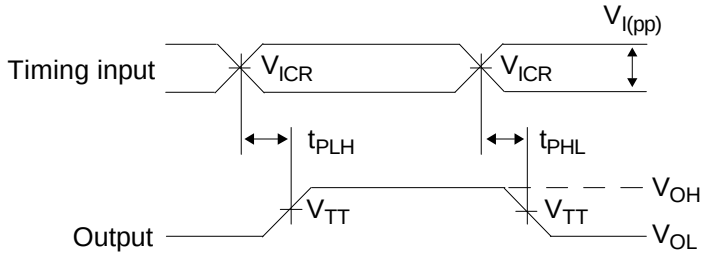
Pulse duration

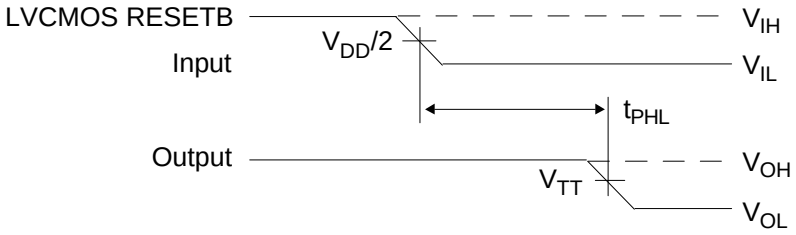


Setup and hold times



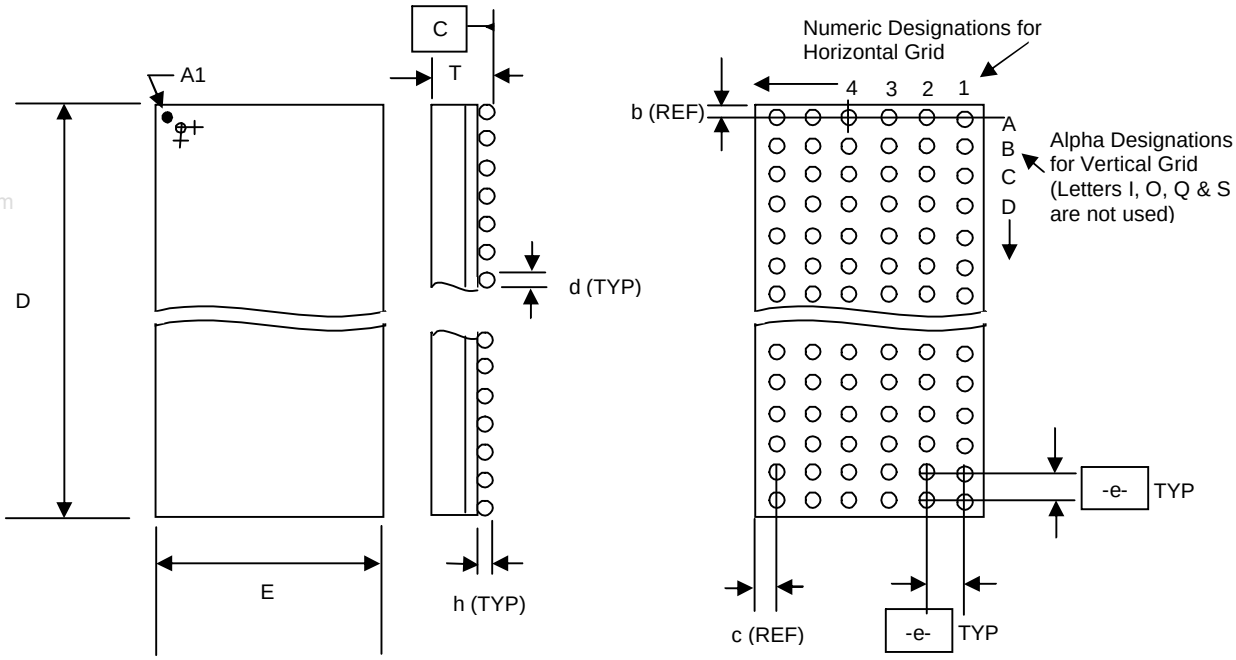
Propagation delay times





Package Dimensions

114-Pin Ball BGA



D	E	T Min/Max	e	BALL GRID			d	h Min/Max	REF. DIMENSIONS	
				HORIZ	VERT	TOTAL			b	c
16.00 BSC	5.50 BSC	1.30/1.50	0.80 BSC	6	19	114	0.46	0.31/0.41	0.80	0.75

Ordering Codes

Ordering Number	Marking	Package Type	Quantity per reel	Temperature
ASM4SSTVF32852-114BT	AS4SSTVF32852B	114-pin Ball, BGA, tray/tube		0°C to 70°C
ASM4SSTVF32852-114BR	AS4SSTVF32852B	114-pin Ball, BGA, tape and reel	2500	0°C to 70°C
ASM4ISSTVF32852-114BT	AS4ISSTVF32852B	114-pin Ball, BGA, tray/tube		-40°C to +85°C
ASM4ISSTVF32852-114BR	AS4ISSTVF32852B	114-pin Ball, BGA, tape and reel	2500	-40°C to +85°C

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Advance Information
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