ASM3P2854C

ON Semiconductor®

Custom Clock Generator for Fax System

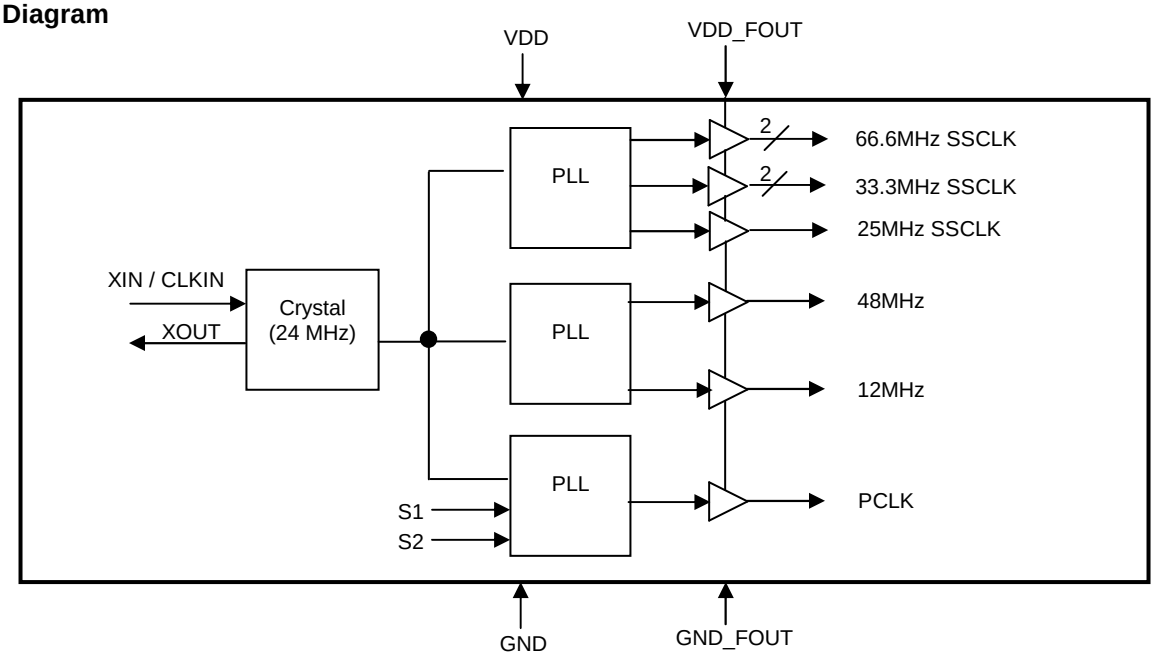
Features

- Generates Custom Clocks for FAX system from an inexpensive 24MHz Crystal
- 2x 66.66MHz low EMI (Spread Spectrum) clocks for ASIC1 (System / DDR SDRAM)
- 1 x 48MHz for USB1.1 HOST
- 2 x 33.33MHz low EMI (Spread Spectrum) clocks for System / DDR SDRAM of ASIC2 and ASIC3
- 1x 25MHz low EMI (Spread Spectrum) clock for LCD, Serial port, and buzzer of ASIC1
- 1x 12MHz for USB PHY (USB2.0)
- 1x Programmable clock for printer engine control
- One of the four programmable clock outputs selection through two Select Pins
- Supply Voltage 3.3V ± 0.3V
- Available in 16L TSSOP, Green package

Product Description

ASM3P2854C is a part of the two chip custom clock generator solution for NEC FAX system. Together with ASM3P2855D, ASM3P2854C realizes all the seventeen clocks required by the various components and subsystems of the FAX system. It uses an inexpensive 24MHz crystal as the input to generate two 66.66MHz low EMI (spread spectrum) clocks used by ASIC1 for system/ DDR SDRAM, two 33.33MHz low EMI (spread spectrum) clocks used by ASIC2 and ASIC3 for system/ DDR SDRAM, a 25MHz low EMI (Spread Spectrum) clock used by ASIC1 for LCD, Serial port, and buzzer, a 48MHz clock used by USB1.1 HOST, and a 12MHz clock used by USB PHY (USB2.0). One of the four Programmable clock (PCLK) frequencies of 24.00448MHz, 21.33732MHz, 21.19962MHz and 20.40464MHz used for Printer Engine control selectable through two Select pins S1 and S2. The accuracy of the synthesized programmable clocks is within ±18ppm. The custom clock generator works is with a Supply Voltage for 3.3V. The device is available in a 16L TSSOP Green package, over 0℃ to +70℃ temperature range. The output Clocks h ave an accuracy of ±50ppm.

Block Diagram



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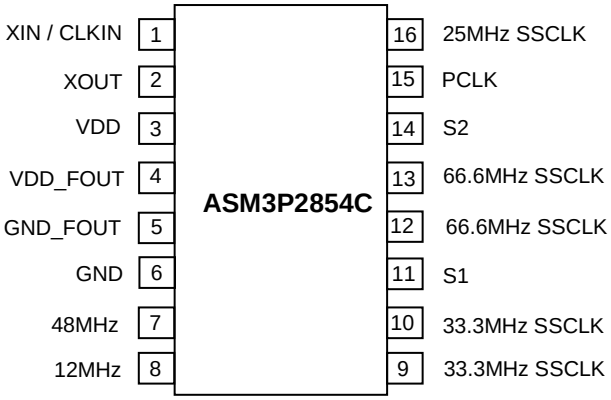
ASM3P2854/D

Pin Diagram



Pin Description

Pin#	Pin Name	Type	Description
1	XIN / CLKIN	I	Crystal connection or external reference clock input.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	VDD	P	Power supply for the core
4	VDD_FOUT	P	Power supply for the output buffers.
5	GND_FOUT	P	Ground connection for the output buffers
6	GND	P	Ground connection
7	48MHz	O	48MHz Clock Output
8	12MHz	O	12MHz Clock Output
9	33.3MHz	O	33.3 MHz low EMI Clock Output
10	33.3MHz	O	33.3 MHz low EMI Clock Output
11	S1	I	Selection Bit for Programmable Clock. To be Pulled HIGH or LOW suitably. See the PCLK Selection Table for details
12	66.6MHz	O	66.6 MHz low EMI Clock Output
13	66.6MHz	O	66.6 MHz low EMI Clock Output
14	S2	I	Selection Bit for Programmable Clock. To be Pulled HIGH or LOW suitably. See the PCLK Selection Table for details
15	PCLK	O	Programmable Clock Output
16	25MHz	O	25 MHz low EMI Clock Output

PCLK Selection Table

S2	S1	Programmable Clock (MHz)
0	0	24.00448
0	1	21.33732
1	0	21.19962
1	1	20.40464

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, VDD_FOUT	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
T_A	Operating Temperature	0		+70	℃
VDD	Core Voltage	+3.0	+3.3	+3.6	V
VDD_FOUT	Output Buffer Voltage	+3.0	+3.3	+3.6	V

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND-0.3		0.8	V
V_{IH}	Input high voltage	2.0		VDD+0.3	V
I_{IL}	Input low current			-35	µA
I_{IH}	Input high current			35	µA
I_{XOL}	XOUT output low current (V_{XOL}@ 0.4V, VDD = 3.3V)		3		mA
I_{XOH}	XOUT output high current (V_{XOH}@ 2.5V, VDD = 3.3V)		3		mA
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 10mA)			0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OH} = -10mA)	2.5			V
I_{DD}	Static supply current[1]			15	mA
I_{CC}	Dynamic supply current (VDD=3.3V, No Load)		33		mA
VDD	Operating Core Voltage	3.0	3.3	3.6	V
VDD_FOUT	Operating Output Buffer Voltage	3.0	3.3	3.6	V
t_{ON}	Power-up time (first locked cycle after power-up)[2]			5	mS
Z_O	Output impedance		30		Ω

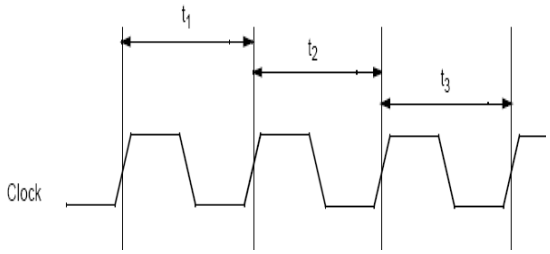
Notes: 1. XIN / CLKIN pin is pulled to GND.
2. VDD and CLKIN inputs are stable.

AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
XIN / CLKIN	Input frequency			24		MHz
F_{OUT}	Output frequency	At Pin 7		48		
		At Pin 8		12		
		At Pins 9 and 10		33		
		At Pins 12 and 13		66		
		At Pin 15[1]		PCLK		
		At Pin 16		25		
f_d	Frequency Deviation for Spread Spectrum Clocks			-0.5		%
t_{LH}[2]	Output rise time (measured from 20% to 80%)			1.0		nS
t_{HL}[2]	Output fall time (measured from 80% to 20%)			1.0		
t_{JC}	Cycle to Cycle Jitter (For Modulated Clocks); unloaded outputs			±300		pS
t_{JP}	Period Jitter (For Non-Modulated Clocks)); unloaded outputs				±275	
t_D	Output duty cycle		45	50	55	%

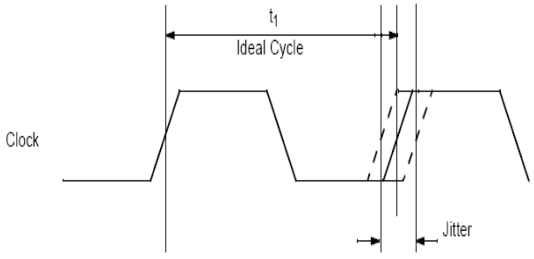
Notes: 1. See the PCLK Selection Table for PCLK Frequency.
2. t_{LH} and t_{HL} are measured into a capacitive load of 15pF.

Cycle-Cycle Jitter



Jitter=J1=t2-t1
Jitter =J2=t3-t2

Period Jitter

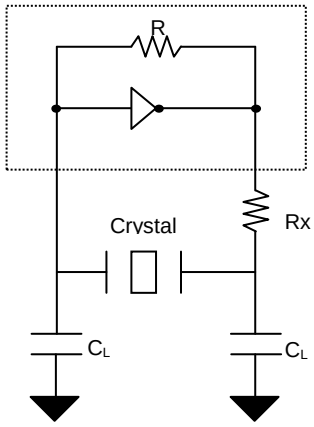


Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	24MHz
Frequency tolerance	± 50 ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance(C_P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

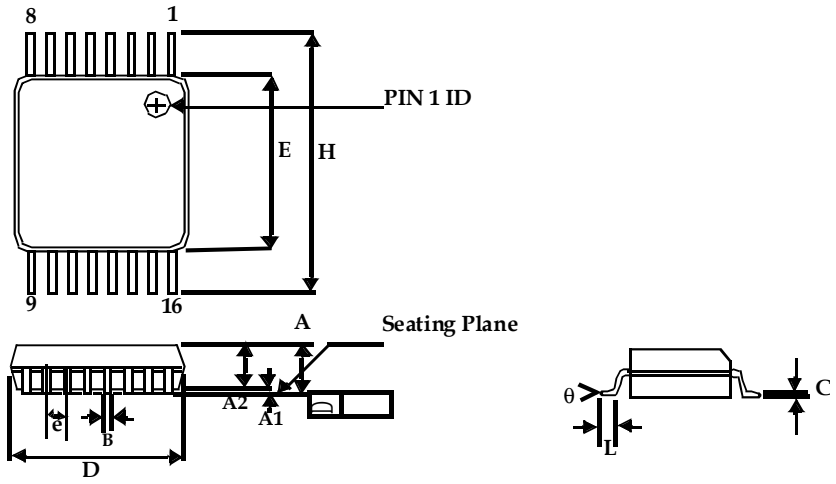
Typical Crystal Interface Circuit



$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace etc.

Package Information

16-lead Thin Shrunk Small Outline Package (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
θ	0°	8°	0°	8°

Ordering Code

Ordering Code	Marking	Package Type	Temperature
ASM3P2854CG-16TR	3P28 54C	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	0℃ to +7 0℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.

PUBLICATION ORDERING INFORMATION

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