



Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Application

- Battery protection
- Load switch
- Uninterruptible power supply

Product Summary

● N-Channel

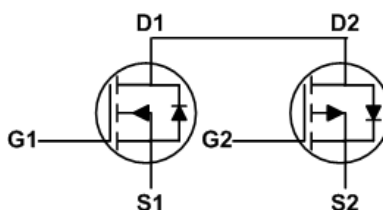
V_{DS}	40	V
$R_{DS(on), Typ} V_{GS}=10V$	18	mΩ
$R_{DS(on), Typ} V_{GS}=4.5V$	21	mΩ
I_D	21	A

● P-Channel

V_{DS}	-40	V
$R_{DS(on), Typ} V_{GS}=-10V$	31	mΩ
$R_{DS(on), Typ} V_{GS}=-4.5V$	41	mΩ
I_D	-20	A



TO252-4



N-Channel&P-Channel

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	21	-20	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	17	-16	A
I_{DM}	Pulsed Drain Current ²	84	-80	A
EAS	Single Pulse Avalanche Energy ³	32.1	38	mJ
I_{AS}	Avalanche Current	17.5	-26.1	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	21	25	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	62	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	6	5	$^{\circ}C/W$

N-Channel Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.032	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=15A$	---	18	23	$m\Omega$
		$V_{GS}=4.5V, I_D=10A$	---	21	27	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.7	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.8	---	$mV/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=15A$	---	35	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.8	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=32V, V_{GS}=4.5V, I_D=15A$	---	11	---	nC
Q_{gs}	Gate-Source Charge		---	2.61	---	
Q_{gd}	Gate-Drain Charge		---	4.7	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=20V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	2.8	---	ns
T_r	Rise Time		---	11.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	23.1	---	
T_f	Fall Time		---	6.4	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	891	---	pF
C_{oss}	Output Capacitance		---	86	---	
C_{rss}	Reverse Transfer Capacitance		---	68	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	21	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	84	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=15A, di/dt=100A/\mu s, T_J=25^{\circ}\text{C}$	---	11	---	nS
Q_{rr}	Reverse Recovery Charge		---	3.3	---	nC

Note :

- 1 .The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3 .The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=25A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

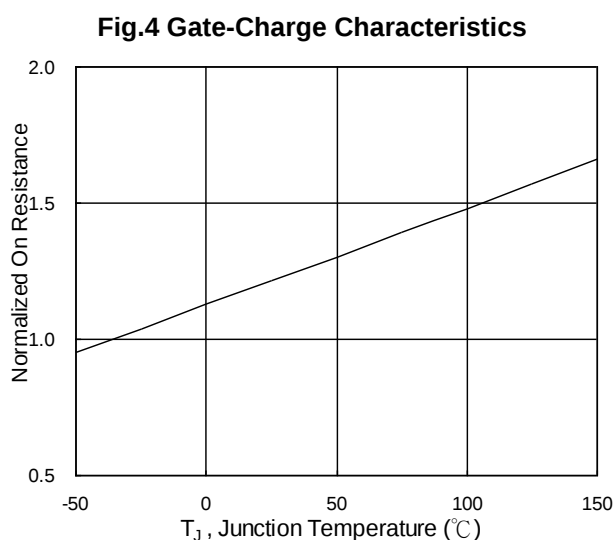
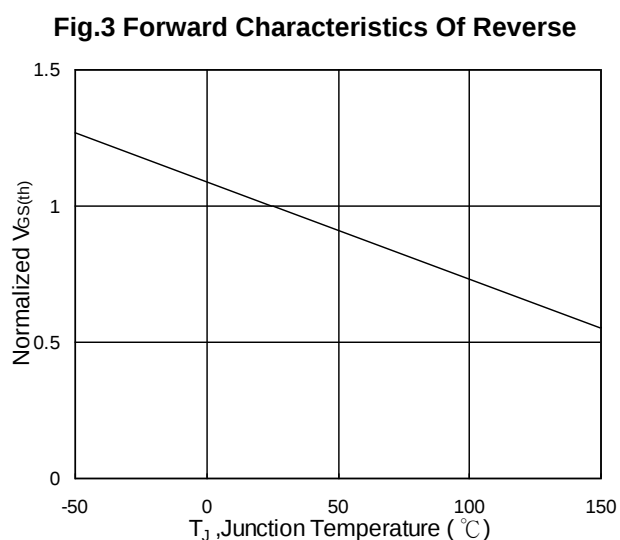
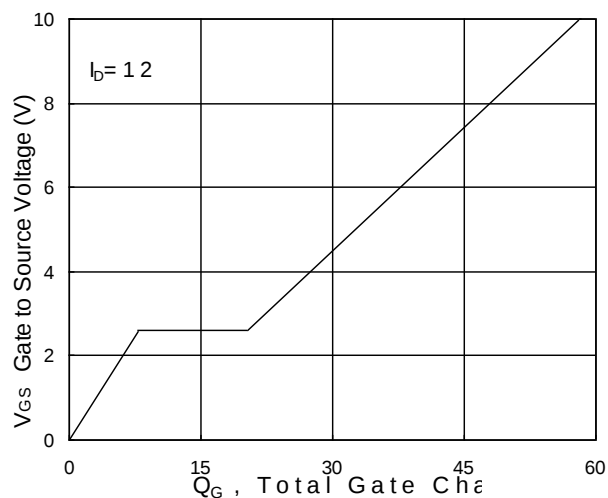
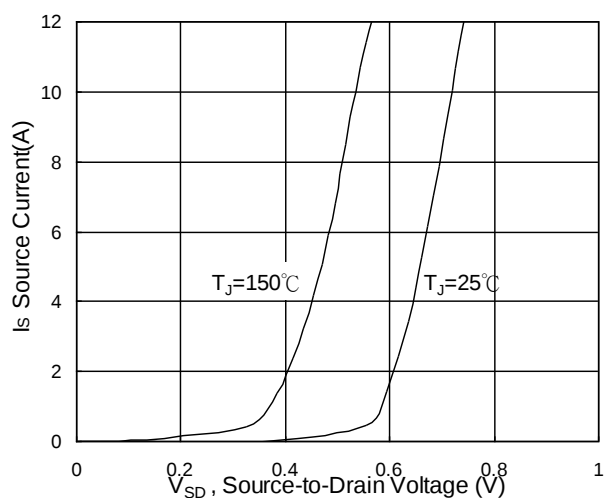
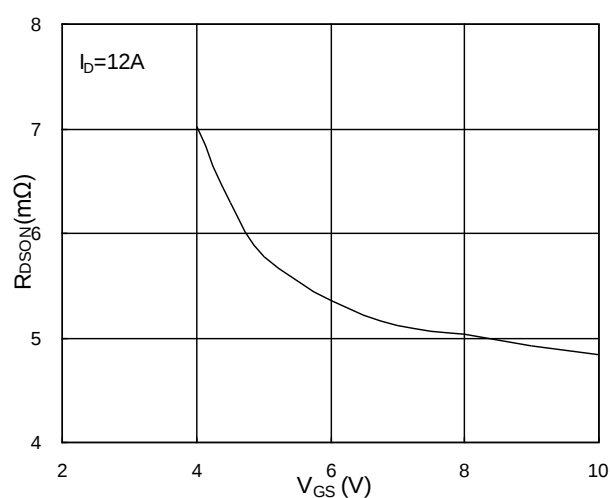
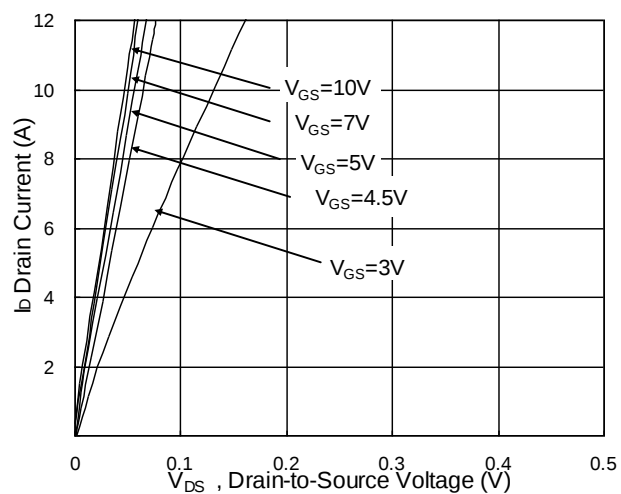
P-Channel Electrical Characteristics (T_c=25°C unless otherwise noted)

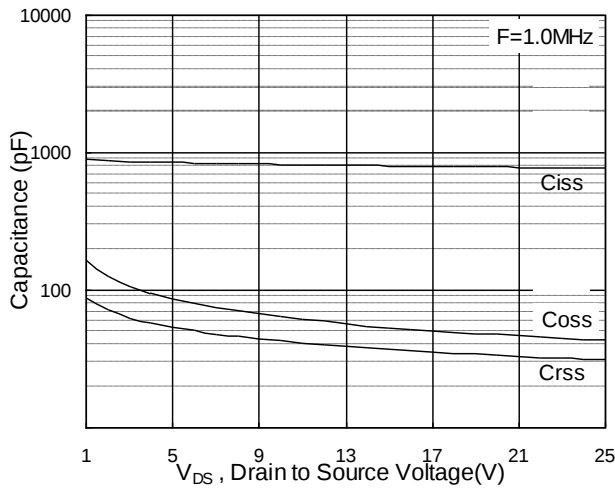
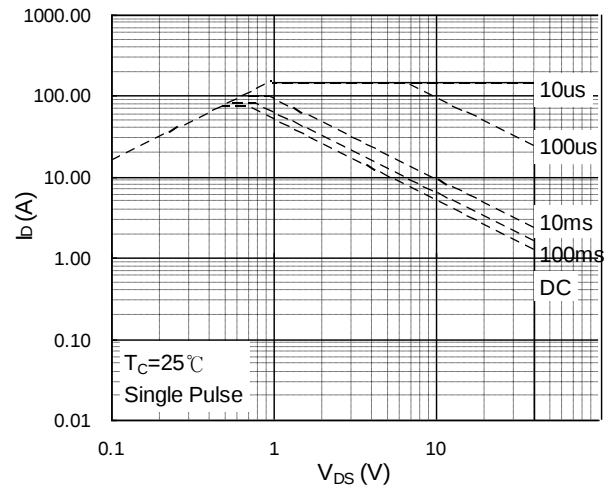
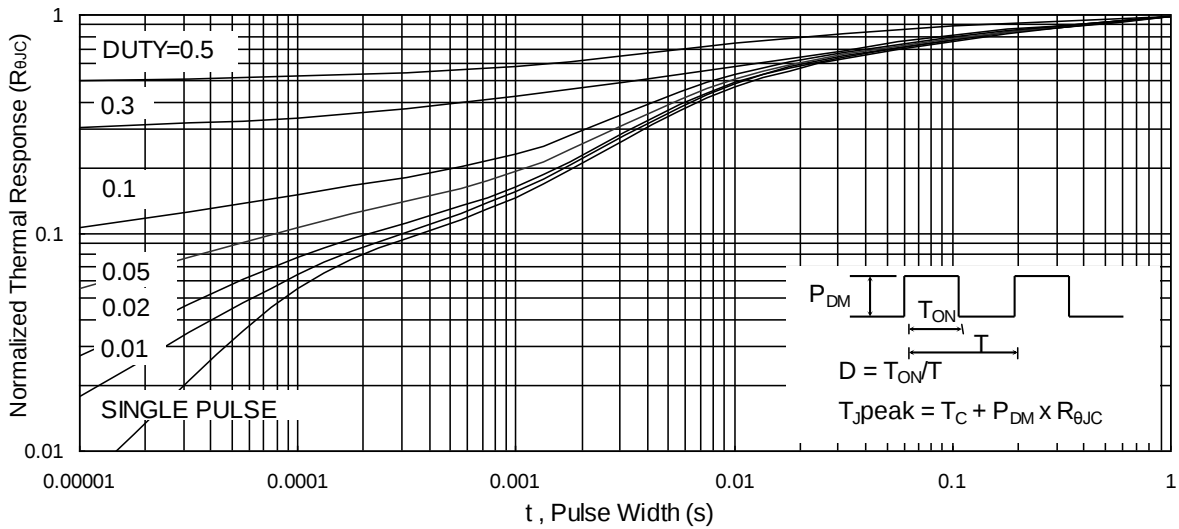
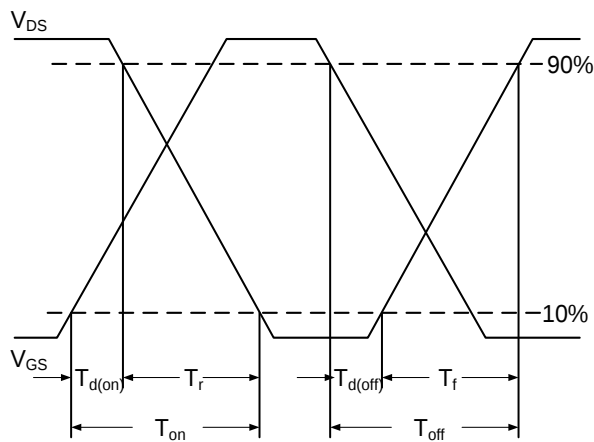
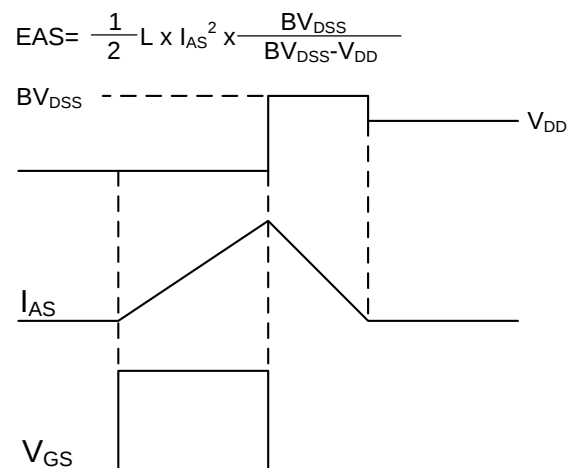
Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-40	-	-	V
Gate-body Leakage current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = -40V, V _{GS} = 0V	-	-	-1	μA
	T _J =100°C			-	-	-100	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance ⁴		R _{DS(on)}	V _{GS} = -10V, I _D = -8A	-	31	45	mΩ
			V _{GS} = -4.5V, I _D = -4A	-	41	58	
Forward Transconductance ⁴		g _{fs}	V _{DS} = -10V, I _D = -6A	-	16	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C _{iss}	V _{DS} = -20V, V _{GS} =0V, f =1MHz	-	1080	-	pF
Output Capacitance		C _{oss}		-	87	-	
Reverse Transfer Capacitance		C _{rss}		-	77	-	
Gate Resistance		R _g	f =1MHz	-	10.3	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q _g	V _{GS} = -10V,V _{DS} = -20V, I _D = -5A	-	17	-	nC
Gate-Source Charge		Q _{gs}		-	4.2	-	
Gate-Drain Charge		Q _{gd}		-	3.7	-	
Turn-On Delay Time		t _{d(on)}	V _{GS} = -10V, V _{DD} = -20V, R _G = 3Ω, I _D = -5A	-	5.9	-	ns
Rise Time		t _r		-	7.1	-	
Turn-Off Delay Time		t _{d(off)}		-	25	-	
Fall Time		t _f		-	8.2	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V _{SD}	I _S = -5A, V _{GS} = 0V	-	-	-1.2	V
Continuous Source Current	T _A =25°C	I _S	-	-	-	-26.1	A

Note :

1. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

N-Channel Typical Characteristics




Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Switching Wave

P-Channel Typical Characteristics

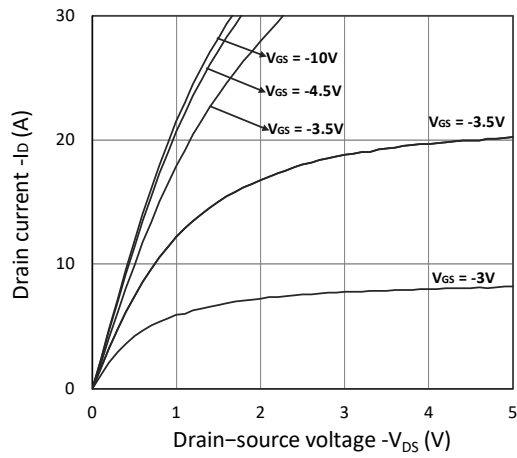


Figure 1. Output Characteristics

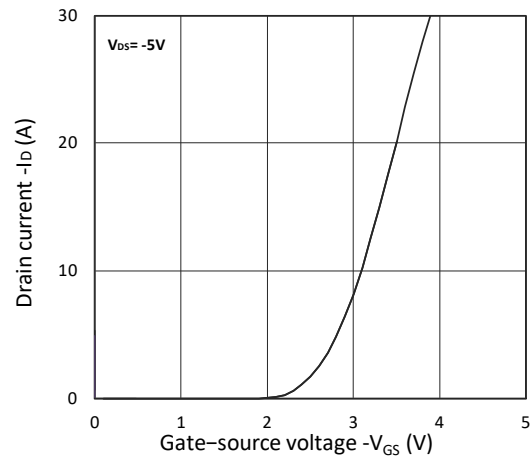


Figure 2. Transfer Characteristics

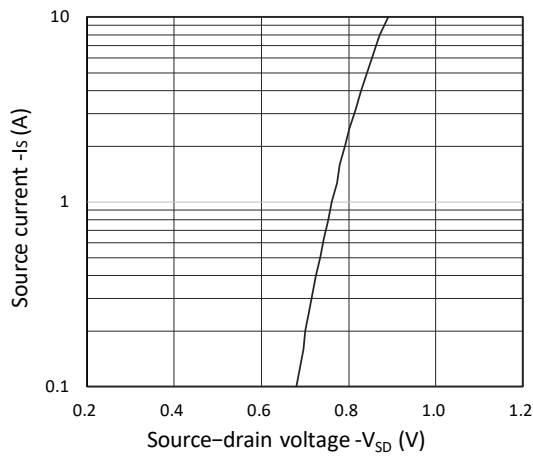


Figure 3. Forward Characteristics of Reverse

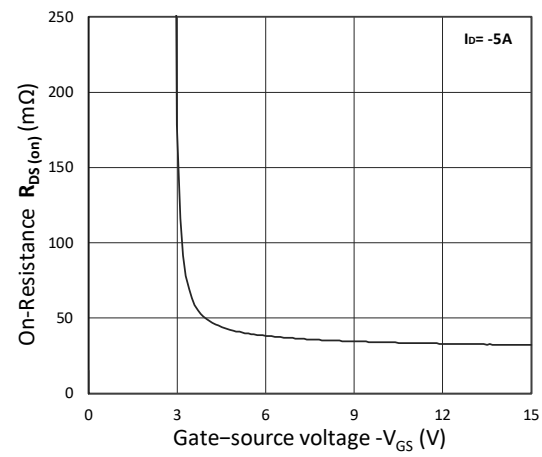


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

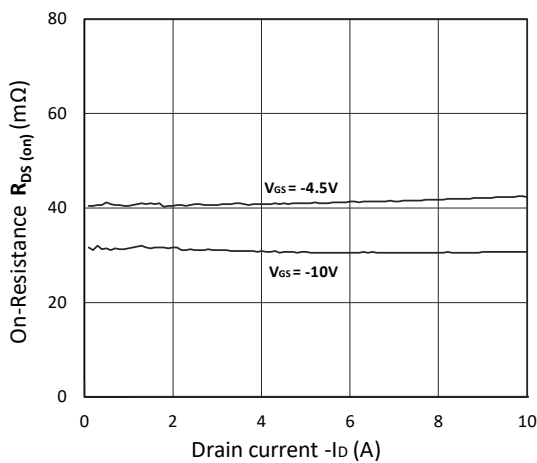


Figure 5. $R_{DS(ON)}$ vs. I_D

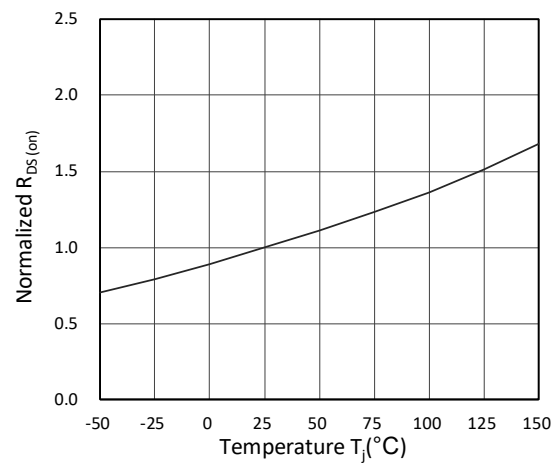


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

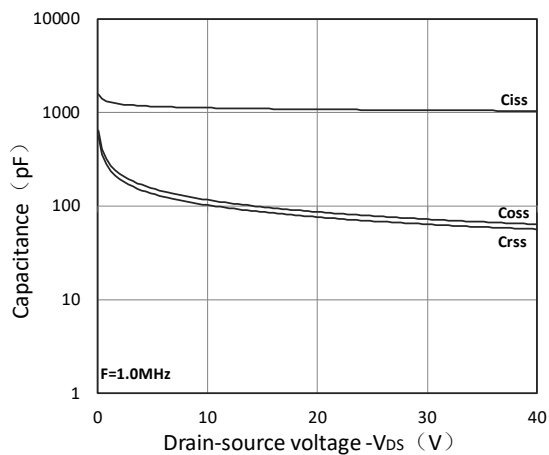


Figure 7. Capacitance Characteristics

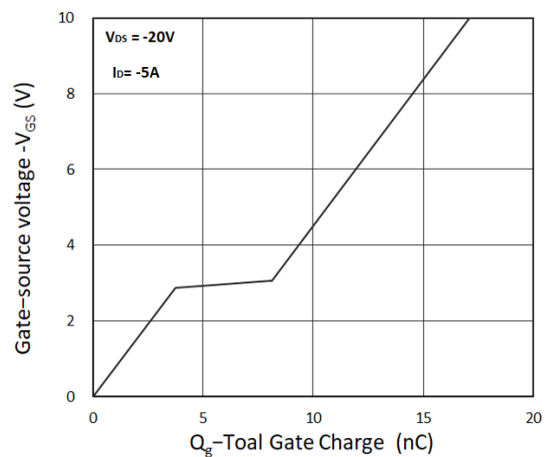


Figure 8. Gate Charge Characteristics

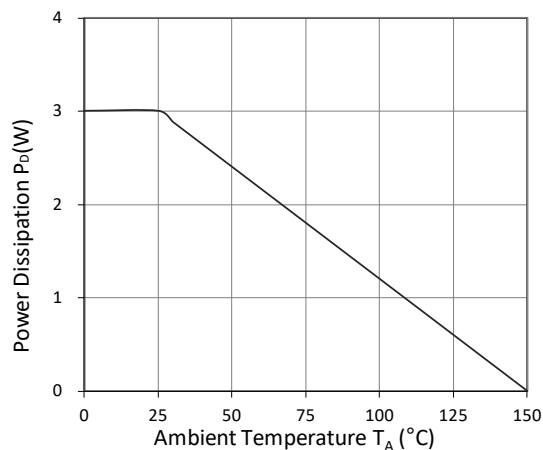


Figure 9. Power Dissipation

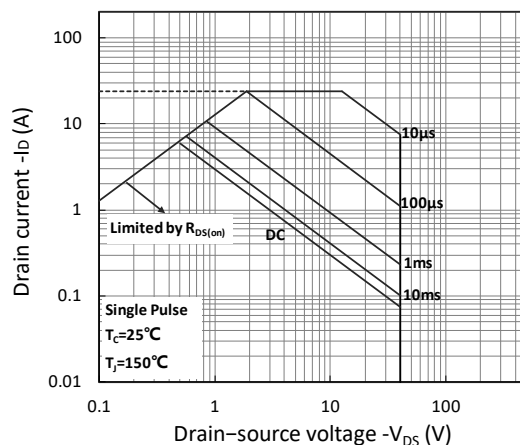


Figure 10. Safe Operating Area

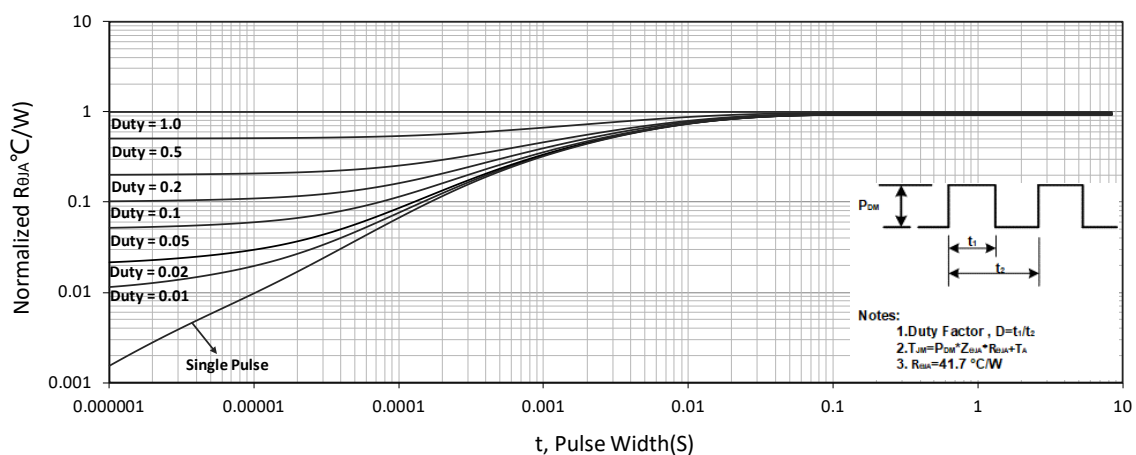
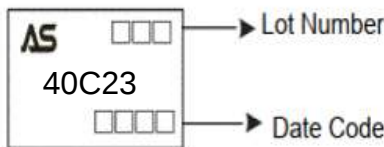


Figure 11. Normalized Maximum Transient Thermal Impedance

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM40C23JQ-R	40C23	TO-252-4	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252-4	 The diagram shows a TO-252-4 package with the following markings: - Top left: ASDsemi logo (AS) - Top right: Lot Number (indicated by two empty boxes) - Middle: 40C23 - Bottom right: Date Code (indicated by four empty boxes)

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