

General Description

The AS9632 is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost. The AS9632 is capable of delivering 2-Vrms output into a 10k Ω load with 3.3V supply. The gain settings can be set by users from $\pm 1\text{V/V}$ to $\pm 10\text{V/V}$ externally, and gain can be configured individually for R/L channel. The AS9632 has built-in active-mute control for pop-less audio on/off control. The AS9632 has internal and external under voltage protection to prevent POP noise. Built-in de-pop control sequence also help AS9632 to be a pop-less device.

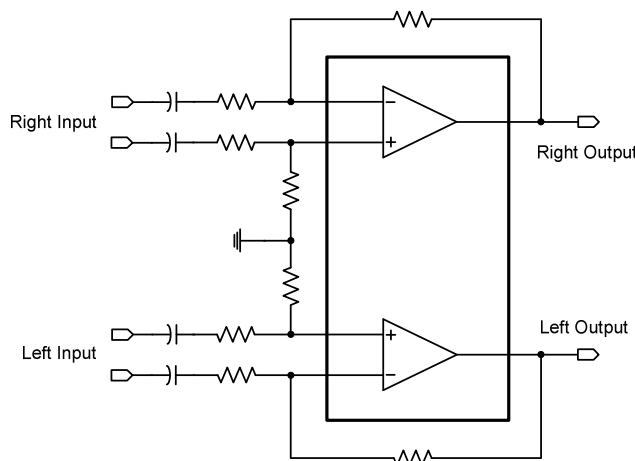
Applications

- ◆ LCD / PDP TVs
- ◆ DVD players
- ◆ Set-Top Boxes
- ◆ Home Theater in Box

Features

- ◆ Operation Voltage: 3.0V to 3.6V
- ◆ Cap-less Output
 - Eliminates Output Capacitors
 - Improves Low Frequency Response
 - Reduces POP/Clicks
 - Reduce Board Area and Component Cost
- ◆ Low Noise and THD
 - SNR > 102dB
 - Typical $V_n < 12\mu\text{Vrms}$
 - THD+N < 0.02% at 20Hz~20kHz
- ◆ Maximum Output Voltage Swing into 10k Ω Load
 - 2Vrms at 3.3V Supply Voltage
- ◆ 600 Ω Output Load Compliant
- ◆ Differential Input, single-Ended Output
- ◆ External Gain Setting from 1V/V to 10V/V
- ◆ Fast Start-up Time : 0.5ms
- ◆ Integrated De-Pop Control
- ◆ External Under Voltage Protection
- ◆ Thermal Protection
- ◆ Active Mute Control for Pop-less Audio ON/OFF Control
- ◆ +/-8kV IEC ESD Protection at line outputs
- ◆ TSSOP-14

Typical Application



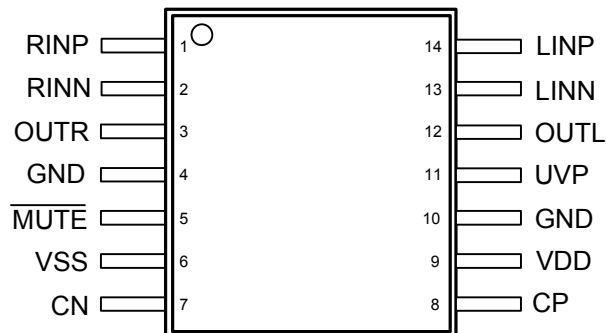
Order Information

Part Number	Package	Packing	Remark
AS9632DT/TR-HF	TSSOP-14	Tape & Reel MPQ=2.5k	Green

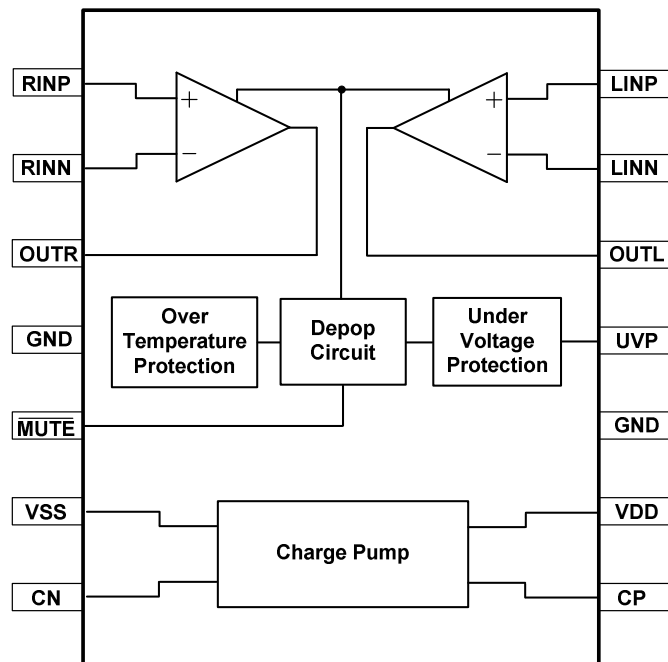
Pin Description

Pin#	Name	Type ⁽¹⁾	Description
1	LINP	I	Left channel OP positive input
2	LINN	I	Left channel OP negative input
3	OUTL	O	Left channel OP output
4	SGND	P	Signal ground
5	MUTE	I	Mute, active low
6	PVSS	O	Supply voltage
7	CN	I/O	Charge-pump flying capacitor negative terminal
8	CP	I/O	Charge-pump flying capacitor positive terminal
9	PVDD	P	Positive supply
10	PGND	P	Power ground
11	UVP	I	Under-voltage protection input
12	OUTR	O	Right channel OP output
13	RINN	I	Right channel OP negative input
14	RINP	I	Right channel OP positive input

(1) I=input, O=output, P=power

TSSOP-14
(Top View)

Functional Block Diagram



Available Package

Part Number	Package	θ_{ja} (°C/W) ⁽¹⁾	θ_{jc} (°C/W) ⁽²⁾
AS9632DT/TR-HF	TSSOP-14	100	32

(1) θ_{ja} is measured at room temperature ($T_A=25^{\circ}\text{C}$), natural convection environment test board, which is constructed with a thermal efficient, 2-layers PCB. The measurement is tested using the JEDEC51-3 thermal measurement standard.

(2) θ_{jc} represents the heat resistance for the heat flow between the chip and package's top surface.

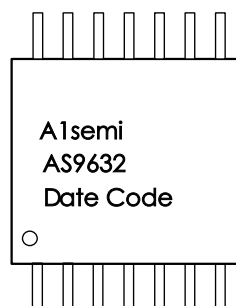
Marking Information.

AS9632

Line 1 : LOGO

Line 2 : Product No.

Line 3 : Date Code



Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Value	Unit
	Supply Voltage, VDD to GND	-0.3 to 5.5	V
V _I	Input Voltage	VSS -0.3 to VDD+0.3	V
R _L	Minimum load impedance	> 600	Ω
	$\overline{\text{MUTE}}$ to GND	-0.3 to VDD+0.3	V
T _{stg}	Storage temperature range	-65 to 150	°C
T _J	Maximum junction temperature	125	°C

(1) The absolute maximum ratings are limiting values of operation, safety of the device cannot be guaranteed if beyond those values.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Unit
V _{DD}	Supply Voltage		3.0	3.3	3.6	V
V _{IH}	High Level Input Voltage	$\overline{\text{MUTE}}$		60		% of V _{DD}
V _{IL}	Low Level Input Voltage	$\overline{\text{MUTE}}$		40		% of V _{DD}
T _A	Operating Ambient Temperature Range		0		70	°C
T _J	Operation junction temperature range		-40		125	°C
R _L	Load Resistance		600			Ω

Electrical Characteristics

PVDD=3.3V, T_A=25°C, R_L=10k Ω , C_{FLY}=C_{PVSS}=1 μ F, C_{IN}=1 μ F, R_I=10k Ω , R_F=20k Ω (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Nom	Max	Unit
I _{DD}	V _{DD} Supply Current	$\overline{\text{MUTE}}=\text{VDD}$		7	15	mA
I _{SD}	V _{DD} Shutdown Current	$\overline{\text{MUTE}}=0\text{V}$			100	μ A
I _I	Input Current	$\overline{\text{MUTE}}$ pin		0.1		μ A
V _O	Output Voltage (Outputs In Phase)	THD+N=1%, V _{DD} =3.3V, f _{IN} =1kHz		2.3		Vrms
THD+N	Total Harmonic Distortion Plus Noise	V _O =2Vrms, f _{IN} =1kHz		0.002		%
Crosstalk	Channel Separation	V _O =2Vrms, f _{IN} =1kHz		-110		dB
V _N	Output Noise	R _I =10k, R _F =10k		11	15	μ Vrms
V _{SR}	Slew Rate			8		V/ μ s
SNR	Signal to Noise Ratio	V _O =2Vrms, R _I =10k, R _F =10k, A-weighted	102	107		dB
G _{BW}	Unit-Gain Bandwidth			8		MHz
A _{VO}	Open-Loop Gain		80			dB
V _{OS}	Output Offset Voltage	V _{DD} =3.0V to 3.6V, Input Grounded	-5		5	mV

Electrical Characteristics (Con't)

PVDD=3.3V, T_A=25°C, R_L=10k Ω , C_{FLY}=C_{PVSS}=1 μ F, C_{IN}=1 μ F, R_I=10k Ω , R_F=20k Ω (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Nom)	Max	Unit
PSRR	Power Supply Rejection Ratio	V _{DD} =3.0V to 3.6V, V _{rr} =200mVrms, f _{IN} =1kHz		-80	-60	dB
R _I	Input Resistor Range		1	10	47	k Ω
R _F	Feedback Resistor Range		4.7	20	100	k Ω
f _{CP}	Charge-Pump Frequency		400	500	600	kHz
	Maximum capacitive Load			220		pF
V _{UVP}	External Under Voltage Detection			1.25		V
I _{HYS}	External Under Voltage Detection Hysteresis Current			5		μ A
TSD	Over Temperature Protection Level			150		°C
T _{start-up}	Start-up Time			0.5		ms

Application Information

Line Driver Amplifiers Operation

A conventional inverting line-driver amplifier always requires an output dc-blocking capacitor and a bypass capacitor, see Figure 1. DC blocking capacitors are large in size and cost a lot. It also restricts the output low frequency response. POP will occur if the charge and discharge processes on output capacitors are not carefully take cared. Besides, it needs to wait for a long time to charge V_{OUT} from 0V to V_{DD}/2.

For a cap-less line driver, see figure 2, a negative supply voltage (-V_{DD}) is produced by the integrated chargepump, and feeds to line driver's negative supply instead of ground. The positive input can directly connect to ground without a C_{BYPASS}, and V_{OUT} is biased at ground which can eliminate the output dcblocking capacitors. The output voltage swing is doubled compared to conventional amplifiers.

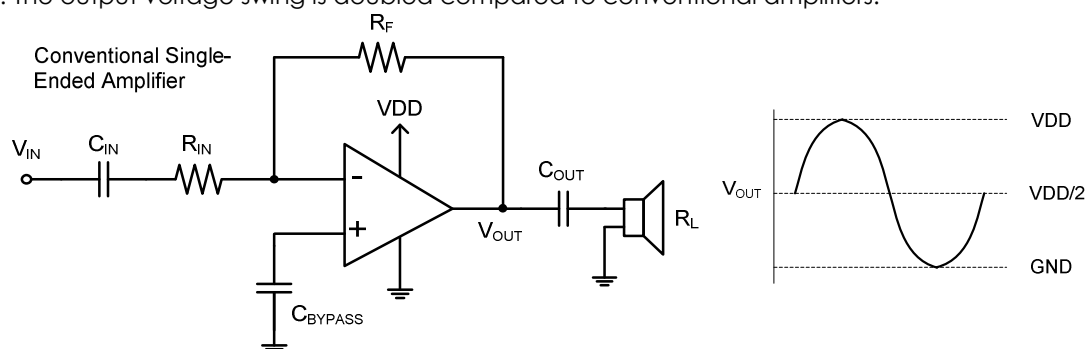


Figure 1. Conventional Line Driver Amplifier

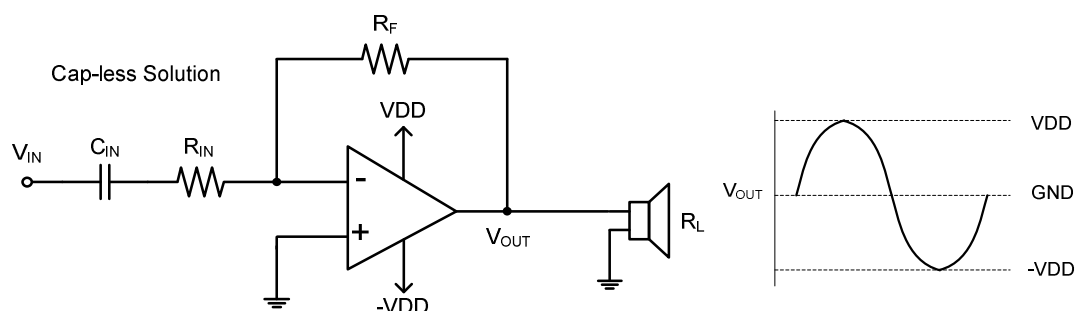


Figure 2. Cap-less Line Driver Amplifier

External Under-Voltage Protection

The external under-voltage protection is used to mute the line-driver before any input voltage change to generate a POP. The threshold of UVP pin is designed to 1.25V. By using a resistor divider, users can decide the UVP level and hysteresis level. The levels can be obtained by following equations:

$$V_{UVP} = (1.25V - 6\mu A \times R13) \times (R11 + R12) / R12$$

$$Hysteresis = 5\mu A \times R13 \times (R11 + R12) / R12$$

With the condition $R13 \gg (R11 // R12)$. For example, to obtain $V_{UVP}=2.67V$, $Hysteresis=0.37V$, $R11=1.5k\Omega$, $R12=1k\Omega$, $R13=30k\Omega$.

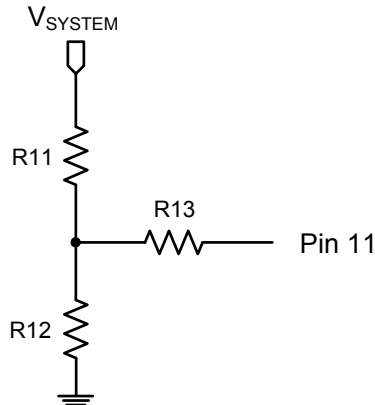


Figure 3. Application Circuit of UVP Pin

Charge-Pump Operation

The charge-pump is used to generate a negative supply voltage to supply to line-driver. It needs two external capacitors, C_{FLY} and C_{PVSS} , for normal operation, see figure 4 (a). The operation can be analyzed with two phase. In phase I, see figure 4 (b), C_{FLY} is charged to $PVDD$, and in phase II, see figure 4 (c), the charges on C_{FLY} are shared with C_{PVSS} , that makes $PVSS$ a negative voltage. After an adequate clock cycles, $PVSS$ will be equaled to $-PVDD$. Low ESR capacitors are recommended, and the typical value of C_{FLY} and C_{PVSS} is 1F. A smaller capacitance can be used, but the maximum output voltage may be reduced.

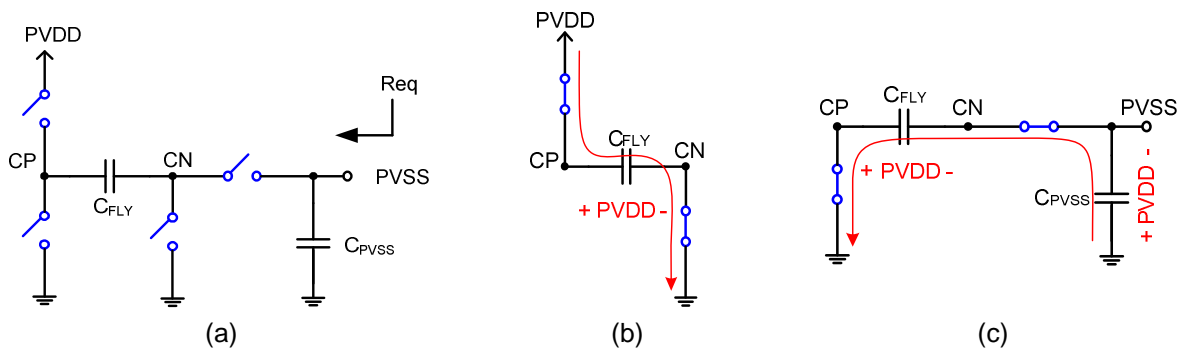


Figure 4. Charge-Pump Operation

Mute Function

The mute function is used to reduce power consumption while the device is not in use. When a logic low is applied to this pin, the output driver circuits are turned off. Line driver output and PVSS are pulled to ground. When a logic high is applied to mute pin, the PVSS is started to build-up and line driver output signal is released after about 0.5ms typically.

Decoupling Capacitors

A low ESR power supply decoupling capacitor is required for better performance. The capacitor should place as close to chip as possible, the value is typically 1 μ F. For filtering low frequency noise signals, a 10 μ F or greater capacitor placed near the chip is recommended.

Input Blocking Capacitors (C_{IN})

An input blocking capacitor is required to block the dc voltage of the audio source and allows the input to bias at a proper dc level for optimum operation. The input capacitor and input resistor (R_I) form a high-pass filter with the corner frequency determined as following equation:

$$f_C = \frac{1}{2\pi R_I C_{IN}}$$

Gain Setting Resistors (R_I and R_F)

The line driver's gain is determined by R_I and R_F . The typical configurations of the amplifier are inverting, non-inverting, and differential input, see figure 5. The gain equations are listed as follows:

(a) Inverting configuration : $A_V = -\frac{R_F}{R_I}$

(b) Non-inverting configuration : $A_V = 1 + \frac{R_F}{R_I}$

(c) Differential-input configuration : $A_V = \frac{R_F}{R_I}$

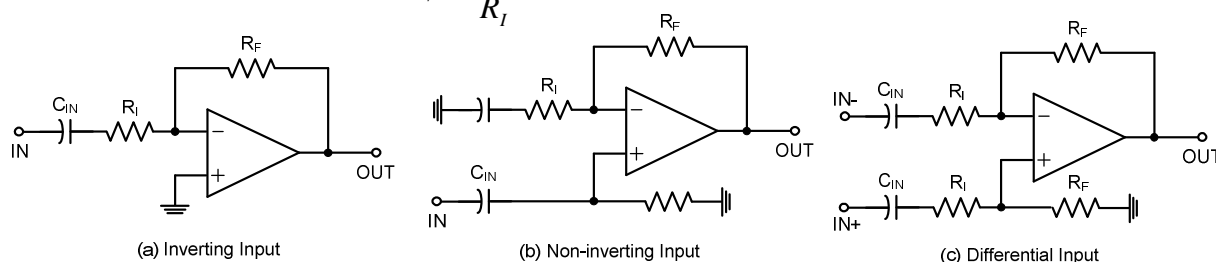


Figure 5. Line Driver Amplifier Configurations

The values of R_i and R_f must be chosen with consideration of stability, frequency response and noise. The recommended value of R_i is in the range from $1k\Omega$ to $47k\Omega$, and R_f is from $4.7k\Omega$ to $100k\Omega$ for. The gain is in the range from $-1V/V$ to $-10V/V$ for inverting configuration. Table 1 lists the recommended resistor values for different configurations.

R_i (k Ω)	R_f (k Ω)	Inverting Input Gain (V/V)	Non-inverting Input Gain (V/V)	Differential Input Gain (V/V)
22	22	-1	2	1
15	30	-2	3	2
33	68	-2.1	3.1	2.1
10	100	-10	11	10

Table 1. Recommended Resistor Values

Second-Order Filter Configuration

AS9632 can be used like a standard OPAMP. Several filter topologies can be implemented by using AS9632, both single-ended and differential input configuration, see figure 6. For inverting input configuration, the overall gain is $-\frac{R_2}{R_1}$, the high-pass filter's cutoff frequency is $\frac{1}{2\pi R_1 C_3}$, the low-pass filter's cutoff frequency is $\frac{1}{2\pi \sqrt{R_2 R_3 C_1 C_3}}$

The detail component values are listed on table 2.

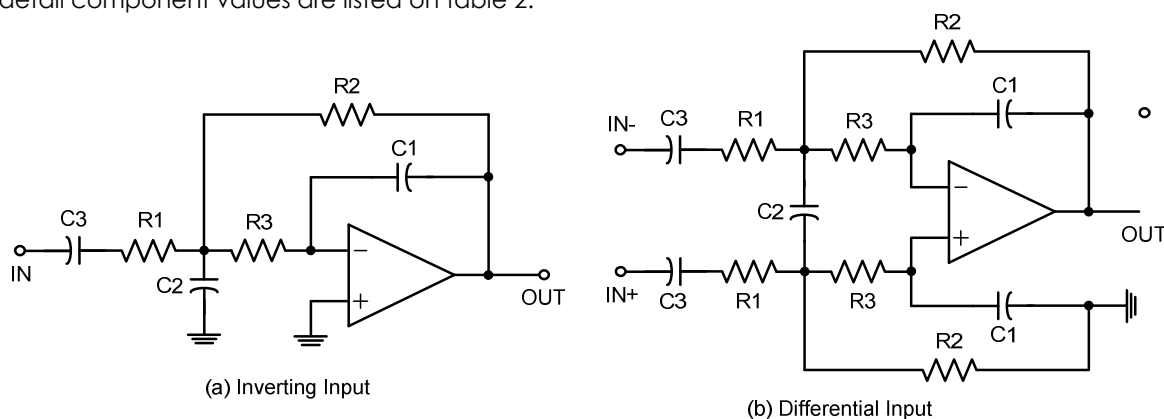


Figure 6. Second-order Active Low-Pass Filter

Gain (V/V)	High Pass (Hz)	Low Pass (kHz)	C1 (pF)	C2 (pF)	C3 (F)	R1 (k Ω)	R2 (k Ω)	R3 (k Ω)
-1	1.6	40	100	680	10	10	10	24
-1.5	1.3	40	68	680	15	8.2	12	30
-2	1.6	60	33	150	6.8	15	30	47
-2	1.6	30	47	470	6.8	15	30	43
-3.33	1.2	30	33	470	10	13	43	43
-10	1.5	30	22	1000	22	4.7	47	27

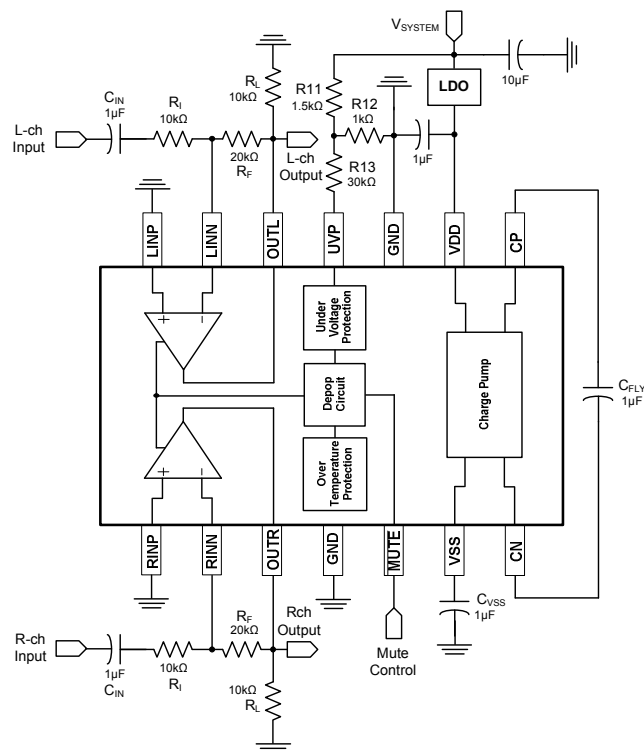
Table 2. Second-order Low-Pass Filter Specifications

Over-Temperature Protection

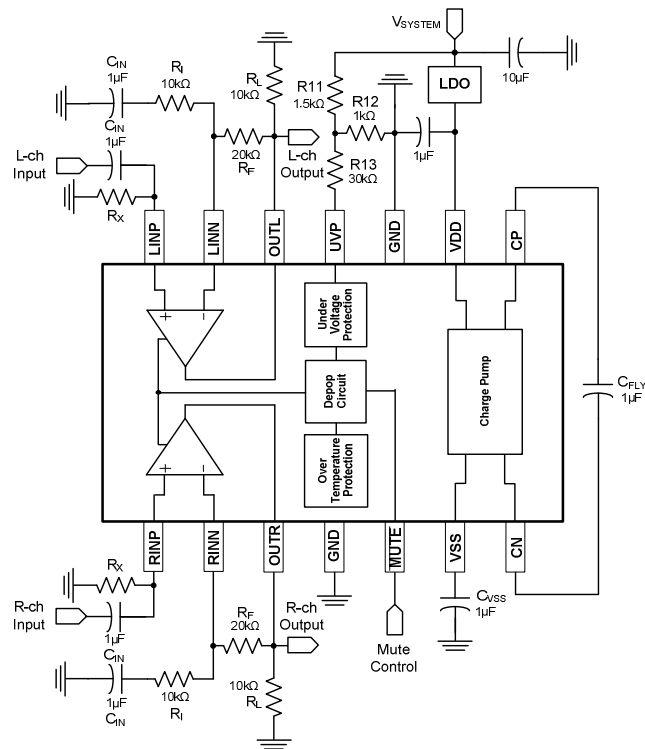
AS9632 provide an over-temperature protection to limit the junction temperature to 150°C. As junction temperature exceeds 150°C, internal thermal sensor will turn off the drivers immediately. The drivers will turn on again if the junction temperature is smaller than 130°C. A 20°C hysteresis is designed to lower the average junction temperature during continuous thermal overload conditions, increasing lifetime of the chip.

Typical Performance Characteristics

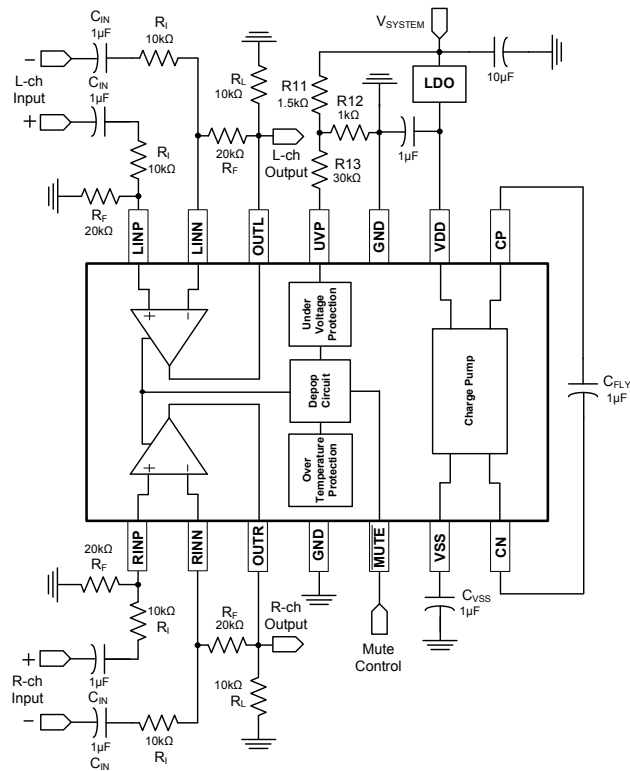
Inverting Input Line Driver Amplifier



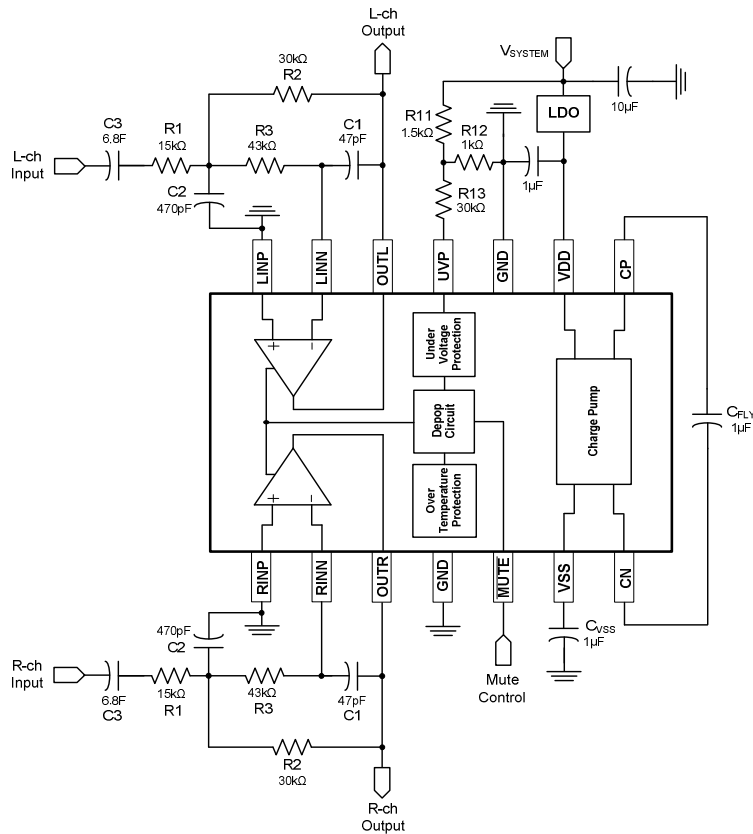
Non-inverting Input Line Driver Amplifier



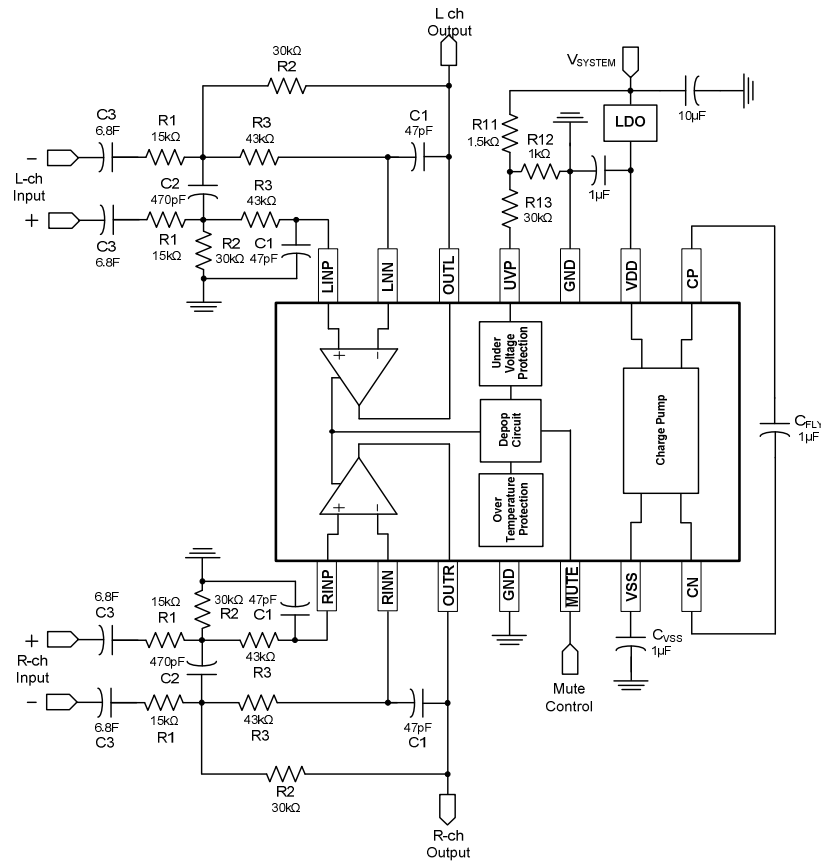
Differential Input Line Driver Amplifier



Inverting Input Second-Order Active Low-Pass Filter

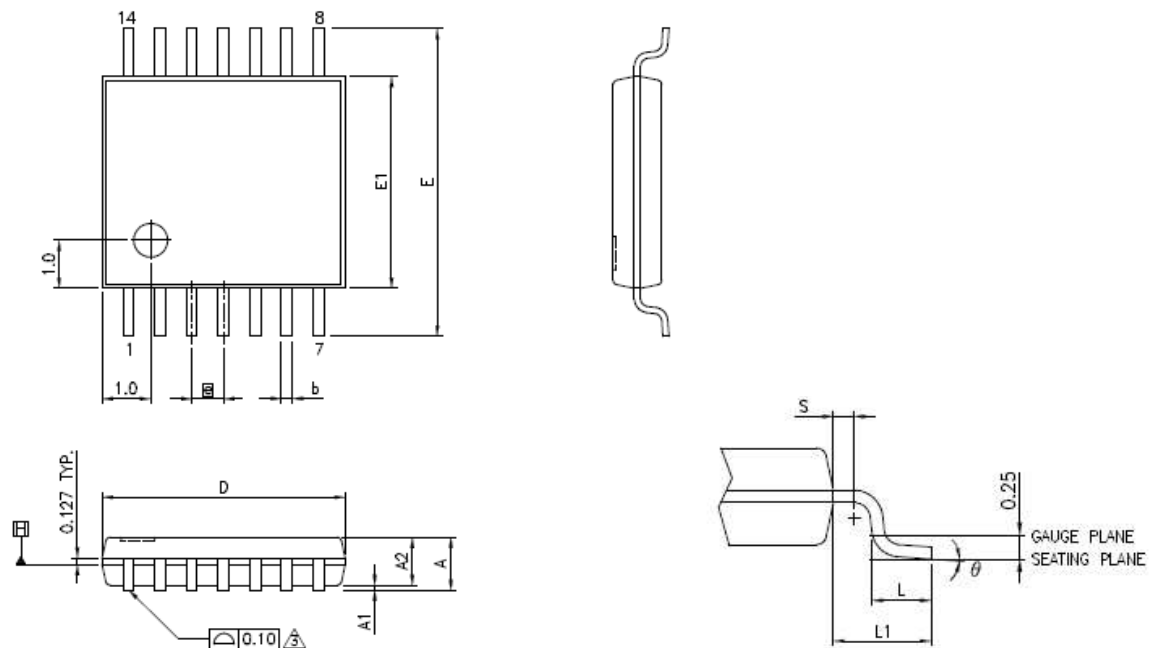


Differential Input Second-Order Active Low-Pass Filter



Package

TSSOP-14



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS		MIN.	NOM.	MAX.
A1	A	—	—	1.20
	STANDARD	0.05	—	0.15
	THERMALLY ENHANCED	0.00	—	0.15
A2		0.80	1.00	1.05
b		0.19	—	0.30
D		4.90	5.00	5.10
E1		4.30	4.40	4.50
E		6.40 BSC		
[e]		0.65 BSC		
L1		1.00 REF		
L		0.50	0.60	0.75
S		0.20	—	—
θ		0°	—	8°

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