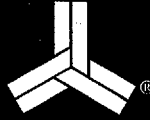


High Performance 64K×8 CMOS SRAM



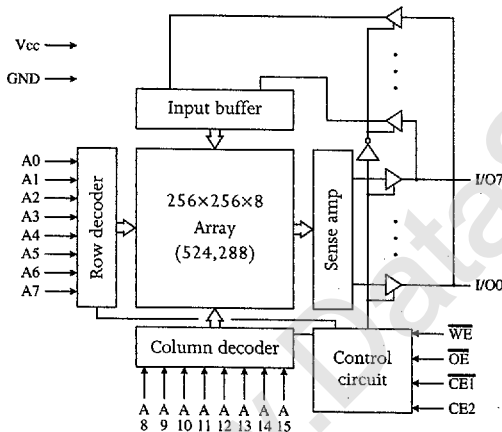
64K×8 CMOS SRAM

AS7C512
AS7C512L

Features

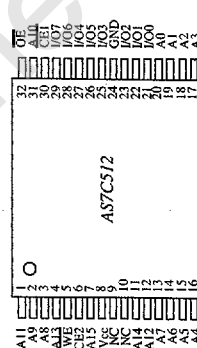
- Organization: 65,536 words × 8 bits
- High speed
 - 12/15/20/25/35 ns address access time
 - 3/4/5/6/8 ns output enable access time
- Low power consumption
 - Active: 688 mW max (12 ns cycle)
 - Standby: 27.5 mW max, CMOS I/O
 - 4.25 mW max, CMOS I/O, L version
 - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, $CE2$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
 - 32-pin JEDEC standard packages
 - 300 mil PDIP and SOJ
 - Socket compatible with 7C256 and 7C1024
 - 525 mil SOIC
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram

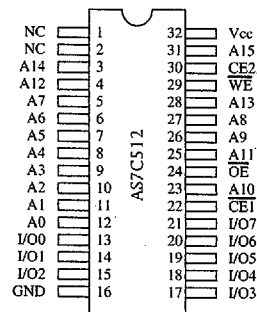


Pin arrangement

TSOP 8×20



DIP, SOJ, SOIC



Selection guide

	7C512-12	7C512-15	7C512-20	7C512-25	7C512-35	Unit
Maximum address access time		15	20	25	35	ns
Maximum output enable access time		4	5	6	8	ns
Maximum operating current		115	105	95	80	mA
Maximum CMOS standby current		5.0	5.0	5.0	5.0	mA
	L	0.75	0.75	0.75	0.75	mA

Shaded areas contain advance information.



Functional description

The AS7C512 is a high performance CMOS 524,288-bit Static Random Access Memory (SRAM) organized as 65,536 words $\times$ 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 12/15/20/25/35 ns with output enable access times (t_{OE}) of 3/4/5/6/8 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, $CE2$) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or $CE2$ is LOW the device enters standby mode. The standard AS7C512 is guaranteed not to exceed 27.5 mW power consumption in standby mode; the L version is guaranteed not to exceed 4.25 mW, and typically requires only 800 μ W. The L version also offers 2.0V data retention, with maximum power of 400 μ W.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, $CE2$). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or $CE2$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, $CE2$), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C512 is packaged in all high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	-0.5	+7.0	V
Power dissipation	P_D	—	1.0	W
Storage temperature (plastic)	T_{stg}	-55	+150	$^{\circ}$ C
Temperature under bias	T_{bias}	-10	+85	$^{\circ}$ C
DC output current	I_{out}	—	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	$CE2$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High-Z	Standby (I_{SB} , I_{SB1})
X	L	X	X	High-Z	Standby (I_{SB} , I_{SB1})
L	H	H	H	High-Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

($T_a = 0^{\circ}$ C to $+70^{\circ}$ C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.2	—	$V_{CC}+1$	V
	V_{IL}	-0.5	—	0.8	V

V_{IL} min = -3.0V for pulse width less than $t_{RC}/2$

DC operating characteristics¹(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test conditions	-12		-15		-20		-25		-35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	I _{LI}	V _{CC} = Max, V _{in} = GND to V _{CC}	—	—	—	1	—	1	—	1	—	1	μA
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} , V _{CC} = Max, V _{out} = GND to V _{CC}	—	—	—	1	—	1	—	1	—	1	μA
Operating power supply current	I _{CC}	CE1 = V _{IL} , CE2 = V _{IH} , f = f _{max} , I _{out} = 0 mA	—	125	—	115	—	105	—	95	—	80	mA
			L	130	—	110	—	100	—	90	—	75	mA
Standby power supply current	I _{SB}	CE1 = V _{IH} or CE2 = V _{IL} , f = f _{max}	—	15	—	35	—	35	—	30	—	25	mA
			L	40	—	30	—	30	—	25	—	20	mA
	I _{SB1}	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V, V _{in} ≤ 0.2V or V _{in} ≥ V _{CC} - 0.2V, f = 0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	mA
			L	0.75	—	0.75	—	0.75	—	0.75	—	0.75	mA
Output voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V
	V _{OH}	I _{OH} = -4 mA, V _{CC} = Min	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V

Shaded areas contain advance information.

Capacitance²(f = 1 MHz, T_a = Room temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, CE1, CE2, WE, OE	V _{in} = 0V	5	pF
I/O capacitance	C _{I/O}	I/O	V _{in} = V _{out} = 0V	7	pF

Read cycle

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	12	—	15	—	20	—	25	—	35	—	ns	
Address access time	t _{AA}	12	—	15	—	20	—	25	—	35	—	ns	3
Chip enable (CE1) access time	t _{ACE1}	12	—	15	—	20	—	25	—	35	—	ns	3, 12
Chip enable (CE2) access time	t _{ACE2}	12	—	15	—	20	—	25	—	35	—	ns	3, 12
Output enable (OE) access time	t _{OE}	4	—	4	—	5	—	6	—	8	—	ns	
Output hold from address change	t _{OH}	3	—	3	—	3	—	3	—	3	—	ns	5
Chip enable (CE1) to output in Low Z	t _{CLZ1}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
Chip enable (CE2) to output in Low Z	t _{CLZ2}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
Chip disable (CE1) to output in High Z	t _{CHZ1}	3	—	4	—	5	—	6	—	8	—	ns	4, 5, 12
Chip disable (CE2) to output in High Z	t _{CHZ2}	3	—	4	—	5	—	6	—	8	—	ns	4, 5, 12
Output enable to output in Low Z	t _{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Output disable to output in High Z	t _{OHZ}	3	—	4	—	5	—	6	—	8	—	ns	4, 5
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	0	—	0	—	ns	4, 5, 12
Chip disable to power down time	t _{PD}	12	—	15	—	20	—	25	—	35	—	ns	4, 5, 12

Shaded areas contain advance information.



Key to switching waveforms

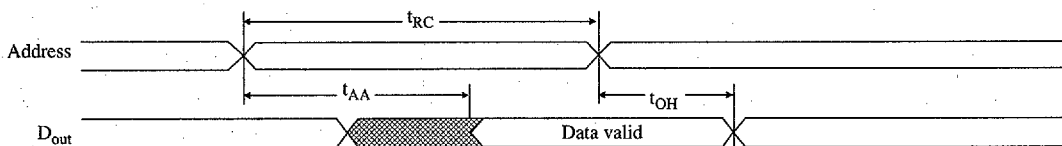
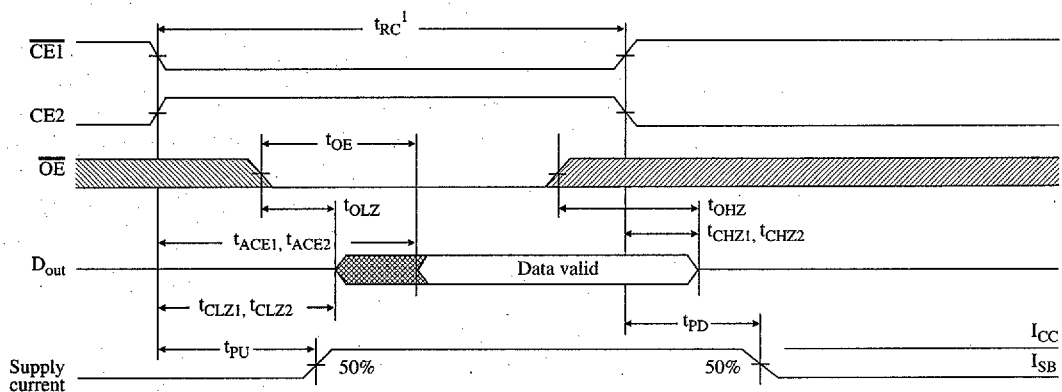
Rising input

Falling input

Undefined output/don't care

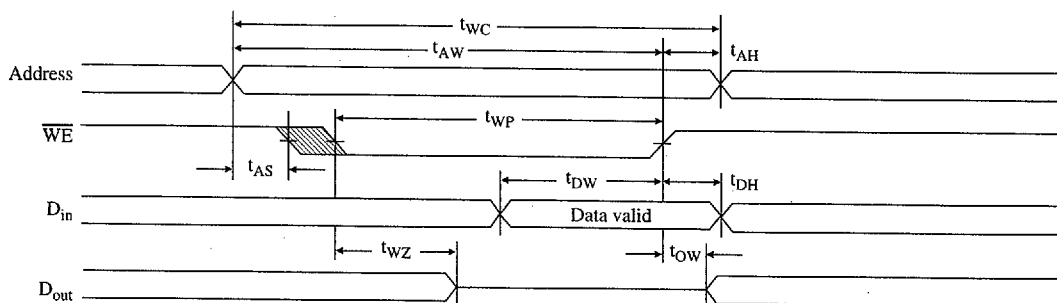
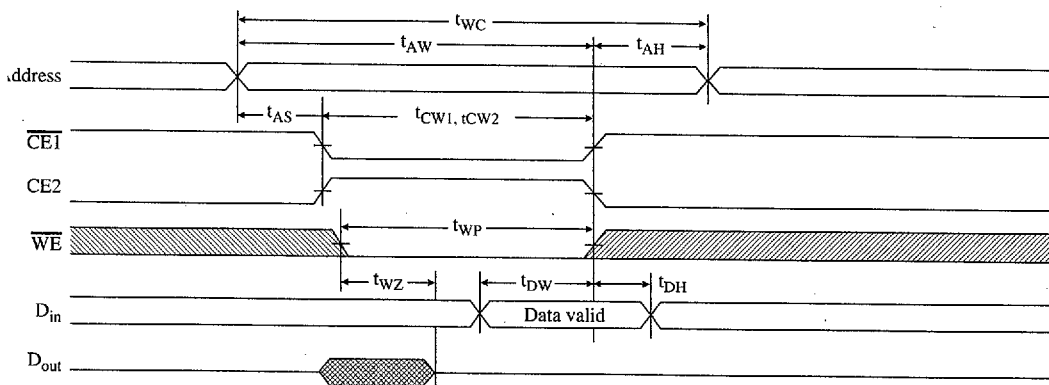
Read waveform 1 ^{3,6,7,9,12}

Address controlled

Read waveform 2 ^{3,6,8,9,12} $\overline{\text{CE1}}$ and CE2 controlledWrite cycle ^{11,12} $(V_{CC} = 5V \pm 10\%, GND = 0V, T_a = 0^\circ\text{C to } +70^\circ\text{C})$

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	12	—	15	—	20	—	20	—	30	—	ns	
Chip enable ($\overline{\text{CE1}}$) to write end	t_{CW1}	10	—	10	—	12	—	15	—	20	—	ns	12
Chip enable (CE2) to write end	t_{CW2}	10	—	10	—	12	—	15	—	20	—	ns	12
Address setup to write end	t_{AW}	10	—	10	—	12	—	15	—	20	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	12
Write pulse width	t_{WP}	8	—	9	—	12	—	15	—	17	—	ns	
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to write end	t_{DW}	9	—	9	—	12	—	15	—	15	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Write enable to output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	—	5	ns	4, 5
Output active from write end	t_{OW}	3	—	3	—	3	—	3	—	3	—	ns	4, 5

Shaded areas contain advance information.

Write waveform 1 ^{10,11,12} $\overline{\text{WE}}$ controlledWrite waveform 2 ^{10,11,12} $\overline{\text{CE1}}$ and CE2 controlled

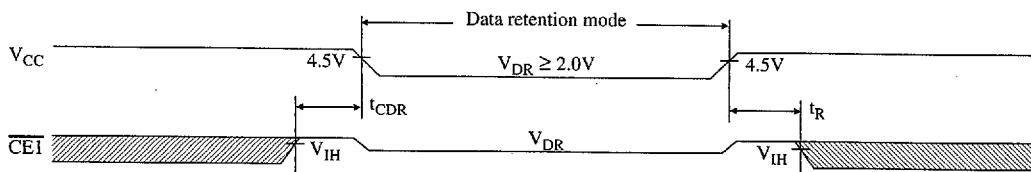
Data retention characteristics

L version only

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	$V_{\text{CC}} = 2.0\text{V}$	2.0	—	V
Data retention current	I_{CCDR}	$\overline{\text{CE1}} \geq V_{\text{CC}} - 0.2\text{V}$ or $\text{CE2} \leq 0.2\text{V}$	—	200	μA
Chip deselect to data retention time	t_{CDR}		0	—	ns
Operation recovery time	t_{R}	$V_{\text{in}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{in}} \leq 0.2\text{V}$	t_{RC}	—	ns
Input leakage current	$ I_{\text{LI}} $		—	1	μA

Data retention waveform

L version only





AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

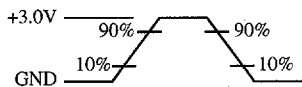


Figure A: Input waveform

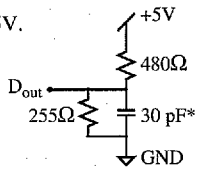


Figure B: Output load

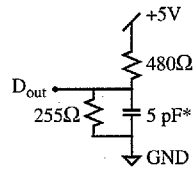
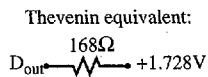


Figure C: Output load for t_{CLZ} , t_{CHZ}

*including scope and jig capacitance

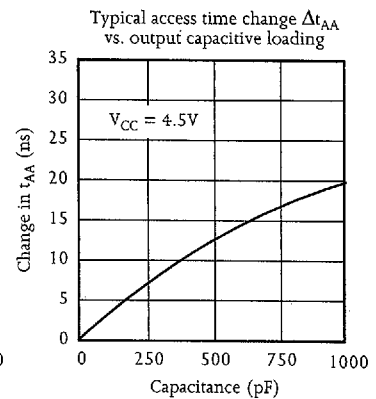
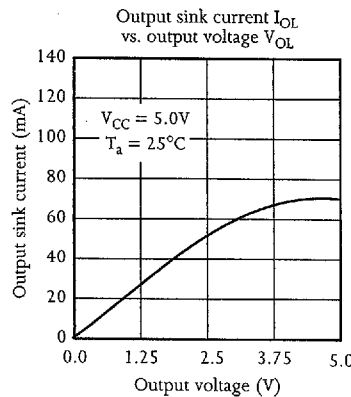
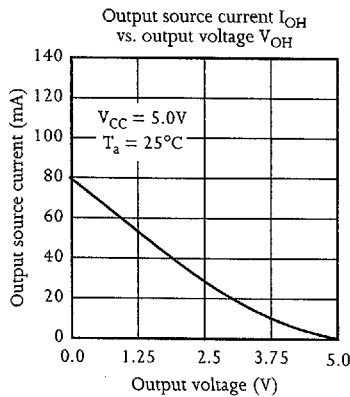
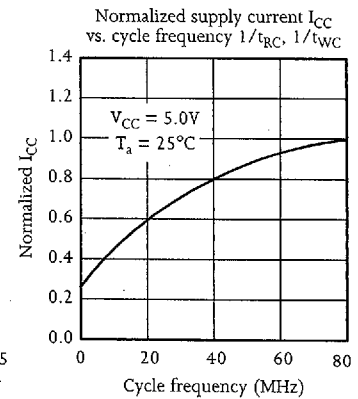
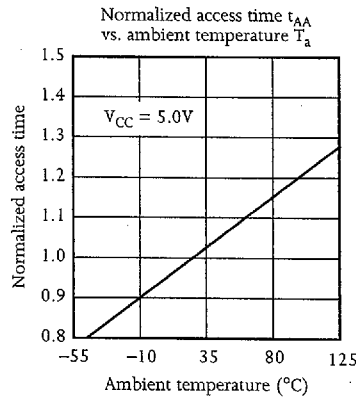
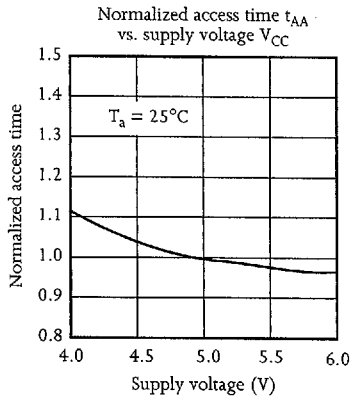
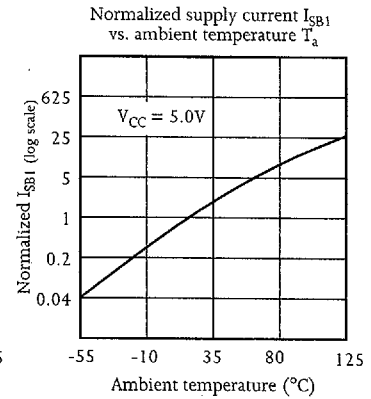
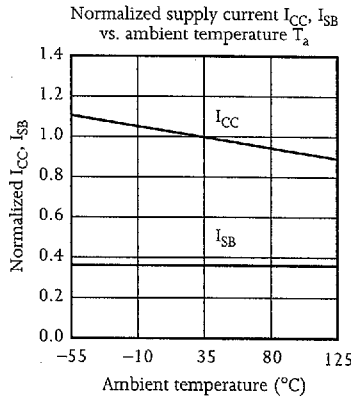
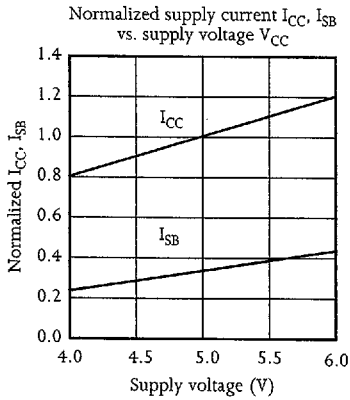
Notes

- During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
- This parameter is sampled and not 100% tested.
- For test conditions, see AC Test Conditions, Figures A, B, C.
- t_{CLZ} and t_{CHZ} are specified with $CL = 5pF$ as in Figure C. Transition is measured $\pm 500mV$ from steady-state voltage.
- This parameter is guaranteed but not tested.
- $\overline{WE}$ is HIGH for read cycle.
- $\overline{CE1}$ and $\overline{OE}$ are LOW and $CE2$ is HIGH for read cycle.
- Address valid prior to or coincident with $\overline{CE1}$ transition LOW and $CE2$ transition HIGH.
- All read cycle timings are referenced from the last valid address to the first transitioning address.
- $\overline{CE1}$ or $\overline{WE}$ must be HIGH or $CE2$ LOW during address transitions.
- All write cycle timings are referenced from the last valid address to the first transitioning address.
- $\overline{CE1}$ and $CE2$ have identical timing.



Typical DC and AC characteristics

SRAM



AS7C512
AS7C512L



AS7C512 ordering codes

Package \ Access Time	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil		AS7C512-15PC AS7C512L-15PC	AS7C512-20PC AS7C512L-20PC	AS7C512-25PC AS7C512L-25PC	AS7C512-35PC AS7C512L-35PC
Plastic SOJ, 300 mil		AS7C512-15JC AS7C512L-15JC	AS7C512-20JC AS7C512L-20JC	AS7C512-25JC AS7C512L-25JC	AS7C512-35JC AS7C512L-35JC
Plastic SOIC, 525 mil		AS7C512-15SC AS7C512L-15SC	AS7C512-20SC AS7C512L-20SC	AS7C512-25SC AS7C512L-25SC	AS7C512-35SC AS7C512L-35SC

Shaded areas contain advance information.

AS7C512 part numbering system

AS7C	512	X	-XX	X	C
SRAM prefix	Device number	Blank = Standard power L = Low power	Access time	Package: P = PDIP 300 mil J = SOJ 300 mil S = SOIC 525 mil	Commercial temperature range, 0°C to 70 °C