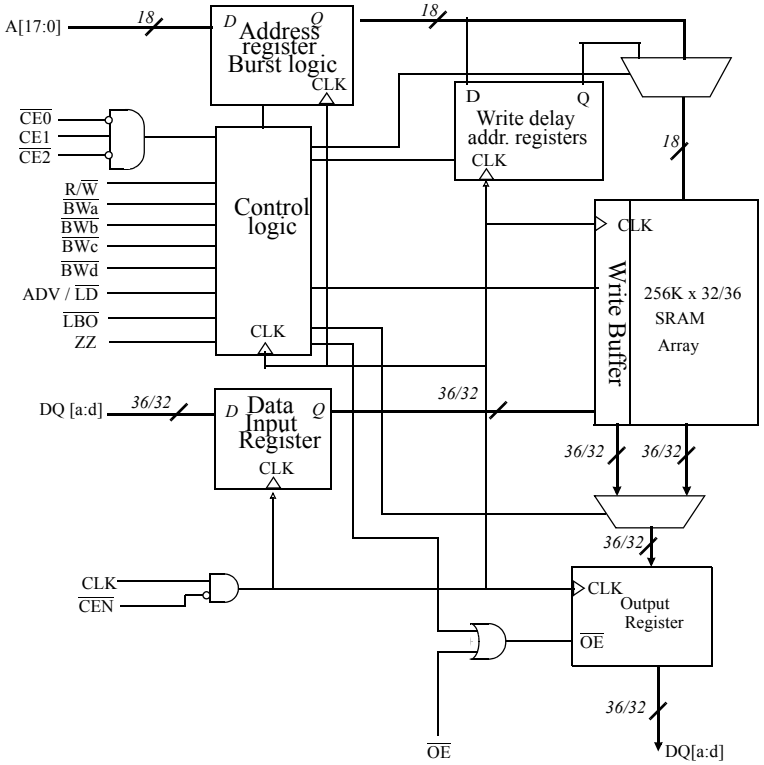
3.3V 256K×32/36 Pipelined burst Synchronous SRAM with NTD™

Features

- Organization: 262,144 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 166 MHz
- Fast clock to data access: 3.5/4.0 ns
- Fast $\overline{OE}$ access time: 3.5/4.0 ns
- Fully synchronous operation
- Common data inputs and data outputs
- Asynchronous output enable control
- Available in 100-pin TQFP
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3 core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- Self-timed write cycles
- Interleaved or linear burst modes
- Snooze mode for standby operation

Logic Block Diagram



Selection Guide

	-166	-133	Units
Minimum cycle time	6	7.5	ns
Maximum clock frequency	166	133	MHz
Maximum clock access time	3.5	4	ns
Maximum operating current	475	400	mA
Maximum standby current	130	100	mA
Maximum CMOS standby current (DC)	30	30	mA

8 Mb Synchronous SRAM products list[1,2]

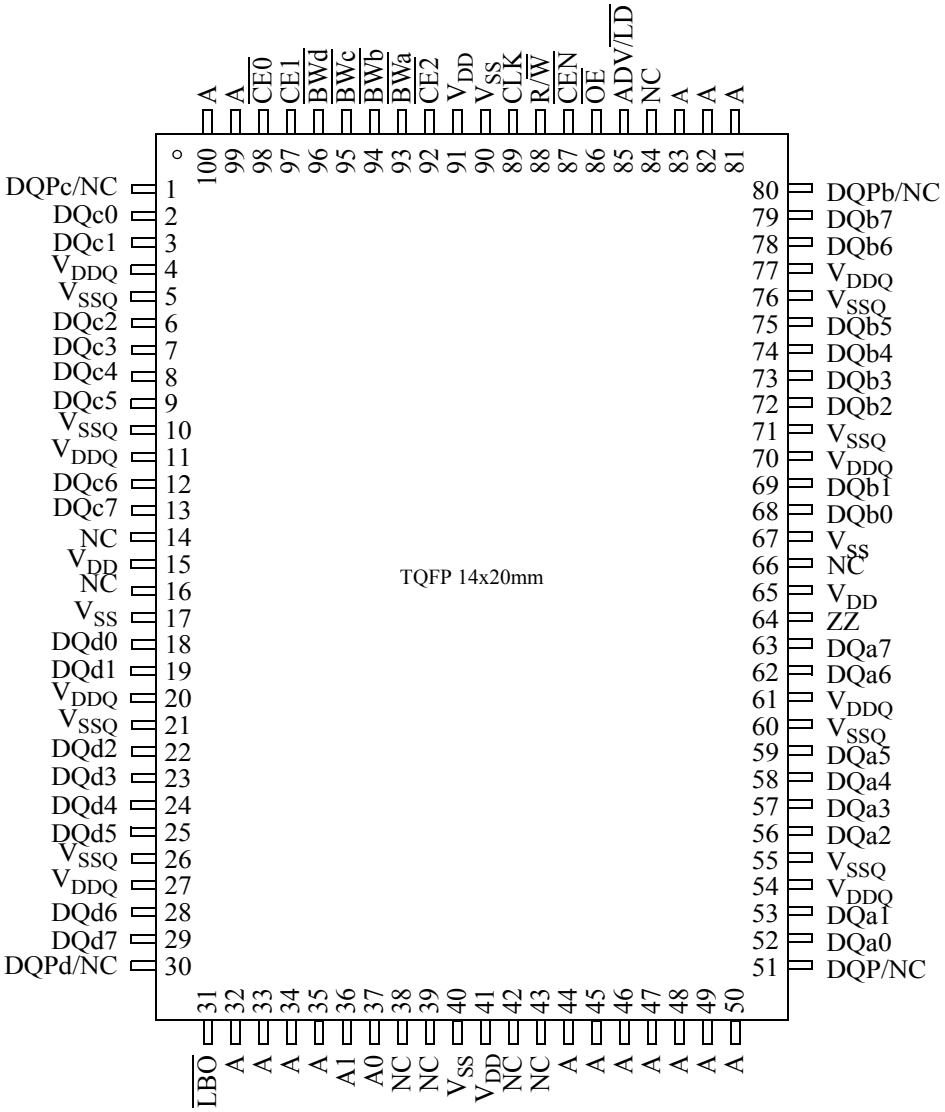
Org	Part Number	Mode	Speed
512KX18	AS7C33512PFS18A	PL-SCD	166/133 MHz
256KX32	AS7C33256PFS32A	PL-SCD	166/133 MHz
256KX36	AS7C33256PFS36A	PL-SCD	166/133 MHz
512KX18	AS7C33512PFD18A	PL-DCD	166/133 MHz
256KX32	AS7C33256PFD32A	PL-DCD	166/133 MHz
256KX36	AS7C33256PFD36A	PL-DCD	166/133 MHz
512KX18	AS7C33512FT18A	FT	7.5/8.5/10 ns
256KX32	AS7C33256FT32A	FT	7.5/8.5/10 ns
256KX36	AS7C33256FT36A	FT	7.5/8.5/10 ns
512KX18	AS7C33512NTD18A	NTD-PL	166/133 MHz
256KX32	AS7C33256NTD32A	NTD-PL	166/133 MHz
256KX36	AS7C33256NTD36A	NTD-PL	166/133 MHz
512KX18	AS7C33512NTF18A	NTD-FT	7.5/8.5/10 ns
256KX32	AS7C33256NTF32A	NTD-FT	7.5/8.5/10 ns
256KX36	AS7C33256NTF36A	NTD-FT	7.5/8.5/10 ns

1 Core Power Supply: VDD = 3.3V ± 0.165V
2 I/O Supply Voltage: VDDQ = 3.3V ± 0.165V for 3.3V I/O
VDDQ = 2.5V ± 0.125V for 2.5V I/O

PL-SCD : Pipelined Burst Synchronous SRAM - Single Cycle Deselect
PL-DCD : Pipelined Burst Synchronous SRAM - Double Cycle Deselect
FT : Flow-through Burst Synchronous SRAM
NTD[1]-PL : Pipelined Burst Synchronous SRAM with NTD™
NTD-FT : Flow-through Burst Synchronous SRAM with NTD™

1. NTD: No Turnaround Delay. NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners.

Pin arrangement for TQFP (top view)



Note: Pins 1, 30, 51 , and 80 are NC for ×32

Functional description

The AS7C33256NTD32/36A family is a high performance CMOS 8 Mbit synchronous Static Random Access Memory (SRAM) organized as 262,144 words × 32 or 36 bits and incorporates a LATE LATE Write.

This variation of the 8Mb sychronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipelined burst devices. In a normal pipelined burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write command, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write latency which matches the two-cycle pipelined or one-cycle flow-through read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

Assert R/$\overline{W}$ low to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied low for full 32/36 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable $\overline{OE}$ does not need to be toggled for write operations; it can be tied low for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs. In pipelined mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read, write and deselect operations. When ADV is high, external addresses, chip select, R/$\overline{W}$ pins are ignored, and internal address counters increment in the count sequence specified by the $\overline{LBO}$ control. Any device operations, including burst, can be stalled using the $\overline{CEN}$=1, the clock enable input.

The AS7C33256NTD36A and AS7C33256NTD32A operate with a 3.3V ± 5% power supply for the device core (V_{DD}). DQ circuits use a separate power supply (V_{DDQ}) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin 14×20 mm TQFP package

Capacitance

Parameter	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C_{IN}*	V_{in} = 0V	-	5	pF
I/O capacitance	$C_{I/O}$*	V_{in} = V_{out} = 0V	-	7	pF

*Guaranteed not tested

TQFP thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient)[1]	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1–layer	θ_{JA}	40	°C/W
		4–layer	θ_{JA}	22	°C/W
Thermal resistance (junction to top of case)[1]			θ_{JC}	8	°C/W

1 This parameter is sampled

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$, $\overline{LBO}$, and ZZ are synchronous to this clock.
$\overline{CEN}$	I	SYNC	Clock enable. When de-asserted high, the clock input signal is masked.
A, A0, A1	I	SYNC	Address. Sampled when all chip enables are active and ADV/$\overline{LD}$ is asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$, CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Sampled at the rising edge of CLK, when ADV/$\overline{LD}$ is asserted. Are ignored when ADV/$\overline{LD}$ is high.
ADV/$\overline{LD}$	I	SYNC	Advance or Load. When sampled high, the internal burst address counter will increment in the order defined by the $\overline{LBO}$ input value. (refer to table on page 2) When low, a new address is loaded.
R/$\overline{W}$	I	SYNC	A high during LOAD initiates a READ operation. A low during LOAD initiates a WRITE operation. Is ignored when ADV/$\overline{LD}$ is high.
$\overline{BW[a,b,c,d]}$	I	SYNC	Byte write enables. Used to control write on individual bytes. Sampled along with WRITE command and BURST WRITE.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are not driven when $\overline{OE}$ is inactive.
$\overline{LBO}$	I	STATIC	Selects Burst mode. When tied to V_{DD} or left floating, device follows Interleaved Burst order. When driven Low, device follows linear Burst order. *This signal is internally pulled High.*
ZZ	I	ASYNC	Snooze. Places device in low power mode; data is retained. Connect to GND if unused.
NC	-	-	No connect. Note that pin 84 will be used for future address expansion to 16Mb density.

Snooze Mode

SNOOZE MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SNOOZE MODE is dictated by the length of time the ZZ is in a High state.

The ZZ pin is an asynchronous, active high input that causes the device to enter SNOOZE MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. After entering SNOOZE MODE, all inputs except ZZ is disabled and all outputs go to High-Z. Any operation pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during t_{PUS}, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SNOOZE MODE.

Burst Order

Interleaved Burst Order ($\overline{LBO}$=1)					Linear Burst Order ($\overline{LBO}$=0)				
	A1 A0	A1 A0	A1 A0	A1 A0		A1 A0	A1 A0	A1 A0	A1 A0
Starting Address	0 0	0 1	1 0	1 1	Starting Address	0 0	0 1	1 0	1 1
First increment	0 1	0 0	1 1	1 0	First increment	0 1	1 0	1 1	0 0
Second increment	1 0	1 1	0 0	0 1	Second increment	1 0	1 1	0 0	0 1
Third increment	1 1	1 0	0 1	0 0	Third increment	1 1	0 0	0 1	1 0

Synchronous truth table[5,6,7,8,9]

$\overline{CE0}$	CE1	$\overline{CE2}$	ADV/$\overline{LD}$	R/$\overline{W}$	$\overline{BWn}$	$\overline{OE}$	$\overline{CEN}$	Address source	CLK	Operation	DQ	Notes
H	X	X	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	X	H	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	L	X	L	X	X	X	L	NA	L to H	DESELECT Cycle	High-Z	
X	X	X	H	X	X	X	L	NA	L to H	CONTINUE DESELECT Cycle	High-Z	1
L	H	L	L	H	X	L	L	External	L to H	READ Cycle (Begin Burst)	Q	
X	X	X	H	X	X	L	L	Next	L to H	READ Cycle (Continue Burst)	Q	1,10
L	H	L	L	H	X	H	L	External	L to H	NOP/DUMMY READ (Begin Burst)	High-Z	2
X	X	X	H	X	X	H	L	Next	L to H	DUMMY READ (Continue Burst)	High-Z	1,2,10
L	H	L	L	L	L	X	L	External	L to H	WRITE CYCLE (Begin Burst)	D	3
X	X	X	H	X	L	X	L	Next	L to H	WRITE CYCLE (Continue Burst)	D	1,3,10
L	H	L	L	L	H	X	L	External	L to H	NOP/WRITE ABORT (Begin Burst)	High-Z	2,3
X	X	X	H	X	H	X	L	Next	L to H	WRITE ABORT (Continue Burst)	High-Z	1,2,3, 10
X	X	X	X	X	X	X	H	Current	L to H	INHIBIT CLOCK	-	4

Key: X = Don't Care, H = HIGH, L = LOW. $\overline{BW}$n = H means all byte write signals ($\overline{BW}$a, $\overline{BW}$b, $\overline{BW}$c, and $\overline{BW}$d) are HIGH. $\overline{BW}$n = L means one or more byte write signals are LOW.

Notes:

1 CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chose in the initial BEGIN BURST cycle. A CONINUE DESELECT cycle can only be entered if a DESELECT CYCLE is executed first.

2 DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.

3 $\overline{OE}$ may be wired LOW to minimize the number of control signal to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. $\overline{OE}$ may be used when the bus turn-on and turn-off times do not meet an application's requirements.

4 If an INHIBIT CLOCK command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the INHIBIT CLOCK cycle.

5 $\overline{BW}$a enables WRITEs to byte "a" (DQa pins/balls); $\overline{BW}$b enables WRITEs to byte "b" (DQb pins/balls); $\overline{BW}$c enables WRITEs to byte "c" (DQc pins/balls); $\overline{BW}$d enables WRITEs to byte "d" (DQd pins/balls).

6 All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

7 Wait states are inserted by setting $\overline{CEN}$ HIGH.

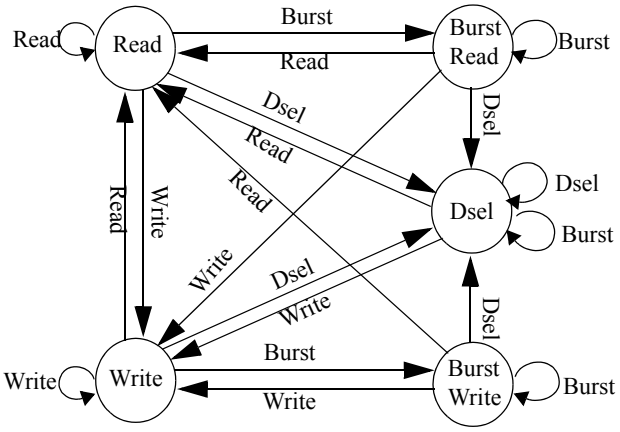
8 This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.

9 The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST CYCLE.

10 The address counter is incremented for all CONTINUE BURST cycles.

11 ZZ pin is always Low in this truth table.

State Diagram for NTD SRAM



Absolute maximum ratings[1]

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	V_{DD} + 0.5	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_D	–	1.8	W
DC output current	I_{OUT}	–	50	mA
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature under bias (Junction)	T_{bias}	–65	+150	°C

1 Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Recommended operating conditions at 3.3V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	3.135	3.3	3.465	V
Ground supply	Vss	0	0	0	V

Recommended operating conditions at 2.5V I/O

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage for inputs	V_{DD}	3.135	3.3	3.465	V
Supply voltage for I/O	V_{DDQ}	2.375	2.5	2.625	V
Ground supply	Vss	0	0	0	V

DC electrical characteristics for 3.3V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current[1]	$\|I_{LI}\|$	V_{DD} = Max, 0V ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, 0V ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	2*	V_{DD}+0.3	V
		I/O pins	2*	V_{DDQ}+0.3	
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3**	0.8	V
		I/O pins	-0.5**	0.8	
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135V	2.4	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.465V	–	0.4	V

1 $\overline{LBO}$, and ZZ pins have an internal pull-up or pull-down, and input leakage = ±10 µA.

DC electrical characteristics for 2.5V I/O operation

Parameter	Sym	Conditions	Min	Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{DD} = Max, 0V ≤ V_{IN} ≤ V_{DD}	-2	2	µA
Output leakage current	$\|I_{LO}\|$	OE ≥ V_{IH}, V_{DD} = Max, 0V ≤ V_{OUT} ≤ V_{DDQ}	-2	2	µA
Input high (logic 1) voltage	V_{IH}	Address and control pins	1.7*	V_{DD}+0.3	V
		I/O pins	1.7*	V_{DDQ}+0.3	V
Input low (logic 0) voltage	V_{IL}	Address and control pins	-0.3**	0.7	V
		I/O pins	-0.3**	0.7	V
Output high voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375V	1.7	–	V
Output low voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 2.625V	–	0.7	V

*V_{IH} max < VDD +1.5V for pulse width less than 0.2 X t_{CYC}

**V_{IL} min = -1.5 for pulse width less than 0.2 X t_{CYC}

I_{DD} operating conditions and maximum limits

Parameter	Sym	Test conditions	-166	-133	Unit
Operating power supply current[1]	I_{CC}	$\overline{CE0}$ ≤ V_{IL}, CE1 ≥ V_{IH}, $\overline{CE2}$ ≤ V_{IL}, f = f_{Max}, I_{OUT} = 0 mA, ZZ ≤ V_{IL}	475	400	mA
Standby power supply current	I_{SB}	All V_{IN} ≤ 0.2V or ≥ V_{DD} – 0.2V, Deselected, f = f_{Max}, ZZ ≤ V_{IL}	130	100	mA
	I_{SB1}	Deselected, f = 0, ZZ ≤ 0.2V, all V_{IN} ≤ 0.2V or ≥ V_{DD} – 0.2V	30	30	
	I_{SB2}	Deselected, f = f_{Max}, ZZ ≥ V_{DD} – 0.2V, all V_{IN} ≤ V_{IL} or ≥ V_{IH}	30	30	

1 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.

Timing characteristics for 3.3 V I/O operation

Parameter	Symbol	–166		–133		Unit	Notes[1]
		Min	Max	Min	Max		
Clock frequency	f_{Max}	–	166	–	133	MHz	
Cycle time	t_{CYC}	6	–	7.5	–	ns	
Clock access time	t_{CD}	–	3.5	–	4.0	ns	
Output enable low to data valid	t_{OE}	–	3.5	–	4.0	ns	
Clock high to output low Z	t_{LZC}	0	–	0	–	ns	2,3,4
Data output invalid from clock high	t_{OH}	1.5	–	1.5	–	ns	2
Output enable low to output low Z	t_{LZOE}	0	–	0	–	ns	2,3,4
Output enable high to output High Z	t_{HZOE}	–	3.5	–	4.0	ns	2,3,4
Clock high to output High Z	t_{HZC}	–	3.5	–	4.0	ns	2,3,4
Output enable high to invalid output	t_{OHOE}	0	–	0	–	ns	
Clock high pulse width	t_{CH}	2.4	–	2.5	–	ns	5
Clock low pulse width	t_{CL}	2.3	–	2.5	–	ns	5
Address and control setup to clock high	t_{AS}	1.5	–	1.5	–	ns	6
Data setup to clock high	t_{DS}	1.5	–	1.5	–	ns	6
Write setup to clock high	t_{WS}	1.5	–	1.5	–	ns	6,7
Chip select setup to clock high	t_{CSS}	1.5	–	1.5	–	ns	6,8
Address hold from clock high	t_{AH}	0.5	–	0.5	–	ns	6
Data hold from clock high	t_{DH}	0.5	–	0.5	–	ns	6
Write hold from clock high	t_{WH}	0.5	–	0.5	–	ns	6,7
Chip select hold from clock high	t_{CSH}	0.5	–	0.5	–	ns	6,8
Clock enable setup to clock high	t_{CENS}	1.5	–	1.5	–	ns	6
Clock enable hold from clock high	t_{CENH}	0.5	–	0.5	–	ns	6
ADV/$\overline{LD}$ setup to clock high	t_{ADVS}	1.5	–	1.5	–	ns	6
ADV/$\overline{LD}$ hold from clock high	t_{ADVH}	0.5	–	0.5	–	ns	6

1 Refer to “notes” on page 16.

Timing characteristics for 2.5 V I/O operation

Parameter	Symbol	–166		–133		Unit	Notes[1]
		Min	Max	Min	Max		
Clock frequency	f_{Max}	–	166	–	133	MHz	
Cycle time	t_{CYC}	6	–	7.5	–	ns	
Clock access time	t_{CD}	–	3.8	–	4.2	ns	
Output enable low to data valid	t_{OE}	–	3.5	–	4.0	ns	
Clock high to output low Z	t_{LZC}	0	–	0	–	ns	2,3,4
Data output invalid from clock high	t_{OH}	1.5	–	1.5	–	ns	2
Output enable low to output low Z	t_{LZOE}	0	–	0	–	ns	2,3,4
Output enable high to output High Z	t_{HZOE}	–	3.5	–	4.0	ns	2,3,4
Clock high to output High Z	t_{HZC}	–	3.5	–	4.0	ns	2,3,4
Output enable high to invalid output	t_{OHOE}	0	–	0	–	ns	
Clock high pulse width	t_{CH}	2.4	–	2.5	–	ns	5
Clock low pulse width	t_{CL}	2.3	–	2.5	–	ns	5
Address setup to clock high	t_{AS}	1.7	–	1.7	–	ns	6
Data setup to clock high	t_{DS}	1.7	–	1.7	–	ns	6
Write setup to clock high	t_{WS}	1.7	–	1.7	–	ns	6,7
Chip select setup to clock high	t_{CSS}	1.7	–	1.7	–	ns	6,8
Address hold from clock high	t_{AH}	0.7	–	0.7	–	ns	6
Data hold from clock high	t_{DH}	0.7	–	0.7	–	ns	6
Write hold from clock high	t_{WH}	0.7	–	0.7	–	ns	6,7
Chip select hold from clock high	t_{CSH}	0.7	–	0.7	–	ns	6,8
Clock enable setup to clock high	t_{CENS}	1.7	–	1.7	–	ns	6
Clock enable hold from clock high	t_{CENH}	0.7	–	0.7	–	ns	6
ADV/$\overline{LD}$ setup to clock high	t_{ADVS}	1.7	–	1.7	–	ns	6
ADV/$\overline{LD}$ hold from clock high	t_{ADVH}	0.7	–	0.7	–	ns	6

1 Refer to “notes” on page 16.

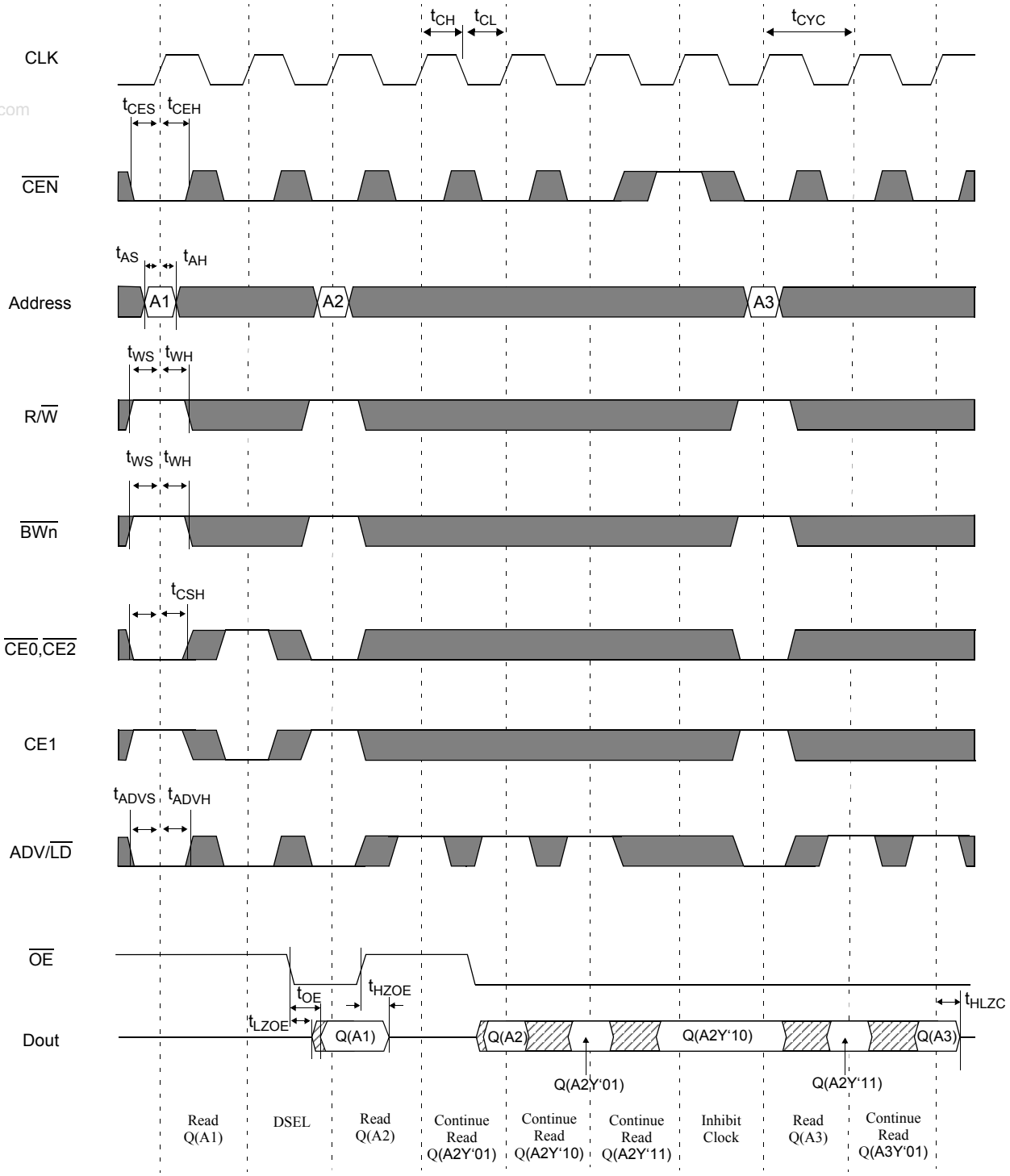
Snooze Mode Electrical Characteristics

Description	Conditions	Symbol	Min	Max	Units
Current during Snooze Mode	ZZ ≥ V_{IH}	I_{SB2}		30	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SNOOZE current		t_{ZZI}		2	cycle
ZZ inactive to exit SNOOZE current		t_{RZZI}	0		

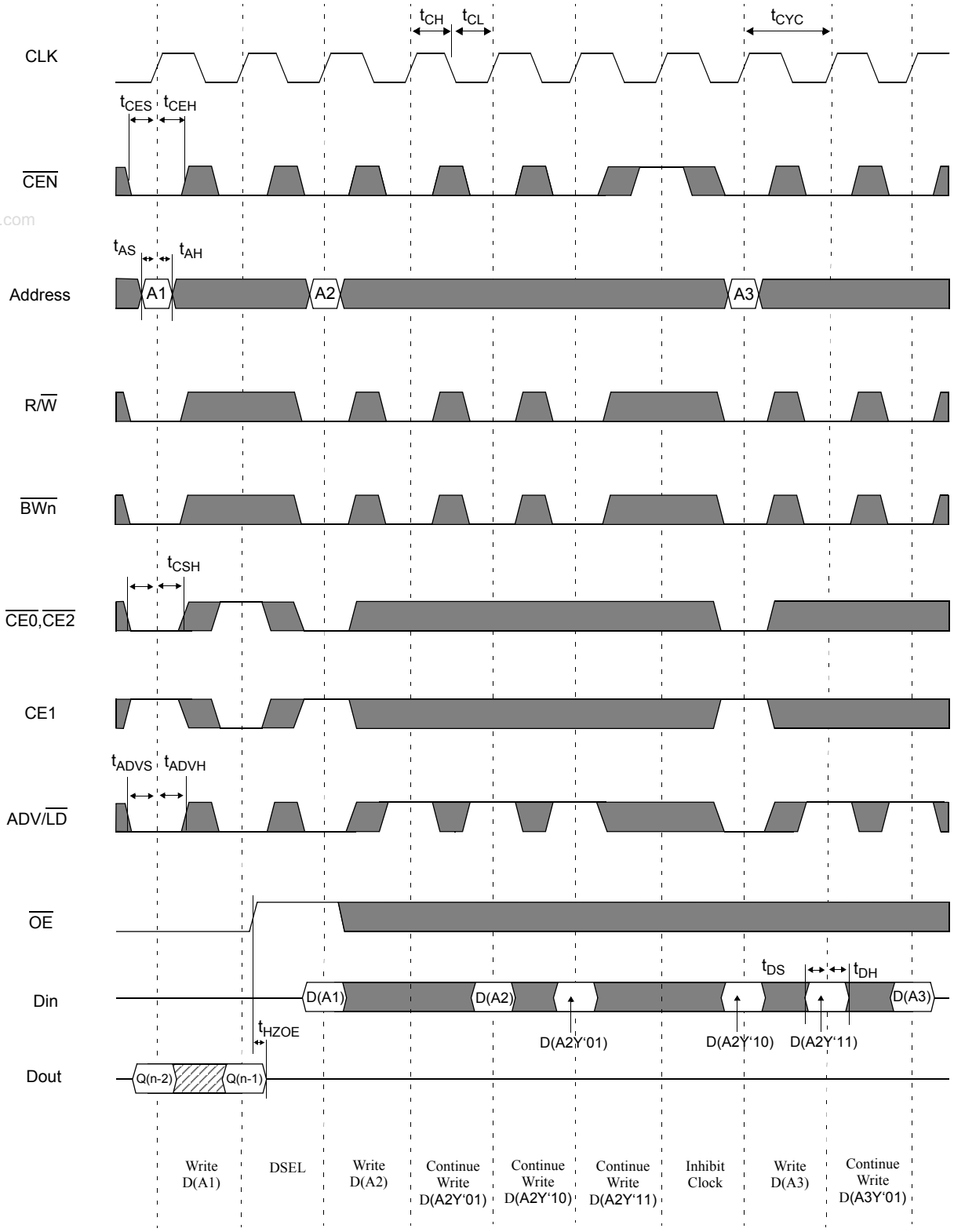
Key to switching waveforms

Rising input Falling input don't care Undefined

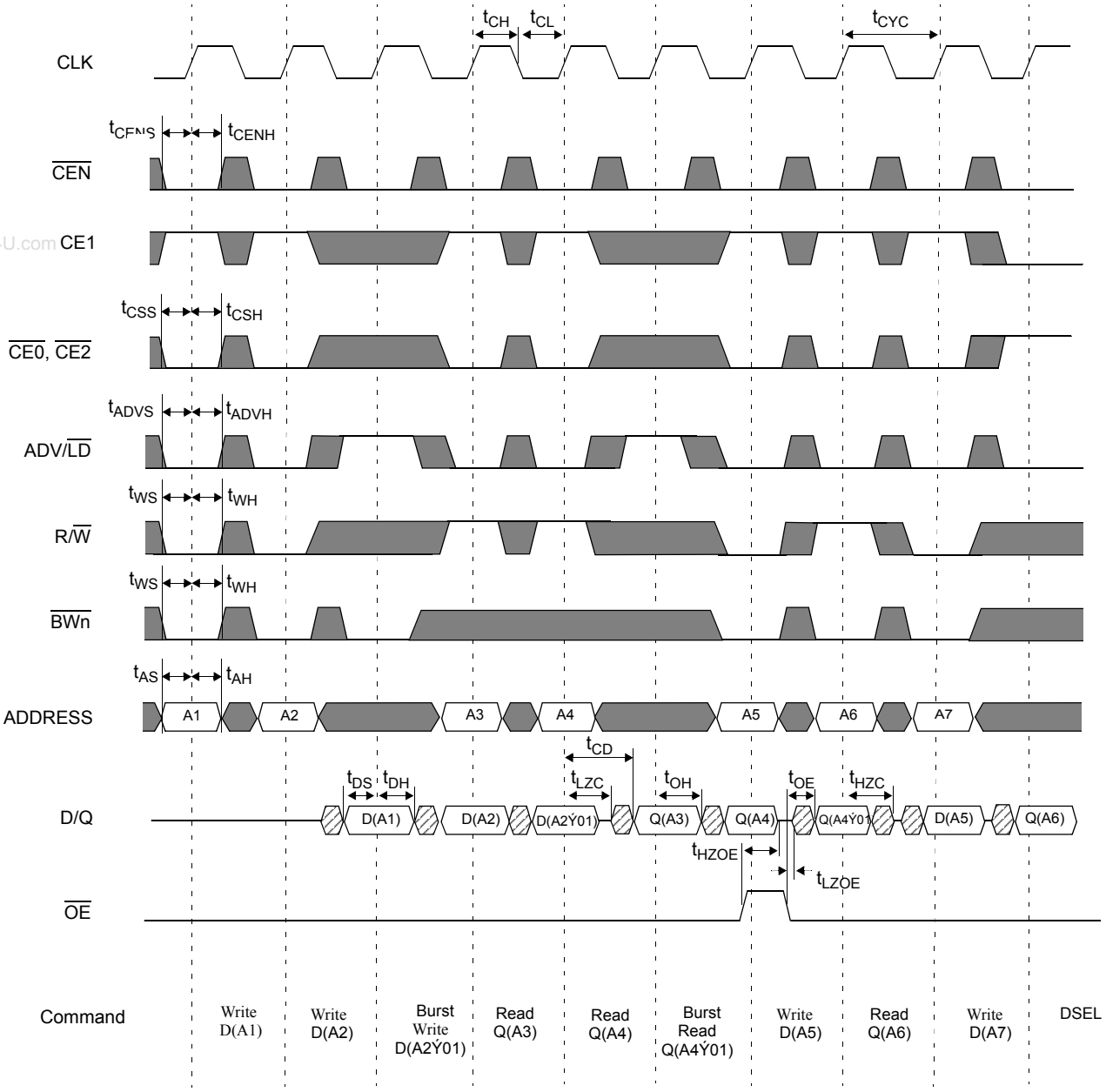
Timing waveform of read cycle



Timing waveform of write cycle

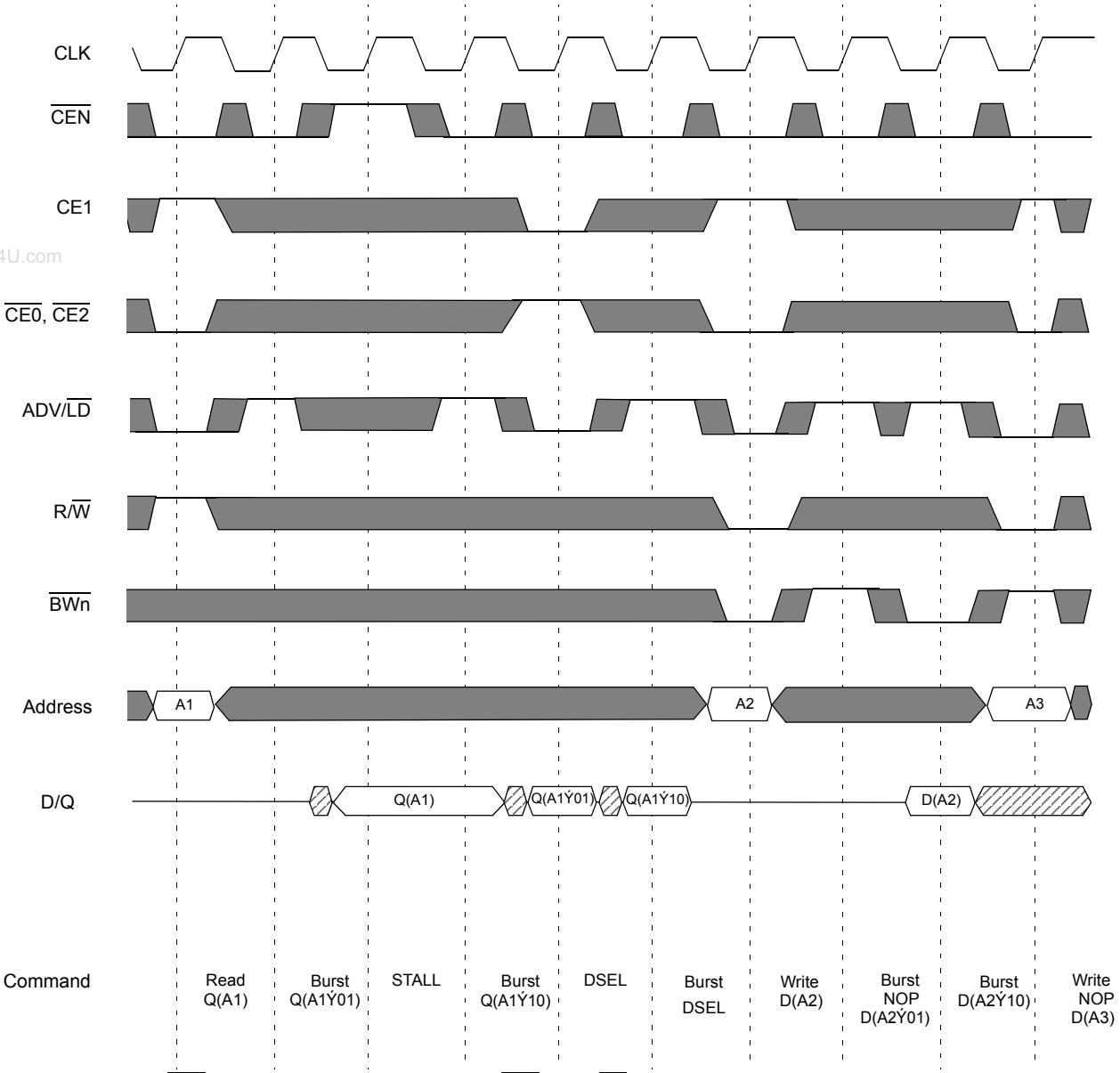


Timing waveform of read/write cycle



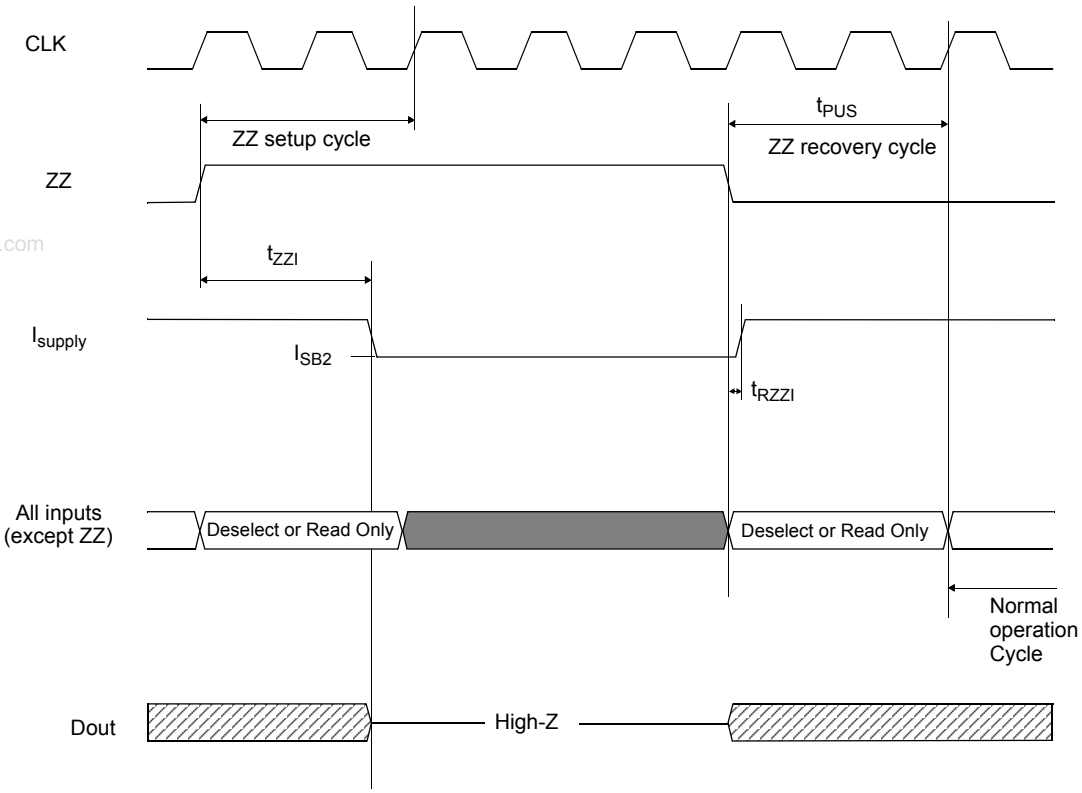
Note: Ý = XOR when $\overline{LBO}$ = high/no connect. Ý = ADD when $\overline{LBO}$ = low. $\overline{BW[a:d]}$ is don't care.

NOP, stall and deselect cycles



Note: Ý = XOR when $\overline{LBO}$ = high/no connect; Ý = ADD when $\overline{LBO}$ = low. $\overline{OE}$ is low.

Timing waveform of snooze mode



AC test conditions

- Output Load: see Figure B,
  except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC} see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (Measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

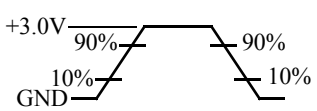


Figure A: Input waveform

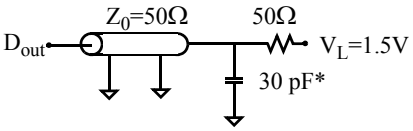


Figure B: Output load (A)

Thevenin equivalent:

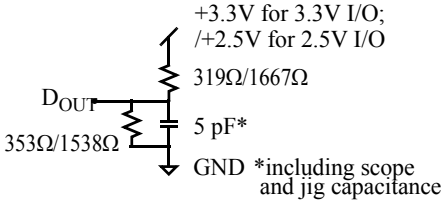


Figure C: Output load(B)

Notes

1 For test conditions, see *AC Test Conditions*, Figures A, B, C.

2 This parameter measured with output load condition in Figure C

3 This parameter is sampled and not 100% tested.

4 t_{HZOE} is less than t_{LZOE}; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.

5 t_{HZCN} is a'no load' parameter to indicate exactly when SRAM outputs have stopped driving.

6 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.

7 Transitions are measured ±500 mV from steady state voltage. Output loading specified with C_L = 5 pF as in Figure C.

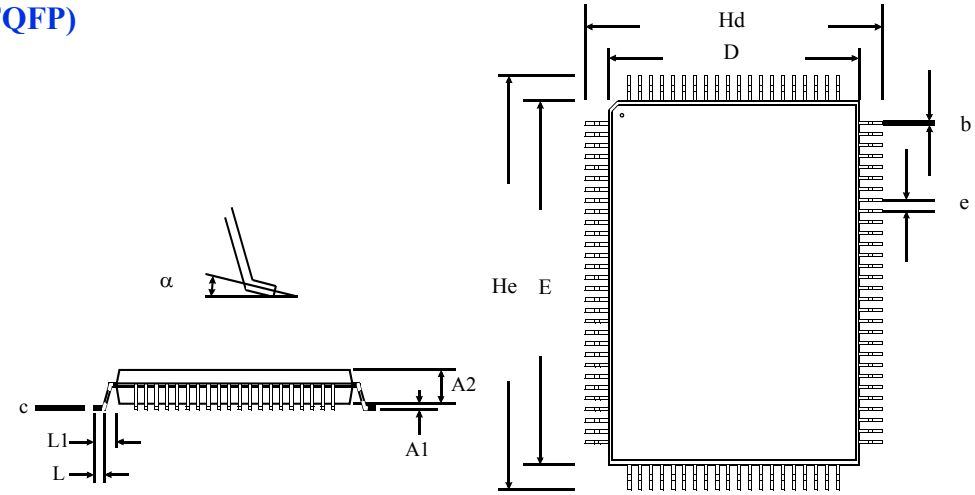
8 t_{CH} measured as high above VIH, and t_{CL} measured as low below VIL

9 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.

Package Dimensions

100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.80	14.20
E	19.80	20.20
e	0.65 nominal	
Hd	15.80	16.20
He	21.80	22.20
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°
Dimensions in millimeters		



Ordering information

Package	Width	166 MHz	133 MHz
TQFP	×32	AS7C33256NTD32A-166TQC	AS7C33256NTD32A-133TQC
TQFP	×32	AS7C33256NTD32A-166TQI	AS7C33256NTD32A-133TQI
TQFP	×36	AS7C33256NTD36A-166TQC	AS7C33256NTD36A-133TQC
TQFP	×36	AS7C33256NTD36A-166TQI	AS7C33256NTD36A-133TQI

Note: Add suffix 'N' to he above part numbers for Lead Free Parts (Ex. AS7C33256NTD32A-166TQCN)

Part numbering guide

AS7C	33	256	NTD	32/36	A	–XXX	TQ	C/I	X
1	2	3	4	5	6	7	8	9	10

1.Alliance Semiconductor SRAM prefix

2.Operating voltage: 33 = 3.3V

3.Organization: 256 = 256K

4.NTD^{TM} = No Turn-around Delay. Pipelined mode.

5.Organization: 32 = x32; 36 = x36

6.Production version: A = first production version

7.Clock speed (MHz)

8.Package type: TQ = TQFP.

9.Operating temperature: C = commercial (0° C to 70° C); I = industrial (-40° C to 85° C)

10. N = Lead free part

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Part Number:AS7C33256NTD36A
AS7C33256NTD32A

Document Version: v. 2.1