

AS3603**Data Sheet****Multi-Standard Power Management Unit****1 General Description**

The AS3603 is a highly-integrated CMOS power management device designed specifically for portable devices such as any mobile phone standard, PDAs, CD players, digital cameras and other devices powered by 1-cell lithium-based or 3- to 4-cell nickel-based batteries.

The device incorporates low dropout regulators (LDOs), DC/DC converters, a complete battery charger, and an audio power amplifier onto one die.

The linear analog LDOs feature extremely high performance regarding:

- Noise – typ $30\mu\text{V}_{\text{RMS}}$ from 100Hz to 100kHz
- Line/Load Regulation – $< 1\text{mV}$ static and $< 10\text{mV}$ transient
- Power Supply Rejection – $> 70\text{dB}$ @ 1kHz

The integrated Step Down DC/DC Converter does not require an external Schottky diode yet provides very high efficiency (up to 95%) throughout the whole operating range. It can be either used as a stand-alone device or as a pre-regulator for LDOs to increase overall device efficiency.

A Step Up DC/DC Converter is included to supply power for white LEDs together with programmable current sources to control LED brightness.

A low-distortion audio power amplifier (1 Watt @ 8Ω) supports handsfree mobile phone operation and HiFi ringtones.

The device also features a chemistry-independent battery charger including fuel gauge circuitry, automatic trickle charging, programmable constant current, constant voltage and pulse charging.

The AS3603 is controlled via a serial interface and integrates all necessary system specific functions such as Reset, Watchdog, and Power-On Detection.

Regulator output voltages are programmable by software. Eight preset startup timings can be selected by an external resistor.

This data sheet is applicable for device versions:

- AS3603-Jxx-x
- AS3603-Hxx-x

2 Key Features

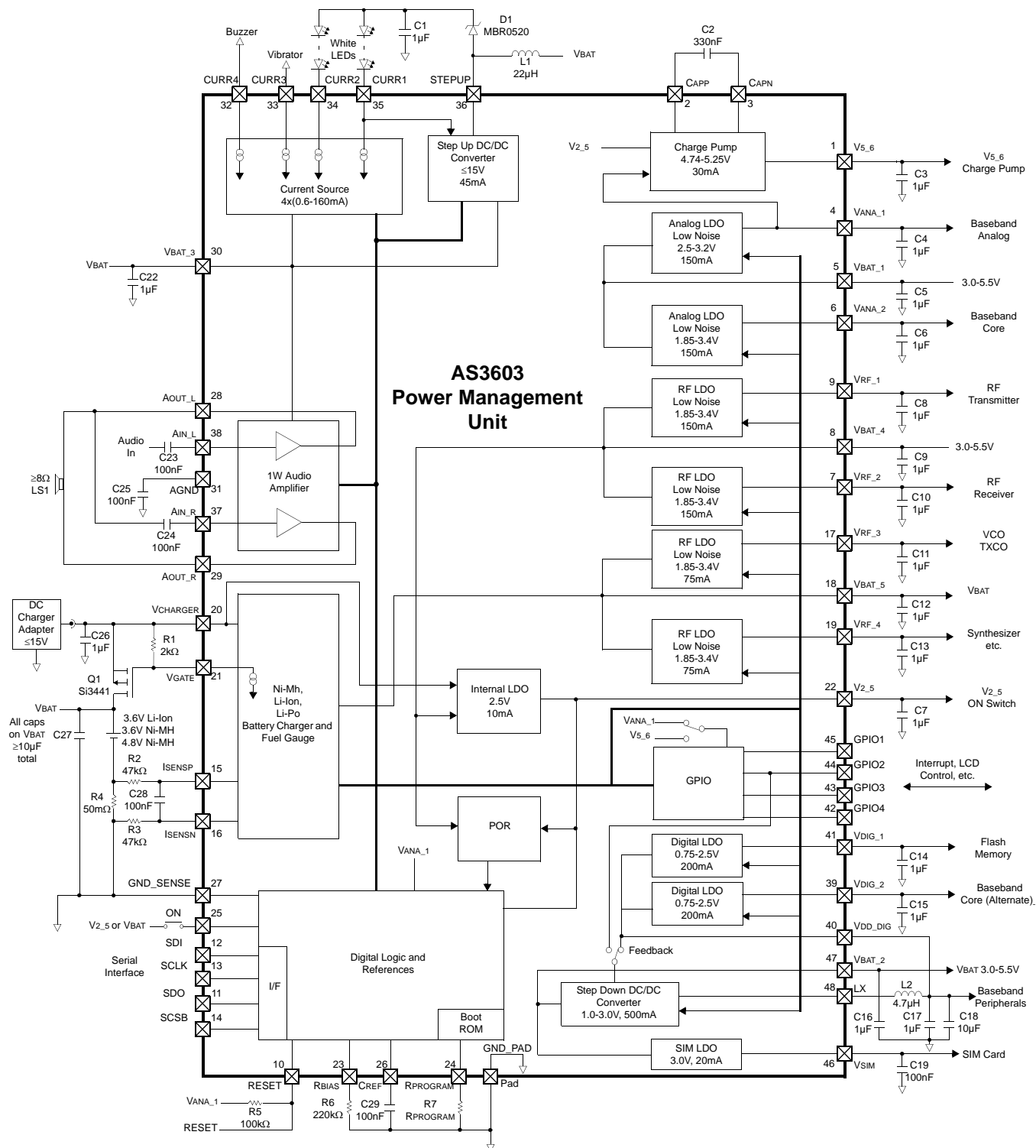
- Ten Programmable High Performance LDOs
 - Two Digital Low-Power LDOs (0.75 to 2.5V, 200mA)
 - Three RF Low-Noise LDOs (1.85 to 3.4V, 150mA)
 - Two RF Low-Noise LDOs (1.85 to 3.4V, 75mA)
 - One SIM Low-Power LDO (3.0V, 20mA)
 - One Periphery Low-Noise LDO (2.5 to 3.2V, 150mA)
 - One Low-Power LDO (2.5V, 10mA)
- Programmable High Efficiency DC/DC Converters
 - Step Down: 1.0 to 3.0V, up to 500mA
 - Step Up: 15V, 45mA, (for White LEDs)
- Stereo Audio Power Amplifier
 - 0.5W @ 4Ω – Stereo
 - 1W @ 8Ω – Bridged
 - Digital Volume Control, 3dB Steps
 - Click- and Pop-Less Start-Up and Power-Down
- Complete Chemistry-Independent Battery Charger
 - Integrated Fuel Gauge
 - Automatic Trickle Charging
 - Programmable Constant Current Charging
 - Programmable Constant Voltage Charging
 - Programmable Pulse Charging
 - Safety Functions (Low Battery Shutdown)
 - Operation without Battery
 - No-Battery detection
- Four 8-Bit Programmable Current Sources (0.625mA to 160mA) support:
 - Buzzer
 - Vibrator
 - LEDs
- Wide Battery Supply Range 3.0 to 5.5V
- Four General Purpose Switches (1Ω and 2Ω)
- Four Programmable General Purpose I/O Pins
- On-Chip Bandgap Tuning for High Accuracy ($\pm 1\%$)
- Integrated Programmable Watchdog (7.5 to 1900ms)
- Programmable Reset (10 to 110ms)
- Shutdown Current typ $7\mu\text{A}$ (2.5V Always On)
- Overcurrent and Thermal Protection
- 0.35 μm CMOS Solution
- 48-pin, 6x6mm QFN Package (0.4mm pitch)
- 48-pin, 7x7mm QFN Package (0.5mm pitch)
- 2.1 Watt Power Dissipation @ $T_{\text{AMBIENT}} = 70^\circ\text{C}$

3 Application

Multi-standard power management for mobile phones, PDAs, and 1-cell Li+ or 3 to 4-cell Ni-MH powered devices.

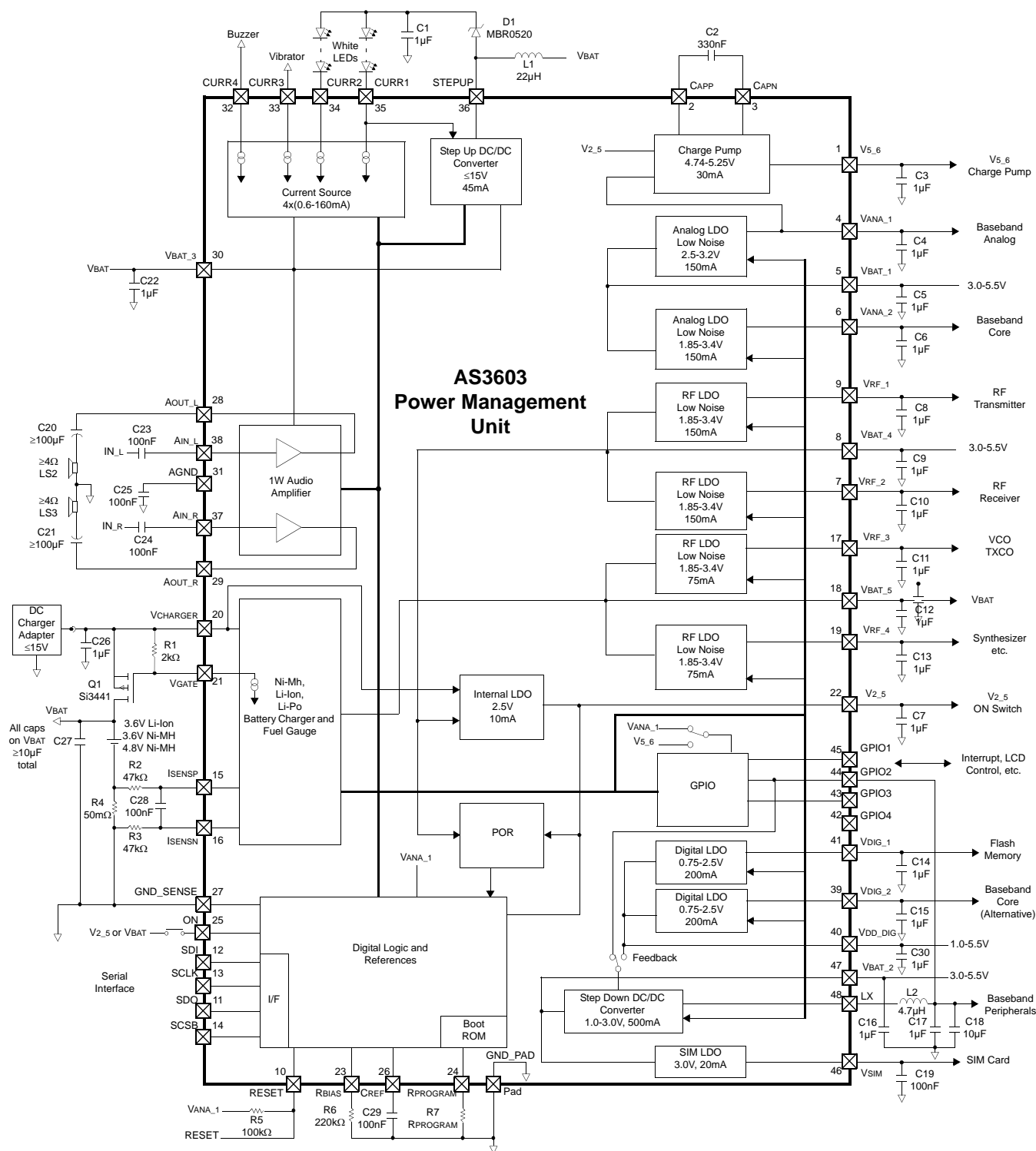
4 Block Diagrams

Figure 1. AS3603 Block Diagram. Option: Audio Amplifier In Differential Mode, Step Down DC/DC Converter as Pre-regulator for Digital LDOs



Note: Refer to Table 38 on page 74 for specifications of external components.

Figure 2. AS3603 Block Diagram. Option: Audio Amplifier in Stereo Single-ended Mode, Digital LDOs separated from Step Down DC/DC Converter



Note: Refer to Table 38 on page 74 for specifications of external components.

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Revision History

Revision	Date	Owner	Description
3.0	4 February 2005	ptr	<ul style="list-style-type: none"> - Various minor updates implemented. - Extended operating temperature range.
3.1	24 February 2005	ptr	<ul style="list-style-type: none"> - Updated Audio Amplifier Block Diagram – Stereo Mode on page 51. - Updated Audio Amplifier Block Diagram – Differential Mode on page 52. - Updated GPIO pullup currents. - Added new feature for Audio Amplifier on page 51 (high impedance in power-down). - Updated Startup on page 56; added new feature (configurable shutdown after battery insertion). - Increased minimum value of VSTARTCHARGER on page 56. - Added Errata on page 76.
3.2	7 April 2005	ptr	<ul style="list-style-type: none"> - Increased V_{chmin} Min parameter. - Added charger resume operation. - Updated res_timer bit description on page 55.
3.3	22 August 2005	ptr	<ul style="list-style-type: none"> - Updated soldering conditions to <i>IPC/JEDEC JSTD 020C</i>.
3.31	3 July 2006	ptr	<ul style="list-style-type: none"> - Updated data sheet status to public viewable.
3.32	2 August 2006	ptr	<ul style="list-style-type: none"> - Updated Audio Amplifier Characteristics on page 52.
3.33	22 November 2006	ptr	<ul style="list-style-type: none"> - Updated ambient temperature range.

5 Absolute Maximum Ratings (Non-Operating)

Stresses beyond the absolute maximum ratings may cause permanent damage to the AS3603. These are stress ratings only. Functional operation of the device at these or beyond those in Section 5.1 Operating Conditions is not implied.

Caution: Exposure to absolute maximum rating conditions may affect device reliability.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V _{IN_HV}	High Voltage Pins	-0.3	17.0	V	Applicable for high voltage pins: VCHARGER, VGATE, and STEPUP
V _{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for pins 5V pins: VBAT_1 - VBAT_5, V5_6, VBUCK, GPIO1 - GPIO4, CURR1 - CURR4, AIN_L, AIN_R, AOUT_L, AOUT_R, VRF_1 - VRF_4 (when not in LDO-mode), ON, and Lx
V _{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins: RESET, SCSB, SCLK, SDI, SDO, VANA_1, VANA_2, VSIM, VDIG_1, VDIG_2, CAPN, AGND, ISENSP, ISENSN, V2_5, CREF, RBIAS, and RPROGRAM
I _{IN}	Input Pin Current	-25	+25	mA	At 25°C Norm: Jedec 17
T _{strg}	Storage Temperature Range	-55	125	°C	
	Humidity	5	85	%	Non-condensing
V _{ESD}	Electrostatic Discharge	-1000	1000	V	Norm: MIL 883 E Method 3015; ±1000V.
P _t	Total Power Dissipation		2.1	W	T _{AMB} = 70°C
T _{max}	Peak Reflow Soldering Temperature		260	°C	T = 20 to 40s, according to the IPC/JEDEC J-STD 020C.

5.1 Operating Conditions

Table 2. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V _{HV}	High Voltage	0.0		15.0	V	Pins VCHARGER, VGATE and STEPUP
V _{BAT}	Battery Voltage	3.0	3.6	5.5	V	For pins VBAT_1 - VBAT_5. During startup from the external battery charger adapter, the battery voltage can be below 3.0V.
V _{DD}	Periphery Supply Voltage (for RESET and SPI pins)	2.5	Boot ROM	3.2	V	Internally generated from VANA_1.
V _{ON}	Activation voltage for ON pin	1.75	V2_5	V _{BAT}	V	
V2_5	Voltage on Pin V2_5	2.4	2.5	2.6	V	Internally generated.
V5_6	Output Voltage of Charge Pump	5.0	5.2	5.6	V	2 x VANA_1
T _{AMB}	Ambient Temperature	-40	25	85	°C	
I _{BAT}	Operating Current		155		μA	Normal operating current. With bit low_power_on (page 60) = 0; only VANA_1 active, no additional external loads.
I _{LOWPOWER}	Low-Power Mode Current Consumption		110		μA	With bit low_power_on (page 60) = 1; only VANA_1 active, no additional external loads.
I _{PowerOff}	Power-Off Mode Current Consumption		7		μA	With bit power_off (page 55) = 1; only V2_5 is active in power off mode.

6 Detailed Functional Descriptions

6.1 Battery Charger Controller

The AS3603 can serve as a standalone Battery Charger Controller supporting rechargeable lithium-ion (Li+), lithium-polymer (LiPo) and 3- or 4-cell nickel metal-hydride (Ni-MH) batteries.

The main features of the Battery Charger Controller are:

- Constant Voltage Charge Mode – Described on page 10
- Pulse Charge Mode – Described on page 12
- Battery Presence Detection – Described on page 14
- Operation Without Battery – Described on page 14
- Charge Controller Bypass – Described on page 14
- Overvoltage and Undervoltage Supervision – Described on page 15

Figure 3. Battery Charger Controller Block Diagram

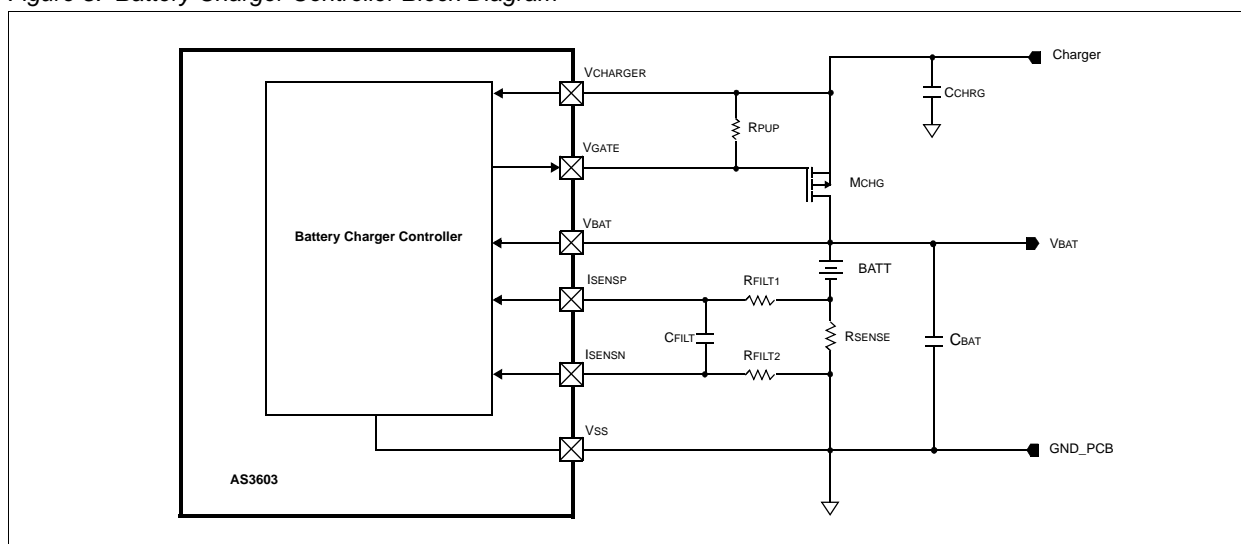


Table 3. Battery Charger Controller Components

Symbol	Parameter	Value	Notes
MCHG	P-channel MOSFET	Si3441BDV, Si8401DB or similar	The maximum power dissipation of this transistor is not limited by the AS3603.
RPUP	Pull-up Resistor	2K Ω \pm 5%	
RSense	Current Sense Resistor	50m Ω \pm 1%, 125mW for $I_{VBAT,DC} < 1.5A$	e.g. Vishay Dale WSL0805
Rfilt1,2	Filter Resistor	47K Ω \pm 1%	Can be omitted if Fuel Gauge functionality is not used ($R_{filt1,2} = 0\Omega$)
Cfilt	Filter Capacitor	100nF \pm 20%, X5R or X7R Dielectric	
CCHRG	Bypass Capacitor on pin VCHARGER	1 μ F \pm 20%, X5R or X7R Dielectric	
CBAT	Minimum Total Capacitance Parallel to Battery	10 μ F	

Table 4. Battery Charger Controller Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V _{chdet}	Charger Detection Threshold. V _{Charger} - V _{BAT_5} : Charger On	50	75	105	mV	Hysteresis is (V _{chdet} - V _{chmin}) < 40mV
V _{chmin}	Charger Detection Threshold. V _{Charger} - V _{BAT_5} : Charger Off	5	20	35	mV	
V _{chreg}	Bootstrap Regulator Voltage	2.4	2.5	2.6	V	V _{CHARGER} > 5V
V _{UVLO}	Undervoltage Lockout Threshold		3.1		V	V _{BAT} rising
			2.8			V _{BAT} falling
V _{OVLO}	Overvoltage Lockout Threshold		5.5		V	V _{BAT} rising
			5.4			V _{BAT} falling
V _{CHOFF}	Charge Termination Threshold	4.14	4.20	4.26	V	Li+ Battery: BatType (page 19) = 0, Li4v2 (page 19) = 1
		4.05	4.1	4.15		Li+ Battery: BatType = 0, Li4v2 = 0. From -5 to +50°
		5.44	5.5	5.6		Ni-MH Battery: BatType = 1
V _{NOBATDET}	"No Battery" Detection Threshold and Charger Resume Detection Threshold		3.644		V	DisOWB (page 20) = 0

6.1.1 Low-Current Trickle Charge Mode

Low-current Trickle Charge mode is initiated when an external battery charger has been detected, bit **chDet** (page 19) = 1, and the battery voltage is below the V_{UVLO} threshold; bits **ChAct** (page 19) and **Trickle** (page 19) will be set. In Trickle Charge mode the charge current will be limited to the value specified by **TrickleCurrent** (page 20) to prevent undue stress on either the battery or the Battery Charger in case of deeply discharged batteries.

Once V_{UVLO} has been exceeded, the Battery Charger will terminate Trickle Charge mode, reset bits **ChAct** and **Trickle**, and switch on the device.

The trickle charge is terminated in any case after approximately 60 minutes (as it is assumed that the battery is damaged in this case)

6.1.2 Constant Current Charge Mode

Constant Current mode is initiated by setting bit **ChEn** (page 19) and resetting bit **Fast** (page 19). Bit **ChAct** (page 19) is set automatically when the Battery Charger starts. Charge current will be limited to the value specified by bit **ConstantCurrent** (page 20) by the Battery Charger Controller.

6.1.3 Charging Nickel-based Batteries

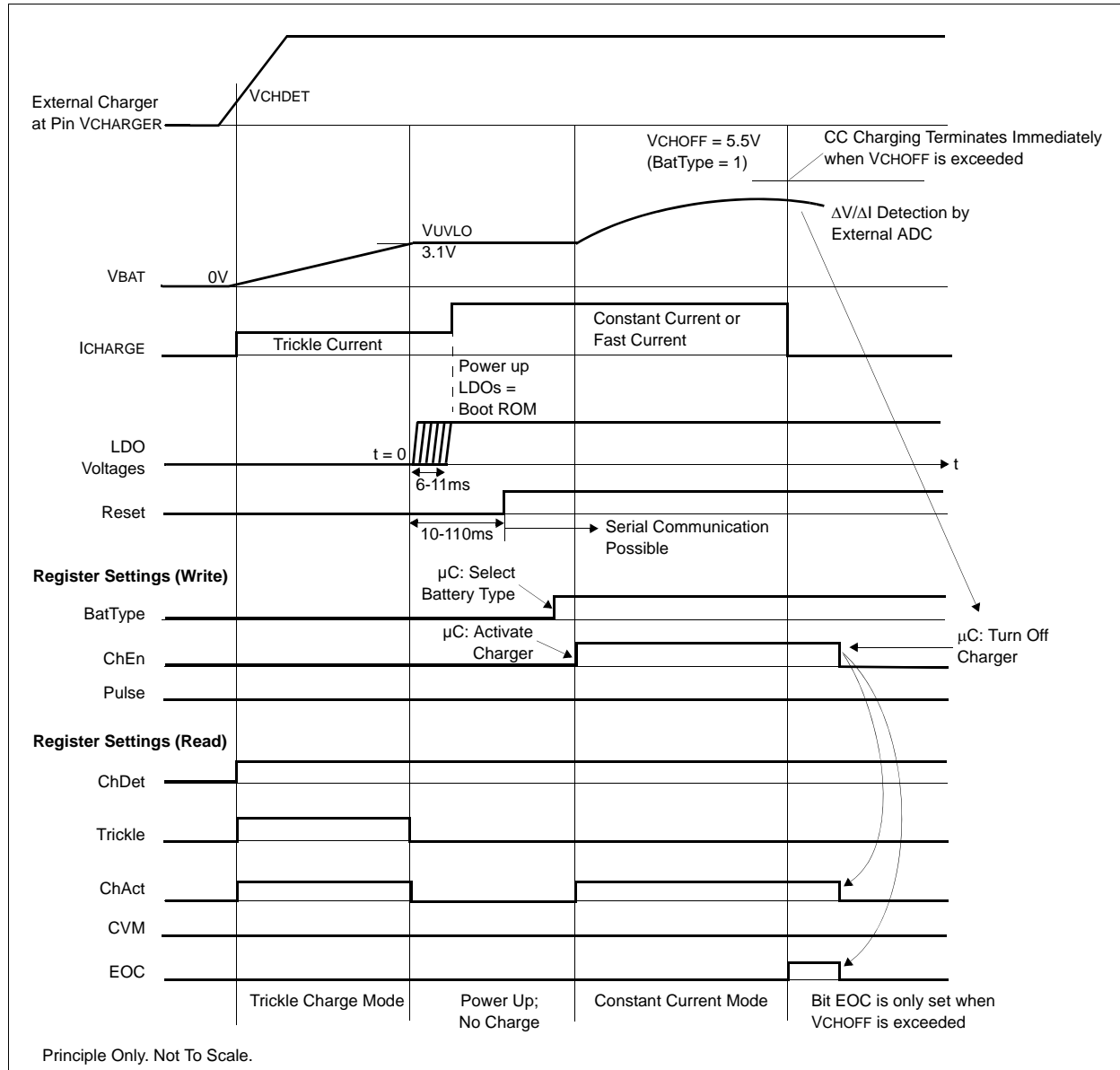
For nickel-based batteries (Ni-MH, NiCd), **BatType** (page 19) must be 1 (see Figure 4 on page 10). The endpoint detection ($\Delta V/\Delta t$) must be performed by the host controller. It must turn off the charger duly to avoid overcharging. In any case, when the battery voltage exceeds the charge termination threshold (typ. 5.5V), the charger will be turned off and bit **EOC** (page 19) will be set.

6.1.4 Charging Lithium-based Batteries

For lithium-based batteries (lithium-ion, lithium-polymer), **BatType** (page 19) must be 0. Additionally, bit **Li4v2** (page 19) can select between coke- and graphite-anode, setting different charge termination thresholds (typ. 4.1V or 4.2V). The charger is designed to charge 1-cell lithium-based batteries independently, using Trickle Charge, Constant Current, Constant Voltage, or Pulse Charge modes.

When the battery voltage exceeds the charge termination threshold during Constant Current mode, it automatically continues charging with either Constant Voltage mode, bit **Pulse** (page 19), or Pulse Charge mode, **Pulse**, and terminates when the end-of-charge conditions are met (see Figure 5 on page 11 and Figure 6 on page 13).

Figure 4. Startup and Constant Current Charging of Nickel-based Batteries



6.1.5 Fast Charge Mode

As an alternative to Constant Current mode, Fast Charge mode may be selected. The charge current will not be controlled in this mode and is only limited by the external battery charger adapter.

Fast Charge mode is initiated by setting bits **ChEn** (page 19) and **Fast** (page 19). Bit **ChAct** (page 19) is set when the Battery Charger has started.

End of Charge

In Fast Charge mode, the same charge termination thresholds apply as for Constant Current mode. Additionally, depending on bit **Fast** (page 19), the current during pulse charging is either the selected constant current or maximum. Charging will resume if the battery voltage drops below $VNOBATDET$.

6.1.6 Constant Voltage Charge Mode

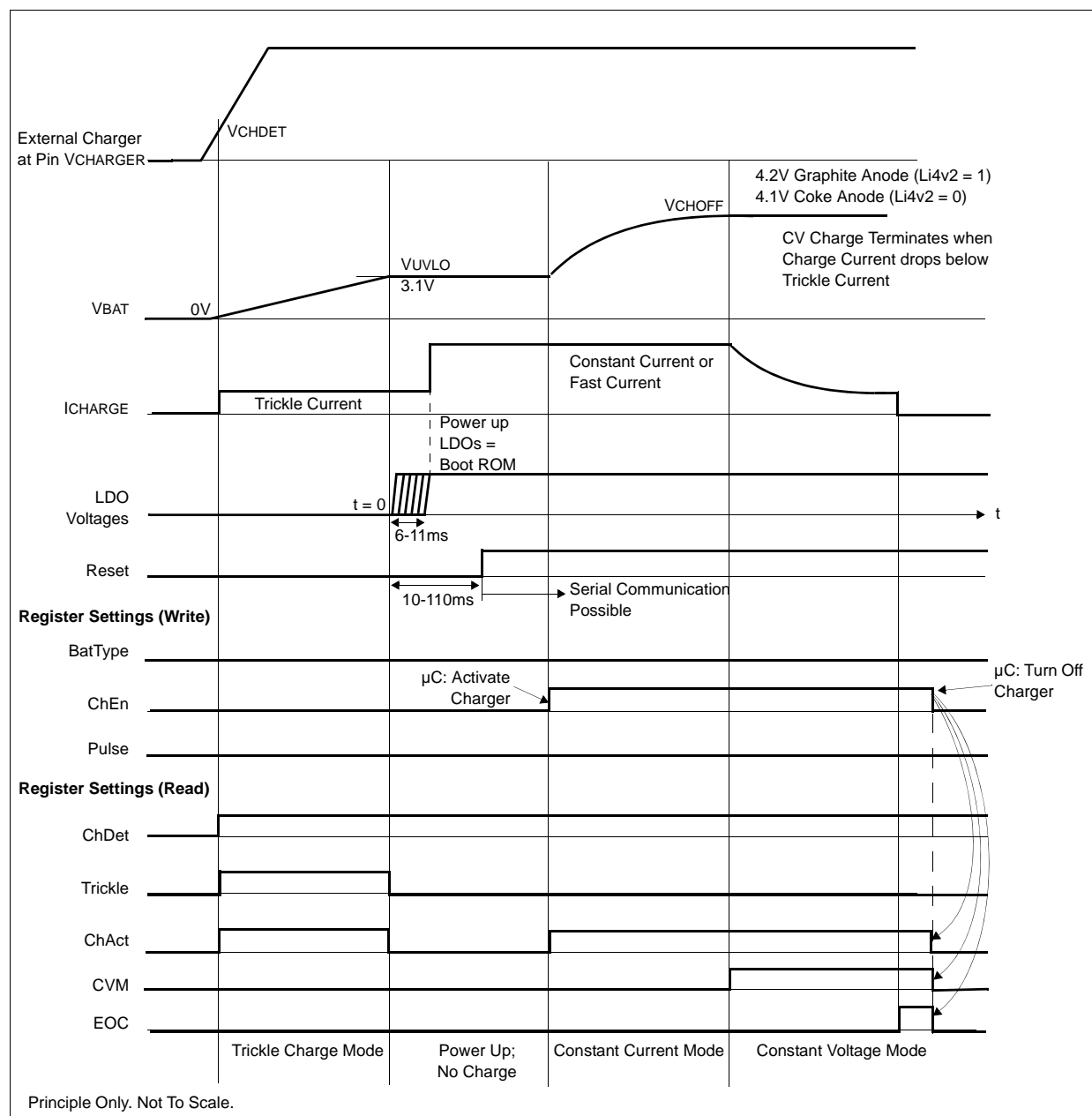
Constant Voltage mode is initiated and bit **CVM** (page 19) will be set when threshold $VCHOFF$ (page 9) has been exceeded for the first time and bit **Pulse** (page 19) is not set.

The charge controller will regulate the battery voltage to a value set by bit **Li4v2** (page 19):

- During Constant Voltage mode, the charge current will decrease and eventually drop below the value set by **TrickleCurrent** (page 20). If the measured charge current is less than or equal to **TrickleCurrent** for 2 consecutive times, charging is terminated and bit **EOC** (page 19) is set. Charging will resume if the battery voltage drops below **VNOBATDET**.
- If the battery voltage (**VBAT_5**) drops below **Vnbatdet** (page 9), e.g. if the battery is removed after charging is finished, **EOC** will be cleared and the battery charger controller will resume in constant voltage mode to enable operation of the device without battery. The "no battery" status is indicated with bit **NoBat** (page 19).

If the battery is replaced after charging is finished and the charge current exceeds the value set by **ConstantCurrent** (page 20), the charge controller will clear bit **CVM** and return to Constant Current or Fast Charge mode, depending on bit **Fast** (page 19). Note that bit **CVM** will be ambiguous if bit **Fast** is set.

Figure 5. Startup and Constant Voltage Charging of Lithium-based Batteries



6.1.7 Pulse Charge Mode

Pulse Charge mode is initiated and bit **CVM** (page 19) will be set when the **VCHOFF** (page 9) threshold has been exceeded for the first time and bit **Pulse** (page 19) is set. If the battery voltage is below the **VCHOFF** threshold, the Battery Charger will be enabled for a minimum on-time specified by bit **TPON** (page 20).

If the battery voltage drops below **VCHOFF** at the end of the minimum on-time, the Battery Charger will remain switched on until the battery voltage exceeds **VCHOFF**. The Battery Charger will then be disabled for at least the minimum off-time specified by bit **TPOFF** (page 20), and the Battery Charger will only be switched on again when the battery voltage falls below **VCHOFF**. In any case, whenever the instantaneous battery voltage exceeds the overvoltage lockout threshold **VOVLO**, charging is disabled immediately.

During on-pulses, the charge current will be limited to the value set by **ConstantCurrent** (page 20) if bit **Fast** (page 19) = 0. If bit **Fast** = 1, the charger transistor Q1 (page 2) will be fully on and the charge current during on-pulses will only be limited by the external charge adapter.

At the beginning of a Pulse Charge cycle, the Battery Charger will operate at a duty cycle close to 100%. Toward the end of the Pulse Charge cycle the Battery Charger will be switched off for long periods between short on-pulses. Eventually, the off-time will become longer than the value specified by bit **TPOFFMAX** (page 20), and the charging cycle will terminate (bit **EOC** (page 19) is set). Charging will resume if the battery voltage drops below **VNOBATDET**.

If the battery voltage (**VBAT_5**) drops below **Vnobatdet** (page 9), e.g. if the battery is removed after charging is finished, **EOC** (page 19) will be cleared and the battery charger controller will resume in pulse charge mode to enable operation of the device without battery. The “no battery” status is indicated with bit **NoBat** (page 19).

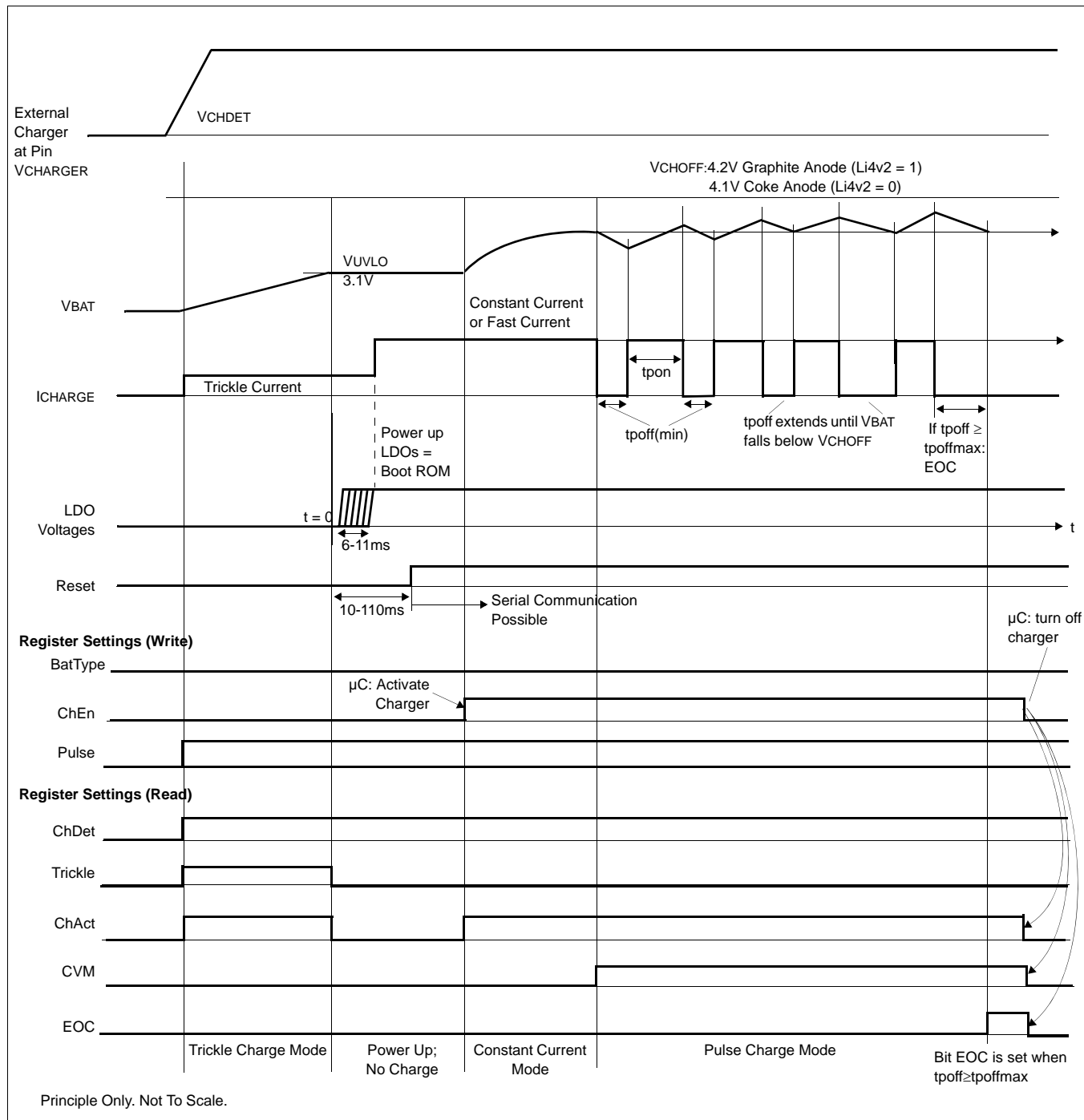
If the battery is replaced after charging is finished and the on-pulse duration **TPON** (page 20) becomes longer than **TPOFFMAX** (page 20), the charge controller will clear bit **CVM** and return to Constant Current or Fast Charge mode, depending on bit **Fast**.

Note that with **TPOFFMAX** = 11 (no termination), the condition for returning to Constant Current or Fast Charge mode will never be met. Bit **CVM** will be ambiguous in this case.

During on-pulses the instantaneous battery voltage may exceed **VCHOFF** by several hundred millivolts. However, no harm will be done to the battery if **TPON** is selected to be shorter than the electrochemical time constant of the battery.

By adding an external gate-source capacitor the switching edges of the P-channel MOSFET can be slowed down further. This prevents an external battery charge adapter with poor transient response from subjecting the **VCHARGER** pin to excessive voltage when the P-channel MOSFET turns off, and prevents excessive current into the battery when the P-channel MOSFET turns on.

Figure 6. Startup and Pulse Charging for Lithium-Based Batteries



6.1.8 Battery Presence Detection

When active, the charge controller constantly monitors the voltage drop across an external current sense resistor (R_{sense}) connected in series between the negative battery terminal and ground. In case no battery is connected to the system, no current can flow through R_{sense} . If no (dis)charge current flow is detected for 2 consecutive times in Pulse Charge mode (during on-pulse) or Constant Voltage mode, bits **NoBat** (page 19) and **CVM** (page 19) will be set.

If a battery is re-connected to the system, current will be flowing through R_{sense} . If a (dis)charge current flow is detected for 2 consecutive times bits **NoBat** and **CVM** will be cleared. Battery presence indication can be disabled by setting bit **DisBDet** (page 20).

6.1.9 Operation Without Battery

This feature allows operation of the device without a battery if a charge adapter is applied to the **VCHARGER** pin and bit **ChEn** (page 19) is set. The battery voltage is regulated to the charge termination threshold **VCHOFF** (page 9), depending on the setting of bits **BatType** (page 19) and **Li4v2** (page 19).

Note that when the charge controller is disabled by clearing bit **ChEn** e.g., during measurement of the battery voltage by an external ADC, the device will be reset when the battery is removed. The “operation without battery” feature can be disabled by setting **DisOWB** (page 20). The minimum required capacitance on **VBAT** (all buffer caps combined) must be $\geq 10\mu\text{F}$ to reduce the ripple on **VBAT** when operating the AS3603 without battery.

6.1.10 Charge Controller Bypass

The charge controller can be bypassed by setting bit **Bypass** (page 19). In bypass mode, the charger transistor **Q1** (page 2) is fully on. The overvoltage protection however will turn off the transistor, when $\text{VBAT} \geq \text{VOVLO}$ (page 9). End-of-charge detection is disabled and has to be performed by the system host, bit **EOC** is cleared.

Removal of the charge adapter will be indicated in the **Charger Status Register** (page 19) but the charge controller will not be disabled. This feature is especially useful when using current-limited charge adapters with an output voltage close to the charge termination threshold and the system is operating without battery. Note that when the voltage difference between the charge adapter output voltage and the battery is smaller than V_{chmin} (page 9) the charger detection circuit will indicate that no charge adapter is connected. Furthermore, Trickle Charge mode is not supported in bypass mode.

```

graph TD
    NonCharging[Non-Charging Mode] --> ChDet1{Charger detected?}
    ChDet1 -- NO --> NonCharging
    ChDet1 -- YES --> DevAct1{Device active?}
    DevAct1 -- YES --> ChAct0_CVM0[ChAct=0; CVM=0]
    DevAct1 -- NO --> VbatUVLO1{V_BAT > V_UVLO?}
    VbatUVLO1 -- YES --> ChAct1_Trickle1[ChAct=1; Trickle=1]
    VbatUVLO1 -- NO --> TrickleCharge[Trickle Charge]
    TrickleCharge --> ChDet2{Charger detected?}
    ChDet2 -- YES --> ChDet0_ChAct0_Trickle0[ChDet=0; ChAct=0; Trickle=0]
    ChDet2 -- NO --> VbatUVLO2{V_BAT > V_UVLO?}
    VbatUVLO2 -- YES --> Trickle0[Trickle=0]
    VbatUVLO2 -- NO --> StartupDevice[Startup Device]
    StartupDevice --> ActiveCharging[Active Charging Mode]
    ActiveCharging --> ChDet3{Charger detected?}
    ChDet3 -- YES --> ChAct0[ChAct=0]
    ChDet3 -- NO --> ChDet0_ChAct0[ChDet=0; ChAct=0]
    ChDet0_ChAct0 --> ChEn1_1{ChEn=1?}
    ChEn1_1 -- YES --> FastCharge[Fast Charge / Constant Current Charge]
    ChEn1_1 -- NO --> ChAct0_CVM0
    ChAct0_CVM0 --> TopOffCharge[Top-Off Charge]
    TopOffCharge --> ChDet4{Charger detected?}
    ChDet4 -- YES --> ChEn1_2{ChEn=1?}
    ChDet4 -- NO --> ChDet0_ChAct0_CVM0[ChDet=0; ChAct=0; CVM=0]
    ChEn1_2 -- YES --> ChargingComplete{Charging complete?}
    ChargingComplete -- YES --> EOC1[EOC = 1]
    ChargingComplete -- NO --> ChAct0_CVM0
    EOC1 --> BatType1{BatType=1?}
    BatType1 -- YES --> VbatVchoff{V_BAT > V_CHOFF?}
    VbatVchoff -- YES --> ChEn1_3{ChEn=1?}
    ChEn1_3 -- YES --> ChDet5{Charger detected?}
    ChDet5 -- YES --> FastCharge
    ChDet5 -- NO --> ChDet0_ChAct0
    ChEn1_3 -- NO --> ChEn1_2
    VbatVchoff -- NO --> ChEn1_2
    EOC1 -- NO --> VbatVnogatet[V_BAT < V_NOGATET]
    VbatVnogatet --> EOC0[EOC=0]
    EOC0 --> ChEn0[ChEn=0]
    ChEn0 --> ChAct0_CVM0
    ChAct0_CVM0 --> NonCharging
    
```

When the battery voltage exceeds the VOVLO (page 9) threshold (VBAT rising), the charger transistor Q1 (page 2) is turned off. Charging will resume if the battery voltage drops below VOVLO (VBAT falling).

Likewise, when the battery voltage drops below the Undervoltage Lockout Threshold VUVLO (VBAT falling) (page 9), a Reset is generated (page 54), which also clears bit **ChEn** (page 19).

The charger will remain in low current Trickle Charge mode (page 9) until the VUVLO threshold (VBAT rising) has been exceeded.

6.1.12 Charger Detection Circuit

The Battery Charger Controller uses an integrated Charger Detection Circuit to determine if an external battery charger adapter has been applied to the VCHARGER pin.

Charger register bits will be set/reset when any of the following conditions are met:

1. When the charger voltage exceeds the battery voltage by V_{chdet} (page 9), Bit **chDet** (page 19) will be set.
2. When the charger voltage drops below V_{chmin} (page 9) above the battery voltage, bit **chDet** will be reset. If the charger was active, bit **ChEn** (page 19) = 1, bit **ChAct** (page 19) will also be reset. Charging will resume when the conditions for bit **chDet** = 1 are met.
3. If a Reset occurs during charging, the charger will also be reset (**ChAct** = 0). Bits **ChEn** and **chDet** will remain set to 1. To resume charging, the charger must be turned off (**ChEn** = 0) and then on (**ChEn** = 1).

6.1.13 Bootstrap Voltage Regulator

To charge even completely discharged batteries, the AS3603 contains an internal bootstrap voltage regulator (LDO V2_5) which generates a bootstrap voltage (V_{chreg}) to supply power to the internal Battery Charger circuitry.

When LDO V2_5 is active, bit **IntReg** (page 19) will be set. As soon as the battery voltage exceeds the undervoltage lockout threshold V_{UVLO} (page 9), LDO V2_5 is disabled (bit **IntReg** reset) and the battery will supply power to the Battery Charger circuitry.

6.1.14 Battery Charger Operation

The Battery Charger Controller controls an 8-bit current DAC which delivers a current (I_{DAC}) that will generate a voltage (V_{GS}) over an external resistor (R_{GS}) connected between the gate and source of an external P-channel MOSFET.

Charge Current Regulator

The Charge Current Regulator has a resolution of 0.625mV or 12.5mA when using a 50mΩ sense resistor. The resolution is programmable using the **Charger Control Register** (page 19).

Table 5. Charge Current Regulator Parameters

Symbol	Parameter	Min	Typ	Max	Unit
IVGATE,LSB	Resolution of VGATE current; bit Boost (page 19) = 0		0.5		μA
IVGATE,FS	Full-scale value of VGATE current; bit Boost = 0		127.5		μA

6.1.15 Fuel Gauge

The Fuel Gauge enables remaining capacity estimation of the battery by tracking the net current flow into and out of the battery using a Voltage-to-Frequency Converter.

Table 6. Fuel Gauge Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
fclk	Internal Reference Clock	1.0	1.1	1.2	MHz	
fVFC	Sample Frequency		fCLK/59		Hz	fCLK: internal reference clock.
VSNSP/ VSNSN	Input Voltage	-0.1		0.1	V	
ZSNSP/ ZSNSN	Input Impedance	4.67			MΩ	
AVFC	(Dis)Charge Gain		91.0		Hz/V	fclk = 1.1MHz
FRVFC	Fundamental Rate		3.05		μVh	
	Supply Voltage Gain Coefficient		tbd		% / V	
	Temperature Gain Coefficient		tbd		% / °C	
VOFF	Uncompensated Offset Voltage	-500		500	μV	Offset voltage $I_{snp} - I_{snsN}$
VOFF,COMP	Compensated Offset Voltage	-50	±10	50	μV	Offset error after offset compensation

Voltage-to-Frequency Converter

The Voltage-to-Frequency Converter constantly monitors the voltage drop across an external current sense resistor (R_{sense}) connected in series between the negative battery terminal and ground.

The use of an additional external RC lowpass filter is highly recommended. Using two 47k Ω resistors, R2 and R3 (page 2), and a 0.1 μ F ceramic capacitor, C28 (page 2), the filter cutoff is approximately 16.9 Hz. This filter will capture the effect of most spikes, and will thus allow the Fuel Gauge to accurately detect the total charge that has gone into or out of the battery.

Charge Current Accumulator

The Charge Current Accumulator is an internal 15-bit up/down counter with sign bit. It is incremented when current is charged into the battery and decremented when current is drawn out of the battery. It is updated at a rate of one count per 3.05 μ Vh, which is equivalent to one count per 61.03 μ Ah (using a 50m Ω current sense resistor).

If the counter is not read, it will roll over beyond FFFF_h, which occurs after approximately 2000mAh of charge (using a 50m Ω sense resistor). It is the responsibility of the host system to read and reset the counter before rollover occurs.

The contents of the Charge Current Accumulator will be transferred into the **Delta Charge MSB Register** (page 21) and the **Delta Charge LSB Register** (page 21) when bit **UpdReq** (page 21) has been set. After the Delta Charge MSB/LSB registers have been updated successfully, bit **UpdReq** is cleared automatically and the Charge Current Accumulator will be reset along with bit **sign**.

Constant Voltage Regulator

The Constant Voltage Regulator acts directly on the setting of the 8-bit current DAC. It will commence when threshold VCHOFF (page 9) has been exceeded for the first time as long as bit **Pulse** (page 19) is not set.

Elapsed Time Counter

The sample clock (fvfc) of the Fuel Gauge is fed to a 14-bit clock count divider, whose output signal is used as a clocking signal for the 16-bit Elapsed Time Counter, resulting in an equivalent rate of 1.1379 counts per second (4096.60 counts = 1 hour, 1 count = 0.8788s).

The Elapsed Time Counter can rollover beyond FFFF_h which occurs after about 16 hours. If this happens the value given by the counter will be ambiguous. It is the responsibility of the host system to read the Elapsed Time Counter before rollover occurs.

The content of the Elapsed Time Counter is transferred into the **Elapsed Time MSB Register** (page 22) and the **Elapsed Time LSB Register** (page 22) when bit **UpdReq** (page 21) has been set. After the Elapsed Time MSB/LSB registers have been updated successfully, bit **UpdReq** is cleared automatically and the Elapsed Time Counter is reset.

Offset Calibration Mode

Although the Voltage-to-Frequency Converter compensates for the offset of the Integrator, the Fuel Gauge features an additional offset calibration mode to enhance the measurement accuracy even further. By setting bit **CalReq** (page 21) the Integrator is reset and the offset calibration mode is activated.

The offset is accumulated during 16 clocks of the elapsed time counter (16x0.8788s = 14.06 sec). When offset calibration is complete, bit **CalReq** is cleared automatically and the offset value is transferred into the **Delta Charge MSB Register** (page 21) and the **Delta Charge LSB Register** (page 21) for calculating the actual average current (page 18).

The calculated value defines the measured offset between I_{sensP} and I_{sensN} . It has a resolution of 3.05 μ V. This offset value is used as a correction factor for calculating the actual average current.

Note: Offset calibration is not possible while the charger is active. If bit **CalReq** is set while the charger is active, the calibration will start automatically after the charger has been disabled by clearing bit **ChEn** or if the external battery charger adapter has been removed. If, during offset calibration, the charger is enabled, offset calibration mode is terminated, bit **CalReq** is cleared, the current value of the Elapsed Time Counter is transferred to the Elapsed Time MSB/LSB registers, and the Delta Charge MSB/LSB registers are loaded with FFFF_h.

Calculation of Battery Status

The host system can calculate all the parameters necessary for estimating the remaining battery capacity by evaluating FGOFFCal (the Elapsed Time MSB/LSB (page 22) and the Delta Charge MSB/LSB (page 21) registers).

Calculating Elapsed Time

The host system can evaluate the change in time (Δt) by setting bit **UpdReq** (page 21) and reading the Elapsed Time MSB/LSB registers after bit **UpdReq** has been automatically cleared. The change in time in seconds is given by:

$$\Delta t = \text{ElapsedTime} \times 3600 / 4096.60 \text{ [s]} \quad (\text{EQ 1})$$

The absolute accuracy of (Δt) is directly related to the absolute accuracy of f_{CLK} . To cancel errors associated with the accuracy of the oscillator, a correction factor (CV) can be introduced. CV can be evaluated by comparing the change in time calculated by (EQ 1) with a reference value (Δt_{REF}) obtained from a RTC or measured during system calibration. CV is given by:

$$CV = \Delta t_{\text{REF}} / \Delta t \quad (\text{EQ 2})$$

By multiplying Δt with CV, the correct value for the change in time (Δt_{CORR}) can be calculated:

$$\Delta t_{\text{CORR}} = CV \times \Delta t \text{ [s]} \quad (\text{EQ 3})$$

Calculating Average Current

The host system can calculate the average current (I_{AVG}) during the last time period by setting bit **UpdReq** (page 21) and reading the Delta Charge MSB/LSB registers and the Elapsed Time MSB/LSB registers after **UpdReq** has been automatically cleared. Together with FGOFFCAL, determined during offset calibration mode, I_{AVG} is given by:

$$I_{\text{AVG}} = \text{DeltaCharge} / (\Delta t \times A_{\text{VFC}} \times R_{\text{sense}}) - \text{FGOffCal} \times 3.05 \mu\text{V} / R_{\text{sense}} \text{ [A]} \quad (\text{EQ 4})$$

Δt is the change in time in seconds calculated by (EQ 1), A_{VFC} is the gain of the Voltage-to-Frequency Converter in Hz/V, R_{sense} is the value of the sense resistor in ohms, and FGOFFCAL is the offset calibration value. As Δt and DeltaCharge both are proportional to the oscillator frequency, no correction factor needs to be introduced in the formula.

Calculating Accumulated Capacity

Accumulated capacity is used to calculate the absolute remaining capacity of the battery. It is given by:

$$Q_{\text{ACC}} = I_{\text{AVG}} \times \Delta t_{\text{CORR}} \text{ [As]} \quad (\text{EQ 5})$$

Calculating the Remaining Capacity

Calculation of the remaining battery capacity (RC) is the goal of the Fuel Gauge. It is given by:

$$RC = RC + Q_{\text{ACC}} \text{ [As]} \quad (\text{EQ 6})$$

Calculating the Time to Empty

Time to empty (t_{te}) is calculated from the average current (I_{AVG}) given by (EQ 4). The longer the time period for which I_{AVG} is calculated, the more accurate the value for I_{AVG} and therefore the estimated t_{te} will be. It is given by:

$$t_{\text{TE}} = RC / I_{\text{AVG}} \text{ [s]} \quad (\text{EQ 7})$$

6.1.16 Battery Charger Controller Registers

The Battery Charger Controller is controlled by the registers listed in Table 7.

Table 7. Battery Charger Controller Register Summary

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Page
Charger Status Register	53	Bypass	NoBat	EOC	CVM	Trickle	IntReg	ChAct	chDet	19
Charger Control Register	20	N/A	Boost	Bypass	Pulse	Li4v2	Fast	BatType	ChEn	19
Charger Timing Register	44	TPOFFMAX		TPOFF			TPON			20
Charger Current Register	22	N/A			ConstantCurrent			TrickleCurrent		20
Charger Config Register	66	N/A		CVMtst	DisOWB	DisBDet	Dis Hyst	Wide	N/A	20
Fuel Gauge Register	21	N/A				CalMod	CalReq	UpdReq	FGEn	21
Delta Charge MSB Register	54	sign	214	213	212	211	210	29	28	21
Delta Charge LSB Register	55	27	26	25	24	23	22	21	20	21
Elapsed Time MSB Register	56	215	214	213	212	211	210	29	28	22
Elapsed Time LSB Register	57	27	26	25	24	23	22	21	20	22
PreCurDac Register	67	27	26	25	24	23	22	21	20	22

Addr: 53		Charger Status Register		
		Displays status of Battery Charger Controller.		
Bit	Bit Name	Default	Access	Bit Description
0	chDet	00 _h	R	0 = No external battery charger detected. 1 = External battery charger adapter has been detected. Charger voltage exceeds battery voltage by V _{chdet} .
1	ChAct	00 _h	R	0 = Charger is off or in Trickle Charge mode. 1 = Charger is in Constant Current, Fast Charge, or Pulse Charge mode.
2	IntReg	00 _h	R	0 = Bit is cleared when V _{BAT} > V _{UVLO} . 1 = LDO V _{2_5} is operating.
3	Trickle	00 _h	R	0 = Trickle charging is off. 1 = Charger is in Trickle Charge mode. Trickle current is set by the Charger Current Register (page 20).
4	CVM	00 _h	R	0 = Battery charger is not in top-off charge mode. 1 = Battery charger is in top-off charge mode (constant voltage or pulse charge mode).
5	EOC	00 _h	R	0 = Battery charger is off or charging is in progress; automatically cleared when ChEn (page 19) is cleared. 1 = End of Charge. Automatically set when CV or pulse charging is completed or when V _{CHOFF} is exceeded during charging of Ni-based batteries.
6	NoBat	00 _h	R	No battery detection. 0 = Battery is connected, when DisBDet (page 20) is set, and/or ChEn (page 19) is cleared. 1 = No battery detected at V _{BAT} .
7	Bypass	00 _h	R	Indicates charger bypass mode. 0 = Normal charger operating mode. 1 = Indicates that charger is in bypass mode; charger transistor Q1 (page 2) is fully on and EOC detection is disabled.

Addr: 20		Charger Control Register		
		Controls operation of the Battery Charger Controller.		
Bit	Bit Name	Default	Access	Bit Description
0	ChEn	Boot ROM	R/W	0 = Disables charging. 1 = Enables charging.
1	BatType	Boot ROM	R/W	Li4v2 BatType Description 00 = LLi-ion battery with coke anode; V _{CHOFF} (page 9) = 4.1V 10 = Li-ion battery with graphite anode; V _{CHOFF} = 4.2V x1 = Nickel-based battery; V _{CHOFF} = 5.52V
2	Fast	Boot ROM	R/W	0 = Selects Constant Current charge mode. 1 = Selects Fast Charge mode.
3	Li4v2	Boot ROM	R/W	Selects the type of lithium-based battery. 0 = V _{CHOFF} (page 9) = 4.1V for Li+ battery with coke anode. 1 = V _{CHOFF} = 4.2V for Li+ battery with graphite anode.
4	Pulse	Boot ROM	R/W	Selects top-off charging mode. 0 = Select constant voltage charging mode. 1 = Select pulse charging mode.
5	Bypass	Boot ROM	R/W	Enable bypassing of charge controller. 0 = Normal charger operation. 1 = Select charger bypass mode; charger transistor Q1 (page 2) is fully on and EOC detection is disabled.
6	Boost	Boot ROM	R/W	Selects output of current DAC at pin V _{GATE} . 0 = Nominal current (max. 128μA). 1 = 10x nominal current (default; max. 1.28mA).
7				N/A

Addr: 44		Charger Timing Register		
		Sets parameters for pulse charging.		
Bit	Bit Name	Default	Access	Bit Description
2:0	TPON	001	R/W	Sets the minimum on-time in pulse charge mode from 137.31ms to 1098.74ms in steps of 137.31ms. 000 = 137.31ms 100 = 686.55ms 001 = 274.62ms (default) 101 = 823.86ms 010 = 411.93ms 110 = 961.17ms 011 = 549.24ms 111 = 1098.48ms
5:3	TPOFF	001	R/W	Sets the minimum off-time in pulse charge mode from 68.65ms to 549.24ms in steps of 68.65ms. 000 = 68.65ms 100 = 343.28ms 001 = 137.31ms (default) 101 = 411.93ms 010 = 205.97ms 110 = 480.59ms 011 = 274.62ms 111 = 549.24ms
7:6	TPOFFMAX	01	R/W	Sets the maximum off-time in pulse charge mode before charging is terminated. 00 = 4 x TPON (page 20) (yields 1/5 of the constant charging current. 10 = 19 x TPON (yields 1/20 of the constant charging current. 01 = 9 x TPON (yields 1/10 of the constant charging current). 11 = No termination (not recommended).

Addr: 66		Charger Config Register		
		Sets additional charger configurations.		
Bit	Bit Name	Default	Access	Bit Description
0				N/A
1	Wide	00h	R/W	For test purposes only.
2	Dis Hyst	00h	R/W	For test purposes only.
3	DisBDet	00h	R/W	0 = Enable battery presence indication (default). 1 = Disable battery presence indication.
4	DisOWB	00h	R/W	0 = Enable operation without battery (default). 1 = Disable operation without battery.
5	CVMtst	00h	R/W	0 = Disable CVM testmode (default). 1 = Enable CVM testmode.
7:6				N/A

Addr: 22		Charger Current Register		
		Sets current for trickle and Constant Current charging.		
Bit	Bit Name	Default	Access	Bit Description
1:0	TrickleCurrent	Boot ROM (01)	R/W	Sets the Trickle Charge mode from: (1.25mV to 10mV)/R _{sense} in steps of 1.25mV/R _{sense} . 00 = 1.25mV/R _{SENSE} 10 = 5.00mV/R _{SENSE} 01 = 2.5mV/R _{SENSE} (default) 11 = 10mV/R _{SENSE}
4:2	ConstantCurrent	Boot ROM (011)	R/W	Sets the charging current in Constant Current mode from: (0mV to 35mV) x R _{sense} -1 in steps of 5mV x R _{sense} -1. 000 = No current. 100 = 20mV/R _{sense} 001 = 5mV/R _{sense} 101 = 25mV/R _{sense} 010 = 10mV/R _{sense} 110 = 30mV/R _{sense} 011 = 15mV/R _{sense} (default) 111 = 35mV/R _{sense}
7:5				N/A

Addr: 21		Fuel Gauge Register		
		Controls the Fuel Gauge.		
Bit	Bit Name	Default	Access	Bit Description
0	FGEn	0b	R/W	Controls the operation of the Fuel Gauge. 0 = Disables Fuel Gauge. 1 = Enables Fuel Gauge.
1	UpdReq	0b	R/W	Controls the updates of the Delta Charge MSB/LSB registers and the Elapsed Time MSB/LSB registers. When set, this bit is cleared automatically after the Delta Charge MSB/LSB registers and the Elapsed Time MSB/LSB registers have been successfully updated. 0 = Indicates update of Delta Charge MSB/LSB registers and Elapsed Time MSB/LSB registers has been completed. 1 = Request update of Delta Charge and Elapsed Time Registers
2	CalReq	0b	R/W	Controls offset calibration. When set, this bit is cleared automatically after offset calibration has successfully completed. 0 = Indicates offset calibration has completed or forces termination of offset calibration. 1 = Request offset calibration.
3	CalMod	0b	R/W	Sets the offset calibration mode. 0 = Connect inputs to ground. 1 = Use ISENSP and ISENSN (for testing purposes only).
7:4				N/A

Addr: 54		Delta Charge MSB Register		
		Holds the amount of charge since last reading.		
Bit	Bit Name	Default	Access	Bit Description
0	28	00 _h	R	This register (along with Delta Charge LSB Register) is maintained in two's complement form with a resolution of 3.05μVh and a full-scale value of ±99.98mVh. When using a 50mΩ current sense resistor, this is equivalent to a resolution of 61.03uAh and a full-scale value of 1.999Ah. The sign bit is set for negative values. This register will be updated after setting bit UpdReq (page 21) = 1.
1	29	00 _h	R	
2	2 ¹⁰	00 _h	R	
3	2 ¹¹	00 _h	R	
4	2 ¹²	00 _h	R	
5	2 ¹³	00 _h	R	
6	2 ¹⁴	00 _h	R	
7	sign	00 _h	R	

Addr: 55		Delta Charge LSB Register		
		Holds the amount of charge since last reading.		
Bit	Bit Name	Default	Access	Bit Description
0	2 ⁰	00 _h	R	This register (along with Delta Charge MSB Register) is maintained in two's complement form with a resolution of 3.05μVh and a full-scale value of ±99.98mVh. When using a 50mΩ current sense resistor, this is equivalent to a resolution of 61.03uAh and a full-scale value of 1.999Ah. This register is updated after setting bit UpdReq (page 21) = 1.
1	2 ¹	00 _h	R	
2	2 ²	00 _h	R	
3	2 ³	00 _h	R	
4	2 ⁴	00 _h	R	
5	2 ⁵	00 _h	R	
6	2 ⁶	00 _h	R	
7	2 ⁷	00 _h	R	

Addr: 56		Elapsed Time MSB Register		
		Holds the elapsed time since last reading.		
Bit	Bit Name	Default	Access	Bit Description
0	28	00 _h	R	This register (along with the Elapsed Time LSB Register) stores the elapsed time count with a resolution of 0.8788 seconds and a full-scale value of 15.997 hours. This register will be updated after setting bit UpdReq (page 21) = 1.
1	29	00 _h	R	
2	2 ¹⁰	00 _h	R	
3	2 ¹¹	00 _h	R	
4	2 ¹²	00 _h	R	
5	2 ¹³	00 _h	R	
6	2 ¹⁴	00 _h	R	
7	2 ¹⁵	00 _h	R	

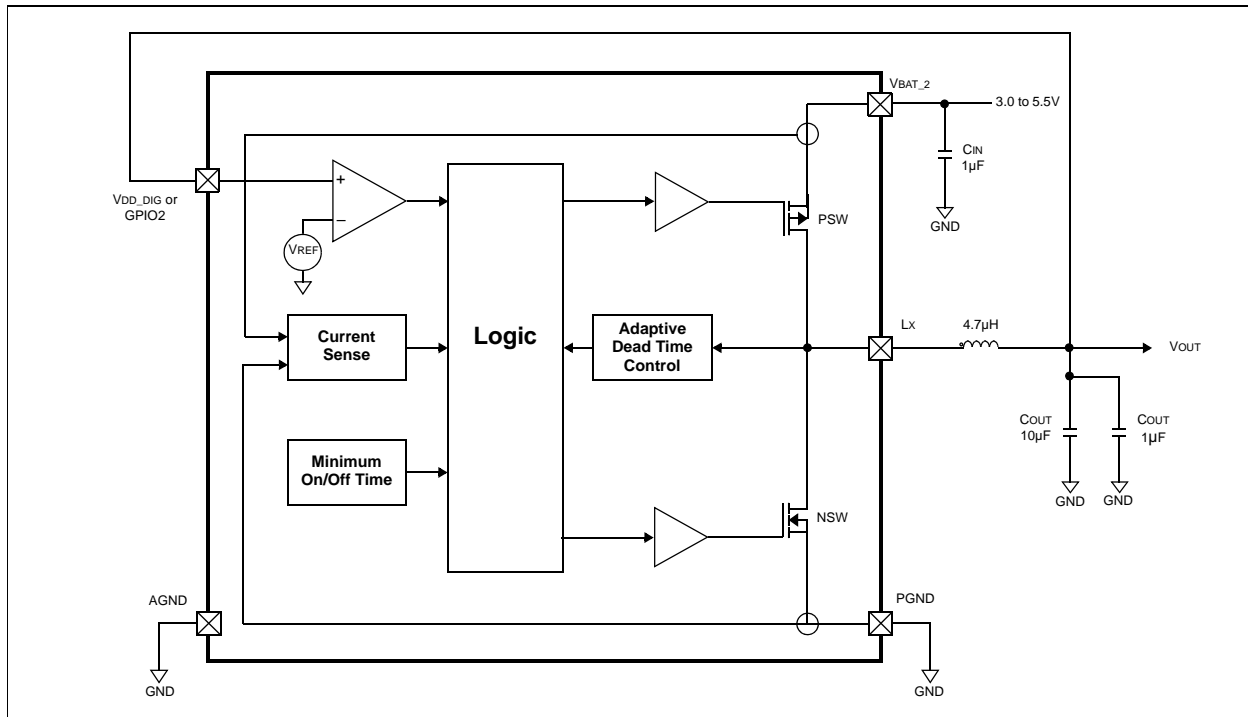
Addr: 57		Elapsed Time LSB Register		
		Holds the elapsed time since last reading.		
Bit	Bit Name	Default	Access	Bit Description
0	2 ⁰	00 _h	R	This register (along with the Elapsed Time MSB Register) stores the elapsed time count with a resolution of 0.8788 seconds and a full-scale value of 15.997 hours. This register will be updated after setting bit UpdReq (page 21) = 1.
1	2 ¹	00 _h	R	
2	2 ²	00 _h	R	
3	2 ³	00 _h	R	
4	2 ⁴	00 _h	R	
5	2 ⁵	00 _h	R	
6	2 ⁶	00 _h	R	
7	2 ⁷	00 _h	R	

Addr: 67		PreCurDac Register		
		Sets starting point for current DAC at pin VGATE.		
Bit	Bit Name	Default	Access	Bit Description
0	2 ⁰	00 _h	R/W	Sets the preset value for the current DAC at pin VGATE to speed up the startup, when the charge controller is enabled. Boost = 0: Boost = 1: 00 _h = 0μA 00 _h = 0μA ...0.5μA ... 5μA FF _h = 127.5μA FF _h = 1.275mA
1	2 ¹	00 _h	R/W	
2	2 ²	00 _h	R/W	
3	2 ³	00 _h	R/W	
4	2 ⁴	00 _h	R/W	
5	2 ⁵	00 _h	R/W	
6	2 ⁶	00 _h	R/W	
7	2 ⁷	00 _h	R/W	

6.2 Step Down DC/DC Converter

The Step Down DC/DC Converter uses a unique current-limited control scheme to ensure high-efficiency and fast transient-response, and requires small external components.

Figure 8. Step Down DC/DC Converter Block Diagram



The Step Down DC/DC Converter control scheme is such that when the output voltage is out of regulation, the error comparator triggers a switching cycle by turning on the high-side switch (PSW). This switch remains on until the minimum on-time – specified by bit **tMIN_ON** (page 24) – of 200ns expires and the output voltage regulates or the current-limit threshold is exceeded.

Once off, the high-side switch remains off until the minimum off-time – specified by bit **tMIN_OFF** (page 24) – of 200ns expires, and the output voltage falls out of regulation. During this period, the low-side synchronous rectifier (NSW) turns on and remains on until either the high-side switch turns on again or the inductor current falls below the lower current-limit threshold (or approaches zero).

This control scheme allows the circuit to provide excellent performance throughout a wide load-current range. When delivering light loads, the high-side switch turns off after the minimum on-time to reduce peak inductor current, resulting in increased efficiency and reduced output voltage ripple.

Using bit **stepdown_fb** (page 43), the regulator feedback input can be configured at two pins:

- **VBUCK** – When used as feedback input, configures the Step Down DC/DC Converter as a pre-regulator for the digital LDOs (VDIG_1 and VDIG_2)
- **GPIO2** – When used as feedback input, allows the digital LDOs (VDIG_1 and VDIG_2) to be connected to a separate input voltage source.

Table 8. Step Down DC/DC Converter Parameters

Symbol	Parameter	Min	TYP	Max	Unit	Notes
V _{IN}	Input Voltage	3.0		5.5	V	Pin V _{BAT}
V _{OUT}	Regulated Output Voltage	1.0		3.0	V	Sense pin V _{BUCK} (or GPIO2)
V _{OUT_tol}	Output Voltage Tolerance	-50		50	mV	Sense pin V _{BUCK} (or GPIO2)
I _{LIMIT}	Current Limit		350		mA	Supply current into PMOS transistor
R _{PSW}	PSW On-Resistance			0.5	Ω	
R _{NSW}	NSW On-Resistance			0.5	Ω	
I _{load}	Load Current	0		500	mA	
f _{SW}	Switching Frequency			2.5	MHz	Using external clock
C _{out}	Output Capacitor		10		μF	Tantalum
L _x	Inductor		4.7		μH	
η _{eff}	Efficiency		90		%	I _{load} = 100mA, V _{IN} = 2.3V, V _{BAT} = 3V
I _{VDD}	Current Consumption		150		μA	Operating Current
			100			Quiescent Current
				0.1		Shutdown Current
t _{MIN_ON}	Minimum On Time		200		ns	
t _{MIN_OFF}	Minimum Off Time		200		ns	

6.2.1 Step Down DC/DC Converter Registers

The Step Down DC/DC Converter is controlled by the registers listed in Table 9.

Table 9. Step Down DC/DC Converter Register Summary

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Page
Step Down Voltage Register	01					buck_v				24
Reg Power Control Register	09	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25
Step Down Configuration Register	23	dis_xnc	dis_ilim	force_pwm	N/A		sync_rect_off	buck_nsw_on	buck_psw_on	25

Addr: 01		Step Down Voltage Register			
		Sets the output voltage of the Step Down DC/DC Converter.			
Bit	Bit Name	Default	Access	Bit Description	
4:0	buck_v		R/W	Controls the voltage selection for the Step Down DC/DC Converter. 00000 = 1.0V(LSB = 100mV) 10011 = 2.9V 10100-11111 = 3.0V	
7:5				N/A	

Addr: 09		Reg Power Control Register		
		Enables/disables voltage regulators.		
Bit	Bit Name	Default	Access	Bit Description
0	ldo_ana1_on			Refer to page 34.
1	ldo_ana2_on			Refer to page 34.
2	ldo_dig1_on			Refer to page 34.
3	ldo_dig2_on			Refer to page 34.
4	ldo_sim_on			Refer to page 34.
5	buck_on	Boot ROM	R/W	Enables the Step Down DC/DC Converter. 0 = Step Down DC/DC Converter is off. 1 = Step Down DC/DC Converter is on.
7:6				N/A

Addr: 23		Step Down Configuration Register		
		Configures the operation mode of the Step Down DC/DC Converter.		
Bit	Bit Name	Default	Access	Bit Description
0	buck_psw_on	Boot ROM	R/W	Activate PSW (0.5Ω PMOS) only if buck_on (page 25) and buck_nsw_on (page 25) = 0. 0 = Default setting. P-Channel switching transistor is off. 1 = Turns on P-Channel switching transistor. Bits buck_on and buck_nsw_on must both be = 0.
1	buck_nsw_on	Boot ROM	R/W	Activates NSW (0.5Ω NMOS) only if buck_on (page 25) = 0 and buck_psw_on = 0. 0 = Default setting. N-Channel switching transistor is off. 1 = Turns on N-Channel switching transistor. Bits buck_on and buck_psw_on must both be = 0.
2	sync_rect_off	Boot ROM	R/W	0 = Enable the synchronous rectifier. This bit should always be set to 0. 1 = The synchronous rectifier is disabled. For test purposes only.
4:3				N/A
5	force_pwm	Boot ROM	R/W	0 = Default setting. Caution: Do not change the setting of this bit. 1 = Forces output stage into PWM mode; reduced noise, but also reduced efficiency.
6	dis_ilim	Boot ROM	R/W	0 = Default setting, current limit = 350mA. Caution: Do not change the setting of this bit. 1 = Disables current limitation (not recommended).
7	dis_xnc	Boot ROM	R/W	0 = Default setting. Caution: Do not change the setting of this bit. 1 = Disables adaptive dead time control. For test purposes only.

6.2.2 Typical Performance Characteristics

Figure 9. Step Down DC/DC Converter Load Regulation

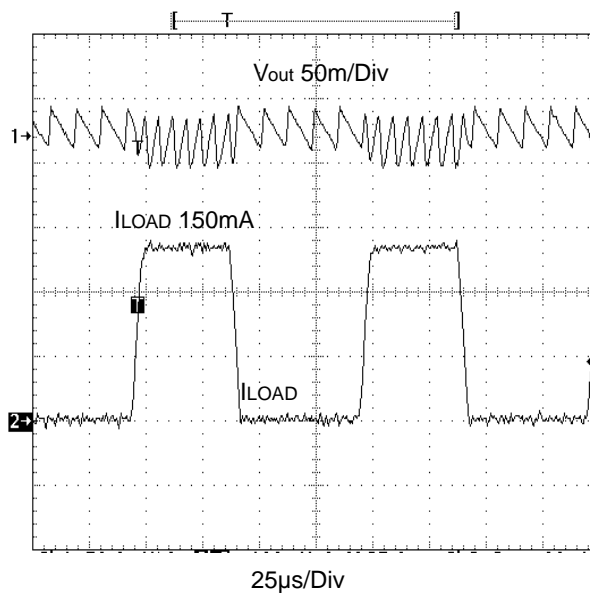
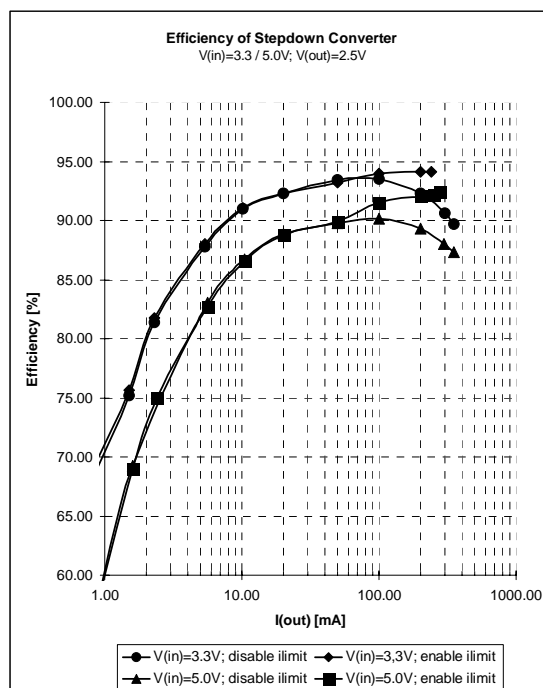


Figure 10. Step Down DC/DC Converter Efficiency



6.3 Low Dropout Regulators

The Low Dropout Regulators (LDOs) are linear high performance regulators with programmable output voltages. The LDOs can be controlled by either software (voltage, on/off) or hardware (on/off) using highly configurable GPIO1 to GPIO4 pins.

The Low Dropout Regulators include the following:

- RF and Analog Low Dropout Regulators – Described on page 27
- Digital Low Dropout Regulators – Described on page 28
- SIMCard Low Dropout Regulator – Described on page 29
- Low Power Low Dropout Regulator – Described on page 30

6.3.1 RF and Analog Low Dropout Regulators

The RF LDOs (VRF_1 - VRF_4) and Analog LDOs (VANA_1 and VANA_2) are designed to supply power to sensitive analog circuits like LNAs, Transceivers, VCOs and other critical RF components of cellular radios. Additionally, these LDOs are suitable for supplying power to audio devices or as a reference for A/D and D/A converters.

The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices. Stability is guaranteed with ceramic output capacitors (see Figure 11) of $1\mu\text{F} \pm 20\%$ (X5R) or $2.2\mu\text{F} +100/-50\%$ (Z5U).

The low ESR of these capacitors ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress ripple on the battery caused by the PA in TDMA systems. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 11. Analog LDO Block Diagram

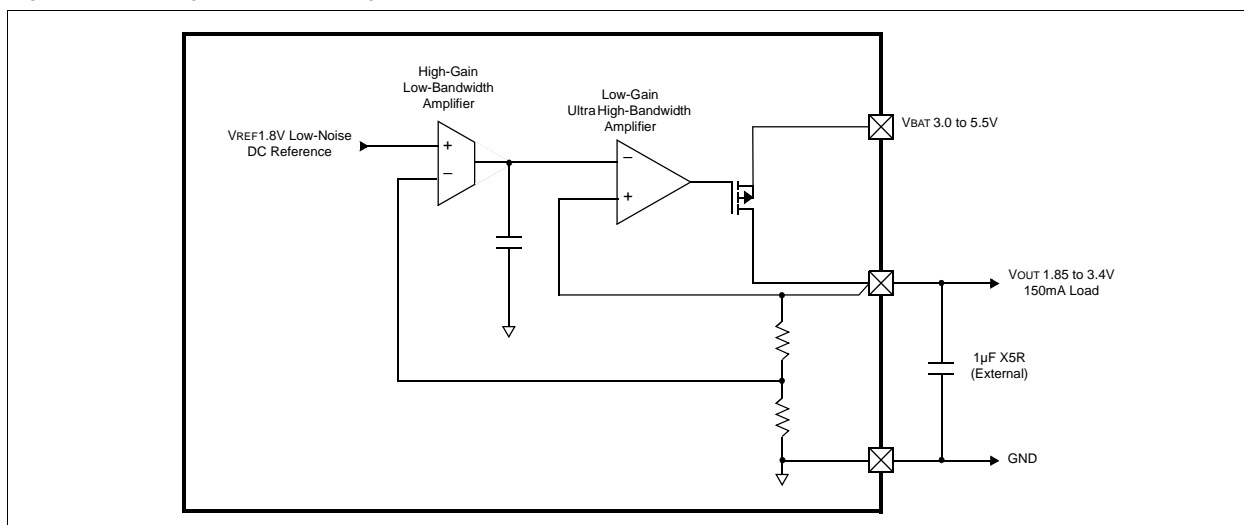


Table 10. RF and Analog LDO Characteristics

VBAT = 4V; I_{LOAD} = 150mA; T_{AMB} = 25°C; C_{LOAD} = 2.2µF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VBAT	Supply Voltage Range	3		5.5	V	
RON	On-Resistance			1	Ω	VANA_1, VANA_2, VRF_1, VRF_2
				2		VRF_3, VRF_4

Table 10. RF and Analog LDO Characteristics (Continued)

$V_{BAT} = 4V$; $I_{LOAD} = 150mA$; $T_{AMB} = 25^{\circ}C$; $C_{LOAD} = 2.2\mu F$ (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
PSRR	Power Supply Rejection Ratio	70			dB	$f = 1kHz$
		40				$f = 100kHz$
I _{OFF}	Shut Down Current			100	nA	
I _{VDD}	Supply Current			50	μA	Without load
Noise	Output Noise		30	50	μV_{rms}	$10Hz < f < 100kHz$
t _{start}	Startup Time			200	μs	
V _{out}	Output Voltage	1.85		2.85	V	$V_{BAT} > 3.0V$
		1.85		3.4		Full programmable range
		2.5		3.2		For VANA_1, $V_{BAT} > 3.0V$
V _{out_tol}	Output Voltage Tolerance	-50		50	mV	
V _{LineReg}	Line Regulation	-1		1	mV	Static
		-10		10		Transient; Slope: $t_r = 10\mu s$
V _{LoadReg}	Load Regulation	-1		1	mV	Static
		-10		10		Transient; Slope: $t_r = 10\mu s$
I _{LIMIT}	Current Limitation		400		mA	VANA_1, VANA_2, VRF_1, VRF_2
			200			VRF_3, VRF_4

6.3.2 Digital Low Dropout Regulators

Digital LDOs V_{DIG_1} and V_{DIG_2} can be used in any medium-power system or subsystem where quiescent power consumption of the regulator itself needs to be minimized without sacrificing performance.

In order for the Digital LDOs to operate at full range, the Charge Pump (page 38) must be operating to provide adequate gate voltage. This requires that the Charge Pump capacitors C2 and C3 (see Figure 1 on page 2) are installed.

Figure 12. Digital LDO Block Diagram

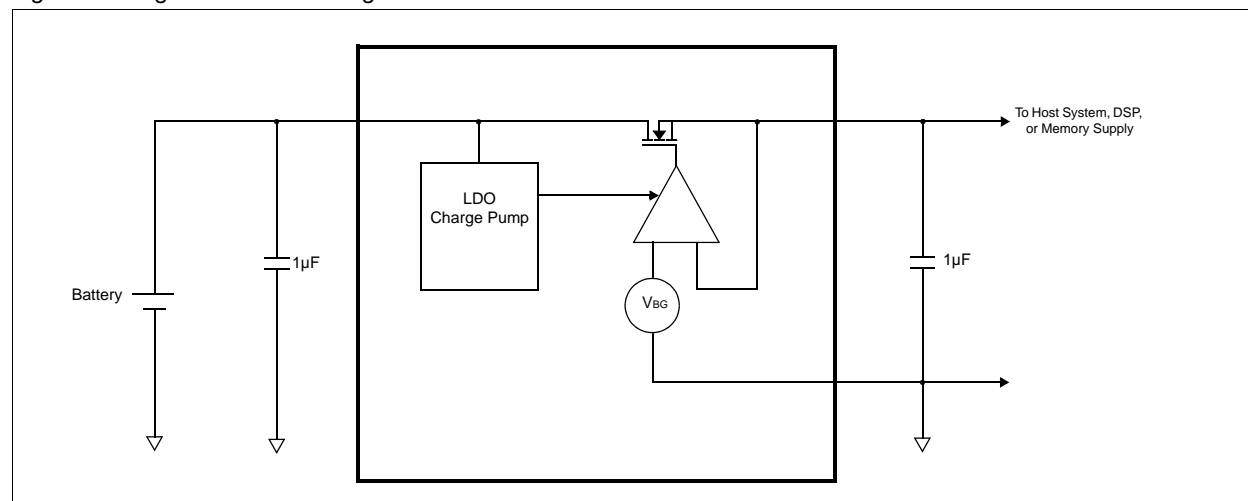


Table 11. Digital LDO Characteristics

$V_{BAT} = 4V$; $I_{LOAD} = 200mA$; $T_{AMB} = 25^{\circ}C$; $C_{LOAD} = 1\mu F$ (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VBUCK	Supply Voltage Range	1		5.5	V	
RON	On-Resistance			4	Ω	
PSRR	Power Supply Rejection Ratio	60			dB	f = 1kHz
		30				f = 100kHz
IOFF	Shut Down Current			100	nA	
IVDD	Supply Current			20	μA	Without load
tstart	Startup Time			200	μs	
Vout	Output Voltage	.75		2.2	V	$V_{BAT} > 3.0V$, $V_{5_6} = 5.2V$, $I_{load} < 200mA$
		.75		2.5		$V_{BAT} > 3.0V$, $V_{5_6} = 5.2V$, $I_{load} < 100mA$
Vout_tol	Output Voltage Tolerance	-50		50	mV	
VLineReg	Line Regulation	-10		10	mV	Static
		-50		50		Transient; Slope: $t_r = 10\mu s$
VLoadReg	Load Regulation	-20		20	mV	Static
		-50		50		Transient; Slope: $t_r = 10\mu s$
ILIMIT	Current Limitation		400		mA	

6.3.3 SIMCard Low Dropout Regulator

The SIMCard LDO (VSIM) is optimized for SIMCard supply. It is designed to achieve the lowest possible power consumption and still provide reasonable regulation characteristics. To ensure high PSRR and stability, a low-ESR ceramic capacitor of 100nF (min.) must be connected to the output.

Table 12. LDO VSIM Characteristics

$V_{BAT} = 4V$; $I_{LOAD} = 20mA$; $T_{AMB} = 25^{\circ}C$; $C_{LOAD} = 100nF$ (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VBAT	Supply Voltage Range	3		5.5	V	
RON	On-Resistance			50	Ω	
PSRR	Power Supply Rejection Ratio	40			dB	f = 1kHz
		20				f = 100kHz
IOFF	Shut Down Current			100	nA	
IVDD	Supply Current		40		μA	
tstart	Startup Time			200	μs	
Vout	Output Voltage	1.8		3.0	V	$V_{BAT} > 3.2V$
Vout_tol	Output Voltage Tolerance	-50		50	mV	
VLineReg	Line Regulation	-10		10	mV	Static
		-100		100		Transient; Slope: $t_r = 10\mu s$
VLoadReg	Load Regulation	-10		10	mV	Static
		-100		100		Transient; Slope: $t_r = 10\mu s$

6.3.4 Low Power Low Dropout Regulator

The low-power bootstrap LDO (V_{2_5}) is needed to supply power to the core (analog and digital) of the AS3603. LDO V_{2_5} is designed to achieve the lowest possible power consumption, and still provide reasonable regulation characteristics. LDO V_{2_5} has two supply inputs selecting automatically the higher one. This gives the possibility to supply the AS3603 core either with the battery or with the Battery Charger, depending on the conditions.

To ensure high PSRR and stability, a low-ESR ceramic capacitor of 1μF (min.) must be connected to the output.

Note: Levelshifters in both directions (input and output) are placed between digital pins (VANA_1) and the digital core (V_{2_5}) of the device, because of the different power supplies.

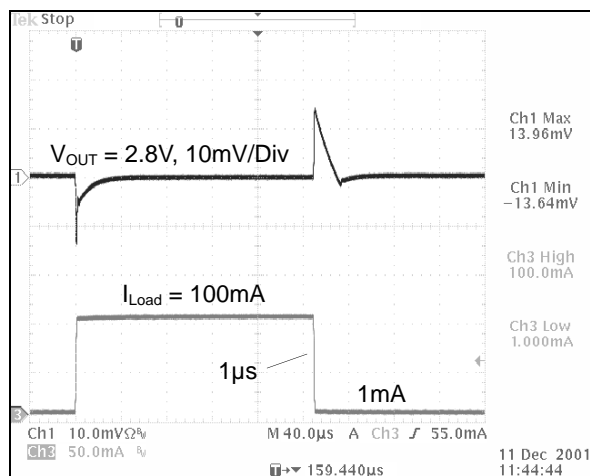
Table 13. LDO V_{2_5} Characteristics

V_{BAT} = 4V; C_{LOAD_EXT} = 0; T_{AMB} = 25°C; C_{LOAD} = 2.2μF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V _{BAT}	Supply Voltage Range	2.8		5.5	V	
V _{CHARGER}	External Charger Adapter voltage	4		15	V	
R _{ON}	On-Resistance			50	Ω	Guaranteed per design
PSRR	Power Supply Rejection Ratio	60			dB	f = 1kHz
		40				f = 100kHz
I _{OFF}	Shut Down Current			100	nA	
I _{VDD}	Supply Current			3	μA	Guaranteed per design; consider device internal load for measurement
t _{start}	Startup Time			200	μs	
V _{out}	Output Voltage	2.4	2.5	2.6	V	
V _{out_tol}	Output Voltage Tolerance	-50		50	mV	
V _{LineReg}	Line Regulation	-10		10	mV	Static
		-50		50		Transient; Slope: t _r = 10μs
V _{LoadReg}	Load Regulation	-10		10	mV	Static
		-50		50		Transient; Slope: t _r = 10μs

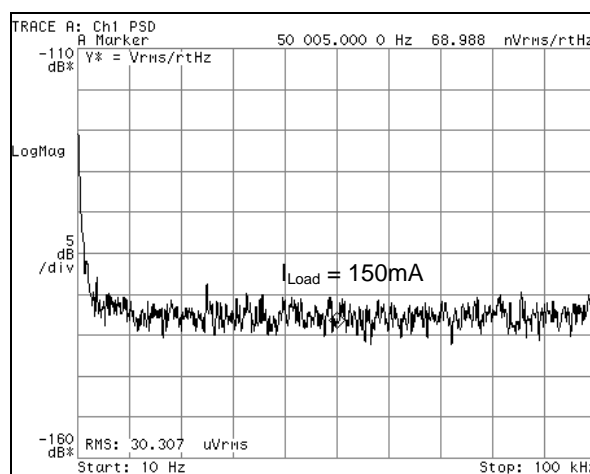
6.3.5 Typical Performance Characteristics

Figure 13. Load Regulation of LDOs VANA_1, VANA_2, VRF_1, VRF_2



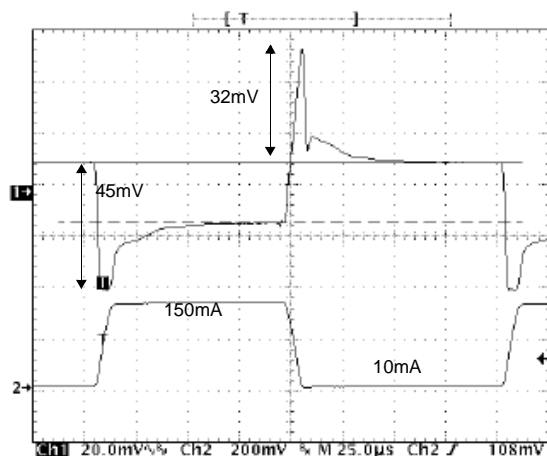
X-Axis: 40μs/Div

Figure 14. Output Noise of LDOs VANA_1, VANA_2, VRF_1, VRF_2



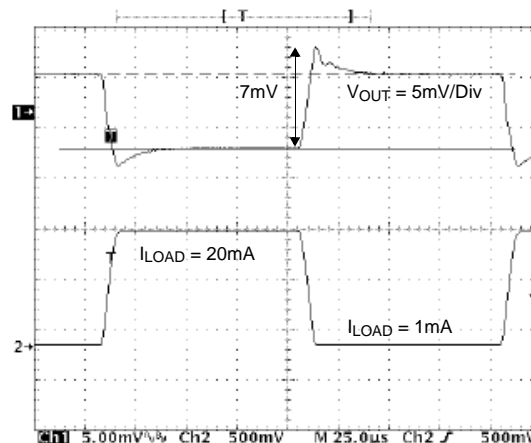
Spectral Distribution at 150mA Output Load

Figure 15. Load Regulation of LDOs VDIG_1, VDIG_2



X-Axis: 25μs/Div

Figure 16. Load Regulation of LDO V2_5



X-Axis: 25μs/Div

Figure 17. Line Regulation of LDOs VANA_1, VANA_2, VRF_1, VRF_2

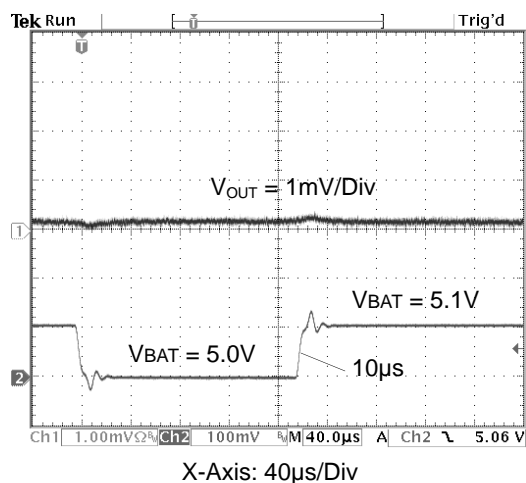
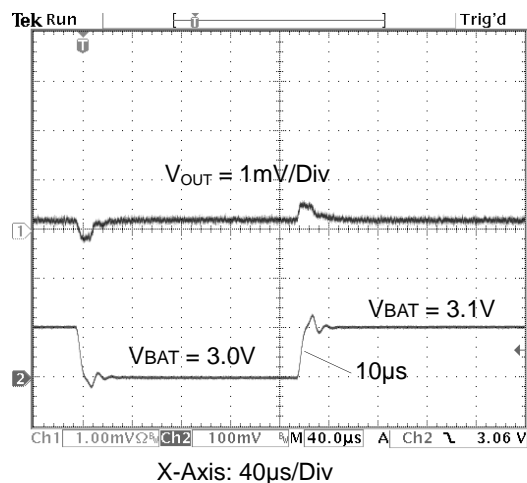


Figure 18. Line Regulation of LDOs VANA_1, VANA_2, VRF_1, VRF_2



6.3.6 LDO Registers

The Low Dropout Regulators are controlled by the registers listed in Table 14.

Table 14. Low Dropout Regulators Register Summary

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Page
LDO_RF1 Voltage Register	2	N/A			ldo_rf1_v					32
LDO_RF2 Voltage Register	3	N/A			ldo_rf2_v					33
LDO_RF3 Voltage Register	4	N/A			ldo_rf3_v					33
LDO_RF4 Voltage Register	5	N/A			ldo_rf4_v					33
LDO_ANA Voltage Register	6	ldo_ana1_v			ldo_ana2_v					33
LDO_DIG1 Voltage Register	7	N/A		ldo_dig1_v						33
LDO_DIG2 Voltage Register	8	N/A	ldo_sim_v	ldo_dig2_v						33
Reg Power Control Register	9	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	34
LDO_GPIO Active Register	15	ldo_dig2_gpio	ldo_dig1_gpio	ldo_rf4_gpio	ldo_rf3_gpio	ldo_rf2_gpio	ldo_rf1_gpio	ldo_ana2_gpio	ldo_buck_gpio	36
LDO_RF Switch Register	16	ldo_rf4_on	ldo_rf3_on	ldo_rf2_on	ldo_rf1_on	rf4_sw	rf3_sw	ana2_sw	ana1_sw	35
LDO_AD GPIO Register	17	ldo_dig2_gpio_sel		ldo_dig1_gpio_sel		ldo_ana2_gpio_sel		ldo_buck_gpio_sel		36
LDO_RF GPIO Register	18	ldo_rf4_gpio_sel		ldo_rf3_gpio_sel		ldo_rf2_gpio_sel		ldo_rf1_gpio_sel		37

Addr: 02		LDO_RF1 Voltage Register			
		Sets the voltage for LDO VRF_1.			
Bit	Bit Name	Default	Access	Bit Description	
4:0	ldo_rf1_v	Boot ROM	R/W	00000 = 1.85V ... (LSB = 50mV) 11111 = 3.40V	
7:5				N/A	

Addr: 03		LDO_RF2 Voltage Register		
		Sets the voltage for LDO V _{RF_2} .		
Bit	Bit Name	Default	Access	Bit Description
4:0	ldo_rf2_v	Boot ROM	R/W	00000 = 1.85V ... (LSB = 50mV) 11111 = 3.40V
7:5				N/A

Addr: 04		LDO_RF3 Voltage Register		
		Sets the voltage for LDO V _{RF_3} .		
Bit	Bit Name	Default	Access	Bit Description
4:0	ldo_rf3_v	Boot ROM	R/W	00000 = 1.85V ... (LSB = 50mV) 11111 = 3.40V
7:5				N/A

Addr: 05		LDO_RF4 Voltage Register		
		Sets the voltage for LDO V _{RF_4} .		
Bit	Bit Name	Default	Access	Bit Description
4:0	ldo_rf4_v	Boot ROM	R/W	00000 = 1.85V ... (LSB = 50mV) 11111 = 3.40V
7:5				N/A

Addr: 06		LDO_ANA Voltage Register		
		Sets the voltage for LDOs V _{ANA_1} and V _{ANA_2} .		
Bit	Bit Name	Default	Access	Bit Description
4:0	ldo_ana2_v	Boot ROM	R/W	Sets the voltage for LDO V _{ANA_2} . 00000 = 1.85V ... (LSB = 50mV) 11111 = 3.40V
7:5	ldo_ana1_v	Boot ROM	R/W	Sets the voltage for LDO V _{ANA_1} . 000 = 2.5V ... (LSB = 100mV) 111 = 3.2V

Addr: 07		LDO_DIG1 Voltage Register		
		Sets the voltage for Digital LDO V _{DIG_1} .		
Bit	Bit Name	Default	Access	Bit Description
5:0	ldo_dig1_v	Boot ROM	R/W	Table 15 lists the Digital LDO programmable voltages.
7:6				N/A

Addr: 08		LDO_DIG2 Voltage Register		
		Sets the voltage for Digital LDOs V _{DIG_2} and V _{SIM} .		
Bit	Bit Name	Default	Access	Bit Description
5:0	ldo_dig2_v	Boot ROM	R/W	Sets the voltage for Digital LDO V _{DIG_2} . Table 15 lists the Digital LDO programmable voltages.
6	ldo_sim_v	Boot ROM	R/W	Sets the voltage for LDO V _{SIM} . 0 = 1.8V 1 = 3.0V (default)
7				N/A

Table 15. Digital LDOs V_{DIG_1} and V_{DIG_2} Programming Voltage

Decimal Code	Binary Code	V _{out} [V]	Decimal Code	Binary Code	V _{out} [V]
0	000000	0.75	22	010110	1.80
1	000001	0.80	23	010111	1.80
2	000010	0.85	24	011000	1.80
3	000011	0.90	25	011001	1.80
4	000100	0.95	26	011010	1.80
5	000101	1.00	27	011011	1.80
6	000110	1.05	28	011100	1.80
7	000111	1.10	29	011101	1.80
8	001000	1.15	30	011110	1.80
9	001001	1.20	31	011111	1.80
10	001010	1.25	32	100000	1.50
11	001011	1.30	33	100001	1.60
12	001100	1.35	34	100010	1.70
13	001101	1.40	35	100011	1.80
14	001110	1.45	36	100100	1.90
15	001111	1.50	37	100101	2.00
16	010000	1.55	38	100110	2.10
17	010001	1.60	39	100111	2.20
18	010010	1.65	40	101000	2.30
19	010011	1.70	41	101001	2.40
20	010100	1.75	42	101010	2.50
21	010101	1.80	-	-	-

Note: Full performance for V_{out} ≤ 2.20V (max.), 100mA output current for V_{out} ≤ 2.50V.

Caution: Do not use values for V_{out} > 2.50V.

Addr: 09		Reg Power Control Register			
		Enables/disables voltage regulators.			
Bit	Bit Name	Default	Access	Bit Description	
0	ldo_ana1_on	Boot ROM	R/W	Enables control of LDO V _{ANA_1} . 0 = LDO V _{ANA_1} is off. 1 = LDO V _{ANA_1} is on. Note: Do not set this bit = 0 or serial interface access will be disabled.	
1	ldo_ana2_on	Boot ROM	R/W	Enables control of LDO V _{ANA_2} . 0 = LDO V _{ANA_2} is off. 1 = LDO V _{ANA_2} is on.	
2	ldo_dig1_on	Boot ROM	R/W	Enables control of LDO V _{DIG_1} . 0 = LDO V _{DIG_1} is off. 1 = LDO V _{DIG_1} is on.	
3	ldo_dig2_on	Boot ROM	R/W	Enables control of LDO V _{DIG_2} . 0 = LDO V _{DIG_2} is off. 1 = LDO V _{DIG_2} is on.	
4	ldo_sim_on	Boot ROM	R/W	Enables control of LDO V _{SIM} . 0 = LDO V _{SIM} is off. 1 = LDO V _{SIM} is on.	
5	buck_on			Refer to page 25.	
7:6				N/A	

Addr: 16		LDO_RF Switch Register		
		Enables LDOs as high-side switches.		
Bit	Bit Name	Default	Access	Bit Description
0	ana1_sw	Boot ROM	R/W	0 = Vana_1 operates as LDO. 1 = VANA_1 is operating as high-side switch ($R_{on} = 1\Omega$); valid if ldo_rf1_on = 0.
1	ana2_sw	Boot ROM	R/W	0 = Vana_2 operates as LDO. 1 = VANA_2 is operating as high-side switch ($R_{on} = 1\Omega$); valid if ldo_rf2_on = 0.
2	rf3_sw	Boot ROM	R/W	0 = VRF_3 operates as LDO. 1 = LDO VRF_3 is operating as high-side switch ($R_{on} = 2\Omega$); valid if ldo_rf3_on = 0.
3	rf4_sw	Boot ROM	R/W	0 = VRF_4 operates as LDO. 1 = LDO VRF_4 is operating as high-side switch ($R_{on} = 2\Omega$); valid if ldo_rf4_on = 0.
4	ldo_rf1_on	Boot ROM	R/W	Enables control of LDO VRF_1. Set ana1_sw = 0 before setting this bit = 1. 0 = LDO VRF_1 is off. 1 = LDO VRF_1 is on.
5	ldo_rf2_on	Boot ROM	R/W	Enables control of LDO VRF_2. Set ana2_sw = 0 before setting this bit = 1. 0 = LDO VRF_2 is off. 1 = LDO VRF_2 is on.
6	ldo_rf3_on	Boot ROM	R/W	Enables control of LDO VRF_3. Set rf3_sw = 0 before setting this bit = 1. 0 = LDO VRF_3 is off. 1 = LDO VRF_3 is on.
7	ldo_rf4_on	Boot ROM	R/W	Enables control of LDO VRF_4. Set rf4_sw = 0 before setting this bit = 1. 0 = LDO VRF_4 is off. 1 = LDO VRF_4 is on.

ldo_rfx_on*	rfx:sw*	RF LDO Function
0	0	Off
0	1	Fully On, $R_{on} = 1$ or 2Ω
1	0	Linear Voltage Regulator
1	1	Not Allowed

* Where x = 1-4

Addr: 15		LDO_GPIO Active Register		
		Activates GPIO on/off control for voltage regulators.		
Bit	Bit Name	Default	Access	Bit Description
0	buck_gpio	Boot ROM	R/W	Activates GPIO control of Step Down DC/DC Converter. 0 = Controlled by software. 1 = On when assigned GPIO pin = 1 and bit buck_on (page 25) = 1.
1	ldo_ana2_gpio	Boot ROM	R/W	Activates GPIO control for LDO VANA_2. 0 = Controlled by software. 1 = On when assigned GPIO pin = 1 and bit ldo_ana2_on (page 34) = 1.
2	ldo_rf1_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_1. 0 = Controlled by software. 1 = On when assigned GPIO pin = 1 and bit ldo_rf1_on (page 35) = 1.
3	ldo_rf2_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_2. 0 = Controlled by software. 1 = On when assigned GPIO pin = 1 and bit ldo_rf2_on (page 35) = 1.
4	ldo_rf3_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_3. 0 = Controlled by software. 0 = On when assigned GPIO pin = 1 and bit ldo_rf3_on (page 35) = 1.
5	ldo_rf4_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_4. 0 = Controlled by software. 1 = LDO VRF_4 is on when assigned GPIO pin = 1 and bit ldo_rf4_on (page 35) = 1.
6	ldo_dig1_gpio	Boot ROM	R/W	Activates GPIO control for LDO VDIG_1. 0 = Controlled by software. 1 = On when assigned GPIO pin = 1 and bit ldo_dig1_on (page 34) = 1.
7	ldo_dig2_gpio	Boot ROM	R/W	Activates GPIO control for LDO VDIG_2. 0 = Controlled by software. 1 = On when assigned GPIO pin = 1 and bit ldo_dig2_on (page 34) = 1.

Addr: 17		LDO_AD GPIO Register		
		Selects GPIO pin for power on/off control.		
Bit	Bit Name	Default	Access	Bit Description
1:0	buck_gpio_sel	Boot ROM	R/W	Valid if GPIO activation bit buck_gpio (page 36) = 1. 00 = GPIO1 01 = GPIO2 – this setting cannot be selected when GPIO2 is used as feedback pin. 10 = GPIO3 11 = GPIO4
3:2	ldo_ana2_gpio_sel	Boot ROM	R/W	Valid if GPIO activation bit ldo_ana2_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4
5:4	ldo_dig1_gpio_sel	Boot ROM	R/W	Valid if GPIO-activation bit ldo_dig1_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4
7:6	ldo_dig2_gpio_sel	Boot ROM	R/W	Valid if GPIO-activation bit ldo_dig2_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4

Addr: 18		LDO_RF GPIO Register		
		Selects GPIO pin for power on/off control for RF LDOs VRF_1 - VRF_4.		
Bit	Bit Name	Default	Access	Bit Description
1:0	ldo_rf1_gpio_sel	Boot ROM	R/W	Valid if ldo_rf1_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4
3:2	ldo_rf2_gpio_sel	Boot ROM	R/W	Valid if ldo_rf2_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4
5:4	ldo_rf3_gpio_sel	Boot ROM	R/W	Valid if ldo_rf3_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4
7:6	ldo_rf4_gpio_sel	Boot ROM	R/W	Valid if ldo_rf4_gpio (page 36) = 1. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4

6.4 Charge Pump

The Charge Pump uses VANA_1 (supplied by Analog LDO VANA_1) as input and doubles this voltage using a flying capacitor between pins CAPP and CAPN (see Figure 1 on page 2) to its output, V5_6. If bit **cp_pulseskip** (page 38) is set, the Charge Pump compares its output voltage against a voltage reference, defined by **cp_vref** (page 38), and only starts charging cycles if its output voltage is below **cp_vref**. If V5_6 is > 5.6V (when VANA_1 is > 2.8V), pulseskip will automatically be enabled (depending on bit **cp_vref**) to protect the pin from overvoltage (bit **cp_pulseskip** will not be set in this case).

The Charge Pump requires the external components specified in Table 16.

Table 16. Charge Pump External Components

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Cfly (C2)	External Flying Capacitor		330		nF	Ceramic low-ESR capacitor between pins CAPP and CAPN (page 2).
Cstore (C3)	External Storage Capacitor	1		4.7	μF	Ceramic low-ESR capacitor between pins V5_6 and Vss (page 2).

Note: Connections to the two external capacitors should be kept as short as possible.

Table 17. Charge Pump Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
ICPOUT	Output Current	0		30	mA	VANA_1 = 2.8V, internal clock selected, cp_vref (page 38) = 5.25V or cp_pulseskip = 0.
VCPOUT	Output Voltage	5.0	5.2	5.6	V	
VCPOUTi0	Output Voltage (No Load)	2 x VANA_1				VANA_1 ≥ 2.0V, no load at output, cp_pulseskip = 0.
IQUIESCENT	Quiescent Current		980		μA	cp_pulseskip = 0, cp_freq (page 38) = 0 (1.1MHz).
			498			cp_pulseskip = 0, cp_freq = 1 (550kHz).
			5			cp_pulseskip = 1, cp_freq = 0, VANA_1 = 2.8V.
			4			cp_pulseskip = 1, cp_freq = 1, VANA_1 = 2.8V.
ISHUTDOWN	Shutdown Current			0.1	μA	@25°C
VRIPPLE	Ripple Voltage		28.8		mVp-p	cp_pulseskip = 0, cp_freq = 0, ILOAD = 30mA.

6.4.1 Charge Pump Control Register

Addr: 24		Charge Pump Control Register		
		Sets the operation mode of the Charge Pump.		
Bit	Bit Name	Default	Access	Bit Description
0	cp_on	Boot ROM	R/W	0 = Charge Pump is off. 1 = Activates the Charge Pump. The Charge Pump is automatically activated when any of the following blocks are active: Audio Amplifier, VDIG_1, VDIG_2.
1	cp_pulseskip	Boot ROM	R/W	Controls the Charge Pump pulseskip mode. 0 = Always try to double the voltage on VANA_1. 1 = Only start a cycle if V5_6 is lower than the voltage defined by bit cp_vref .
2	cp_vref	Boot ROM	R/W	If in pulseskip mode, regulate to the following voltage by leaving out complete cycles: 0 = 4.74V 1 = 5.25V
3				N/A
4	cp_freq	Boot ROM	R/W	Sets the Charge Pump clock frequency. 0 = System clock 1 = System clock/2 (half frequency)
5	onkey_pulldown			Controls the pulldown on pin ON. 0 = Switches on the pulldown on pin ON. 1 = Switches off the pulldown on pin ON.
7:6				N/A

6.5 Step Up DC/DC Converter

The integrated Step Up DC/DC Converter is a high-efficiency current-mode PWM regulator, providing an output voltage of up to 15V. A constant switching-frequency results in low noise on supply and output voltages. An optional digital NMOS switch is provided for cases when the Step Up DC/DC Converter is not used.

Figure 19. Step Up DC/DC Converter Block Diagram

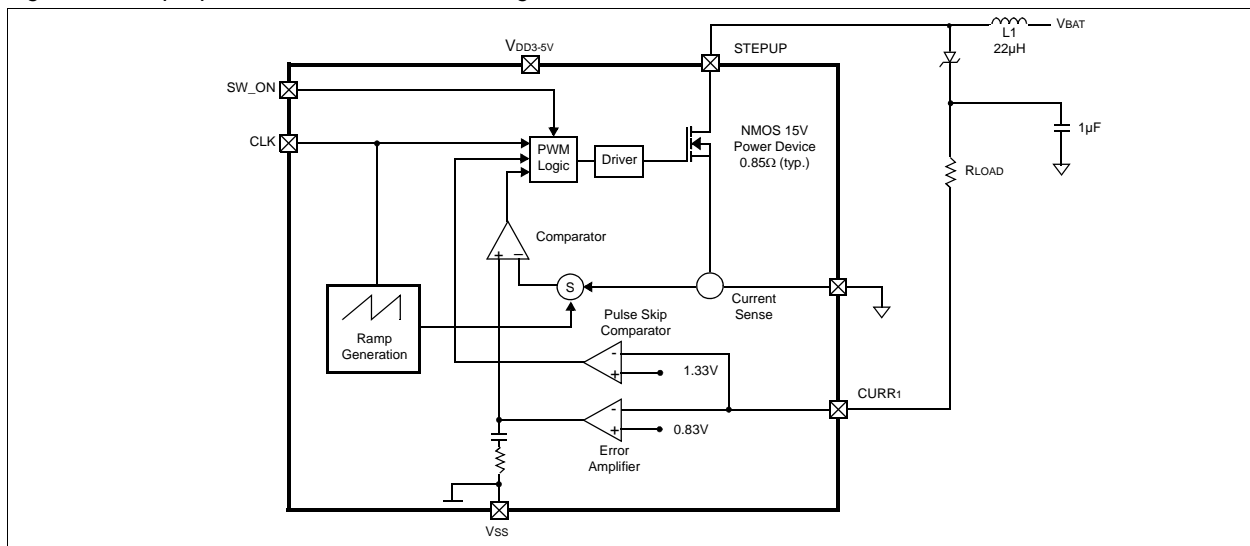


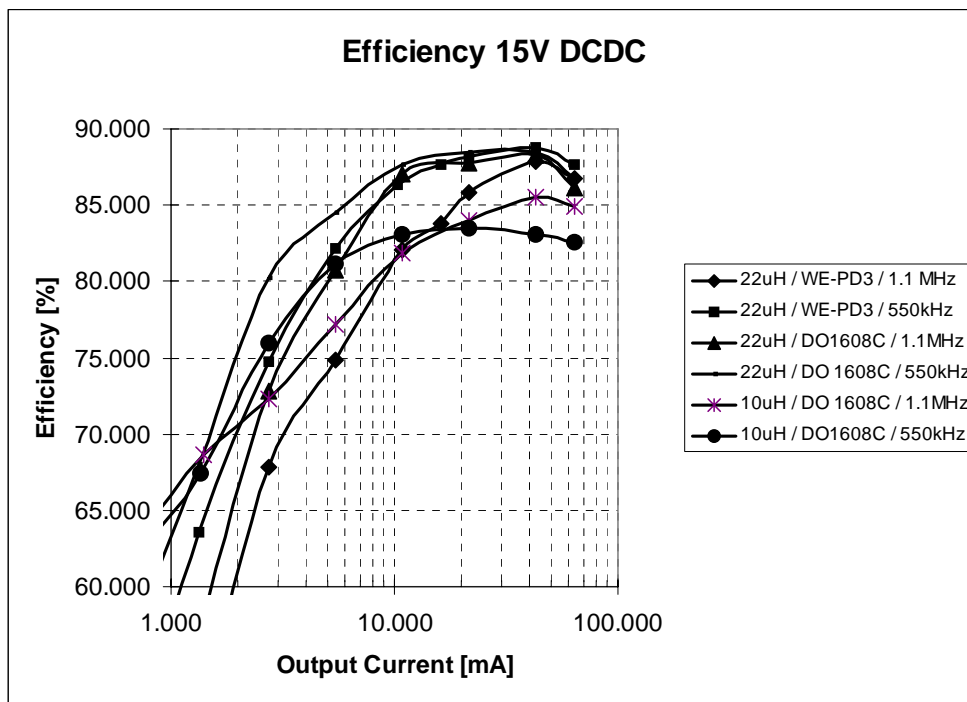
Table 18. Step Up DC/DC Converter Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VSW	High Voltage Pin	0		15	V	Pin STEPUP
IVDD	Quiescent Current		140		μA	Pulse skipping mode
ISHUTDOWN	Shutdown Current			100	nA	@25°C
VFB	Feedback Voltage, Transient	0		5.5	V	Pin CURR1
VFB	Feedback Voltage during Regulation	0.65	0.83	1.0	V	Pin CURR1
ISW_max	Current Limit	550	780	1100	mA	stpup_on (page 40) = 1 stpup_low_curr (page 40) = 0
		350	510	750	mA	stpup_on = 1, stpup_low_curr = 1
RSW	Switch Resistance		0.85	1.54	Ω	stpup_on = 0, stpup_low_curr = 1
ILOAD	Load Current	0		45	mA	At 15V output voltage.
Vpulseskip	Pulseskip Threshold	1.2	1.33	1.5	V	PIN CURR1. Note: Voltage at pin CURR1, pulse skips are introduced when load current becomes too low.
VRIPPLE	Ripple Voltage		146		mVp-p	stpup_freq = 0, VOUT = 15V, ILOAD = 45mA, BW ≤ 20MHz.
fIN	Fixed Switching Frequency	1	1.1	1.2	MHz	1.1MHz; stpup_freq (page 40) = 0
		0.5	0.55	0.6		0.55MHz; stpup_freq = 1
Cout	Output Capacitor		1		μF	Ceramic
L (Inductor)	ILOAD > 20mA	17	22	27	μH	Use inductors with small Cparasitic (<100pF) for high efficiency.
	ILOAD < 20mA	8	10	27		
tMIN_ON	Minimum On-Time	90		180	ns	
MDC	Maximum Duty Cycle	88	91	94	%	Guaranteed per design.

6.5.1 Step Up DC/DC Converter Register

Addr: 25		Step Up DC/DC Converter Control Register		
		Sets the operation mode of the Step Up DC/DC Converter.		
Bit	Bit Name	Default	Access	Bit Description
0	stpup_on	Boot ROM	R/W	Activates the Step Up DC/DC Converter. 0 = Step Up DC/DC Converter is off. 1 = Step Up DC/DC Converter is on.
1	stpup_sw_on	Boot ROM	R/W	This bit controls the NMOS switch on pin STEPUP only if stpup_on = 0. 0 = Switch open (STEPUP floating). 1 = Switch closed (STEPUP pulled to Vss).
2	stpup_freq	Boot ROM	R/W	Defines the clock frequency of the Step Up DC/DC Converter. 0 = System clock (typ. 1.1MHz). 1 = System clock/2 (half frequency).
3	stpup_low_curr	Boot ROM	R/W	NMOS-switch current-limit control only if stpup_on = 1. 0 = High current limit (600mA). 1 = Low current limit (300mA).
7:4				N/A

Figure 20. Typical Performance Characteristics



6.6 General Purpose Input/Output

The general purpose input/output pins (GPIO1 - GPIO4) are highly configurable and independently controlled.

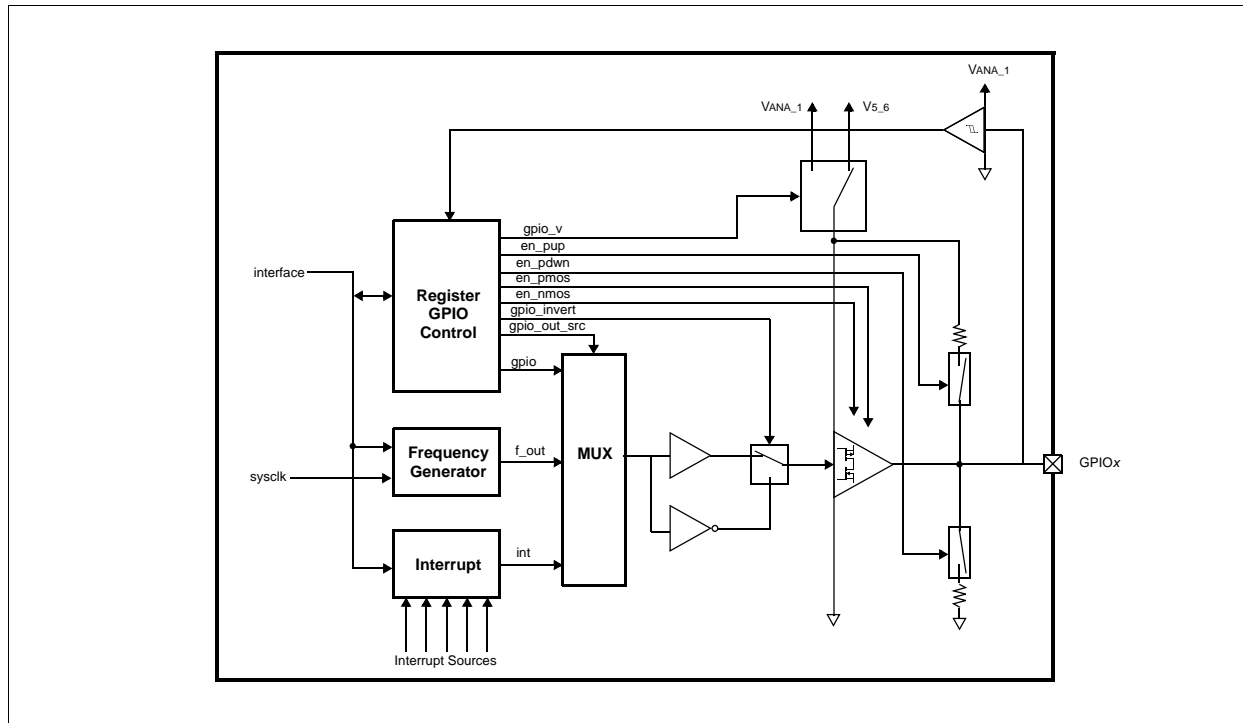
Table 19. DC Characteristics Input/Output Pin with Selectable Supply GPIO1:GPIO4

Parameter	Symbol	Min	Max	Unit	Notes
High-Level Input Voltage	V_{IH}	$0.7 \times V_{ANA_1}$		V	
Low-Level Input Voltage	V_{IL}		$0.3 \times V_{ANA_1}$	V	
Hysteresis	V_{HYS}	$0.2 \times V_{ANA_1}$		V	
Input Leakage Current (if not used as pulldown/pullup)	I_{LEAK}	-5	5	μA	to V_{ANA_1} and V_{SS}
Pulldown Current (if configured as pulldown)	$I_{PULLDOWN}$	5	50	μA	to V_{SS}
Pullup Current (if configured as pullup)	I_{PULLUP}	-200	-20	μA	to V_{5_6} or V_{ANA_1} as configured
High-Level Output Voltage Supply V_{ANA_1}	V_{OH}	$0.8 \times V_{ANA_1}$		V	at -2mA
High-Level Output Voltage Supply V_{5_6} (V_{5_6} min. 5.0V)	V_{OHHV}	$0.8 \times V_{5_6}$		V	at -2mA
Low-Level Output Voltage	V_{OL}		$0.2 \times V_{ANA_1}$	V	at 2mA
Capacitive Load	CL		50	pF	

GPIO1 - GPIO4 can be used to accommodate the following functionality:

- Software controlled input and output
- Input pin for the Watchdog
- Signal input (GPIO1-GPIO4)
- Interrupt output with configurable interrupt source
- Configurable frequency and duty cycle output
- External clock input for Step Up/Down DC/DC Converters and Charge Pump synchronization (GPIO1 only)
- Active pullup or pulldown; can be combined with other I/O functions
- Output open drain (push or pull type)
- Output high-level voltage selection between V_{5_6} or V_{ANA_1} ; (V_{5_6} not possible on GPIO2)
- Optional feedback input for Step Down DC/DC Converter (GPIO2)

Figure 21. General Purpose I/O Block Diagram



6.6.1 GPIO Registers

GPIO1 - GPIO4 are controlled by the registers listed in Table 20.

Table 20. GPIO Register Summary

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Page
GPIO1 Control Register	26	gpio1_out_src	gpio1_invert	gpio1_pulls	gpio1_voltage	gpio1_mode				43
GPIO2 Control Register	27	gpio2_out_src	gpio2_invert	gpio2_pulls	stepdown_fb	gpio2_mode				43
GPIO3 Control Register	28	gpio3_out_src	gpio3_invert	gpio3_pulls	gpio3_voltage	gpio3_mode				44
GPIO4 Control Register	29	gpio4_out_src	gpio4_invert	gpio4_pulls	gpio4_voltage	gpio4_mode				44
GPIO Signal Register	33	N/A				gpio4	gpio3	gpio2	gpio1	45
GPIO Frequency Control High Time Register	34	gpio_h_time								45
GPIO Frequency Control Low Time Register	35	gpio_l_time								45
Clock Generation Register	30	N/A							ext_clk	45
Interrupt Enable Register	31	N/A			chdet_int_en	onkey_int_en	ovtmp_int_en	vchoff_int_en	wdog_int_en	47
Interrupt Status Register	32	N/A			chdet_i	onkey_i	ovtmp_i	vchoff_i	wdog_i	47

Addr: 26		GPIO1 Control Register		
		Configures pin GPIO1.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio1_mode	Boot ROM	R/W	Sets the direction for pin GPIO1. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11 = Output (open drain, only pull; only PMOS is active).
2	gpio1_voltage	Boot ROM	R/W	If pin GPIO1 is used as output, sets the positive supply (V _{SS} is always used as negative supply). 0 = V _{ANA_1} 1 = V _{5_6}
4:3	gpio1_pulls	Boot ROM	R/W	Sets pullup/pulldown to pin GPIO1 (independent of bit gpio1_mode setting). 00 = None 01 = Pulldown 10 = Pullup 11 = N/A
5	gpio1_invert	Boot ROM	R/W	0 = Output signal is not inverted. 1 = Inverts any output signal going to GPIO1. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio1_out_src	Boot ROM	R/W	Sets the source of pin GPIO1 output. x0 = Bit gpio1 (page 45) controlled through the serial interface. 01 = Frequency generator defined by bits gpio_h_time (page 45) and gpio_l_time (page 45). 11 = Interrupt signal (see Interrupt Function on page 47).

Addr: 27		GPIO2 Control Register		
		Configures pin GPIO2.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio2_mode	Boot ROM	R/W	Sets the direction for pin GPIO2. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11 = Output (open drain, only pull; only PMOS is active).
2	stepdown_fb	Boot ROM	R/W	0 = GPIO2 is used as regulator configurable I/O pin, Step Down DC/DC Converter feedback is at pin V _{Buck} . 1 = Pin GPIO2 is used as feedback-pin for Step Down DC/DC Converter.
4:3	gpio2_pulls	Boot ROM	R/W	Sets pullup/pulldown to pin GPIO2 (independent of bit gpio2_mode setting). 00 = None 10 = Pullup 01 = Pulldown 11 = N/A
5	gpio2_invert	Boot ROM	R/W	0 = Output signal is not inverted. 1 = Inverts any output signal going to pin GPIO2. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio2_out_src	Boot ROM	R/W	Sets the source of pin GPIO2 output. x0 = Bit gpio2 (page 45) (controlled through the serial interface). 01 = Frequency generator defined by bits gpio_h_time (page 45) and gpio_l_time (page 45). 11 = Interrupt signal (see Interrupt Function on page 47).

Addr: 28		GPIO3 Control Register		
		Configures pin GPIO3.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio3_mode	Boot ROM	R/W	Sets the direction for pin GPIO3. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11 = Output (open drain, only pull; only PMOS is active).
3:2	gpio3_voltage	Boot ROM	R/W	If pin GPIO3 is used as output, sets the positive supply (V _{SS} is always used as negative supply). 0 = V _{ANA_1} 1 = V _{5_6}
4	gpio3_pulls	Boot ROM	R/W	Sets pullup/pulldown to pin GPIO3 (independent of bit gpio3_mode setting). 00 = None 10 = Pullup 01 = Pulldown 11 = N/A
5	gpio3_invert	Boot ROM	R/W	0 = Output signal is not inverted. 1 = Inverts any output signal going to pin GPIO3. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio3_out_src	Boot ROM	R/W	Sets the source of pin GPIO3. x0 = Bit gpio3 (page 45) (controlled through the serial interface) 01 = Frequency generator defined by bits gpio_h_time (page 45) and gpio_l_time (page 45). 11 = Interrupt signal (see Interrupt Function on page 47).

Addr: 29		GPIO4 Control Register		
		Configures pin GPIO4.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio4_mode	Boot ROM	R/W	Sets the direction for the GPIO4. 00 = Input only. 01 = Output (push and pull). 10 = Output (open drain, only push; only NMOS is active). 11 = Output (open drain, only pull; only PMOS is active).
2	gpio4_voltage	Boot ROM	R/W	If GPIO4 is used as output, sets the positive supply (V _{SS} is always used as negative supply). 0 = V _{ANA_1} 1 = V _{5_6}
4:3	gpio4_pulls	Boot ROM	R/W	Sets pullup/pulldown to pin GPIO4 (independent of gpio4_mode setting). 00 = None 10 = Pullup 01 = Pulldown 11 = N/A
5	gpio4_invert	Boot ROM	R/W	0 = Output signal is not inverted. 1 = Inverts any output signal going to pin GPIO4. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio4_out_src	Boot ROM	R/W	Sets the source of pin GPIO4. x0 = Bit gpio4 (page 45) (controlled through the serial interface). 01 = Frequency generator defined by bits gpio_h_time (page 45) and gpio_l_time (page 45). 11 = Interrupt signal (see Interrupt Function on page 47).

Addr: 33		GPIO Signal Register		
		Reads the logic signal of the GPIO pins, independently of any other GPIO bit setting.		
Bit	Bit Name	Default	Access	Bit Description
0	gpio1	N/A	R/W	Reads the logic signal from pin GPIO1. If gpio1_out_src (page 43) = 00, this is the output signal at pin GPIO1.
1	gpio2	N/A	R/W	Reads the logic signal from pin GPIO2. If gpio2_out_src (page 43) = 00, this is the output signal at pin GPIO2.
2	gpio3	N/A	R/W	Reads the logic signal from pin GPIO3. If gpio3_out_src (page 44) = 00, this is the output signal at pin GPIO3.
3	gpio4	N/A	R/W	Reads the logic signal from pin GPIO4. If gpio4_out_src (page 44) = 00, this is the output signal at pin GPIO4.
7:4				N/A

6.6.2 Programmable Frequency Generator

The Programmable Frequency Generator is controlled by bits **gpio_h_time** (page 45) and **gpio_l_time** (page 45). It generates a waveform with 0.9 microseconds times **gpio_h_time** high-level and 0.9 microseconds times **gpio_l_time** low-level. The accuracy of these timings is $\pm 10\%$.

The frequency of the Programmable Frequency Generator is:

$$f = 1 / (tclk * gpio_h_time + tclk * gpio_l_time) \quad (EQ\ 8)$$

where $tclk = 1/fclk$ (page 16) = $1/1.1\text{MHz}$ (typ.) = $0.909\mu\text{s}$ (typ.)

The purpose of the Programmable Frequency Generator is to have a controlled sweepable frequency or duty cycle source for one of the following:

- General User-Defined Clock
- 8-Bit DAC (output should be filtered by an RC filter)
- (High) Positive and Negative Voltage Generation (see 25V/-20V Voltage Generator on page 46)

6.6.3 Programmable Frequency Generator Registers

Addr: 34		GPIO Frequency Control High Time Register		
		Configures programmable frequency generator.		
Bit	Bit Name	Default	Access	Bit Description
7:0	gpio_h_time	64 _h	R/W	Defines the number of system clock cycles (typ. 0.9 μs), that the programmable frequency generator at the GPIO output(s) is high. 00 _h = 0.909 μs FF _h = 232.7 μs

Addr: 35		GPIO Frequency Control Low Time Register		
		Configures programmable frequency generator.		
Bit	Bit Name	Default	Access	Bit Description
7:0	gpio_l_time	64 _h	R/W	Defines the number of system clock cycles (typ. 0.9 μs), that the programmable frequency generator at the GPIO output(s) is low. 00 _h = 0.909 μs FF _h = 232.7 μs

Addr: 30		Clock Generation Register		
		Sets the source for the system clock.		
Bit	Bit Name	Default	Access	Bit Description
0	ext_clk	Boot ROM	R/W	0 = Internal 1.1MHz RC-oscillator. 1 = System clock controlled by pin GPIO1.
7:1				N/A

6.6.4 25V/-20V Voltage Generator

Using the Programmable Frequency Generator a voltage generator for +25V or -20V can be built with only 4 external capacitors and 5 external Shottky diodes as shown in the following diagrams.

Figure 22. 25V Positive Voltage Generator Block Diagram

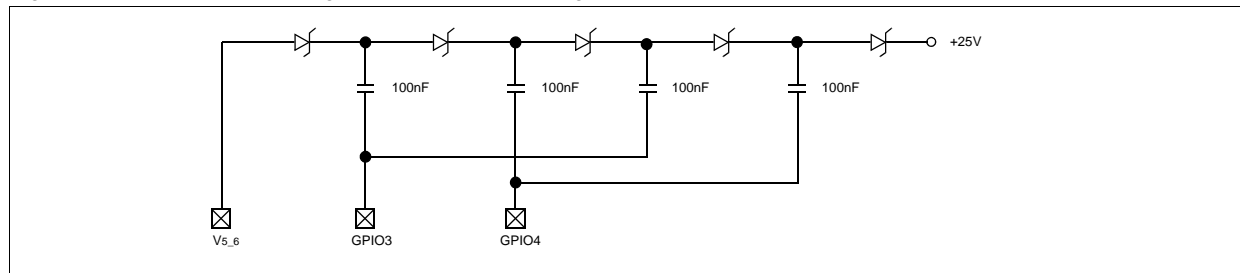
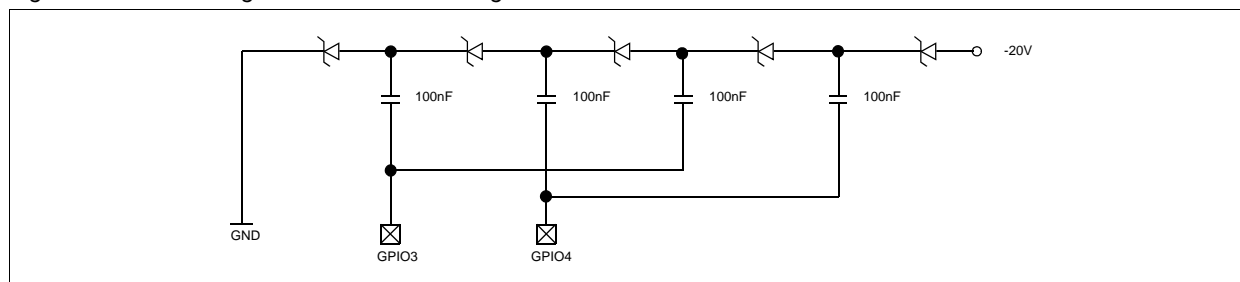


Figure 23. -20V Voltage Generator Block Diagram



Note: GPIO3 and GPIO4 must be 180° out of phase, e.g., set bit `gpio3_invert` (page 44) = 1 and bit `gpio4_invert` (page 44) = 0.

6.6.5 Interrupt Function

Any of the GPIO pins (GPIO1 - GPIO4) can be configured as interrupt output pins. To enable this function, the corresponding GPIO control bits must be set to 1b. See **gpio1_out_src** (page 43), **gpio2_out_src** (page 43), **gpio3_out_src** (page 44), or **gpio4_out_src** (page 44).

Several signals can be configured as interrupt source using the **Interrupt Enable Register**. A rising edge of an enabled interrupt control signal sets the selected GPIO interrupt output pin = 1.

The **Interrupt Status Register** shows the currently active interrupt signals. Reading this register resets the **Interrupt Status Register** bits and sets the active GPIO pin (GPIO 1 - GPIO4) = 0.

6.6.6 Interrupt Registers

Addr: 31		Interrupt Enable Register		
		Enables/disables interrupt sources.		
Bit	Bit Name	Default	Access	Bit Description
0	wdog_int_en	Boot ROM	R/W	0 = Disables watchdog alarm as interrupt source signal. 1 = Enables watchdog alarm as interrupt source signal.
1	vchoff_int_en	Boot ROM	R/W	0 = Disables charge termination voltage as interrupt source signal. 1 = Enables charge termination voltage as interrupt source signal.
2	ovtmp_int_en	Boot ROM	R/W	0 = Disables ov_temp_110 (device temperature alert at 110°C). 1 = Enables ov_temp_110 (device temperature alert at 110°C).
3	onkey_int_en	Boot ROM	R/W	0 = Disables pin ON (active high). 1 = Enables pin ON (active high).
4	chdet_int_en	Boot ROM	R/W	0 = Disables charger detection. 1 = Enables charger detection.
7:5				N/A

Addr: 32		Interrupt Status Register		
		Displays the status of the interrupt inputs.		
Bit	Bit Name	Default	Access	Bit Description
0	wdog_i	Boot ROM	R/W	0 = Software or hardware watchdog is off or has not rolled over. 1 = Software or hardware watchdog is rollover.
1	vchoff_i	Boot ROM	R/W	0 = Battery voltage is below VCHOFF (page 9) threshold. 1 = Battery voltage has reached VCHOFF threshold.
2	ovtmp_i	Boot ROM	R/W	0 = Device temperature is below 110°C. 1 = 110°C temperature threshold ov_temp_110 (page 57) has been reached.
3	onkey_i	Boot ROM	R/W	0 = ON key has not been pressed. 1 = ON key has been pressed (rising edge).
4	chdet_i	Boot ROM	R/W	Charger detection interrupt, active if bit chDet (page 19) = 1. 0 = No charger detected. 1 = External charger has been detected.
7:5				N/A

6.7 Current Sinks

The AS3603 contains general purpose current sinks intended to control backlights, buzzers, and vibrators. All current sinks have an integrated protection (V_{PROTECT}) against overvoltage and can therefore also drive inductive loads. CURR1 is also used as feedback for Step Up DC/DC Converter and in this configuration regulated to 0.8V.

The current sinks can also be used as switches to V_{ss} with configurable impedance as indicated in Table 21.

Table 21. Current Source Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I _{currx}	curr _x _current = 01 _h - FF _h	0.625		160	mA	curr _x _sw = 0, resolution = 0.625mA
R _{PD_SW}	curr _x _current = 01 _h - FF _h	0.3		77	Ω	curr _x _sw = 1, 00 _h = open, resolution = 0.3Ω
V _{PROTECT}	Maximum voltage at pin curr _x to protect driver transistor			V _{BAT} +2.0V	V	I _{SINK} ≥ 20mA (1)

Note: If a voltage higher than V_{PROTECT} is applied to pins CURR1 - CURR4, a current of more than 20mA will flow into the AS3603. This protects the device from voltage rises caused by inductive loads.

6.7.1 Current Sink Registers

The current sinks are controlled by the registers listed in Table 22.

Table 22. Current Sink Register Summary

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Page
CURR1 Value Register	36	curr1_current								48
CURR2 Value Register	37	curr2_current								48
CURR3 Value Register	38	curr3_current								49
CURR4 Value Register	39	curr4_current								49
CURR Control Register	40	curr4_ctrl		curr3_ctrl		curr2_ctrl		curr1_ctrl		49
CURR Mode Register	41	N/A				curr4_sw	curr3_sw	curr2_sw	curr1_sw	49
CURR GPIO Map Register	42	curr4_gpio		curr3_gpio		curr2_gpio		curr1_gpio		50

Addr: 36		CURR1 Value Register								
		Sets the current / resistance of current source CURR1.								
Bit	Bit Name	Default	Access	Bit Description						
7:0	curr1_current	00 _h	R/W	00 _h 01 _h ... FF _h	curr1_sw (page 49) = 0 Power Down 0.625mA ... 160mA		curr1_sw = 1 Open 77Ω ... 0.3Ω			

Addr: 37		CURR2 Value Register								
		Sets the current / resistance of current source CURR2.								
Bit	Bit Name	Default	Access	Bit Description						
7:0	curr2_current	00 _h	R/W	00 _h 01 _h ... FF _h	curr2_sw (page 49) = 0 Power Down 0.625mA ... 160mA		curr2_sw = 1 Open 77Ω ... 0.3Ω			

Addr: 38		CURR ₃ Value Register				
		Sets the current / resistance of current source CURR ₃ .				
Bit	Bit Name	Default	Access	Bit Description		
7:0	curr3_current	00 _h	R/W	00 _h 01 _h ... FF _h	curr3_sw (page 49) = 0 Power Down 0.625mA ... 160mA	curr3_sw = 1 Open 77Ω ... 0.3Ω

Addr: 39		CURR ₄ Value Register				
		Sets the current / resistance of current source CURR ₄ .				
Bit	Bit Name	Default	Access	Bit Description		
7:0	curr4_current	00 _h	R/W	00 _h 01 _h ... FF _h	curr4_sw (page 49) = 0 Power Down 0.625mA ... 160mA	curr4_sw = 1 Open 77Ω ... 0.3Ω

Addr: 40		CURR Control Register				
		Selects software/ hardware control of current sources.				
Bit	Bit Name	Default	Access	Bit Description		
1:0	curr1_ctrl	00b	R/W	00 = Pin CURR ₂ is turned off. 01 = Pin CURR ₂ is active. 1x = GPIO control; pin is active when curr1_gpio (page 50) = 1.		
3:2	curr2_ctrl	00b	R/W	00 = Pin CURR ₂ is turned off. 01 = Pin CURR ₂ is active. 1x = GPIO control; pin is active when curr2_gpio (page 50) = 1.		
5:4	curr3_ctrl	00b	R/W	00 = Pin CURR ₄ is turned off. 01 = Pin CURR ₄ is active. 1x = GPIO control; pin is active when curr3_gpio (page 50) = 1.		
7:6	curr4_ctrl	00b	R/W	00 = Pin CURR ₄ is turned off. 01 = Pin CURR ₄ is active. 1x = GPIO control; pin is active when curr4_gpio (page 50) = 1.		

Addr: 41		CURR Mode Register				
		Selects operation mode for current sources.				
Bit	Bit Name	Default	Access	Bit Description		
0	curr1_sw		R/W	0 = Pin CURR ₁ is operating as current sink. 1 = Pin CURR ₁ is operating as resistive load current. Resistance is defined by bits curr1_current (page 48).		
1	curr2_sw		R/W	0 = Pin CURR ₂ is operating as current sink. 1 = Pin CURR ₂ is operating as resistive load current. Resistance is defined by bits curr2_current (page 48).		
2	curr3_sw		R/W	0 = Pin CURR ₃ is operating as current sink. 1 = Pin CURR ₃ is operating as resistive load current. Resistance is defined by bits curr3_current (page 49).		
3	curr4_sw		R/W	0 = Pin CURR ₄ is operating as current sink. 1 = Pin CURR ₄ is operating as resistive load. Resistance is defined by bits curr4_current (page 49).		
7:4				N/A		

Addr: 42		CURR GPIO Map Register		
		Selects GPIO pin to control current sources.		
Bit	Bit Name	Default	Access	Bit Description
1:0	curr1_gpio	Boot ROM	R/W	If bits curr1_ctrl (page 49) = 1x, the following pin is assigned for turning the CURR1 pin on and off. 00 = GPIO1 01 = GPIO2 10 = GPIO3 11 = GPIO4
3:2	curr2_gpio	Boot ROM	R/W	If bits curr2_ctrl (page 49) = 1x, the following pin is assigned for turning the CURR2 pin on and off. 00 = GPIO1 01 = GPIO2 10 = GPIO3 11 = GPIO4
5:4	curr3_gpio	Boot ROM	R/W	If bits curr3_ctrl (page 49) = 1x, the following pin is assigned for turning the CURR3 pin on and off. 00 = GPIO1 01 = GPIO2 10 = GPIO3 11 = GPIO4
7:6	curr4_gpio	Boot ROM	R/W	If bits curr4_ctrl (page 49) = 1x, the following pin is assigned for turning the CURR4 pin on and off. 00 = GPIO1 01 = GPIO2 10 = GPIO3 11 = GPIO4

6.8 Audio Amplifier

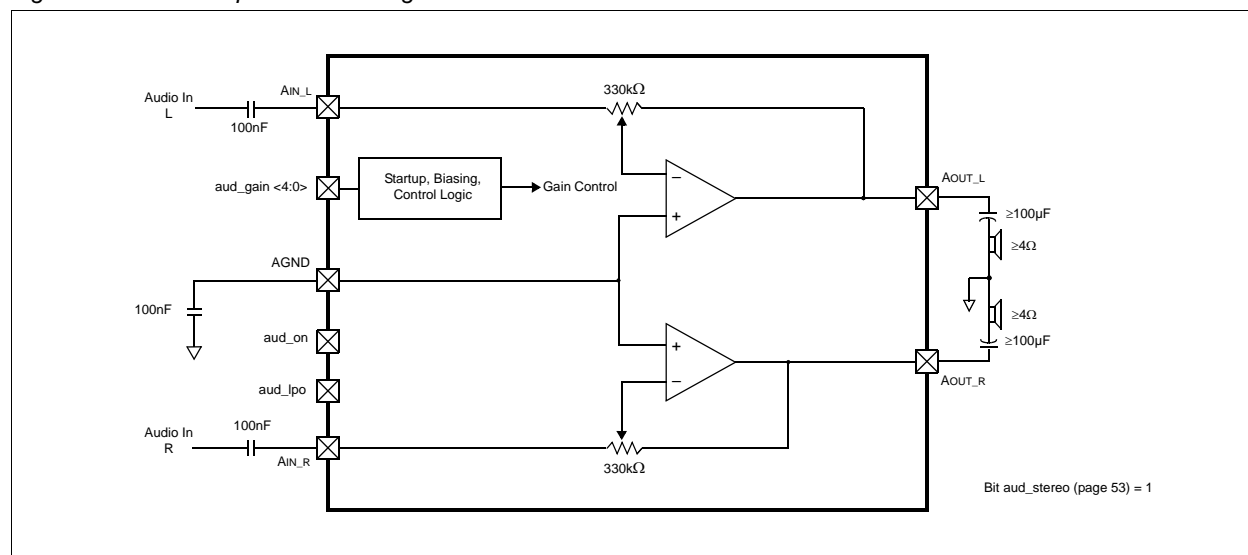
The integrated Audio Amplifier provides real CD-quality audio and can be used as a headphone amplifier for portable devices. It is designed to meet the operational and power requirements of portable devices by delivering:

- 1WRMS continuous power into 8Ω differential at 5V supply
- 2 x 50mWRMS into 32Ω single-ended at 5V supply

The Audio Amplifier provides the following operational features:

- Total harmonic distortion is less than 0.1% at 1kHz and the quiescent current does not exceed 8mA.
- Power supply rejection is always better than 50dB and allows direct connection to noisy batteries, e.g. in TDMA systems.
- The internal programmable gain can be used for volume control.
- Only a few external components are required for AC-coupling and reference bypass.
- An internal smooth-rampup circuit ensures pop- and click-less startup without expensive and bulky external relays.
- Device stability even with high capacitive loads of 1nF and does not require external snubber networks.
- Inputs are high-impedance in power-down.

Figure 24. Audio Amplifier Block Diagram – Stereo Mode



Note: The value of the audio output decoupling capacitors depends on the speaker impedance and the desired minimum output frequency:

$$C = \frac{1}{2 \times \pi \times f \times R}$$

Where:

f = minimum output cutoff frequency, -3dB point.

R = speaker impedance in Ω.

C = decoupling capacitance in F.

Figure 25. Audio Amplifier Block Diagram – Differential Mode

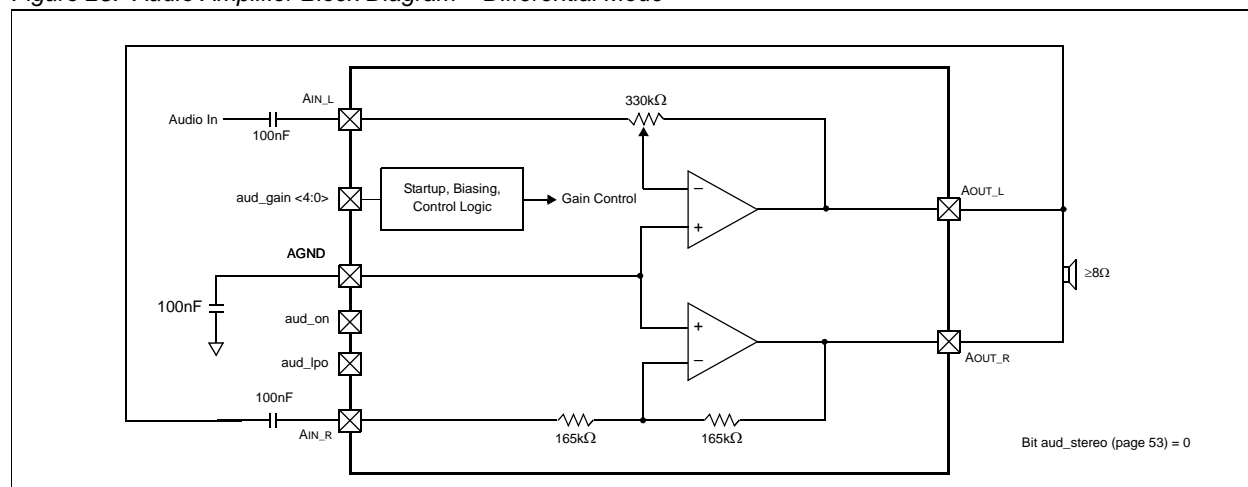


Table 23. Audio Amplifier Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDDH	Supply Voltage Range	3		5.5	V	
PSRR	Power Supply Rejection Ratio, Differential		70		dB	f = 1kHz
			50			f = 20kHz
PSRR	Power Supply Rejection Ratio, Single-Ended		50		dB	f = 1kHz
			40			f = 20kHz
I _{off}	Shut Down Current			100	nA	
I _{VDDH}	Supply Current (Differential Mode)			9	mA	aud_lpo (page 53) = 0 and aud_ib_red (page 53) = 00
				4		aud_lpo = 1 and aud_ib_red = 00
				2.7		aud_lpo = 1 and aud_ib_red = 11
I _{VDDH}	Supply Current (Stereo Mode)			8	mA	aud_lpo = 0 and aud_ib_red = 00
				3		aud_lpo = 1 and aud_ib_red = 00
				1.7		aud_lpo = 1 and aud_ib_red = 11
RL	Output Load	8			Ω	Differential mode
		4				Stereo mode
THD+N	Total Harmonic Distortion			0.1	%	P _{OUT} = 1W, RL = 8Ω, f = 1kHz Differential
				0.5	%	P _{OUT} = 1W, RL = 8Ω, f = 20kHz Differential
				0.05	%	P _{OUT} = 50mW, RL = 32Ω, f = 1kHz Single-Ended
				0.2	%	P _{OUT} = 50mW, RL = 32Ω, f = 20kHz Single-Ended
A ₀	Gain	-22	0	20	dB	Programmable gain: A _{out} /A _{in}
ΔA _x	Programmable Gain Step-Size		3		dB	
I _{ov_on}	Overcurrent On_limit	591	650	744	mA	Current rising into PMOS driver; when aud_lpo = 0 and aud_ib_red = 00, and aud_overcur = 1.
I _{ov_off}	Overcurrent Off_limit	397	550	650	mA	Current decreasing in PMOS driver; when aud_lpo = 0 and aud_ib_red = 00, and aud_overcur (page 53) is cleared.
I _{ov_hyst}	Overcurrent Hysteresis		100		mA	
t _{STARTUP}	Startup Time of Audio Amplifier Measured from Rising Edge of aud_on		140	500	ms	To reduce the startup time see austriamicrosystems Application Note AN3603_21092005; Indirect Production Test

6.8.1 Audio Amplifier Registers

Addr: 43		Audio Control Register		
		Configures the Audio Amplifier.		
Bit	Bit Name	Default	Access	Bit Description
0	aud_on	0	R/W	Activates the Audio Amplifier. 0 = Audio amplifier off; inputs AIN_L and AIN_R are high-impedance. 1 = Audio amplifier on.
1	aud_lpo	0	R/W	Select Low-Power Operation; reduced output power. 0 = Use for speakers < 32Ω (nominal impedance) in stereo mode; < 64Ω differential. 1 = Use for speakers ≥ 32Ω (nominal impedance) in stereo mode; ≥ 64Ω differential.
3:2	aud_ib_red	00b	R/W	Reduced bias current into Audio Amplifier circuit. 00 = Use for speakers < 8Ω (nominal impedance) in stereo mode; < 16Ω differential. 01 = N/A 10 = N/A 11 = Use for speakers ≥ 8Ω (nominal impedance) in stereo mode; ≥ 16Ω differential.
7:4	aud_gain	0000b	R/W	Audio Amplifier gain adjust. 0000 = Output off 1000 = 0dB 0001 = -22dB 1001 = +2dB 0010 = -19dB 1010 = +5dB 0011 = -16dB 1011 = +8dB 0100 = -13dB 1100 = +11dB 0101 = -10dB 1101 = +14dB 0110 = -7dB 1110 = +17dB 0111 = -4dB 1111 = +20dB

Addr: 65		Audio Control 2 Register		
		Configures the Audio Amplifier.		
Bit	Bit Name	Default	Access	Bit Description
0	aud_stereo	1	R/W	Selects audio mode. 0 = Differential mono mode (connect AIN_R to AOUT_L) 1 = Stereo mode.
1	aud_overcur	00	R	0 = Normal operation; audio output current below limit of lov_on (page 52). 1 = Audio output current exceeds limit (lov_on).
3:2	aud_pulldwn	00b	R/W	Audio amplifier output pulldown control; active if aud_on (page 53)=0. 00 = 30μA 01 = 0.6mA 10 = 1.2mA 11 = 2.5mA
7:4				N/A

7 System Supervisory Functions

7.1 Reset

RESET is an active low bi-directional pin; an external pullup to LDO VANA_1 has to be added (see Digital Input/Output DC/AC Characteristics on page 62).

During each reset cycle the following states are controlled by the AS3603:

- Pin RESET is Forced to GND
- Programmable Power-off Function
- Programmable Power-on Sequence and Regulator Voltages
- Programmable Reset Timer
- All Register bits Set to Default Values after Power-On (except the **Audio Control 2 Register** (page 53), the **Interrupt Status Register** (page 47), and the **Boot Sequence Detection Register** (page 61).

Note: Programming is controlled by the internal mask-ROM and the external resistor RPROGRAM. The first address of each ROM-bank defines which of the regulators are turned off during reset.

7.1.1 Reset Conditions

Reset can be activated from 7 different sources:

- Power On (Battery or Charger Insertion)
- Low Battery
- Power Off Mode
- Software Forced Reset
- Externally Triggered through the RESET Pin
- Overtemperature
- Watchdog

Power On (Battery or Charger Insertion)

There are two types of voltage dependent resets:

- VPOR – Monitors the voltage on pin V2_5. LDO V2_5 and uses the voltage VCHARGER or VBAT as its source.
- VRESET – Monitors the voltage on the VBAT pins. The pin RESET is only released if V2_5 is above VPOR and VBAT is above VRESETRISE.

Low Battery

A reset is automatically generated if the battery voltage drops below VRESETFALLING for a minimum period of VRESETMASK.

Table 24. Reset Levels

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VPOR	Overall power on reset	1.5	2.0	2.3	V	Monitor voltage on pin V2_5; power on reset for all internal functions. Note: Pin RESET stays low until V2_5 > VPOR
VRESETRISE	Reset level for VBAT rising		3.1		V	Monitor voltage on pin VBAT; rising level.
VRESETFALLING	Reset level for VBAT falling		2.8		V	Monitor voltage on pin VBAT; falling level.
VRESETMASK	Mask time for VRESETFALLING	2.0	2.5	3.0	ms	Duration for VBAT < VRESETFALLING until a reset cycle is started.

Notes:

1. VRESETFALLING is only accepted if the reset condition is longer than VRESETMASK. This guard time is used to avoid a complete reset of the system in case of short drops of VBAT.
2. VRESET signal is debounced with the specified time for rising and falling slope of VBAT.

Power Off

Setting bit **power_off** (page 55) = 1 puts the AS3603 into ultra low-power mode. To start a complete reset cycle, the AS3603 waits until the external pin ON is pulled high, the Battery Charger is inserted, or level VPOR is reached. Bit **power_off** is automatically cleared by this reset cycle. During power off state, all circuits are turned off except LDO V2_5, thus the current consumption of the AS3603 is reduced to less than 10µA. The digital part is supplied by LDO V2_5, all other circuits are turned off in this mode, including internal references and oscillator.

Note: All registers except the **Reset Control Register** (page 55) are set to their default value after power-on.

Software Forced Reset

Setting bit **force_reset** (page 55) = 1 immediately initiates a reset cycle, and is automatically cleared during a reset.

External Triggered Reset

If the pin RESET is pulled from high to low by an external source (microprocessor or button) a reset cycle is initiated.

Overtemperature Reset

The reset cycle can be started by overtemperature conditions (page 57).

Watchdog Reset

If the Watchdog is armed – bit **wtdg_on** (page 58) = 1 and bit **wtdg_res_on** (page 58) = 1 – and the timer expires, a reset is initiated. Refer to page 58 for information about the Watchdog block.

7.1.2 Reset Registers

Addr: 58		Reset Control Register		
		Controls reset and power off.		
Bit	Bit Name	Default	Access	Bit Description
0	force_reset	0b	R/W	0 = Normal operation. 1 = Initiates a complete reset cycle.
1	power_off	0b	R/W	0 = Normal operation. 1 = Initiates power-off mode where all LDOs are turned off except LDO V2_5. The AS3603 waits for a rising edge on pin ON or until the battery charger is detected.
2	on_input	N/A	R	Static indication of ON input pin. 0 = ON input pin is low. 1 = ON input pin is high (external ON key depressed).
5:3	reset_reason	N/A	R	Indicates to the software the reason for the most recent reset. 000 = VPOR (page 54) has been reached (initial battery or charger insertion). 001 = VRESETFALLING (page 54) was reached (VBAT < 2.75V). 010 = Software forced by bit force_reset . 011 = Software forced by bit power_off and ON was pulled high. 100 = Software forced by bit power_off and a Battery Charger was detected. 101 = Externally triggered through pin RESET. 110 = Reset caused by overtemperature T140. 111 = Reset caused by Watchdog.
7:6				N/A

Addr: 19		Reset Timer Register		
		Sets the RESET timer value.		
Bit	Bit Name	Default	Access	Bit Description
2:0	res_timer	Boot ROM	R/W	000 = 15ms 001 = 30ms 010 = 45ms 011 = 60ms 100 = 75ms 101 = 90ms 110 = 105ms 111 = 120ms
7:3				N/A

7.1.3 Reset Cycle

During a reset cycle, pin RESET is forced low for at least the time specified by bits **res_timer** (page 55) and then all register bits are set to their default values except bit **ov_temp_140** (page 57) and the **Boot Sequence Detection Register** (page 61).

During the reset time, a normal startup is initiated (refer to Startup on page 56) and the reset is active until the reset timer (set by bits **res_timer**) expires. The voltage on pin RESET is then pulled high by the external resistor and the whole system is leaving the reset state.

7.1.4 res_con: Reset Control

Reset is internally generated from a power on detection circuit (page 54) and provided to the internal logic as well as externally through the open-drain pin RESET. This pin can also be forced externally by pulling it low. Additionally Reset can be forced by software by setting bit **force_reset** (page 55) = 1.

7.2 Startup

7.2.1 Normal Startup

During a normal reset cycle (page 54), after V_{2_5} is above VPOR and VBAT is above VRESETRISE, a normal startup is initiated as follows:

1. The external capacitor on CREF is charged to 1.8V.
2. A 3-bit A/D conversion of resistor RPROGRAM value is performed, selecting 1 of 8 boot configurations – see bit **rom_adr** (page 61).
3. The DC/DC converters and LDOs are sequentially powered up according to the selected Boot ROM configuration (address 01_h - 31_h – see Table 35 on page 66).
4. Depending on the Boot ROM setting (address 0 Bit 7, Auto-Shutdown):
 - a. The AS3603 enters shutdown mode.
 - or-
 - b. The Reset-Timer is set by the Boot ROM and the reset is released when the Reset-Timer expires (pin RESET is pulled high).

7.2.2 Programmable Startup Sequences

For more details on the available power-on sequences stored in the Boot-ROM, please refer to document *AS3603_BootSeq.PDF*, available from austriamicrosystems, AG upon request.

7.2.3 Startup from Battery Charger

If the voltage on pin VCHARGER is within VSTARTCHARGER, the Battery Charger is started in all cases, even with VBAT = 0V. This allows the battery to be charged (even from deep discharge) and a normal startup to proceed.

Table 25. Battery Charger Startup Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VSTARTCHARGER	Voltage on VCHARGER for the AS3603 to start	4.35	5.0	15	V	On pin VCHARGER.

7.3 Protection Functions

The Step Up DC/DC Converter, the Step Down DC/DC Converter, and all LDOs have integrated overcurrent protection. Overtemperature protection of the AS3603 is also built-in and can be activated with the serial interface bit **temp_pmc_on** (page 57).

The AS3603 has two temperature indicators:

- **ov_temp_110** (page 57) – Automatically reset if the overtemperature condition is removed.
- **ov_temp_140** (page 57) – Must be reset via the serial interface with bit **rst_ov_temp_140** (page 57). If **ov_temp_140** is set, an automatic reset of the complete AS3603 is initiated. Bit **ov_temp_140** is not cleared by this reset cycle to indicate the reason for this (unexpected) shutdown. It must be cleared intentionally by bit **rst_ov_temp_140**. The cause of this reset is stored in the **Reset Control Register** (page 55). This allows a detection of the reset cause, after the device has restarted.

7.3.1 TMP_SV: Temperature Supervision

The AS3603 includes an integrated temperature sensor, implemented to provide overtemperature protection of the device. It generates flags linked to the two temperature thresholds:

- **T110** – 110° threshold. Sets **ov_temp_110** (page 57), signalling the 110° overtemperature condition. Thus software can react and shut down power-consuming functions in order to decrease the device's temperature.
- **T140** – 140° threshold. Reaching this temperature level generates a Reset, when **temp_pmc_on** (page 57) is enabled. This sets all regulators into power-down mode and stops battery charging.

7.3.2 Overtemperature Detection

Table 26. Overtemperature Detection Parameters

Symbol	Parameter	Min	Typ	Max	Unit
T ₁₁₀	ov_temp_110 Rising Threshold	95	110	125	°C
		203	230	257	°F
T ₁₄₀	ov_temp_140 Rising Threshold	125	140	155	°C
		257	284	311	°F
T _{hyst}	ov_temp_110 and ov_temp_140 Hysteresis		5		°C

7.3.3 Overtemperature Detection Register

Addr: 59		Overtemperature Control Register			
		Device temperature supervision.			
Bit	Bit Name	Default	Access	Bit Description	
0	temp_pmc_on	0	R/W	Activates/deactivates temperature supervision. Default: Off - all other bits are only valid if set to 1. 0 = Temperature supervision is disabled. No reset will be generated when the device temperature exceeds 140°C. 1 = Temperature supervision is enabled.	
1	ov_temp_110	N/A	R	1 = Warning flag indicating that the device temperature has exceeded 110°C.	
2	ov_temp_140	N/A	R	1 = Indicates that the device overtemperature has exceeded 140°C. This bit is not cleared by the automatic reset caused by this flag. It must be cleared using bit rst_ov_temp_140 .	
3	rst_ov_temp_140	0	W	Used to clear bit ov_temp_140 ; first set this bit = 1 and then set it = 0.	
5:4	temp_test	00	R/W	Only used for production; must always be set to 00.	
6	tco_110_a	N/A	R	Only used for production – direct output of T110 comparator.	
7	tco_140_a	N/A	R	Only used for production – direct output of T140 comparator.	

7.4 Watchdog Block

The AS3603 includes a Watchdog block to detect a deadlock of the connected controller.

If the Watchdog block is active (**wtdg_on** (page 58) = 1), it must get a continuous trigger signal within a programmable timer window. If there is no signal for a certain time period from a defined GPIO pin or bit **wtdg_sw_sig** (page 59), the Watchdog block starts either a complete reset – bit **wtdg_res_on** (page 58) must be set to 1 – or sets interrupt flag **wdog_i** (page 47).

The Watchdog timer window is defined by bits:

- **wtdg_min_timer** (page 59)
- **wtdg_max_timer** (page 59)

The trigger signal can be configured using bits:

- **wtdg_trigger** (page 58)
- **wtdg_sw_sig** (page 59) – Watchdog is reset by software
- **wtdg_gpio_input** (page 58) – Watchdog is reset by hardware (GPIO)

Any of the general purpose input/outputs can be configured as inputs using bit **wtdg_gpio_input** (page 58), and outputs using bits **gpio1_out_src** (page 43), **gpio2_out_src** (page 43), **gpio3_out_src** (page 44), or **gpio4_out_src** (page 44) = 11, for the Watchdog. While the GPIO input must be continuously re-triggered in order to avoid a Watchdog interrupt, the GPIO output will generate an interrupt when the Watchdog runs over – **wdog_int_en** (page 47).

7.4.1 Watchdog Registers

The Watchdog is controlled by the registers listed in Table 27.

Table 27. Low Dropout Regulators Register Summary

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Page
Watchdog Control Register	46	N/A			wtdg_trigger	wtdg_gpio_input	wtdg_res_on	wtdg_on		58
Watchdog_min Timer Register	47	wtdg_min_timer								59
Watchdog_max Timer Register	48	wtdg_max_timer								59
Watchdog Software Signal Register	49	N/A							wtdg_sw_sig	59

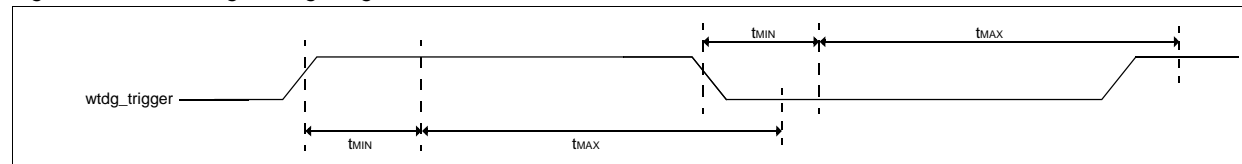
Addr: 46		Watchdog Control Register			
		Controls the Watchdog block.			
Bit	Bit Name	Default	Access	Bit Description	
0	wtdg_on	0	R/W	0 = Disables the Watchdog block. 1 = Enables the Watchdog block.	
1	wtdg_res_on	1	R/W	If the Watchdog expires and this bit = 1, a reset cycle will be started. Refer to page 54 for information about reset cycles. 0 = A watchdog overflow does not generate a reset. 1 = A watchdog overflow generates a reset.	
3:2	wtdg_gpio_input	00	R/W	Specifies the input pin of the Watchdog if bit wtdg_trigger = 1. 00 = GPIO1 01 = GPIO2 10 = GPIO3 11 = GPIO4	
4	wtdg_trigger	0	R/W	Select type of trigger (software or hardware). 0 = Use bit wtdg_sw_sig (page 59) as trigger signal for the Watchdog. 1 = Use the pin defined by bit wtdg_gpio_input as trigger signal for the Watchdog.	
7:5				N/A	

Addr: 47		Watchdog_min Timer Register		
		Sets the minimum Watchdog trigger time.		
Bit	Bit Name	Default	Access	Bit Description
7:0	wtdg_min_timer	00 _h	R/W	00 _h = 0s 01 _h = 7.5ms ... FF _h = 1.9s.

Addr: 48		Watchdog_max Timer Register		
		Sets the maximum Watchdog trigger time.		
Bit	Bit Name	Default	Access	Bit Description
7:0	wtdg_max_timer	FF _h	R/W	01 _h = 7.5ms ... FF _h = 1.9s. Caution: Do not set these bits = 00 _h .

Addr: 49		Watchdog Software Signal Register		
		Resets the Watchdog block by software.		
Bit	Bit Name	Default	Access	Bit Description
0	wtdg_sw_sig	0	R/W	Trigger input by the serial interface if wtdg_trigger (page 58) = 0. 0 = Force watchdog trigger = low (see Figure 26). 1 = Force watchdog trigger = high (see Figure 26).
7:1				N/A

Figure 26. Watchdog Timing Diagram



7.5 Internal Reference Circuits

The internal reference circuits (V, I, f_{clk}) require the external components listed in Table 28.

Table 28. Reference External Components

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C _{EXT}	External filter capacitor	-20%	100	+20%	nF	Ceramic low-ESR capacitor between C _{REF} and V _{SS}
R _{EXT}	External resistor	-1%	220	+1%	kΩ	Between R _{BIAS} and V _{SS}

Table 29. References Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V _{CEXT}	Reference voltage	-1%	1.8	+1%	V	Low noise trimmed voltage reference - connected to pin C _{REF} ; do not load.
f _{CLK}	Internal reference clock	1.0	1.1	1.2	MHz	Trimmed clock reference

To reduce the current consumption of the AS3603, internal references circuit scan be set into a special low-power mode with bit **low_power_on** (page 60).

7.5.1 Internal Reference Registers

Addr: 45		References Control Register		
		Configures low-power mode.		
Bit	Bit Name	Default	Access	Bit Description
0	low_power_on	0	R/W	0 = Standard mode or controlled by GPIO, if low_power_gpio_on = 1. 1 = Low-power mode; all parameters except noise (see LDO parameters, section 6.3) are still valid.
1	low_power_gpio_on	0	R/W	If set and low_power_on = 0 then the low-power mode is controlled by a GPIO pin. 0 = Low-power mode disabled for GPIO control. 1 = Low-power mode is activated by GPIO pin (low_power_gpio). low_power_on must be enabled.
3:2	low_power_gpio	00	R/W	Specifies the pin to be used as GPIO control. 00 = GPIO1 10 = GPIO3 01 = GPIO2 11 = GPIO4
4	low_power_gpio_pol	0	R/W	0 = Low-power mode is activated. If the selected GPIO input, bit low_power_gpio = 1. 1 = Low-power mode is activated. If the selected GPIO input, bit low_power_gpio = 0.
7:5				N/A

7.6 Low Power Mode

Bit **low_power_on** (page 60) controls low-power mode. In low-power mode the integrated voltage reference and the temperature supervision comparators operate in pulsed mode. This reduces the quiescent current of the AS3603 by 45µA (typical). Because of the pulsed function, the LDO output noise parameters do not meet the specification in low-power mode but the full functionality is still available.

Note: Low-power mode can be activated by hardware using one of the GPIO pins, or by software by setting bit **low_power_on** (page 60) = 1.

7.7 Boot Sequence Detection

The AS3603 startup and reset sequences are highly configurable. The configuration of these sequences is defined by the ratio of the external bias resistors **RBIAS** and **RPROGRAM**.

At the beginning of each reset cycle a 3-bit A/D conversion is performed. The result of this conversion is used to select 1 of 8 possible address-ranges of an internal mask-programmable ROM. The information stored in this ROM defines the following parameters:

- The voltage regulators will be turned off at the beginning of the reset cycle.
- The power-on sequence and voltage levels of up to 7 LDOs and the Step-Down DCDC-converter.
- The duration of the reset cycle (4 possible timer values).

For the specified value of $R_{ext} = 220k\Omega$, values of **RPROGRAM** listed in Table 30 select the 8 possible address ranges.

Table 30. *RPROGRAM* Values

Selected Bank	RPROGRAM (Ideal)	Closest E24 Resistor Value (tol. = ± 5%)
Bank 0	Open	Open
Bank 1	320kΩ	330kΩ
Bank 2	160kΩ	160kΩ
Bank 3	80kΩ	82kΩ
Bank 4	40kΩ	39kΩ
Bank 5	20kΩ	20kΩ
Bank 6	10kΩ	10kΩ
Bank 7	5kΩ	5.1kΩ

7.7.1 ON Detection Register

Addr: 60		Boot Sequence Detection Register		
		Displays the detected Boot ROM sequence.		
Bit	Bit Name	Default	Access	Bit Description
2:0	rom_adr	000b	R	Selected boot ROM bank (as set by RPROGRAM). Registers 01 through 31 (see Table 35 on page 66) are configured according to the selected bank.
3	rom_valid	0	R	0 = Not ready. 1 = Boot ROM bank (rom_adr) is valid.
7:4				N/A

7.8 Serial Interface

The AS3603 provides for the automatic selection of serial interface modes SPI and I²C. In I²C mode two of four signals can be defined to support this mode switching.

7.8.1 Digital Input/Output DC/AC Characteristics

The output voltage LDO VANA_1 is used as supply voltage of the pins.

Bit `Ido_ana1_on` (page 34) should never be set to 0, as register access over the serial interface is not possible in this case. It is only set to 0 automatically:

- In power-off state (where it is set to 0 automatically)
- During the startup sequence (Boot ROM Addresses 9:13)
- At reset-state (Boot ROM Address 0)

Table 31. DC Characteristics Input Pin SCLK/SDI

Parameter	Symbol	Min	Max	Unit	Notes
High-Level Input Voltage	V _{IH}	0.7 x VANA_1		V	
Low-Level Input Voltage	V _{IL}		0.3 x VANA_1	V	
Hysteresis	V _{HYS}	0.2 x VANA_1		V	
Input Leakage Current	I _{LEAK}	-5	5	μA	to VANA_1 and Vss

Table 32. DC Characteristics Input/Output Pin SCSB/SDO

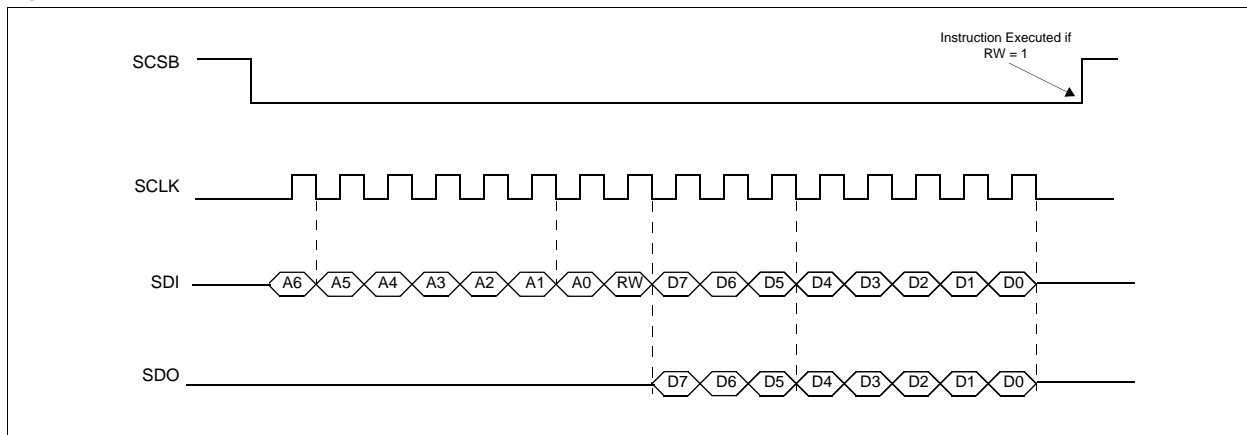
Parameter	Symbol	Min	Max	Unit	Notes
High-Level Input Voltage	V _{IH}	0.7 x VANA_1		V	
Low-Level Input Voltage	V _{IL}		0.3 x VANA_1	V	
Hysteresis	V _{HYS}	0.2 x VANA_1		V	
Input Leakage Current	I _{LEAK}	-5	5	μA	to VANA_1 and Vss
High-Level Output Voltage	V _{OH}	0.8 x VANA_1		V	at -2.0mA
Low-Level Output Voltage	V _{OL}		0.2 x VANA_1	V	at 2.0mA
Capacitive Load	CL		50	pF	

Table 33. DC Characteristics Input/Output Open Drain Pin RESET

Parameter	Symbol	Min	Max	Unit	Notes
High-Level Input Voltage	V _{IH}	0.7 x VANA_1		V	
Low-Level Input Voltage	V _{IL}		0.3 x VANA_1	V	
Hysteresis	V _{HYS}	0.2 x VANA_1		V	
Input Leakage Current	I _{LEAK}	-5	5	μA	to VANA_1 and Vss
Low-Level Output Voltage	V _{OL}		0.2 x VANA_1	V	at 2mA
Capacitive Load	CL		50	pF	
External Pullup Resistor	R _{pullup}		100k	Ω	Connect to VANA_1

7.8.2 SPI Compatible Serial Interface

Figure 27. SPI Waveform



For a read access bit RW (signal SDI) = 1, for a write access bit RW (signal SDI) = 0.

Data is captured at the rising edge of SCLK and written to SDO at the falling edge of SCLK. If the cycle is not completed after the last bit of the addressed cell, the access is continued with next address (address + 1) to allow block transfers. The maximum clock rate is 10MHz.

7.8.3 I²C Compatible Serial Interface

I²C Configuration

The AS3603 can be configured as an I²C-slave. The AS3603 is able to detect automatically that I²C-mode is used when pin SCSB is connected to SDO.

The following pins are used for the I²C interface:

- SDI/SDA = I/O Pin
- SCLK /SCK = Input Pin

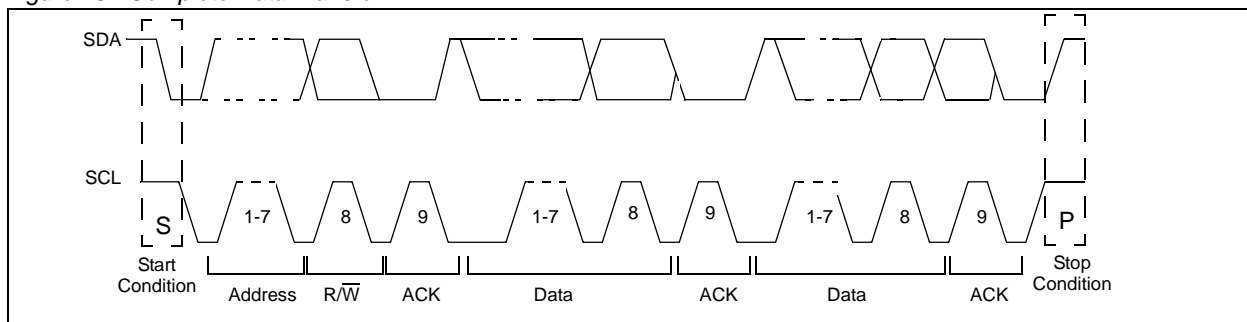
I²C Features

- Fast-mode capability (max. SCL-frequency is 400 kHz @ 100pF capacitive load)
- 7-bit addressing mode
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

I²C Slave Addresses

The AS3603 device address is fixed at 82_h for write commands and 83_h for read commands.

Figure 28. Complete Data Transfer



I²C Data Transfer Formats

Definitions used in the serial data transfer format diagrams (Figures 29 - 33) are listed in Table 34.

Table 34. I²C Data Transfer Byte Definitions

Symbol	Definition	R/W (AS3603 Slave)	Notes
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 0010 (82 _h)
DR	Device address for read	R	1000 0011 (83 _h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	R	1 bit
P	Stop condition	R	8 bit
WA++	Increment word address internally	R	During acknowledge

Figure 29. I²C Byte Write

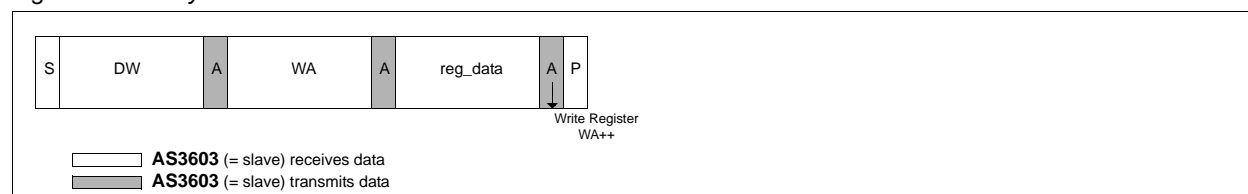
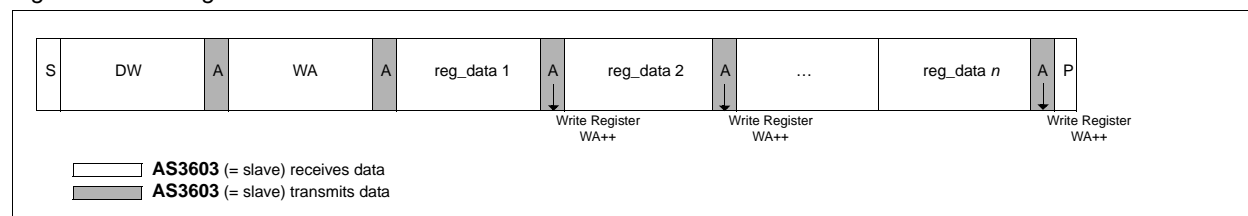


Figure 30. I²C Page Write

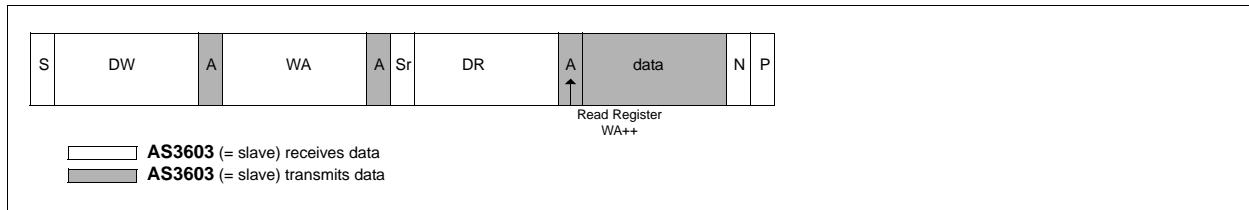


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

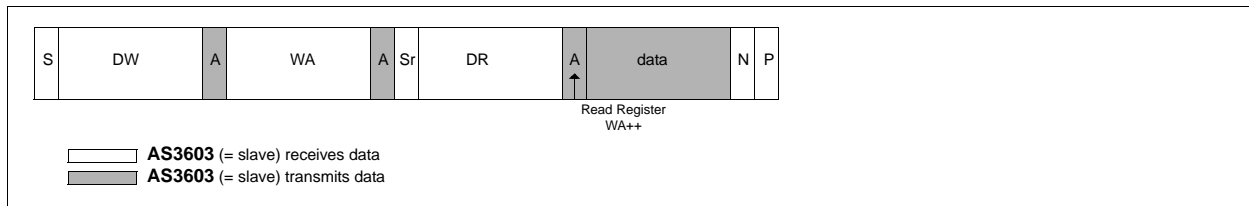
The following diagrams show some of the serial read formats supported by the AS3603.

Figure 31. I²C Random Read

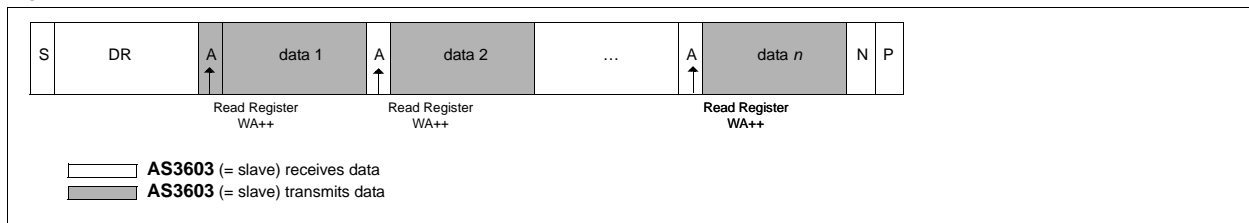
Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 32. I²C Sequential Read

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 33. I²C Current Address Read

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

8 Register Map

The AS3603 registers along with their addresses and default values are listed in Table 35. Fields marked N/A are not used; reading these bits may result in 0s or 1s. Always use 0s, when writing to these bits.

Caution: Do not write to addresses not listed in Table 35.

Table 35. AS3603 Register Summary

Name	Addr	Default	B7	B6	B5	B4	B3	B2	B1	B0	Page	
Reset State*	00	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on		
Step Down Voltage Register	01	ROM	N/A			buck_v					24	
LDO_RF1 Voltage Register	02	ROM	N/A			ldo_rf1_v					32	
LDO_RF2 Voltage Register	03	ROM	N/A			ldo_rf2_v					33	
LDO_RF3 Voltage Register	04	ROM	N/A			ldo_rf3_v					33	
LDO_RF4 Voltage Register	05	ROM	N/A			ldo_rf4_v					33	
LDO_ANA Voltage Register	06	ROM	ldo_ana1_v			ldo_ana2_v					33	
LDO_DIG1 Voltage Register	07	ROM	N/A		ldo_dig1_v						33	
LDO_DIG2 Voltage Register	08	ROM	N/A	ldo_sim_v	ldo_dig2_v						33	
Reg Power Ctrl@6ms*	09	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25, 34	
Reg Power Ctrl@7ms*	10	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25, 34	
Reg Power Ctrl@8ms*	11	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25, 34	
Reg Power Ctrl@9ms*	12	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25, 34	
Reg Power Ctrl@10ms*	13	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25, 34	
Reg Power Ctrl@11ms*	14	ROM	N/A		buck_on	ldo_sim_on	ldo_dig2_on	ldo_dig1_on	ldo_ana2_on	ldo_ana1_on	25, 34	
LDO_GPIO Active Register	15	ROM	ldo_dig2_gpio	ldo_dig1_gpio	ldo_rf4_gpio	ldo_rf3_gpio	ldo_rf2_gpio	ldo_rf1_gpio	ldo_ana2_gpio	buck_gpio	36	
LDO_RF Switch Register	16	ROM	ldo_rf4_on	ldo_rf3_on	ldo_rf2_on	ldo_rf1_on	rf4_sw	rf3_sw	ana2_sw	ana1_sw	35	
LDO_AD GPIO Register	17	ROM	ldo_dig2_gpio_sel		ldo_dig1_gpio_sel		ldo_ana2_gpio_sel		buck_gpio_sel		36	
LDO_RF GPIO Register	18	ROM	ldo_rf4_gpio_sel		ldo_rf3_gpio_sel		ldo_rf2_gpio_sel		ldo_rf1_gpio_sel		37	
Reset Timer Register	19	ROM	N/A					res_timer		55		
Charger Control Register	20	ROM	N/A	Boost	Bypass	Pulse	Li4v2	Fast	BatType	ChEn	19	
Fuel Gauge Register	21	ROM	N/A				CalMod	CalReq	UpdReq	FGEn	21	
Charger Current Register	22	00h	N/A			ConstantCurrent			TrickleCurrent		20	
Step Down Configuration Register	23	ROM	dis_xnc	dis_ilim	force_pwm	N/A		sync_rect_off	buck_nsw_on	buck_psw_on	25	
Charge Pump Control Register	24	ROM	N/A		onkey_pulldown	cp_freq	N/A	cp_vref	cp_pulse_skip	cp_on	38	
Step Up DC/DC Converter Control Register	25	ROM	N/A				stpup_low_curr	stpup_freq	stpup_sw_on	stpup_on	40	
GPIO1 Control Register	26	ROM	gpio1_out_src		gpio1_invert	gpio1_pulls		gpio1_voltage	gpio1_mode		43	
GPIO2 Control Register	27	ROM	gpio2_out_src		gpio2_invert	gpio2_pulls		stepdown_fb	gpio2_mode		43	
GPIO3 Control Register	28	ROM	gpio3_out_src		gpio3_invert	gpio3_pulls		gpio3_voltage	gpio3_mode		44	
GPIO4 Control Register	29	ROM	gpio4_out_src		gpio4_invert	gpio4_pulls		gpio4_voltage	gpio4_mode		44	
Clock Generation Register	30	ROM	N/A								ext_clk	45
Interrupt Enable Register	31	ROM	N/A			chdet_int_en	onkey_int_en	ovtmp_int_en	vchoff_int_en	wdog_int_en	47	
Interrupt Status Register	32	N/A	N/A			chdet_i	onkey_i	ovtmp_i	vchoff_i	wdog_i	47	
GPIO Signal Register	33	N/A	N/A				gpio4	gpio3	gpio2	gpio1	45	
GPIO Frequency Control High Time Register	34	00h	gpio_h_time								45	
GPIO Frequency Control Low Time Register	35	00h	gpio_l_time								45	

Table 35. AS3603 Register Summary (Continued)

Name	Addr	Default	B7	B6	B5	B4	B3	B2	B1	B0	Page	
CURR1 Value Register	36	00 _h	curr1_current								48	
CURR2 Value Register	37	00 _h	curr2_current								48	
CURR3 Value Register	38	00 _h	curr3_current								49	
CURR4 Value Register	39	00 _h	curr4_current								49	
CURR Control Register	40	00 _h	curr4_ctrl		curr3_ctrl		curr2_ctrl		curr1_ctrl		49	
CURR Mode Register	41	00 _h	N/A				curr4_sw	curr3_sw	curr2_sw	curr1_sw	49	
CURR GPIO Map Register	42	00 _h	curr4_gpio		curr3_gpio		curr2_gpio		curr1_gpio		50	
Audio Control Register	43	00 _h	aud_gain				aud_ib_red		aud_lpo	aud_on	53	
Charger Timing Register	44	4B _h	TPOFFMAX		TPOFF			TPON			20	
References Control Register	45	00 _h	N/A			low_power_gpio_pol	low_power_gpio		low_power_gpio_on	low_power_on	60	
Watchdog Control Register	46	02 _h	N/A			wtdg_trigger	wtdg_gpio_input		wtdg_res_on	wtdg_on	58	
Watchdog_min Timer Register	47	00 _h	wtdg_min_timer								59	
Watchdog_max Timer Register	48	FF _h	wtdg_max_timer								59	
Watchdog Software Signal Register	49	00 _h	N/A								wtdg_sw_sig	59
Test_enable	50	00 _h	test_en_code									
Testmux Control	51	00 _h	mux_ain_l_ctrl				mux_ain_r_ctrl					
Testmode Control	52	00 _h	stpup_tm		zzap_force_readout	zzap_test_on	zzap_test_mode	test_mode		atpg_mode		
Charger Status Register	53	N/A	Bypass	NoBat	EOC	CVM	Trickle	IntReg	ChAct	chDet	19	
Delta Charge MSB Register	54	N/A	sign	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	21	
Delta Charge LSB Register	55	N/A	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	21	
Elapsed Time MSB Register	56	N/A	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	22	
Elapsed Time LSB Register	57	N/A	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	22	
Reset Control Register	58	00 _h	N/A		reset_reason			on_input	power_off	force_reset	55	
Overtemperature Control Register	59	00 _h	tco_140_a	tco_110_a	temp_test		rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on	57	
Boot Sequence Detection Register	60	N/A	N/A					rom_valid	rom_adr		61	
ASIC ID 1	61	32 _h	0	0	1	1	0	0	1	0		
ASIC ID 2	62	N/A	rev									
Fuse Reg 1	63	N/A	serial_mode	VrefTrim					Spare	N/A		
Fuse Reg 2	64	N/A	Spare		VrefLpTrim			RefOsc1Mhz1		serial_mode<1>		
Audio Control 2 Register	65	01 _h	N/A				aud_pulldwn		aud_overcur	aud_stereo	53	
Charger Config Register	66	ROM	N/A		CVMtst	DisOWB	DisBDet	Dis Hyst	Wide	N/A	20	
PreCurDac Register	67	00 _h	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	22	

Read-Only Bit



Read/Write Bit



* Reading registers 10 -14 will always return 00_h. These registers are only used during startup sequencing of the respective LDOs. The final sequence in register 14 can be read in register 09 after the boot sequence is completed.

9 Pinout and Packaging

9.1 Pin Descriptions

Table 36. Pin Type Definitions

Pin Type	Description
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
DIO_5	Digital Input/Output with Selectable Supply (V _{5_6} or VDD)
OD	Open Drain - the device can only pulldown this pin
AIO	Analog Pin
AI	Analog Input
AO	Analog Output
S	Supply Pin
GND	Ground Pin

Table 37. Pinlist QFN48

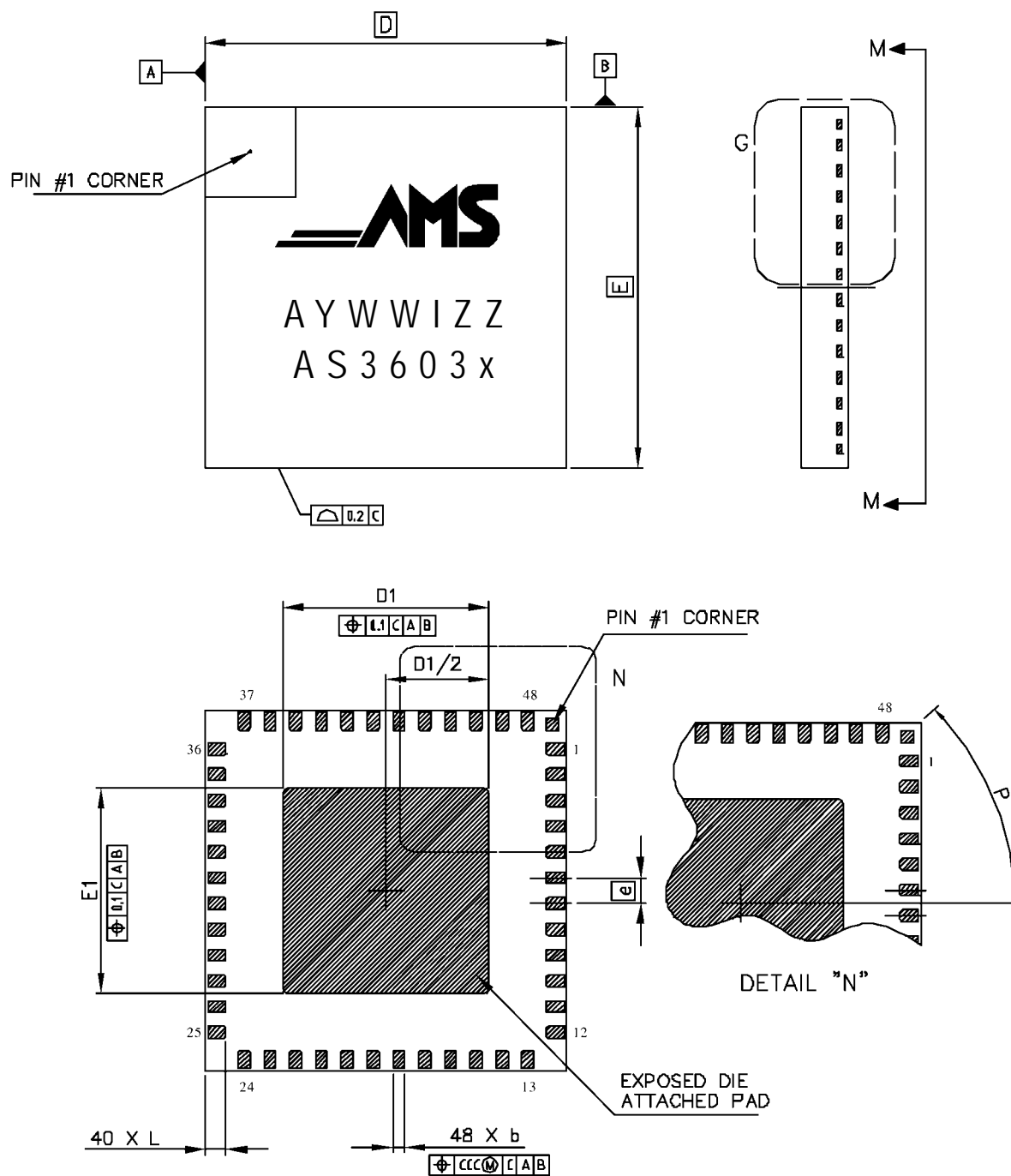
Pin	Name	Type	Description
1	V _{5_6}	AIO	Output voltage of the Charge Pump; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
2	CAPP	AIO	Flying capacitor of the Charge Pump; if used, connect a ceramic capacitor of 330nF (±20%) to this pin.
3	CAPN	AIO	Flying capacitor of the Charge Pump; if used connect a ceramic capacitor of 330nF (±20%) to this pin.
4	VANA_1	AO	Output voltage of Analog LDO VANA_1; if the Charge Pump or this LDO is used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
5	VBAT_1	S	Supply pin for Analog LDOs VANA_1 and VANA_2; can be connected to VBAT or separate supply (3.0-5.5V).
6	VANA_2	AO	Output voltage of one of Analog LDO VANA_2; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
7	VRF_2	AO	Output voltage of RF LDO VRF_2; can be used as high-side switch, if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
8	VBAT_4	S	Supply pad for RF-LDOs VRF_1 and VRF_2; can be connected to VBAT or separate supply (3.0-5.5V).
9	VRF_1	AO	Output voltage of RF LDO VRF_1; can be used as high-side switch, if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
10	RESET	DIO/OD	Bidirectional RESET pin; add an external pullup resistor to pin VANA_1.
11	SDO	DO	SPI digital output in SPI mode; connect to pin SCSB in I2C mode.
12	SDI/SDA	DI	SPI digital input in SPI mode; SDA input/output in I2C mode.
13	SCLK/SCK	DI	SPI clock input in SPI mode; SCK input in I2C mode.
14	SCSB	DI	SPI chip-select in SPI mode; connect to pin SDO in I2C mode.
15	ISENSP	AI	Positive sensing input voltage for the external charging current shunt resistor.
16	ISENSN	AI	Negative sensing input voltage for the external charging current shunt resistor.
17	VRF_3	AO	Output voltage of RF LDO VRF_3; can be used as high-side switch, if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).
18	VBAT_5	S	Supply pin for Charger, internal LDO and RF LDOs VRF_3 and VRF_4. Always connect to VBAT.
19	VRF_4	AO	Output voltage of RF LDO VRF_4; can be used as high-side switch, if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).

Table 37. Pinlist QFN48 (Continued)

Pin	Name	Type	Description
20	VCHARGER	AI	High voltage input coming from the Battery Charger; if the Battery Charger is used, connect a ceramic capacitor of 1 μ F.
21	VGATE	AO	Control pin for the external battery charger MOSFET transistor.
22	V2_5	AO	Output voltage of low power LDO V2_5; always connect a ceramic capacitor of 1 μ F ($\pm 20\%$) or 2.2 μ F (+100%/-50%); do not load this pin during startup.
23	RBIAS	AIO	External resistor; always connect a resistor of 220k Ω ($\pm 1\%$) to ground. Caution: Do not load this pin.
24	RPROGRAM	AIO	External resistor for selecting Boot ROM address; audio input in testmode.
25	ON	DI	Input pin to startup the AS3603 (power on); internal pulldown. Supply pin for Zenerzap programming voltage (for internal use only).
26	CREF	AIO	Bypass capacitor for the internal voltage reference; always connect a capacitor of 100nF. Caution: Do not load this pin.
27	GND_SENSE	AIO	Sensitive GND for Bandgap Voltage Reference.
28	AOUT_L	AO	Audio Amplifier left-channel output.
29	AOUT_R	AO	Audio Amplifier right-channel output.
30	VBAT_3	S	Supply pin for Step-Up Converter, Current Sinks, and Audio Amplifier; always connect to VBAT.
31	AGND	AIO	Audio Amplifier reference GND; if the Audio Amplifier is used, connect a capacitor of 100nF ($\pm 10\%$) to this pin. Caution: Do not connect directly to Vss.
32	CURR4	AI	Analog current sink input (designed for buzzer).
33	CURR3	AI	Analog current sink input (designed for vibrator).
34	CURR2	AI	Analog current sink input (designed for (white LEDs)).
35	CURR1	AI	Analog current sink input (designed for white LEDs); also used as input for the Step Up DC/DC Converter.
36	STEPUP	AIO	Step Up DC/DC Converter output pin; can also be used as a ground switch.
37	AIN_R	AI	Audio Amplifier right-channel input; sense output in test mode.
38	AIN_L	AI	Audio Amplifier left-channel input; sense output in test mode.
39	VDIG_2	AO	Output voltage of Digital LDO VDIG_2; if used, connect a ceramic capacitor of 100nF ($\pm 20\%$).
40	VBUCK	AI	Supply pin for Digital LDOs VDIG_1 and VDIG_2; If the Step Down DC/DC converter is used as pre-regulator, connect this pin to the output of the DC/DC converter. If Step Down DC/DC pre-regulator is not used, this pin can be connected to VBAT or a separate supply (1.0-5.5V).
41	VDIG_1	AO	Output voltage of Digital LDO VDIG_1; if used, connect a ceramic capacitor of 100nF ($\pm 20\%$).
42	GPIO4	DIO_5	General purpose switchable 5V input/output.
43	GPIO3	DIO_5	General purpose switchable 5V input/output.
44	GPIO2	DIO_5	General purpose switchable 5V input/output.
45	GPIO1	DIO_5	General purpose switchable 5V input/output.
46	VSIM	AO	Output voltage of LDO VSIM; if used, connect a ceramic capacitor of 100nF ($\pm 20\%$).
47	VBAT_2	S	Supply pin for the Step Down DC/DC Converter and LDO VSIM; always connect to VBAT.
48	LX	AO	Step Down DC/DC Converter output.
49	VSS	VSS	Ground pad (QFN48: exposed paddle).

9.2 Package Drawings and Markings

Figure 34. QFN 48 - 7x7mm with Exposed Paddle (AS3603-xGx-x)

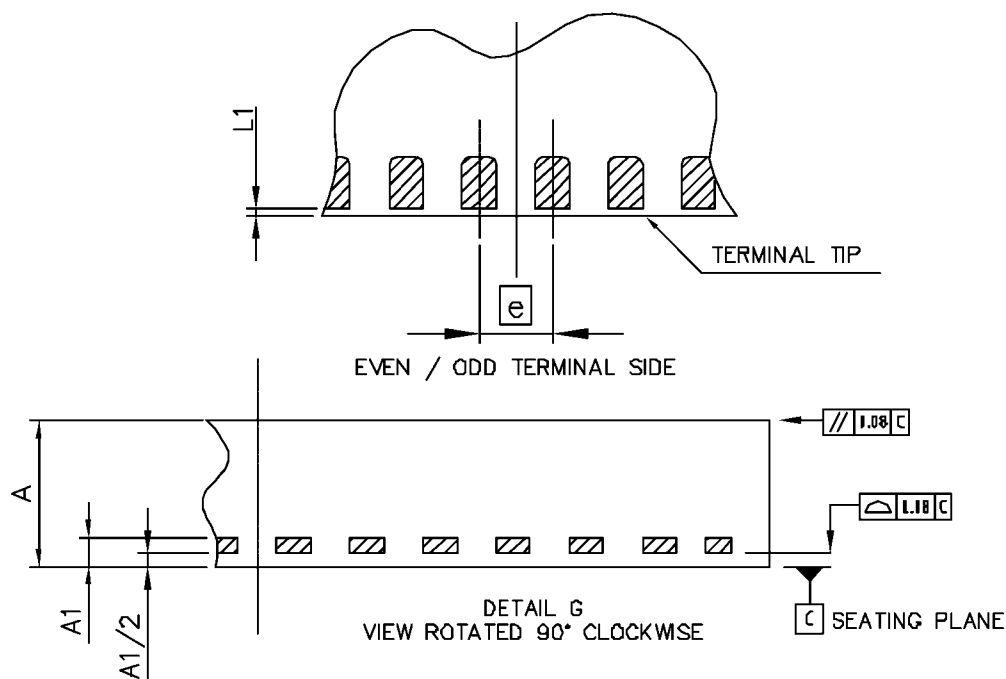


JEDEC Package Outline Standard: MO-220 VHHD-5 – Lead Finish: 100% Sn “Matte Tin”.

Marking: AYWWIZZ

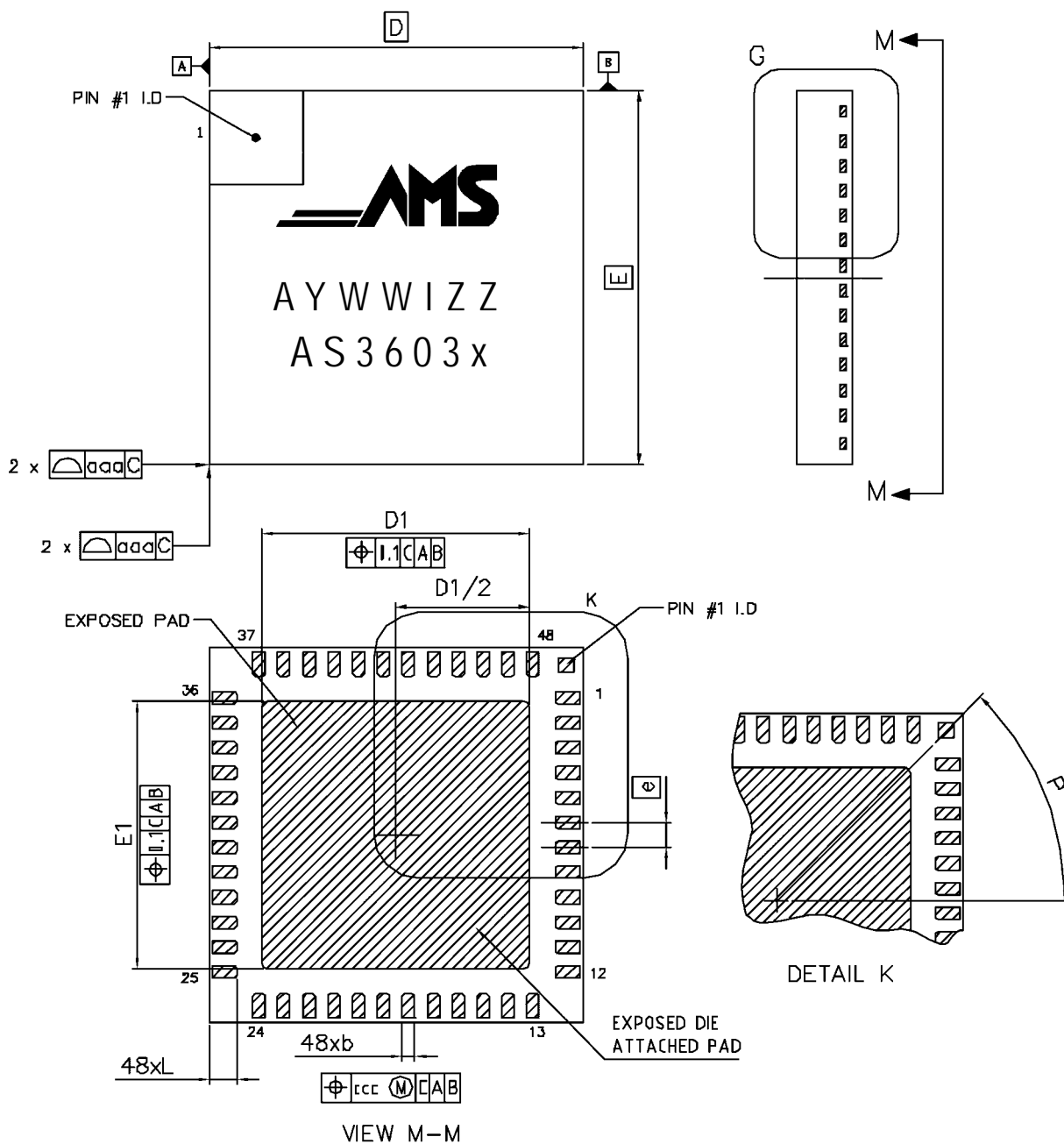
A: Pb-Free Identifier
Y: Last Digit of Manufacturing Year
WW: Manufacturing Week
I: Plant Identifier
ZZ: Traceability Code

Figure 35. QFN 48 – 7x7mm Detail Dimensions



DIM	MIN	NOM	MAX	NOTES
A	0.80		1.00	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A1		0.203 REF		2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
b	0.18	0.23	0.30	
D		7.00 BSC		3.0 DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
E		7.00 BSC		DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.
D1	3.90		4.10	
E1	3.90		4.10	
e		0.50 BSC		4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
L	0.30	0.40	0.50	
L1			0.10	5.0 RADIUS ON TERMINAL IS OPTIONAL.
P		45° BSC		
aaa		0.15		
ccc		0.10		

Figure 36. QFN 48 - 6x6mm with Exposed Paddle (AS3603-xFx-x)

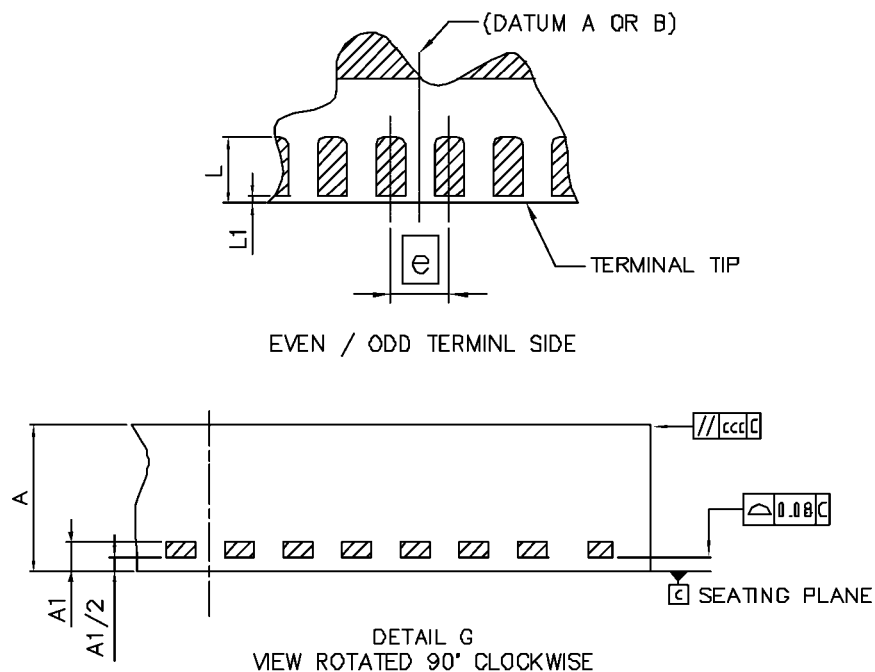


Lead Finish: 100% Sn "Matte Tin".

Marking: AYWWIZZ

A: Pb-Free Identifier
 Y: Last Digit of Manufacturing Year
 WW: Manufacturing Week
 I: Plant Identifier
 ZZ: Traceability Code

Figure 37. QFN 48 – 6x6mm Detail Dimensions



DIM	MIN	NOM	MAX	NOTES
A	0.80		1.00	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A1		0.203 REF		2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
b	0.18	0.20	0.25	
D		6.00 BSC		3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
E		6.00 BSC		DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.
D1	4.20		4.40	
E1	4.20		4.40	
e		0.40 BSC	-	4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
L	0.35	0.45	0.55	
L1			0.10	5.0 RADIUS ON TERMINAL IS OPTIONAL.
P		45° BSC		
aaa		0.15		
ccc		0.10		

10 External Parts List

The recommended specifications for external components (refer to pages 2 and 3) are listed in Table 38.

Table 38. External Parts Specification

Part	Min.	Typ.	Max.	Tol. Min.	Rating Min.	Remarks	Package Min.
C1	1 μ F		4.7 μ F	$\pm 20\%$	25V	Ceramic, X5R, X7R (Step-Up)	1206
C2		330nF		$\pm 20\%$	6.3V	Ceramic, X5R (Charge Pump)	0603
C3	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (V5_6)	0603
C4	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VANA_1)	0603
C5		1 μ F		$\pm 20\%$	6.3V	Ceramic, X5R (VBAT_1)	0603
C6	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VANA_2)	0603
C7	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (V2_5)	0603
C8	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VRF_1)	0603
C9		1 μ F		$\pm 20\%$	6.3V	Ceramic, X5R (VBAT_4)	0603
C10	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VRF_2)	0603
C11	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VRF_3)	0603
C12		1 μ F		$\pm 20\%$	6.3V	Ceramic, X5R (VBAT_5)	0603
C13	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VRF_4)	0603
C14	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VDIG_1)	0603
C15	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VDIG_2)	0603
C16		1 μ F		$\pm 20\%$	6.3V	Ceramic, X5R (VBAT_2)	0603
C17	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VBUCK)	0603
C18		10 μ F		$\pm 20\%$	6.3V	Tantalum or X5R	
C19		100nF		$\pm 20\%$	6.3V	Ceramic, X5R (VSIM)	0402
C20		100 μ F		$\pm 20\%$	6.3V	Tantalum; L Stereo Decoupling Cap.	
C21		100 μ F		$\pm 20\%$	6.3V	Tantalum; R Stereo Decoupling Cap.	
C22		1 μ F		$\pm 20\%$	6.3V	Ceramic, X5R (VBAT_4)	0603
C23		100nF		$\pm 20\%$	6.3V	Ceramic, X5R (Decoupling, AIN_L)	0402
C24		100nF		$\pm 20\%$	6.3V	Ceramic, X5R (Decoupling, AIN_R)	0402
C25		100nF		$\pm 20\%$	6.3V	Ceramic, X5R (AGND)	0402
C26	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VCHARGER)	0603
C27	10 μ F			$\pm 20\%$	6.3V	X5R; all VBAT Caps. Combined	0603
C28		100nF		$\pm 20\%$	6.3V	Ceramic, X5R (ISense)	0402
C29		100nF		$\pm 20\%$	6.3V	Ceramic, X5R (CREF)	0402
C30	1 μ F		4.7 μ F	$\pm 20\%$	6.3V	Ceramic, X5R (VDD_DIG)	0603
R1		2k		$\pm 1\%$		VGATE Pullup Resistor	0201
R2		47k		$\pm 1\%$		ISENSP Series Resistor	0201
R3		47k		$\pm 1\%$		ISENSN Series Resistor	0201
R4	25m	50m	100m	$\pm 1\%$		Shunt resistor	0603
R7				$\pm 5\%$			
R5		100k		$\pm 10\%$		Reset Pullup Resistor	0201
R6		220k		$\pm 1\%$		Bias Resistor	0201
R7		0 10k 20k 39k 82k 160k 330k Inf		$\pm 5\%$		Select ROM Bank 7 Select ROM Bank 6 Select ROM Bank 5 Select ROM Bank 4 Select ROM Bank 3 Select ROM Bank 2 Select ROM Bank 1 Select ROM Bank 0	0201
L1		22 μ H		$\pm 20\%$		Recommended type: Coiltronics SD-12-220	
L2		4.7 μ H		$\pm 20\%$		Recommended type: Coiltronics SD-12-4R7	
D1	MBR0520 or similar					Schottky Diode; ONSEMI, IR	SOD123
D2	xx4148					Universal Diode	
Q1	Si3441 or similar					PMOS Charger Transistor; VISHAY	

11 Ordering Information

Device ID	Part Number	Marking	Delivery Form*	Description
AS3603-RPD-Z	AS3603JFA-Z	AS3603J	Tape and Reel	QFN48 Package Size = 6x6mm; Pitch = 0.4mm
	AS3603JFB-Z	AS3603J	Tube	
	AS3603JGA-Z	AS3603J	Tape and Reel	QFN48 Package Size = 7x7mm; Pitch = 0.5mm
	AS3603JGB-Z	AS3603J	Tube	
AS3603-HFA-Z	AS3603HFA-Z	AS3603H	Tape and Reel	QFN48 Package Size = 6x6mm; Pitch = 0.4mm, Customized Version H

Where:

R = Revision:

J = Standard

H = Customized Version

P = Package Type:

F = QFN48 6x6mm

G = QFN48 7x7mm

D = Delivery Form:

A = Tape and Reel

B = Tube

* Dry-pack sensitivity level = 3 in accordance with IPC/JEDEC J-STD-033A.

Z = Pb-Free IC Package

12 Errata

Marking	Status	ASIC ID2	Issue/Changes/ New Functions	Remark	Workaround
AS3603J, AS3603H	Available	59, 58	V2_5 voltage during shutdown.	During shutdown, the V2_5 voltage can exceed the specified range (2.4 to 2.6V; possible values are between 2.3 and 2.7V)	Do not use V2_5 externally, or do not enter shutdown.
			Charge pump power-off issue.	If not in shutdown mode and the charge pump is switched off (bit cp_on (page 38) = 0), it continues to operate with a different frequency.	Do not set bit cp_on = 0 (charge pump off); entering shutdown is allowed.

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