AS1851A/31A — Digital Power PoE PD Controllers w/HV Isolation & Synchronous DC-DC Converter

GENERAL DESCRIPTION

The AS1851A and AS1831A devices each integrate Akros *GreenEdge*™ High Voltage Isolation technology with Power-over-Ethernet (PoE) PD and Synchronous DC-DC power conversion technology.

The AS1851A includes a 13W/25W (Type 1 and Type 2) IEEE®802.3af/at compliant PD integrated with high-voltage isolation and a digital power Synchronous DC-DC converter.

The AS1831A includes a 13W (Type 1) IEEE®802.3af/at compliant PD integrated with high-voltage isolation and a digital power Synchronous DC-DC converter.

In addition to enabling digital PoE power conversion, Akros *GreenEdge*™ isolation enables direct digital management of both isolated Primary power and Secondary system power for real time end-to-end Green Power application capabilities.

TYPICAL APPLICATIONS

- Voice-over-IP (VoIP) phones
- Wireless LAN & WiMAX access points (WAP)
- Pan, Tilt, Zoom (PTZ) Cameras, IP cameras
- Thin-client and notebook computers
- Fiber-to-the-home (FTTH) terminals
- Point-of-sale (PoS) terminals, RFID readers

ORDERING INFORMATION

The AS1851A and AS1831A pin-compatible devices are available in 64-lead QFN Reduction of Hazardous Substance (RoHS) compliant packages.

Part #	Type 1 PD	Type 2 PD	Hardware Mode	Software Mode	Pwr In (W)
AS1851A*	x	x	x	x	13/30
AS1831A*	x		x	x	13

* Industrial Temperature Range, -40°C to 85°C

FEATURES

Digitally Isolated Programmable Power

PoE PD Controller

- Type 1 and Type 2 IEEE® 802.3af & 802.3at Compliant PD (AS1851A), Type 1 only (AS1831A)
- Automatic PoE-Plus (Type 2) detection in HW and I²C Modes (AS1851A only)
- Low Resistance PD Power FET Switch (0.5Ω typical)

Primary-Side DC-DC Controller

- High-efficiency DC-DC Controller with Digital Optimization
- Primary-Secondary High-voltage integrated Digital Isolation
- Programmable Primary Clock Frequency Local-power operation Down to 9.5V

Secondary-Side Sync Power Output

- Synchronous Controller with programmable power-FET timing for high efficiency at both light and full load
- Programmable PWM Frequencies synched to External Clock

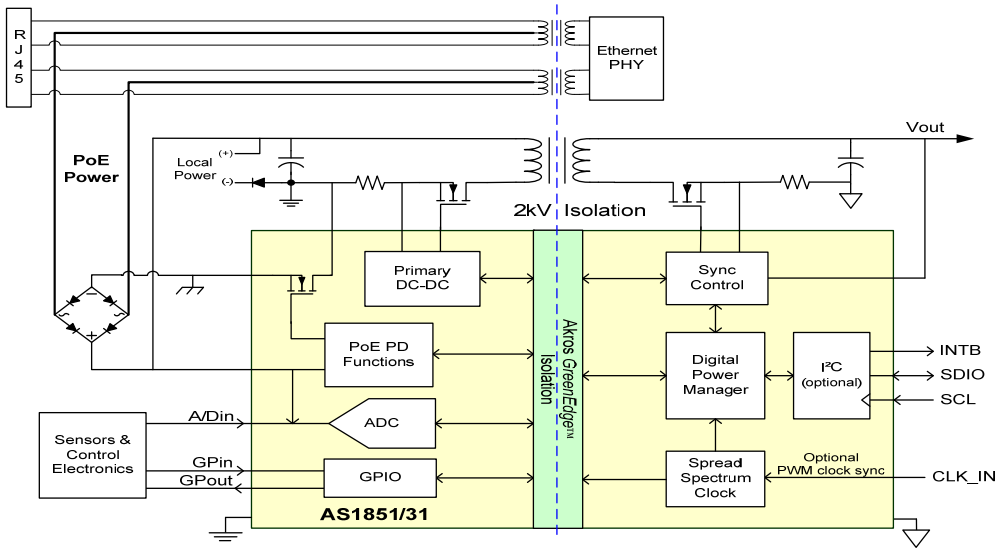
Power Management

- Hardware programmable start-up power sequencing
- Primary-side power monitoring & control from Secondary-side
- Individual output Power-Good management
- Voltage margining for each output
- Primary GPIO/ADC controlled via Secondary GPIO or I²C
- 5V µC-compatible with interrupt on alarm services
- Programmable watchdog timer

EMC Compliance and Protection

- Slew-rate-controlled power drivers
- External PWM sync clock option
- Optional spread-spectrum clocking, SW controlled
- Over-current, Under/Over-voltage and Short-circuit Protection
- High-temperature warning and shutdown
- Meets IEC 61000-4-2/3/4/5/6, IEC60747, IEC 60950, DIN EN60747-5-2 (VDE0884), & UL1577 requirements for EMC compliance and basic isolation to 2120 VDC (1500 VRMS)
- 100V Process for PoE transient voltage robustness

SIMPLIFIED APPLICATION DIAGRAM



Akros Silicon, Inc.
6399 San Ignacio Avenue, Suite 250, San Jose, CA 95119 USA
408.746.9000 ▪ http://www.AkrosSilicon.com

TABLE OF CONTENTS

FIGURES

TABLES

PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 1 - AS1851A/31A Pin Assignments

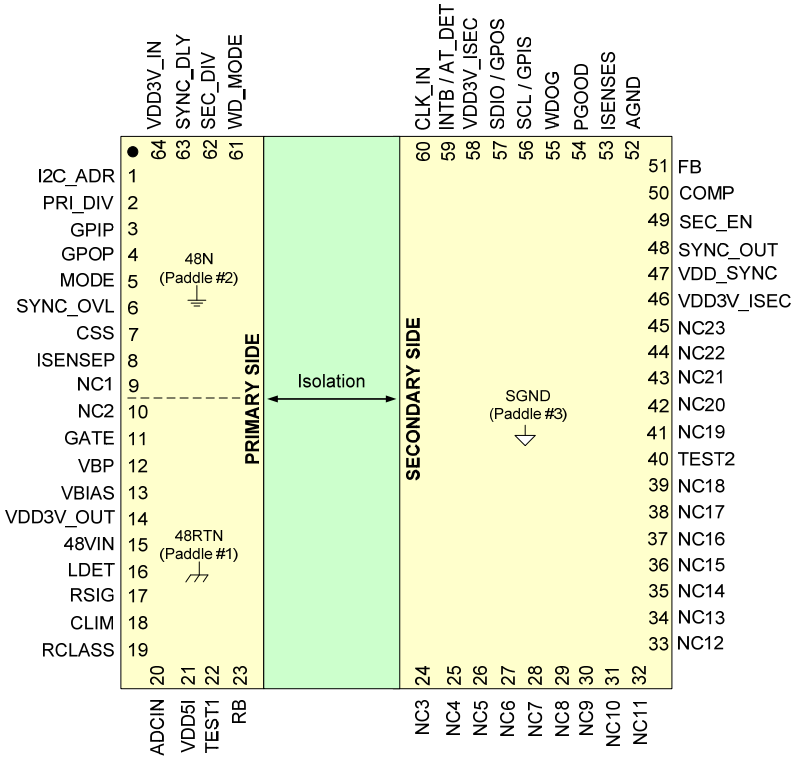


Table 1 - AS1851A/31A Signal Descriptions - Primary Side

Pin	Name	I/O[1]	Description
Primary-Side: PD Controller			
15	48VIN	P	AS1851A/31A startup power input.
Paddle #1	48RTN	P	Input power return. One of three bottom side device connections, 48RTN (Paddle #1) is connected to the internal PD Power MOSFET source. 48RTN is connected to 48N (Paddle #2) via this internal inrush current limiting power MOSFET.
Paddle #2	48N	P	Primary-side Transformer power return. One of three bottom side device connections, 48N (Paddle #2) provides the power return for the DC-DC controller transformer primary. 48N is connected to the internal PD Power MOSFET drain. 48N is connected to 48RTN via this internal inrush current limiting power MOSFET.
16	LDET	D, I	Local Power Enable Input. Enables use of local power for the DC-DC controller and disables PD functions. When activated this disables the PoE PD signature capability that normally uses the RSIG signature resistor. Refer to Figure 3 for a typical LDET circuit configuration and Table 14 for resistor values. If Local power detection is not required, connect LDET to 48VIN. Note that LDET must NOT be tied to 48RTN. In Software mode, the LDET status can be read from the PD Status & Control Register.

19	RCLASS	A	PoE Classification Resistor. See Table 12 for resistor value. Connect the classification resistor between this input and the 48RTN (Paddle #1). The resistor is automatically disconnected after a valid PD classification.
17	RSIG	A, I	PoE Signature Resistor. Connect a 26.7KΩ signature resistor from RSIG to 48VIN. This resistor is automatically disconnected after a valid PD detection.
18	CLIM	I	Sets internal PD Power MOSFET current limit in PoE operation mode; should be pulled either High (VDD5I) or Low (48RTN). In Local Mode (LDET active), CLIM is not used. For AS1851A: High = VDD5I = ILIM_AT (see Electrical Characteristics) Low = 48RTN = ILIM_AF (see Electrical Characteristics) For AS1831A: Must be Low = 48RTN = ILIM_AF (see Electrical Characteristics)
Primary-Side: Common Power Pins			
12	VBP	P	Internal bias node, decouple with an external capacitor to VBIAS.
13	VBIAS	P	Bias voltage input (typically from a power transformer winding).
14	VDD3V_OUT	P	Primary-side supply voltage source (3.3 volts). This supply can be used for additional external circuits on the primary side that are referenced to 48N, see Electrical Characteristics for supply limits.
64	VDD3V_IN	P	Primary-side input supply voltage (3.3 volts) normally connected to VDD3_OUT.
21	VDD5I	P	Low power node that can be used to supply 48RTN referenced devices, see Electrical Characteristics for supply limits. Must be decoupled with an external capacitor.
23	RB	I, PU	PD Controller state machine Power-on-Reset, connect to 48RTN with external capacitor.
Primary-Side: DC-DC Controller			
7	CSS	A	Primary-side PWM Soft Start input, decouple to 48N with an external capacitor.
11	GATE	A	Primary-side external Power FET gate drive.
8	ISENSEP	A	Current sense input, also used to set Primary PWM current limit (with external resistor).
63	SYNC_DLY	A	Along with SYNC_OVL this signal sets Primary and Secondary-side primary sync delay timing for the Output. Connecting a resistor to ground (48N) from this input will optimize output efficiency for a given PD power level or Sync Power-FET choice. See Table 17 for resistor value selection and other details.
6	SYNC_OVL	A	Along with SYNC_DLY this signal sets Primary and Secondary-side primary sync overlap timing for the Output. Connecting a resistor to ground (48N) from this input will optimize output efficiency for a given PD power level or Sync Power-FET choice. See Table 17 for resistor value selection and other details.
Primary-Side: Clock Dividers			
2	PRI_DIV	A, I	Primary PWM frequency divider input. Connect an external resistor (5%) from this input to ground to set the Primary PWM clock divider. Used in either internal or external (if the CLK_IN input is active) clocking operation. Note that the Primary PWM clocking rate is a function of both PRI_DIV and SEC_DIV divider ratios.
62	SEC_DIV	A, I	Secondary PWM frequency divider input. Connect an external resistor (5%) from this input to ground to set the Secondary PWM clock divider for either internal or external (if the CLK_IN input is active) PWM clocking operation. Note that the Secondary PWM clocking rate is a function of this SEC_DIV divider ratio. See PWM Clock Generation description for details.
Primary-Side: Inputs & Outputs			
3	GPIP	I, PU	General purpose digital input on primary side, referenced to 48N. See GPIO operation.
4	GPOP	O	General purpose digital output on primary side, referenced to 48N. See GPIO operation.

20	ADCIN	A, I	General purpose ADC input, referenced to 48RTN.
1	I2C_ADR	A, I	Sets the AS1851A/31A I²C device address. One of 8 possible Device addresses is configured by connecting a resistor on this input to ground (48N). As a result of the chosen resistor, 3 bits of available addressing for the device are configured. See Table 18 for resistor values and other details.
61	WD_MODE	I	Watchdog Timer mode. Enables/disables watchdog timer and sets timer period, operation also varies with MODE input setup. **For Hardware Mode Operation:** WD_MODE = Low (connect to 48N): watchdog off. WD_MODE = Capacitor to 48N: A 1 second timeout generates a PGOOD output transition. WD_MODE = High (connect to VDD3V_OUT): A 32 second timeout generates a PGOOD output transition. **For Software Mode Operation:** WD_MODE = Low (connect to 48N): watchdog off. WD_MODE = Capacitor to 48N: Power-on enables watchdog usage and counter starts (at max count) after PGOOD indicates good power. Use the Watchdog Timeout Register to change timeout count. Watchdog servicing is via Hardware or I²C commands. WD_MODE = High (connect to VDD3V_OUT): Power-on enables watchdog usage but waits for software to enable before starting. Use Watchdog Timeout Register for timeout length (reset to max). Watchdog servicing is via Hardware pin or I²C commands.
5	MODE	I	The MODE pin selects the device operation mode at power-on. For Hardware Mode Operation: – Mode 1 = Reset mode o Mode 1 is selected by holding the MODE pin Low (MODE to 48N). – Mode 2 = HW Operating Mode o Mode 2 is selected with a pull-up resistor (17.8KΩ max) from MODE to VDD3V_OUT plus a required power-on reset capacitor from MODE to 48N. For Software Mode Operation: – Mode 1 = Reset mode o Mode 1 is selected by holding the MODE pin Low (MODE to 48N). – Mode 2 = SW Operating Mode with I²C device address per I2C_ADR pin setting o Mode 2 is selected with a required power-on reset capacitor from MODE to 48N.
Primary-Side: Miscellaneous			
22	TEST1		Must be pulled down to 48RTN with a resistor (4.7KΩ-100KΩ).
9, 10	NC1, NC2		No User Connection. Must be floated.

[1] I = Input, O = Output, I/O = Bidirectional, PU = Internal pull-up, PD = Internal pull-down, P = Power, A = Analog, D = Digital, OD = Open drain

Table 2 - AS1851A/31A Signal Descriptions - Secondary Side

Pin	Name	I/O[1]	Description
Secondary-Side: Common Power Pins			
46, 58	VDD3V_ISEC	P	Secondary-side 3.3V power inputs. Sourced from Vout (if Vout=3.3V), or other external supply.
Paddle #3	SGND	P	Secondary-side ground connection. One of three bottom side device connections, SGND (Paddle #3) is the Secondary-side ground connection.
Secondary-Side: Synchronous Rectification Controller (Vout)			
47	VDD_SYNC	A	Sync FET power decoupling node. Decouple with an external capacitor, VDD_SYNC to SGND. This node is nominally 5V.
51	FB	A	Controller voltage feedback input.
53	ISENSES	A	Controller secondary-side sync switches node current sense. Sensed signal is used to control the external secondary-side power FET, making it an efficient power diode.
50	COMP	A	Controller compensation network connection.
48	SYNC_OUT	A	Controller sync gate drive output. Used for secondary-side synchronization in conjunction with the primary-side controller.
52	AGND	P	Controller secondary-side sense ground, used for both differential feedback and differential current sensing. Should be routed differentially, as the pairs of FB & AGND and ISENSES & AGND.
Secondary-Side: I^2C Interface (or I/O in Hardware Mode)			
57	SDIO / GPOS	OD	SDIO in Software mode, used for I^2C bi-directional data input/output. GPOS in Hardware mode, this output reflects the GPIP pin state (from the primary side).
56	SCL / GPIS	I / I	SCL in Software mode, used as the I^2C clock input. GPIS in Hardware mode is an input that drives the GPOP pin state (on the primary-side).
59	INTB / AT_DET	OD	INTB in Software Mode. The I^2C interface interrupts output, active low. The open drain output allows user defined voltage output high level. AT_DET in Hardware Mode. It is the PoE+ (802.3at) PSE detect indication output. A High level output indicates connection to either a Type 2 PSE or to a Local Power supply. The output is open drain, active High. If a Type 1 PSE is connected, the output of AT_DET remains in the inactive state (Low).
Secondary Side: Inputs & Outputs			
60	CLK_IN	I, PU	DC coupled optional clock input for timing of Primary and Secondary DC-DC regulators & controllers if synchronizing to an external time source is desired. Nominally sourced from the local Ethernet master clock.
54	PGOOD	OD	Logical “AND” of global power good & watchdog status. High = All enabled voltages (#1 with any or all of #2, #3, and #4) are within voltage spec and there is presently no watchdog timeout. Low = one or more of enabled voltages out of spec, or, the watchdog has timed out. Note that PGOOD operation is different for Hardware and Software modes of operation (selected by the MODE input). For Hardware mode PGOOD operation details see HW Mode Power Monitoring (PGOOD). For Software mode PGOOD operation details see SW Mode Power Status Monitoring (PGOOD).
55	WDOG	I	Watchdog timer input, used for hardware reset of the watchdog timer (if enabled). Serviced with a transition of either polarity.
Secondary Side: Miscellaneous			
49	SEC_EN	I, PU	Secondary-side Enable. A capacitor on this input to SGND is required.
40	TEST2		Must be pulled down to SGND with a resistor (100KΩ).
Pins 24-39, 41-45	NC3-NC18, NC19-23		No User Connection. Must be floated.

[1] I = Input, O = Output, I/O = Bidirectional, PU = Internal pull-up, PD = Internal pull-down, P = Power, A = Analog, D = Digital, OD = Open drain

TEST SPECIFICATIONS

Table 3 - Absolute Maximum Ratings

Parameter	Max	Unit
48VIN, 48N, RSIG: to 48RTN	100 [1]	V
48VIN: to 48N	100 [1]	V
48VIN, 48N, RSIG: to 48RTN (under steady-state conditions)	60 [2]	V
48VIN: to 48N (under steady-state conditions)	60 [2]	V
GATE, VBIAS, VBP: to 48N	20	V
LDET: to 48VIN	no more than 6V less than 48VIN	V
RCLASS, CLIM, RB, VDD5I: to 48RTN	6	V
ADCIN to 48RTN	4	V
VDD3V_OUT, VDD3V_IN: to 48N	4	V
ISENSEP, CSS, SYNC_DLY, SYNC_OVL, MODE, GPIP, GPOP, PRI_DIV, I2C_ADR, SEC_DIV, WD_MODE: to 48N	4	V
VBOOST: to SGND	12	V
CLK_IN, ISENSES, SEC_EN, COMP, AGND, PGOOD, VDD3V_ISEC: to SGND	4	V
FB, VDD_SYNC, SYNC_OUT, INTB/AT_DET, SCL/GPIS, SDIO/GPOS, WDOG: to SGND	6	V
ESD Rating, Human body model (per JESD22-A114)	2	kV
ESD charged device model	500	V
ESD machine model	200	V
ESD System level (contact/air) at RJ-45 (per IEC61000-4-2)	8/15	kV
Storage Temperature	165	°C
Operating Junction Temperature	125	°C

[1] The AS1851A/31A has a fast internal surge clamp for transient conditions such as system startup and other noise conditions; the device must not be exposed to sustained over-voltage condition at this level.
[2] Under steady state conditions; higher voltage level is acceptable under transient conditions.
Unless otherwise noted all Test Specifications apply over the full -40°C to 85°C operating temperature range.

Table 4 - Normal Operating Conditions

Parameter	Min	Typ[1]	Max	Unit	Conditions
VIN_AF	37	48	57	V	Measured at the Network Interface
VIN_AT	42.5	48	57	V	Measured at the Network Interface
VAUX (optional local power)	9.5		57	V	Measured at 48VIN for full VLDET range (referenced to 48N)
Thermal Resistance, Junction to Case, θ_{JC}		5		°C/W	Operating Junction Temperature 125°C, max
Thermal Resistance, Junction to Ambient, θ_{JA}		20		°C/W	Operating Junction Temperature 125°C, max
Operating temperature range	-40		85	°C	

[1] Typical specification not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 5 - PD Section Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions[2]
IINRUSH_AF	Inrush current limit - AF PD		120		mA	13W
IINRUSH_AT	Inrush current limit - AT PD		240		mA	30W
ILIM_AF	PoE current limit - AF PD	350	400	500	mA	13W, CLIM = 48RTN
ILIM_AT	PoE current limit - AT PD	720	750	1000	mA	30W, CLIM = VDD5I
RDS_ON	PD Power MOSFET Switch on Resistance		0.5	0.9	Ω	As measured between 48RTN and 48N with source of 48V and 200ma current.
VRESET_MIN	Minimum reset voltage level			2.81	V	Measured at the Network Interface[2].
VSIGMIN	Minimum Signature voltage			2.7	V	Measured at the Network Interface[2].
VSIGMAX	Maximum Signature voltage	10.1			V	Measured at the Network Interface[2].
VCLASSMIN	Minimum Classification voltage			14.5	V	In classification, the AS1851A/31A sinks current as defined in Table 12, measured at the Network Interface[2].
VCLASSMAX	Maximum Classification voltage	20.5			V	In classification, the AS1851A/31A sinks current as defined in Table 12, measured at the Network Interface[2].
VMARKMIN	Min Mark Event voltage		5.2	6.90	V	Measured at the Network Interface[2].
VMARKMAX	Max Mark Event voltage	10			V	Measured at the Network Interface[2].
IMARK	Mark Event current	0.5	2.1	4	mA	Measured at the Network Interface[2].
VCLASSRSET	Classification Reset threshold	2.81	5.2	6.90	V	Measured at the Network Interface[2].
VACT	Full power activation UVLO threshold, voltage rising		37	42	V	Measured at the Network Interface[2].
VDEACT	Full power de-activation UVLO threshold, voltage falling	30			V	Measured at the Network Interface[2].

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.

[2] All measurements at the Network Interface are before the PD diodes (assuming a 1.2V drop across the PD diodes).

Table 6 - Primary Side Digital, I/O, and A/D Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VDD3V_OUT	Voltage from internally generated 3V source.	3.0	3.3	3	V	Decouple VDD3V_OUT with 4.7µF cap. Referenced to 48N.
IVDD3V_OUT	Current output from internally generated 3V source.			5	mA	Decouple VDD3V_OUT with 4.7µF cap. Referenced to 48N.
VDD3V_IN	3V primary side voltage inputs.	3.0	3.3	3	V	Supplied by VDD3_OUT, Referenced to 48N.
VDD5I	Voltage from internally generated 5V node.	4.0	5	6.0	V	Decouple with 1.5µF cap, referenced to 48RTN.
IVDD5I	Current output from internally generated 5V node.			5	mA	Decouple with 1.5µF cap, referenced to 48RTN.
VHGPOP	GPOP voltage output – high	3.0			V	Current at GPOP = 1.0 mA (VDD3V_IN=3.3V, referenced to 48N).
VLGPOP	GPOP voltage output – low			0.4	V	Current at GPOP = -1.0 mA (VDD3V_IN=3.3V, referenced to 48N).
VHGPIP	GPIP voltage input - high	2.0			V	(VDD3V_IN=3.3V, referenced to 48N).
VLGPIP	GPIP voltage input - low			0.8	V	(VDD3V_IN=3.3V, referenced to 48N).
TGPIO	Primary side GPIO pin latency to register update.			10^2	ms	Independent of I^2C clock speed. Pin I/O is automatic to and from I^2C registers.
TADCIN	ADCIN pin latency to register update.			10^2	ms	Independent of I^2C clock speed. Pin I/O is automatic to and from I^2C registers.
VADCIN	ADCIN voltage range	0		2.5	V	Referenced to 48RTN.

RADCIN	ADCIN resolution	8	bits	Referenced to 48RTN.
ADCERROR	ADCIN total unadjusted error	±TBD[3]	LSB	Referenced to 48RTN.
ILADCIN	ADCIN input leakage current	100[2]	nA	Referenced to 48RTN.
CADCIN	ADCIN input capacitance	0.3[2]	pF	Referenced to 48RTN.

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.
[3] Includes offset, full-scale, and linearity.

Table 7 - Primary Side DC-DC Controller Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VIN_AF	Type 1 PD input voltage	37	48	57	V	Measured at the Network Interface
VIN_AT	Type 2 PD input voltage	42.5	48	57	V	Measured at the Network Interface
VAUX	Input Voltage, Local Power Mode	9.5		57	V	Measured at 48VIN (referenced to 48N) over full VLDET range
VLDET_ON	Local input voltage threshold for Local Power Mode - ON	48VIN -2.4V			V	See Table 3 for Absolute Maximum Rating for LDET (referenced to 48VIN).
VLDET_OFF	Local input voltage threshold for Local Power Mode - OFF			48VIN -1.2V	V	
VBIAS	External bias source voltage	8[2]		14[2]	V	Sets VOH of GATE.
FPWM1L	Low end of Primary PWM switching frequency range		104		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 15.
FPWM1H	High end of Primary PWM switching frequency range		512		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 15.
FOSC1	PWM1 clock frequency accuracy	-20		+20	%	See Table 15 for frequency.
FPWM1T	PWM switching frequency temperature coefficient		0.12		%/C°	Refer to Table 15 for PWM Frequency.
RH_GATE	GATE drive impedance		6		Ω	High side output drive resistance, Source.
RL_GATE	GATE drive impedance		6		Ω	Low side output drive resistance, Sink.
VPK1P	Peak current sense threshold voltage at ISENSEP		395		mV	Ipeak = VPK1P / RISENSEP.
DMAX1	Primary PWM Maximum duty cycle	80[3]			%	
DMIN1	Primary PWM Minimum duty cycle			10[3]	%	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by characterization. Not tested in production.
[3] Guaranteed by design. Not tested in production.

Table 8 - Secondary Side Sync Controller (Output) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VSYNC_OUT	SYNC_OUT voltage	4.5	5	6	V	
RH_SYNC	SYNC_OUT Source Impedance VDD_SYNC = 5V			2.5	Ω	Source
RL_SYNC	SYNC_OUT Source Impedance VDD_SYNC = 5V			2.5	Ω	Sink
VMR	Output voltage margining range		±5		%	Software mode, see Table 35.
VREF	FB voltage reference	0.98	1.0	1.02	V	
ILEA	Error amp leakage			1[2]	µA	
Gm	Feedback Transconductance (Siemens)	150	225	350	µS	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 9 - Secondary Side Digital I/O and I²C Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VDD3V_ISEC	Secondary Side Power Supply Input Voltage	3.0	3.3	3	V	Sourced from Vout (if 3.3V) or other external supply
FCLK_IN	External Clock Input Frequency	23.75	25	26.25	MHz	
VCLK_IN_HI	CLK_IN input voltage threshold - high	2.0			V	
VCLK_IN_LOW	CLK_IN input voltage threshold - low			0.8	V	
IOINTB	INTB/AT_DET open drain current drive	1			mA	With $V_{PULL-UP}$ = TBD and $R_{PULL-UP}$ = TBDKΩ, V_{INTB} (typ) = TBD
IOPG	PGOOD open drain current drive	1			mA	With $V_{PULL-UP}$ = TBD and $R_{PULL-UP}$ = TBDKΩ, V_{PGOOD} (typ) = TBD
TPGOOD	PGOOD minimum pulse output (High-Low-High)	10[2]			ms	
TWDOG	Watchdog minimum reset pulse width (WDOG pin)	100[2]			ns	
VHGPOS	GPOS voltage output – high (referenced to SGND)	3.0			V	Current at GPOS = 1.0 mA (VDD3V_ISEC=3.3V, referenced to SGND)
VLGPOS	GPOS voltage output – low (referenced to SGND)			0.4	V	Current at GPOS = -1.0 mA (VDD3V_ISEC=3.3V, referenced to SGND)
VHGPIS	GPIS voltage input – high (referenced to SGND)	2.0			V	(referenced to SGND)
VLGPIS	GPIS voltage input – low (referenced to SGND)			0.8	V	(referenced to SGND)
FSCL	I²C Clock Frequency	10		400	KHz	5V tolerant input
VIH	I²C HIGH level input voltage	1.4			V	5V tolerant input
VILI2C	I²C LOW level input voltage			0.5	V	5V tolerant input
VOLI2C	I²C Output low voltage for pull-up voltage (VDD)			0.4	V	VDD > 2V, 2 mA sink
VOLI2C	I²C Output low voltage for pull-up voltage (VDD)			0.2 VDD	V	VDD < 2V, 2 mA sink
CDIO	Capacitance for each Digital I/O pin			10[2]	pF	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 10 - Thermal Protection Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
TSD	Thermal shutdown temperature		140		°C	Above this temperature, the AS1851A/31A is disabled.
TI2C	Thermal warning temperature for I²C warning		115		°C	
THYS	Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 11 - Isolation Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
IIO_ISO	Input-output insulation			1.0[1]	µA	RH (Relative Humidity) = 45%, Ta = 25°C, t = 5s leakage current VIO_ISO = 2250 VDC
VISO_DC	Withstand insulation voltage DC	2120[1]			VDC	RH ≤ 50%, Ta = 25°C, t = 1 min
VISO_AC	Withstand insulation voltage AC	1500[1]			V_{RMS}	RH ≤ 50%, Ta = 25°C, t = 1 min
RIO_ISO	Resistance (input to output)		TBD[1]	TBD[1]	Ω	VIO = 250 VDC
CM	Common mode transient		10.0[2]		kV/µs	

[1] Device is considered a two terminal device: Primary pins are shorted together and Secondary pins are shorted together.
[2] All outputs to remain within ±3% tolerance during transient.

FUNCTIONAL DESCRIPTION

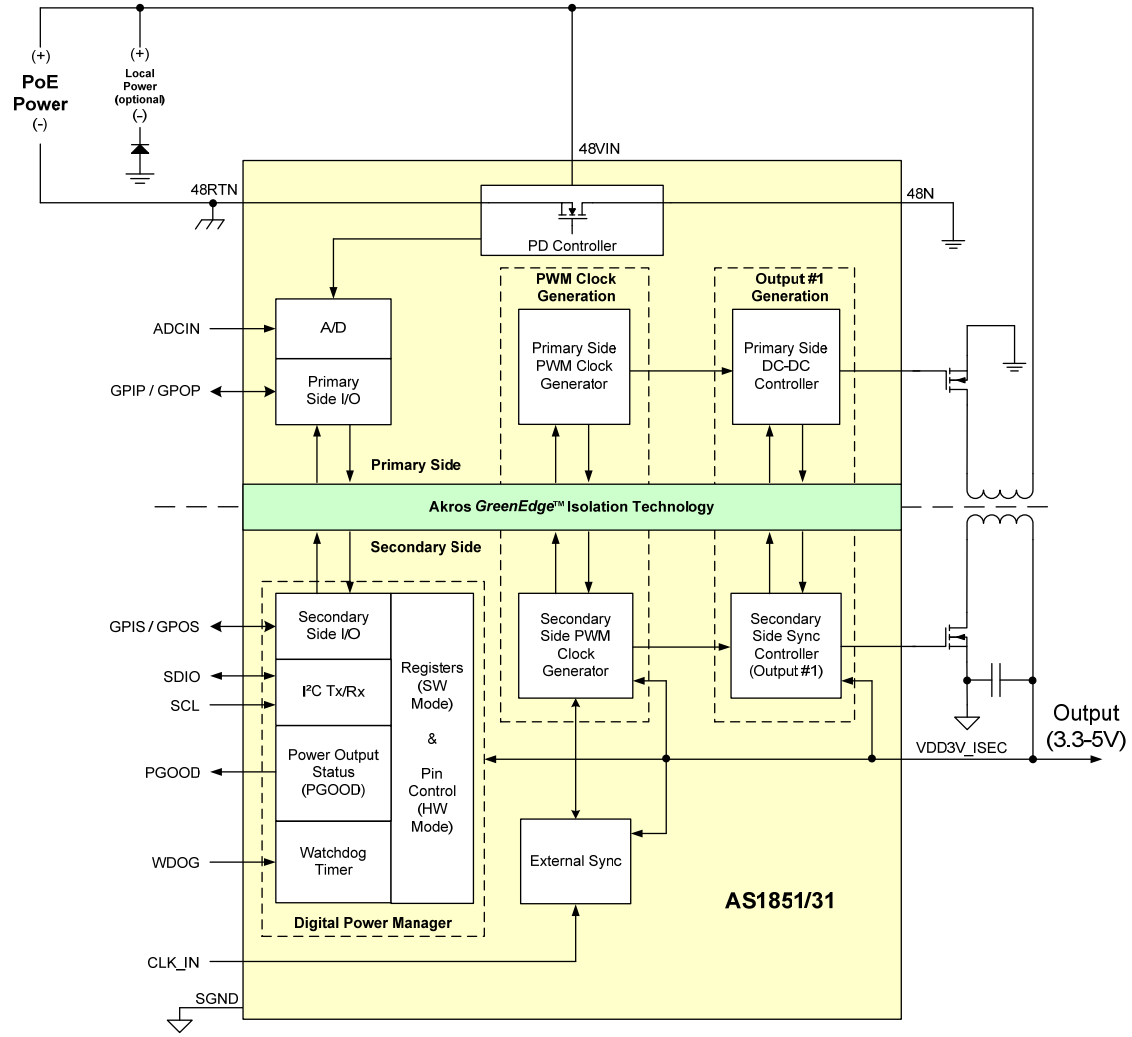
Figure 2 shows the block diagram of the AS1851A/31A. The individual blocks are described in greater detail in the following paragraphs.

(Please also refer to these separate Akros documents for the AS1851A/31A: AN080 for a detailed Design Guide and AN082 for a detailed Software Users Guide.)

ISOLATION

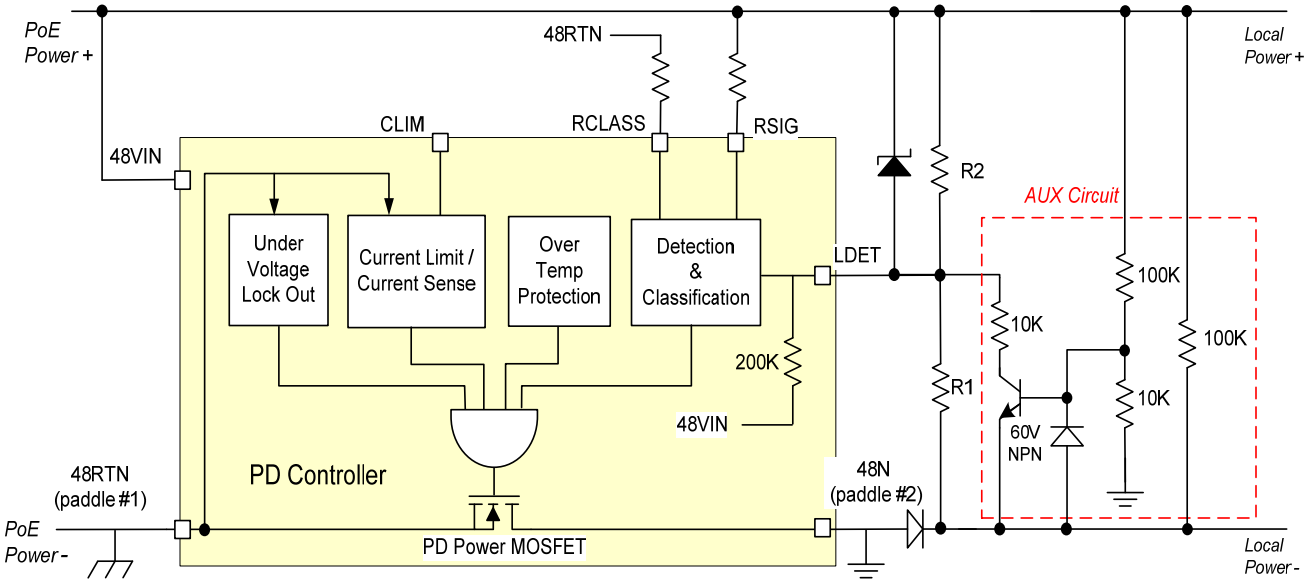
As shown in Figure 2, the AS1851A/31A is divided internally into Primary and Secondary sides. All signals that interconnect the Primary and Secondary sides are isolated using Akros *GreenEdge*™ technology eliminating the need for opto-isolators in both analog power control loop and the digital I²C paths between Primary and Secondary ground planes.

Figure 2 - AS1851A/31A Block Diagram



PD CONTROLLER

Figure 3 - AS1851A/31A PD Controller Block Diagram



The AS1851A/31A contains a fully integrated PD Controller (see Figure 3) that meets all system requirements for the IEEE® 802.3 standard for Ethernet, and, all PD power management requirements for IEEE® Standards 802.3af and 802.3at. See the Power over Ethernet overview in this datasheet for additional PoE information.

PD Power MOSFET

Ethernet power source current is controlled with an integrated low-leakage, low RDSON, NMOS power MOSFET that is used to connect the 48RTN and 48N ground planes. If necessary the FET is throttled back or switched off to protect the AS1851A/31A from damage due to problematic voltage, current, or temperature related conditions.

Under-voltage Lockout (UVLO)

The UVLO circuitry detects low power source voltage conditions and disconnects the power MOSFET to protect the PD (see full power voltage activation and deactivation threshold specifications in the PD Electrical Characteristics).

PoE Current Limit/Current Sense

Current Limit/Current Sense circuitry minimizes on-device temperature peaks by limiting both inrush current and operating current. It monitors the current via an integrated sense circuit that regulates the gate voltage to the PD Power MOSFET.

This inrush current limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges, an action that aids in preventing the PSE from going into current limit mode.

The PoE current limit is set by the CLIM input pin during PoE operating modes. When CLIM is set Low (48RTN) current is limited to 350mA (min); when High (AS1851A only) 720mA (min). If the maximum primary current is exceeded, control of the internal PD Power MOSFET is used to protect the system from overload. In Local Power mode (LDET active), this CLIM based current control is not used (primary side external FET sensed current control can always be used).

Over-temperature Protection

If die temperature exceeds 140°C (typ) the AS1851A/31A is shut down. Power is automatically reapplied when the die temperature returns to 100°C (typ).

PD Operating States

The AS1851A/31A has five states of PD operation:

- ***Reset*** - The classification state machine is reset, and all circuitry blocks are disabled.
- ***Signature Detection*** - The PD signature resistance is applied across the input.
- ***Classification*** - The AS1851A/31A indicates power requirements to the PSE.
- ***Idle*** - This state is entered after classification, where it remains until full-power input voltage is applied.
- ***ON*** - The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry. In this state the PD also provides a Maintain Power Signature (MPS) state as required by the IEEE® PoE standard.

As the supply voltage from the PSE increases from 0V, the AS1851A/31A transitions through these operating states:

These five operating states have specific transition criteria per the IEEE® PoE standard.

PD Reset State

When the voltage supplied to the AS1851A/31A drops below VRESET_MIN, the device enters the reset state. In reset state, the AS1851A/31A consumes very little power, the power supply to the PD is disconnected and state condition reverts to pre-classification.

PD Signature Detection State

During signature detection, the PSE applies a voltage to read the PD power signature and validates the PD as standards compliant.

To ascertain the power signature the PSE applies two voltages in the signature voltage range and extracts a signature resistance value from the I-V slope. The AS1851A/31A signature resistance is specified by an external resistor connected between the RSIG pin and the 48VIN pin. A 26.7kΩ external signature resistor is recommended.

Upon successful detection of the PD by a PSE the AS1851A/31A disconnects the external signature resistor at the RSIG pin to conserve power.

PD Classification State

Each class represents a power allocation level for the PD and allows the PSE to manage power requirements between multiple PDs. The AS1851A/31A supports both IEEE® Std. 802.3af, and the AS1851A supports two event classification per IEEE® Std. 802.3at (PoE+), see Figure 18.

The AS1851A/31A allows the user to set required classification current via an external resistor connected between the RCLASS pin and 48RTN (Paddle #1). See Table 12 for recommended RCLASS resistor values.

During the classification state the PSE presents a voltage between 14.5V and 20.5V which the AS1851A/31A terminates in the RCLASS resistor resulting in a PSE measurable current, Iclass.

Table 12 - Classification Map

Class	Power (Watts)	Iclass	Rclass
0	0.44-12.95	0 - 4 mA	2.05MΩ, 1%
1	0.44-3.84	9 - 12 mA	221kΩ, 1%
2	3.84-6.49	17 - 20 mA	115kΩ, 1%
3	6.49-12.95	26 - 30 mA	75kΩ, 1%
4	12.96-25.5	36 - 44 mA	49.9kΩ, 1%

Upon successful classification of the PD by a PSE the AS1851A/31A disconnects the external classification resistor at the RCLASS pin.

PD Idle State

In the Idle state (between Classification and the ON state) the AS1851A/31A current is limited to monitoring circuitry needed for detection of the ON state threshold.

PD ON State

At a voltage of 42V or higher the AS1851A/31A enters the ON state and full power is available via the DC-DC Controller.

In IEEE® PoE compliant systems the PSE remotely detects either a DC or AC Maintain Power Signature (MPS) state in the PD platform. If either the PD PoE DC current is less than 10mA or the PD input AC impedance is above 26.25KΩ the PSE may disconnect power. To guarantee such a power disconnect the PD PoE DC current must be <5mA, and, the AC impedance must be >2MΩ.

AT Detection Operation (AS1851A only)

The AS1851A has both software (I^2C register bit) and hardware (AT_DET pin) capabilities to indicate a PoE Plus platform operating mode.

The AT_DET detect feature (either pin or software) provides an indication when a PoE+ Power Source is available to the system, from either an Ethernet cable to a Type 2 PSE or via use of Local Power Supply using the LDET input pin. In the case of hardware mode the AT_DET pin can be used to directly drive an LED indicator. Since this pin is on the secondary side of the AS1851A the user can interface it directly to the PD system controller without additional

Interfacing isolation circuitry. A typical platform usage of AT_DET is to self-configure the PD platform based on available power.

If not operating on Local Power, the AT_DET indicator stays low during the PD Reset, Detection and Classification phases. This indicator will be set high once the PD recognizes completion of the 2-event Physical Layer Classification as initiated by a Type 2 PSE. The pin will remain high and be reset to zero after the occurrence of a PD Reset State (48VIN < 2.7V) or a power-down event. AT_DET remains low if the PSE partner is identified to be Type 1 during the classification phase.

Local Power Source

The AS1851A and AS1831A may also be powered from a DC source other than the Ethernet line. This local source is detected when the voltage at the LDET pin is 2 volts (typ) below the voltage at pin 48VIN. When such a local power is present the AS1851A/31A will disable the power FET and thereby disconnect from the PoE power source.

When operating in Local Power mode the AS1851A AT_DET pin does not indicate the far end PSE, and is always HIGH (see Table 13)

Refer to Figure 3 and Table 14 for typical LDET external resistor designs to match the specified Local Power configuration.

Table 13 - AT_DET and LDET Operation

LDET Mode	AT_DET Indication	
	PSE = Type 1	PSE = Type 2
LDET = Inactive (PoE power usage)	LOW	HIGH (AS1851A only)
LDET = Active (Local Power usage)	HIGH	HIGH

Table 14 - Typical LDET External Resistor Design

Local Adaptor or Local Voltage Requirement	R1 (Ω)	R2 (Ω)	AUX Circuit
36V - 57V	47K	5K	Don't Include
12V - 38V	Open	10K	Include

The maximum voltage allowed from 48VIN to LDET is 6.0V; refer to Table 3. Therefore, for protection, a 5.1 V Zener is recommended between 48Vin and LDET, as shown in figure 3.

Figure 4 shows the AS1851A/31A PWM Clock Generation block diagram. During power-up, local oscillators on both sides of the isolation boundary provide separate clocks for Primary-side and Secondary-side PWMs. After power-up internal cross-isolation management automatically transitions the AS1851A/31A PWM clock such that the Secondary-side oscillator becomes the master, and sources clocks to both Primary and Secondary sides of the isolation.

PWM Clock Frequency Configuration

Frequency of the AS1851A/31A PWM clock is set with resistors connected to the PRI_DIV and SEC_DIV pins as shown in Table 15.

External Clock Source (CLK_IN)

For additional EMI management, the CLK_IN pin provides an optional input for an external clock source to govern overall device timing. If used the local Secondary-side oscillator is slaved to CLK_IN, therefore Primary-side and Secondary-side PWM clocks are slaved to CLK_IN after power-up. The CLK_IN frequency should be 25MHz, and it is recommended that the Ethernet PHY clock be used.

EMI Performance Control

A multi-phase clocking technique is used to generate clocks for the Primary DC-DC controller and all Outputs (1-4). This improves Electromagnetic (EM) radiation performance by reducing common mode noise and also reduces the size of external capacitors.

Note that in Software mode PBRS randomization and Fractional-N modulation clocking is available for additional EM performance to reduce PWM clock induced harmonics in the power supply.

Figure 4 - PWM Clock Generation Block Diagram

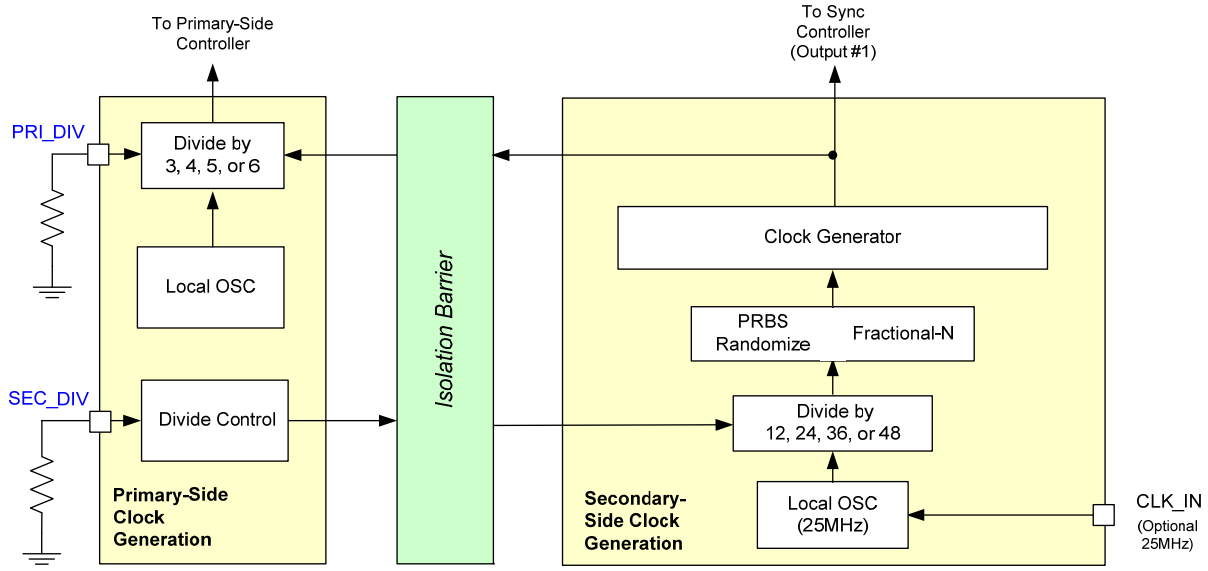


Table 15 - PWM Clock Rate Configuration

	PRI_DIV Resistor (Ω)			
	12.4K	43.2K	68.1K	100.0K
SEC_DIV Resistor (Ω)	Output PWM Clock Rate (KHz)			
12.4K	reserved	521	417	347
43.2K	347	260	208	174
68.1K	231	174	139	116
100.0K	174	130	104	reserved

NOTE: Resistor settings are the same for both Internal Oscillator or 25MHz External (CLK_IN) operation

Power Output

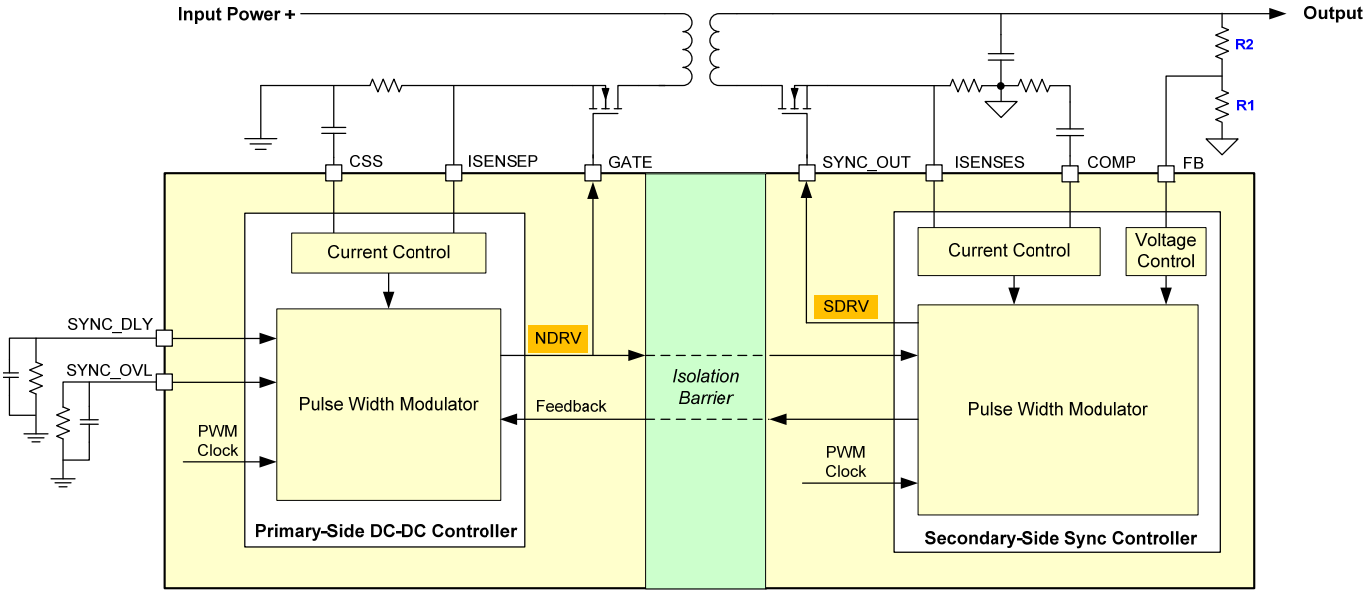
As described in the previous section, the Primary and Secondary-side PWM clocks are generated and automatically synchronized across the integrated isolation barrier. Figure 5 shows a typical synchronous Flyback design topology.

Three power control loop operations take place:

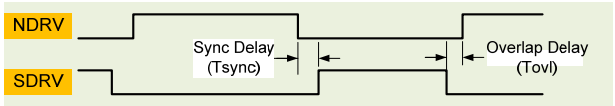
– Primary-side DC-DC controller switches the primary-side power FET from a current and voltage loop error controlled PWM.
– Secondary-side sync controller FET driver switches the Secondary-side power FET to complete the Flyback power transfer cycle.
– The automated AS1851A/31A isolation management transmits Secondary-side voltage loop feedback to the Primary-side PWM.

A typical isolated synchronous Flyback application is shown in more detail in Figure 19.

Figure 5 - Power Output Block Diagram



NDRV and SDRV timing delays, Sync Delay & Overlap Delay, are based on SYNC_DLY and SYNC_OVL resistor settings. These internally generated delays can be used to cost effectively optimize an Isolated Synchronous Flyback Design.



Primary-side DC-DC Controller

The Primary-side DC-DC Controller is a current-mode DC-DC controller which is easily configured with a minimal set of external components. Isolation is provided by the internal Akros *GreenEdge*™ circuitry which eliminates the need for external opto-isolators.

In PoE operation, the Primary-side DC-DC Controller operates from a PD Power MOSFET switched power input (48N, see Figure 2) and includes: an externally controlled soft start; a fixed (after resistor programming) frequency PWM; and a true voltage output error amplifier. In local power operation 48N is sourced directly.

Soft-Start Inrush Current Limit

Internal circuitry automatically controls the inrush current ramp by limiting the maximum current allowed in the transformer primary at startup. The amount of time required to perform this soft-start cycle is determined by a capacitor on the CSS pin. A CSS capacitor of 330nF proelianevides approximately 7ms of soft startup ramp time.

Current-Limit and Current Sense

The primary side controller provides cycle-by-cycle current limiting to ensure the transformer primary current limits are not exceeded through use of an external resistor on ISENSEP. In addition, the maximum average current in the transformer primary is set by internal PWM duty cycle limits.

A short-circuit event is declared by the primary controller if this ISENSEP sensed current limit is triggered on more than 50% of the clock cycles within any 64 cycle window. Once a short-circuit event has been declared, the Output will shut off for 1024 cycles before a restart is attempted. This process will repeat indefinitely until the output short is removed.

Secondary-side Sync Controller

The efficiency of Output can be optimized by designing a non-overlapping solution for the external FETs on the Primary side and Secondary side of the PD power transformer. The FET sync and overlap delays, as shown in **Figure 5**, are controlled by the designer to compensate for rise, fall, and delay times for both Primary and Secondary-side external power FETs. See Table 16 and note the delay timing limit: (Tsync + Tovl) ≤ 25ns.
The required resistors at SYNC_DLY and SYNC_OVL to implement the desired Tsync and Tovl timing are then calculated; see an example in Table 17. The filter capacitors to SGND for these pins (see Figure 5) are 1nF, typical.

Table 16 - Sync & Overlap Delay Timing Limit

Sync Delay (ns)	Overlap Delay (ns)	Delay Timing Limit (ns)
Tsync	**Tovl**	(**Tsync** + **Tovl**) ≤ 25ns

Table 17 - SYNC_DLY & SYNC_OVL Resistor Calculation Example

Desired SYNC Delay (ns)	Desired Overlap Delay (ns)	Delay Timing Limit Check (ns)	SYNC_DLY Resistor Required (Ω)	SYNC_OVL Resistor Required (Ω)
Tsync	**Tovl**	(**Tsync** +**Tovl**) ≤ 25ns	R_{SYNC_DLY} = (**Tsync** + **Tovl**) x 2KΩ	R_{SYNC_OVL} = **Tovl** x 2KΩ
10ns	15ns	Ok	50KΩ	30KΩ

Compensation and Loop Feedback

The output has two power compensation and feedback mechanisms:

– Adaptive slope compensation
– Primary-Secondary (feedback based) control loop

The adaptive slope compensation automatically provides an optimized ramp framework for the overall loop performance, there are no user settings required.

For the Primary-Secondary control loop the device uses an internal transconductance error amplifier with external compensation control. An external secondary-side RC compensation network should be connecting to COMP.

The resulting loop feedback path through the internal isolation channel to the primary-side PWM is automatic and completely user transparent.

Voltage feedback input is provided at the FB pin. At FB, an internal reference of 1V (nominal) is compared to a resistor divided voltage from the output. This sets the desired output voltage level. With the top resistor in the feedback divider designated R2 and the bottom resistor designated R1 (again refer to Figure 5) the programmed voltage for the output is equal to Vref times (R1+R2)/R1. So, for example, with R1=5K, R2=20K, and Vref=1V, the output voltage is set to 5V.

Low-load Current Operation – DCM

The primary output uses both DCM and Pulse Skipping (Burst Mode) design techniques to optimize power efficiency. When a low-load output power condition is detected, the Controller automatically enters a discontinuous current mode (DCM) of operation.

Over-voltage Protection

A built-in over-voltage monitor is set to +10% of nominal voltage. If tripped, the output shuts down until within +5% of the nominal voltage at which point normal operation is then resumed.
If Voltage Margining is used (see Software Mode Operation) the over-voltage protection tracks to the margining selected.

RF & EMI Filtering

In order to mitigate RF interference & EMI, two 4.7nF/2kV capacitors must be connected between 48N and SGND. Capacitor placement is critical.
It is essential that one capacitor be placed underneath the IC on the back side directly across the paddles.
This minimizes the area of the antenna formed by this capacitor between the grounds on the board and prevents RF interference being coupled into the control loop. The second capacitor should be placed next to the transformer.

It is also recommended that a 100Mohm resistor be connected to prevent charge buildup during repetitive ESD events.

HARDWARE MODE OPERATION

The Hardware mode of operation is designed to provide basic control and status of the device via hardware (pin) control signals. Hardware mode functions and operation are described below.

(Please also refer to the Akros document AN080 for a detailed Design Guide.)

Device Initialization & Hardware Mode Selection

Primary-side digital logic is initialized while the MODE pin is Low, A required external capacitor between MODE and 48N provides the power-on reset input required to initialize the device.

Hardware (HW) mode is selected when the MODE pin is also pulled-up High (in addition to the power-on reset capacitor to 48N). The VDD3V_OUT pin can be used for the MODE pin pull-up power source by using a 17.8KΩ (maximum) resistor from MODE to VDD3V_OUT.

Secondary-side digital logic is initialized while the SEC_EN pin is Low, a required external capacitor between SEC_EN and SGND will provide the power-on reset input required to initialize the secondary-side. See Figure 6.

Figure 6 - Hardware Mode Secondary Power-On Sequence

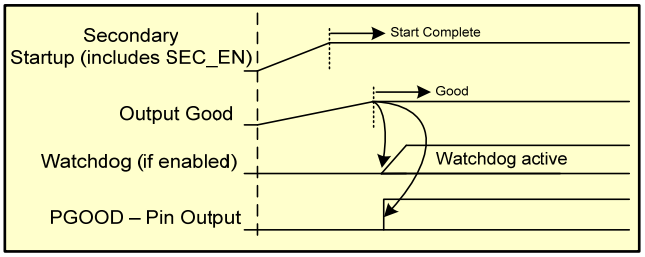
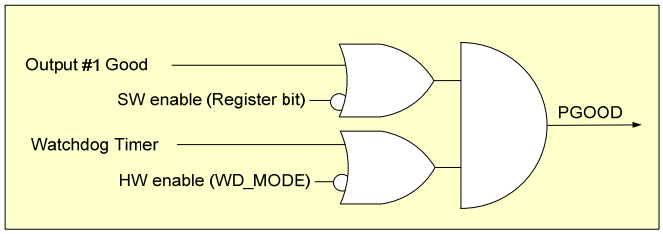


Figure 7 - Hardware Mode PGOOD Generation



HW Mode Power Monitoring (PGOOD)

The output is monitored for power good status, once it reaches a stable state, its internal power good status signal is asserted. Power good is declared (good) at +/- 5% and at fault (bad) at +/- 10% of final voltage value. In either transition case (good to/from bad), continuous operation of 10µS is required before the state change is declared. The user sees the resulting status on the PGOOD pin (10ms minimum pulse).

In Hardware mode, the PGOOD pin is the logical AND of the output power status and any Watchdog timeout events (if enabled) as shown in Figure 7.

HW Mode Watchdog Timer

Watchdog Configuration

The Watchdog timer is configured by the WD_MODE pin as follows:

- When the WD_MODE pin is set High the Watchdog timer is set for a 32 second timeout period.
- When the WD_MODE pin is Floating the Watchdog timer is set for a 1 second timeout period. Decoupling the pin to 48N is also required.
- When the WD_MODE pin is set Low the Watchdog timer function is disabled.

Watchdog Service

The Watchdog timer is serviced by pulsing the WDOG pin for at least 100ns (here a pulse is defined as a continuous level of either polarity after the 1st edge). Correct platform usage is to service before the watchdog timeout period expires.

Watchdog Timeout

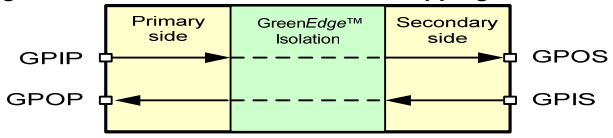
If the Watchdog times out, the following occur:

- The PGOOD pin is pulsed Low for 10ms (min). If coincident with any voltage fault events the PGOOD output pulse could be longer. This pulse can be used for PD platform level alarm or reset.
- Operation of the Watchdog timer is automatically initialized and restarted.

HW Mode General-Purpose I/O Operation

In Hardware mode, the GPIO pins provide a means for controlling and monitoring isolated primary-side signals from the secondary-side of the AS1851A/31A.
The secondary-side GPOS and GPIS pins map to the primary-side pins GPIP and GPOP as shown in Figure 8.

Figure 8 - Hardware Mode GPIO Pin Mapping



SOFTWARE MODE OPERATION

Software mode operation allows a host controller to access the AS1851A/31A internal registers via an I^2C interface. Access to these registers provides extensive status and control functions. Software mode functions and operation details are described below. (Please also refer to Akros document AN082 for a detailed Software Users Guide.)

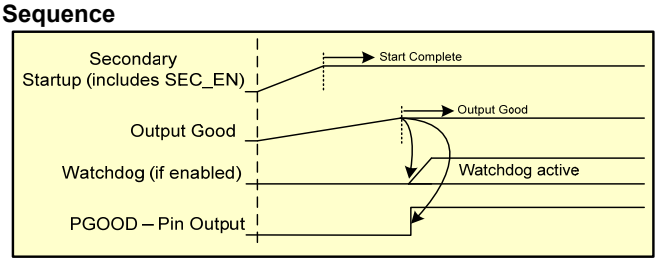
Device Initialization and Software Mode Selection

Primary-side digital logic is initialized while the MODE pin is Low, A required external capacitor between MODE and 48N provides the power-on reset input required to initialize the device.

Software (SW) mode is selected when the MODE pin uses just this initialization capacitor.

Secondary-side digital logic is initialized while the SEC_EN pin is Low, a required external capacitor between SEC_EN and SGND will provide the power-on reset required to initialize the secondary-side. See Figure 9.

Figure 9 – Software Mode Secondary Power-On Sequence



SW Mode Power Status Monitoring (PGOOD)

The output is monitored for power good status; once a supply output reaches a stable state its internal power good status signal is asserted. Power status is declared good at +/- 5% and at fault (bad) at +/- 10% of final voltage value. In either transition case (good to/from bad) a continuous operation of 10µS is required before state change is declared.

As shown in Figure 10, once the output is good the user will see the resulting device power status on both the PGOOD pin and the Global PGOOD bit of Register 00h.

Specific Power Good status for the output is available in the Alarms and Power Status register (00h).

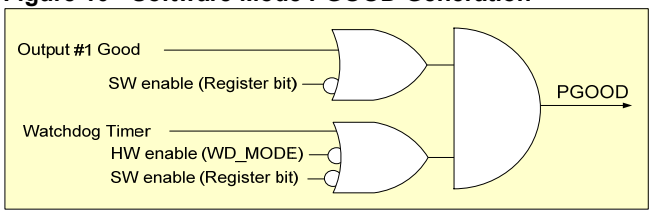
Operation of the PGOOD pin is defined by register 03h as shown in Table 24. Register 03h allows the user to exclude the output's power good status from affecting the PGOOD pin by clearing the output mask bit.

In addition, the Watchdog timer status can be included / excluded in the PGOOD pin logic. Register 04h, bit 2 allows the user to either mask or allow a Watchdog timeout to generate a PGOOD pulse.

The PGOOD pin can be used as part of a board reset logic chain as it is asserted (High) only when all the enabled power outputs are stable. If it does go low (active) PGOOD has a minimum pulse width of 10ms.

Power voltage monitoring will not restart the output. And a PGOOD fault will restore all registers except the history register (Reg 05h) to default state unless bit 4 in the device control register (Reg 06h) is set.

Figure 10 - Software Mode PGOOD Generation



History Register

The PGOOD & Watchdog History register (05h) is used to identify the source of a PGOOD fault. One bit is provided for the power output and one for the Watchdog timer. In the event of a PGOOD fault, the bit corresponding to the source of the PGOOD fault is set.

Once set these bits are latched, they will not change even after the PGOOD fault is resolved unless there is a user command to do so. Therefore the user must clear this register as desired. The PGOOD & Watchdog History register is described in Table 26.

PD Voltage and Current Measurements

The AS1851A/31A contains an A/D converter that measures PD input current to 5-bit accuracy and PD voltage to 8-bit accuracy. The A/D converter measurements are updated automatically at a 100Hz (minimum) rate, and may be accessed at any valid I²C clock rate. A/D values are available in the PD Voltage (0Bh) and PD Current (0Ch) registers (see Table 32 and Table 33).
Current measurement is valid only for PoE PD operation and not during Local Power operation. However, voltage measurement is valid for both PoE and Local Power operation.

PD Over-Current Alarm Threshold

Register 0Dh (see Table 34) allows the user to specify a maximum PD current value that when exceeded sets the PD Over-current Alarm bit in register 00h.

SW Mode Power Margining

The output voltage can be independently margined, to a range of -5% to +5%.

This is configured via the Margin Control register, OEh. The feature allows, for example, platform engineering or manufacturing testing to make test adjustments to compensate for PC board trace IR drops. See Table 35 for details.

If voltage margining is used, the AS1951/31 over-voltage protection tracks to the margining selected for any output.

SW Mode EMI Performance Control

In Software Mode the AS1851A/31A provide two additional methods to generate PWM clocks for optimum EM radiation performance: PRBS Randomization and Fractional-N.

PWM Clocks - PRBS Randomization

This technique enables a randomized PRBS sequence to modulate the clocks thus spreading the noise across the band and reducing the peaks. PRBS randomization is selected via register 0Ah as shown in Table 31.

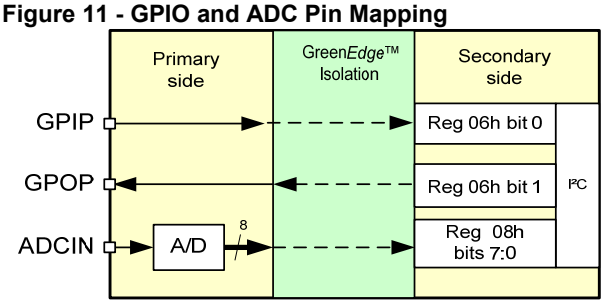
PWM Clocks – Fractional-N

PWM clocks and harmonics can be a major source power supply EMI. Fractional-N clocking provides an “FM like” modulation on the PWM clocks that spreads out the spectral energy thereby reducing peaks in EMI tested frequency bands. One of three modulation rates can be selected via register 0Ah as shown in Table 31.

SW Mode General-Purpose I/O & ADC

As shown in Figure 11, the GPOP, GPIP, and ADCIN pins provide a means for controlling and monitoring isolated Primary-side signals from the Secondary side of the AS1851A/31A.
GPIO and A/D functions are updated automatically at a 100Hz (minimum) rate, and may be accessed at any valid I²C clock rate.

Figure 11 - GPIO and ADC Pin Mapping



General-Purpose I/O Pins

The GPOP bit in the Device Control register (06h) specifies the state of the GPOP output pin. The state of GPIP input pin is reflected in GPIP bit located in the same register. Maximum measurement latency is defined in Table 6.

General-Purpose ADC (ADCIN Pin)

The Primary-side ADCIN pin is an input to an internal A/D converter with a continuous sample/conversion rate. The A/D process is automatic and therefore requires no user action to initiate. This internal 8-bit A/D sub-system contains a successive approximation A/D, track/hold circuitry, internal voltage reference, and conversion clocking. Reading the converted value is done in the A/D Voltage register (08h). Maximum measurement latency is found in Table 6.

In addition, the A/D Alarm Threshold register (09h) allows the user to specify a maximum A/D value that when exceeded automatically sets the A/D Over-threshold Alarm bit in register 00h.

SW Mode Watchdog Timer Operation

The Watchdog timer is serviced using either the WDOG pin or the Watchdog Service Control bit in Register 04h. Correct platform usage is to service before the watchdog timeout occurs. If a Watchdog timeout occurs, the PGOOD pin can generate an output pulse (10ms minimum) that may be used for PD platform level alarm or reset. In addition, an interrupt can be generated and the status can be interrogated by querying the Interrupt Status register (02h) which has a bit to indicate Watchdog timeout.

Watchdog Timer Modes

In Software mode (MODE pin Floating with cap to 48N), the WD_MODE pin selects one of three Watchdog timer operating modes as follows:

Watchdog Timer Function Disabled

When the WD_MODE pin is set Low, the Watchdog timer function is disabled.

Watchdog Timer Enabled at Startup

When the WD_MODE pin is connected to an external capacitor (to 48N), the watchdog timer function is enabled at startup. At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. The timeout period may be changed via the Watchdog Timeout register (07h) as described below.

Watchdog Timer Disabled at Startup

Setting the WD_MODE pin High disables the Watchdog timer function at startup and can only be enabled through software. At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. Once the Watchdog is enabled the timeout period may be changed via the Watchdog Timeout register (07h) as described below.

Watchdog Timer Operation

Watchdog Enable

Enabling of the watchdog function in software must be done with two consecutive writes as follows:

1. The first write is to the Watchdog register (04h) bit "Enable Watchdog", plus any other Watchdog bit masks (for Interrupts, PGOOD, and Register Reset functionality).

2. The next write must be to register 00h with the value BBh with no other intervening read or write operation to the AS1851A/31A. The time between the two writes can be infinite, but the operation will not be enabled until the second write. If a write/read occurs to any other register or if a write occurs but the value is NOT BBh, the Enable Watchdog bit is cleared.

Note that once enabled, watchdog operation cannot be disabled.

Watchdog Service

To service the watchdog via software, the user must issue two consecutive writes as follows:

1. The first write is to the Watchdog register (04h) bit "Watchdog Service Control".

2. The next write must be to register 00h with value AAh with no other intervening read or write operation to the AS1851A/31A. The time between the two writes can vary; however, the second write must be completed before a watchdog timeout occurs. If the watchdog times out before the second write or the second write is not to the 00h register or the data value is not "AAh", then the service request to the watchdog timer is cancelled.

To service the watchdog via hardware (a valid operation in Software mode) the WDOG pin must be pulsed for at least 100ns (continuous pulse of either polarity after the 1st edge). Correct platform usage is to service before the watchdog timeout period expires.

Watchdog Timeout Period

At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. The current user programmed value in the Watchdog Timeout register (07h) is always used for watchdog timeouts. A value of FFh in this register gives the maximum timeout of 32 seconds. A value 01h sets the minimum period of 125ms. Note that 00h is reserved and is not to be used. Intervening values are multiples of 125ms (e.g. a value of 04h = 500ms).

Watchdog Timeout

If the Watchdog times out, the following occur:

– The Watchdog Timeout bit in the History register (05h) is set.

– If the Watchdog Interrupt mask bit is set (register 04h) and interrupts are enabled, the Watchdog Timeout bit in the Interrupt Status register (02h) is set and the INTB pin is driven Low.

– If the Watchdog PGOOD mask bit is set (register 04h), a 10ms (min.) Low pulse is output at the PGOOD pin. If coincident with other voltage fault events the PGOOD output pulse could be extended.

– set (register 04h), the AS1851A/31A registers are reset. This resets the Watchdog Timeout register value to 32 seconds. (Note that an independent PGOOD fault will also reset the registers unless bit 4 in device control register, Reg 06h, is set).

– If the Watchdog Register Reset mask bit is set (register 04h), operation of the Watchdog timer is automatically initialized, with the currently programmed value, and restarted.

SW Mode Interrupt Operation

Interrupts are disabled after a device power on. The Device Control register (06h) is used to enable (or disable) interrupts at a global device level.

The Interrupt Mask (01h) and Interrupt Status (02h) registers are used to enable alarms and service any resulting alarms.

Interrupt Masking

Positive masking is used; therefore a "1" indicates that the specified fault or alarm will cause an interrupt. Interrupts (except for watchdog timeout) are level-driven, thus if a fault condition is active upon enabling it will immediately generate an interrupt.

Interrupt Status

A read from the Interrupt Status register will return the

conditions which have caused an interrupt, and will immediately clear all such pending interrupts. Note that interrupts (except for watchdog timeout) are level driven, so if a fault condition still exists upon interrupts being cleared an interrupt will be re-asserted after a minimum off time of 10µs.

I2C INTERFACE

The AS1851A/31A provides a standard I^2C compatible slave interface that allows a host controller (master) to access its single-byte registers. Note the requirement of "Repeated Start" for I^2C reads.

The Primary-side GPIO pin read/write or ADCIN pin conversion read/write have a 10ms (maximum) pin-to/from-register timing.

The AS1851A/31A registers are summarized in Table 20 and described in Table 21 through Table 36.

The I^2C interface is active when the AS1851A/31A is in Software mode. There are four pins associated with the I^2C interface:

– SDIO: bi-directional serial data
– SCL: clock input
– INTB: interrupt output
– I2C_ADR: device address configuration

Start/Stop Timing

The master device initiates and terminates all I^2C interface operations by asserting Start and Stop conditions respectively.

As shown in Figure 12, a START condition is specified when the SDIO line transitions from High-to-Low while the clock (SCL) is High. A STOP condition is specified when SDIO transitions from Low-to-High while SCL is High.

Data Timing

As shown in Figure 12, data on the SDIO line may change only when SCL is Low and must remain stable during the High period of SCL. All address and data words are serially transmitted as 8-bit words with the MSB sent first.

Acknowledge (ACK)

ACK and NACK are generated by the addressed device that receives data on SDIO. After each byte is transmitted, the receiving interface sends back an ACK to indicate the byte was received.

As shown in Figure 13, to generate an ACK, the transmitter first releases the SDIO line (High) during the Low period of the ACK clock cycle. The receiver then pulls the SDIO line Low during the High period of the clock cycle.

A NACK occurs when the receiver does NOT pull the SDIO line Low during the High period of the clock cycle.

Device address/operation words, register address words, and write data words are transmitted by the master and are acknowledged by the AS1851A/31A. Read data words transmitted by the device are also acknowledged by the master.

Figure 12 - I^2C Interface Start/Stop and Data Timing

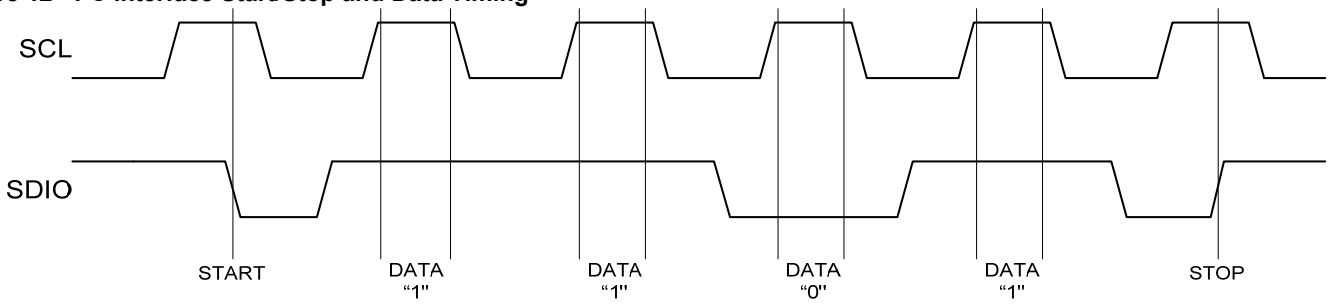
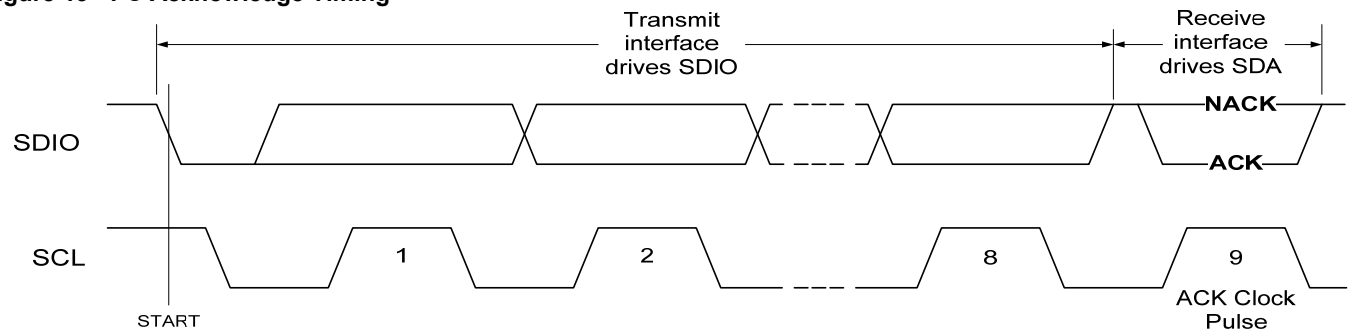


Figure 13 - I²C Acknowledge Timing



Device Address Configuration

The I²C interface is designed to support a multi-device bus system. At the start of an I²C read or write operation, the AS1851A/31A compares its configured device address to the address sent by the master. The AS1851A/31A will only respond (with ACK) when the addresses match.

The device address consists of 7 bits plus a read/write bit. As shown in Table 18, bits A7, A6, A5 and A4 of the AS1851A/31A device address are internally fixed to values A7 = 0, A6 = 1, A5 = 0 and A4 = 0.

The I2C_ADR pin is used to configure bits A3 thru A1 (using an external resistor). The device establishes the bit values of A3 thru A1 during start-up by measuring current flow through this resistor.
Note that A0 functions as the read/write operation bit.

Device Address/Operation Word

Following a START condition the host transmits an 8-bit device address/operation word to initiate a read or write operation. This word consists of a 7-bit device address and the read/write operation bit as shown in Figure 14.

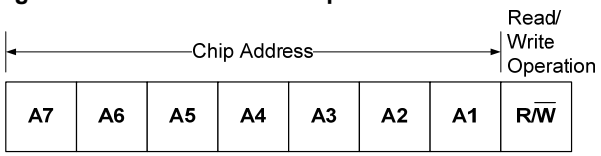
The AS1851A/31A compares the received device address with its configured device address and sends back an ACK only when the addresses match.

Bit 0 is the read/write operation bit. A read operation is specified when the $R/\overline{W}$ bit is set High; a write operation when set Low.

Table 18 - AS1851A/31A Device Address Configuration

Bit	Function	Description
A7	Fixed device address bits	Internally fixed to 0
A6		Internally fixed to 1
A5		Internally fixed to 0
A4		Internally fixed to 0
A3 A2 A1	Configurable device address bits	Device address bits A3, A2 and A1 are configured by connecting a 1% resistor between pin I2C_ADR and ground (48N) as follows: 100KΩ sets A3, A2, A1 = 1,1,1 86KΩ sets A3, A2, A1 = 1,1,0 75.0KΩ sets A3, A2, A1 = 1,0,1 61.9KΩ sets A3, A2, A1 = 1,0,0 49.9KΩ sets A3, A2, A1 = 0,1,1 37.4KΩ sets A3, A2, A1 = 0,1,0 29.4KΩ sets A3, A2, A1 = 0,0,1 12.4KΩ sets A3, A2, A1 = 0,0,0
A0	$R/\overline{W}$	Specifies read or write operation

Figure 14 - Device Address/Operation Word



Register Address Word

For write operations (after the AS1851A/31A acknowledges receipt of the Device Address/Write Word) the master sends the target 8-bit register address word to specify the AS1851A/31A register to be accessed. Table 19 specifies the valid AS1851A/31A register addresses.

Data Word

The 8-bit data word contains read/write data. Data is transferred with the MSB sent first.

Write Cycle

Figure 15 illustrates the sequence of operations to perform an AS1851A/31A register write cycle.

Read Cycle

Figure 16 illustrates the sequence of operations to perform an AS1851A/31A register read cycle. Note that the master must first perform a "dummy write" operation to write the AS1851A/31A internal address pointer to the target register address.

After the AS1851A/31A sends back an ACK, the master sends a repeated START, followed by a device address read word ($R/\overline{W}$ bit = 1). The AS1851A/31A then transmits an ACK followed by the data word that reflects the contents of the target register.

Upon receipt of the register address word, the AS1851A/31A sends back an ACK.

Table 19 - AS1851A/31A Register Address Word

I²C Register Address Word								Selected AS1851A/31A Register (Hex)
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
0	0	0	0	0	0	1	0	02
0	0	0	0	0	0	1	1	03
0	0	0	0	0	1	0	0	04
0	0	0	0	0	1	0	1	05
0	0	0	0	0	1	1	0	06
0	0	0	0	0	1	1	1	07
0	0	0	0	1	0	0	0	08
0	0	0	0	1	0	0	1	09
0	0	0	0	1	0	1	0	0A
0	0	0	0	1	0	1	1	0B
0	0	0	0	1	1	0	0	0C
0	0	0	0	1	1	0	1	0D
0	0	0	0	1	1	1	0	0E
0	0	0	0	1	1	1	1	0F

Figure 15 - I²C Interface Write Cycle Timing

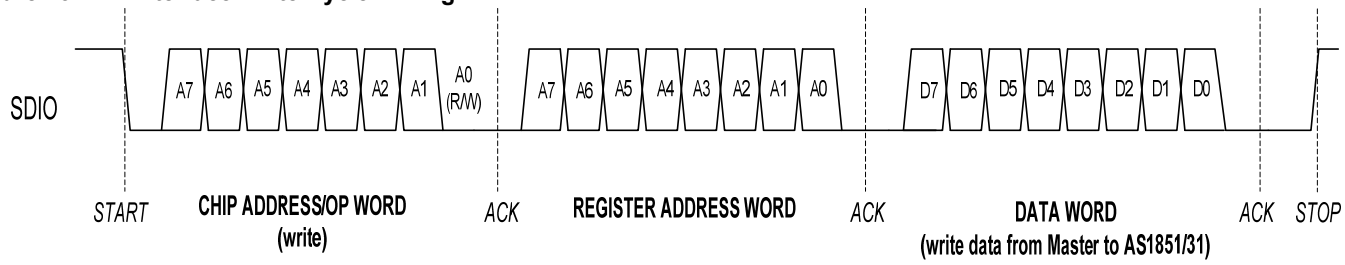
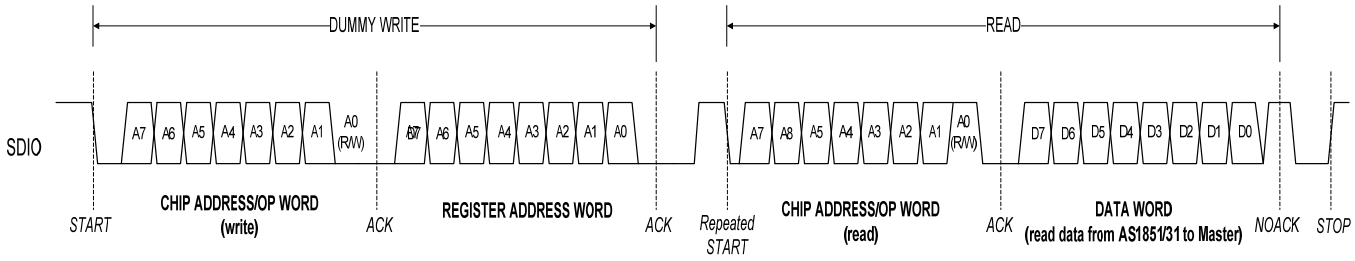


Figure 16 - I²C Interface Read Cycle Timing (with Repeated Start)



Register Descriptions

The AS1851A/31A contains 16 single byte (8-bit) registers. The registers are accessible via the I²C interface when Software mode is enabled.

Table 20 provides a summary of the AS1851A/31A registers and bit functions. Table 21 through Table 36 provides detailed description of the function and operation of each register.

Table 20 - AS1851A/31A Register and Bit Summary

Register	Addr (hex)	Access	Data Bits D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	reserved	reserved	reserved	Output Fault	Global PGOOD Fault
Interrupt Mask	01	R/W	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	reserved	reserved	reserved	Output Fault	reserved
Interrupt Status	02	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	reserved	reserved	reserved	Output Fault	Watchdog Timeout
PGOOD Voltage Masks	03	R/W	reserved	reserved	reserved	reserved	reserved	reserved	Output Mask	reserved
Watchdog Enable, Mask, Service	04	R/W	reserved	reserved	reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	reserved	reserved	reserved	reserved	reserved	reserved	Output caused PGOOD fault	Watchdog Timeout elapsed
Device Control and I/O Status	06	R/W	reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	reserved	reserved	GPOP	GPIP
Watchdog Timeout	07	R/W	WDOG timeout counter (8 bits, in 125ms increments)							
ADCIN Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
ADCIN Alarm Threshold	09	R/W	Alarm Threshold for ADCIN (8 bits)							
PD Status & System Clock Control	0A	R/W	reserved	LDET	AT_DET (AS1851A only)	CLIM (not valid in Local Power mode)	PWM Clock Modulate Enable	PWM Clock Modulate Type	PWM Clock Modulation Amount D1, D0	
PD Voltage Read	0B	Read-Only	PD input voltage measurement (Valid during both PoE and Local Power operation modes)							
PD Current Read	0C	Read-Only	reserved	reserved	reserved	PD input current measurement (PoE only, does not measure Local Power current)				
PD Over-Current Alarm Threshold	0D	R/W	reserved	reserved	reserved	PD over-current alarm trip threshold				
Output Margin Control	0E	R/W	reserved	reserved	reserved	reserved	reserved	Output Voltage Margin setting (D2, D1, D0)		
reserved	0F	R/W	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Table 21 - Alarms and Power Status (Read-Only) - 00h

Bit	Function	Description	Reset State
D7	PD Over-current Alarm	1 = PD has exceeded current limit defined by PD Current Threshold register 0 = No alarm	0
D6	Internal Over-temp Alarm	1 = Temp has tripped warning Threshold 0 = No alarm	0
D5	A/D Threshold Alarm	1 = A/D measurement is > A/D Alarm Threshold register setting 0 = No alarm	0
D4	reserved	do not write to this data bit	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	Power Output Fault	1 = Output Voltage Fault, not within spec 0 = Output in spec This bit always tracks the Output voltage status regardless of whether the output is masked off by Register 03.	0
D0	Global PGOOD Fault	1 = Output not within spec 0 = Output within spec This bit always tracks the PGOOD pin, so Register 03 masks will affect it.	0

Table 22 - Interrupt Mask (R/W) - 01h

Bit	**Function**	**Description (see also Alarms and Power Reg)**	**Reset State**
D7	PD Over-current Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D6	Internal Over-temp Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D5	A/D Threshold Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D4	reserved	do not write to this data bit	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	Interrupt upon Power Output Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D0	reserved	do not write to this data bit	0

Table 23 - Interrupt Status (Read-Only) - 02h

Bit	Function	Description (see also Alarms and Power Reg)	Reset State
D7	PD Over-current Alarm	1 = Fault 0 = normal operation	0
D6	Internal Over-temp Alarm	1 = Fault 0 = normal operation	0
D5	A/D Threshold Alarm	1 = Fault 0 = normal operation	0
D4	reserved	do not write to this data bit	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	Power Output Fault	1 = Fault 0 = normal operation	0
D0	Watchdog Timeout	1 = Timeout 0 = no timeout	0

Table 24 - PGOOD Voltage Masks (R/W) - 03h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	reserved	do not write to this data bit	1
D3	reserved	do not write to this data bit	1
D2	reserved	do not write to this data bit	1
D1	Output masked from PGOOD pin	1= Output part of PGOOD pin or register status 0= Output not part of PGOOD	1
D0	reserved	do not write to this data bit	0

Table 25 - Watchdog Enable, Mask, Service (R/W) - 04h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Watchdog Enable	To change D4, D3, D2, or D1 a two stage write operation must occur:	D4 = 0
D3	Watchdog Interrupt Mask	Stage 1. The Watchdog Enable bit (D4) must be set along with any other (D3-D1) desired bit changes. If D4 is not set the entire write operation is ignored.	D3 = 0 D2 = 1
D2	Watchdog PGOOD Mask	Stage 2. A write to Reg 0 with data BB (hex) must be the next I^2C operation to this device. If not, write will be ignored.	D1 = 0
D1	Watchdog Register Reset Mask	Once this operation is complete (and D4 is set) the D4-D1 bits are sticky and cannot be reset. **D4 (Watchdog Enable):** 1 = enable watchdog countdown operation (timeout value set in watchdog timeout register). 0 = watchdog disabled **D3 (Watchdog Interrupt Mask):** 1 = mask on, interrupt possible 0 = masked off, no interrupt possible **D2 (Watchdog PGOOD Mask):** 1 = mask on, Watchdog part of PGOOD operation 0 = mask off, Watchdog not part of PGOOD operation **D1 (Watchdog Register Reset Disable Mask):** 1 = mask on, a Watchdog timeout will not reset I^2C registers 0= mask off, a Watchdog timeout will reset I^2C registers	
D0	Watchdog Service Control	1 = enable software service of Watchdog 0 = no software service of Watchdog Servicing the Watchdog is a 2-step procedure, after writing a “1” to this bit the next I^2C operation to the AS1851A/31A must be a write to Reg 0 with data AA (hex).	0

Table 26 - PGOOD & Watchdog History (R/W) - 05h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	reserved	do not write to this data bit	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	Output PGOOD history	1 = Output caused PGOOD fault 0 = Output did not cause PGOOD fault	0
D0	Watchdog history	1 = Watchdog timeout occurred 0 = No Watchdog timeout occurred	0

Table 27 - Device Control and I/O Status (R/W) - 06h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	Reset all registers	1 = force reset all registers 0 = no resets	0
D5	Enable Interrupts	1 = enable interrupts that are masked on 0 = no interrupts enabled	0
D4	Disable PGOOD reset	1 = PGOOD fault will not reset registers 0 = PGOOD fault will reset registers	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	General-Purpose Output (GPOP)	GPOP pin reflects the state of this bit	0
D0	General-Purpose Input (GPIP)	This bit reflects the state of the GPIP pin	0

Table 28 - Watchdog Timeout (R/W) - 07h

Bit	Function	Description	Reset State
D7	D7 of 8-bit watchdog timer	Watchdog timeout counter value (125ms increments), used in Software Mode only. FF = max value (32 sec) 01 = min value (125ms) 00 = reserved, do not use	1
D6	D6 of 8-bit watchdog timer		1
D5	D5 of 8-bit watchdog timer		1
D4	D4 of 8-bit watchdog timer		1
D3	D3 of 8-bit watchdog timer		1
D2	D2 of 8-bit watchdog timer		1
D1	D1 of 8-bit watchdog timer		1
D0	D0 of 8-bit watchdog timer		1

Table 29 - ADCIN Voltage (Read-Only) - 08h

Bit	Function	Description	Reset State
D7	D7 of 8-bit voltage measure	8-bit measurement of voltage at ADCIN pin (primary side). The A/D runs continuously with a 100Hz sampling rate (minimum), and can be read at full I^2C speed. FF (hex) = 2.5 V 00 (hex) = 0 V step size = 9.80 mV	0
D6	D6 of 8-bit voltage measure		0
D5	D5 of 8-bit voltage measure		0
D4	D4 of 8-bit voltage measure		0
D3	D3 of 8-bit voltage measure		0
D2	D2 of 8-bit voltage measure		0
D1	D1 of 8-bit voltage measure		0
D0	D0 of 8-bit voltage measure		0

Table 30 - ADCIN Alarm Threshold (R/W) - 09h

Bit	Function	Description	Reset State
D7	D7 of 8-bit A/D Interrupt Threshold	8 bit Threshold for A/D Alarm Interrupt (if enabled) from ADCIN input pin. FF (hex) = 2.5V 00 (hex) = 0 V step size = 9.80 mV	1
D6	D6 of 8-bit A/D Interrupt Threshold		1
D5	D5 of 8-bit A/D Interrupt Threshold		1
D4	D4 of 8-bit A/D Interrupt Threshold		1
D3	D3 of 8-bit A/D Interrupt Threshold		1
D2	D2 of 8-bit A/D Interrupt Threshold		1
D1	D1 of 8-bit A/D Interrupt Threshold		1
D0	D0 of 8-bit A/D Interrupt Threshold		1

Table 31 - PD Status and System Clock Control (R/W) - 0Ah

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	LDET	1 = Local power supply detected 0 = no Local power supply detected	0
D5	AT_DET	1 = IEEE® 802.3at, or, Local Power mode detection 0 = IEEE® 802.3af mode detection	0
D4	CLIM	1 = 750ma (min) PoE current limit (AS1851A only) 0 = 375ma (min) PoE current limit Note that CLIM status is not valid in Local Power mode (LDET status bit D6=1).	0
D3	PWM Clock Modulation Enable	1 = Clock modulation on 0 = off	0
D2	PWM Clock Modulation Type	1 = Fractional-n (see D1, D0 for modulation amount) 0 = Random (PRBS)	0
D1	PWM Fractional-n Modulation Amount	D1, D0: 1,1 = reserved (do not use)	0,0

	(not used for PRBS modulation)	1,0 = 10% 0,1 = 5% 0,0 = 2%	
D0	PWM Fractional-n Modulation Amount (not used for PRBS modulation)	D1, D0: 1,1 = reserved (do not use) 1,0 = 10% 0,1 = 5% 0,0 = 2%	0,0

Table 32 - PD Voltage (Read-Only) - 0Bh

Bit	Function	Description	Reset State
D7	D7 of 8-bit voltage measure	8-bit measurement of PD input voltage (primary side). Also valid during Local Power Operation. FF (hex) = 60 V (±1%) 00 (hex) = 0 V step size = 235.3 mV	0
D6	D6 of 8-bit voltage measure		0
D5	D5 of 8-bit voltage measure		0
D4	D4 of 8-bit voltage measure		0
D3	D3 of 8-bit voltage measure		0
D2	D2 of 8-bit voltage measure		0
D1	D1 of 8-bit voltage measure		0
D0	D0 of 8-bit voltage measure		0

Table 33 - PD Current (Read-Only) - 0Ch

Bit	Function	Description	Reset State
D7	reserved	5-bit measurement of PD input current (primary side). PoE current measurement only, not valid during Local Power operating mode. **With CLIM = Low** D4, D3, D2, D1, D0 11111 = 400 mA (±10%) 00000 = 0 mA step size = 12.90 mA **With CLIM = High (AS1851A only)** D4, D3, D2, D1, D0 11111 = 800 mA (±10%) 00000 = 0 mA step size = 25.81 mA	n/a
D6	reserved		n/a
D5	reserved		n/a
D4	D4 of 5-bit current measurement		0
D3	D3 of 5-bit current measurement		0
D2	D2 of 5-bit current measurement		0
D1	D1 of 5-bit current measurement		0
D0	D0 of 5-bit current measurement		0

Table 34 - PD Over-Current Alarm Threshold (R/W) - 0Dh

Bit	Function	Description	Reset State
D7	reserved	The over-current alarm bit is set when the PD input current (primary side) measurement exceeds this 5-bit value, not valid during Local Power operating mode.	n/a
D6	reserved		n/a
D5	reserved		n/a
D4	D4 of 5-bit current alarm trip setting	With CLIM = Low D4, D3, D2, D1, D0	1
D3	D3 of 5-bit current alarm trip setting	11111 = 400 mA (±10%) 00000 = 0 mA step size = 12.90 mA	1
D2	D2 of 5-bit current alarm trip setting		1
D1	D1 of 5-bit current alarm trip setting	With CLIM = High (AS1851A only) D4, D3, D2, D1, D0	1
D0	D0 of 5-bit current alarm trip setting	11111 = 800 mA (±10%) 00000 = 0 mA step size = 25.81 mA	1

Table 35 - Output Margin Control (R/W) - 0Eh

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	reserved	do not write to this data bit	0
D3	reserved	do not write to this bit	0
D2	Voltage Margin for Output	D2, D1, D0: 1,1,1 = reserved, do not use 1,1,0 = reserved, do not use 1,0,1 = reserved, do not use 1,0,0 = +5% 0,1,1 = +2.5% 0,1,0 = -2.5% 0,0,1 = -5% 0,0,0 = no margining	0,0,0
D1			
D0			

Table 36 - Reserved - 0Fh

Bit	Function	Description	Reset State
D7	reserved	do not write to this bit	0
D6	reserved	do not write to this bit	0
D5	reserved	do not write to this bit	0
D4	reserved	do not write to this bit	0
D3	reserved	do not write to this bit	0
D2	reserved	do not write to this bit	0
D1	reserved	do not write to this bit	0
D0	reserved	do not write to this bit	0

POWER OVER ETHERNET OVERVIEW

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). The PoE standard IEEE® Std. 802.3af is intended to standardize the delivery of power over the Ethernet cables in order to accommodate remotely powered client devices. IEEE® Std. 802.3af defines a method for recognizing PDs on the network and supplying different power levels according to power level classes with which each PD is identified. By employing this method, designers can create systems that minimize power usage, allowing more devices to be supported on an Ethernet network.

The end of the link that provides power through the Ethernet cables is referred to as the power sourcing equipment (PSE). The powered device (PD) is the end of the link that receives the power. The PoE method for recognizing a PD and determining the correct power level to allocate uses the following sequence:

1. Reset - Power is withdrawn from the PD if the applied voltage falls below a specified level.
2. Signature Detection - during which the PD is recognized by the PSE.
3. Classification - during which the PSE reads the power requirement of the PD. The Classification level of a PD identifies how much power the PD requires from the Ethernet line. This permits optimum use of the total power available from the PSE. (Classification is considered optional by IEEE® standard 802.3af.)
4. ON operation - during which the allocated level of power is provided to the PD.

This sequence occurs as progressively rising voltage levels from the PSE as shown in Figure 18.

A summary of the PoE design framework is shown in Table 37.

Table 37 - PoE Design Framework Summary

Requirement	Value
Maximum power to the PD	12.95W (Type 1) 25.5W (Type 2)
Voltage at the PSE Interface	44-57V (Type 1) 50-57V (Type 2)
Maximum operating current	350mA (Type 1) 600mA (Type 2)
Min voltage at the PD interface	37V (Type 1) 42.5V (Type 2)

Power Feed Alternatives for 10/100/1000M Ethernet Systems

The Power Sourcing Equipment (PSE) supplies power to a single PD per node. A PSE located in the Data Terminal Equipment or Repeater is called an endpoint PSE, while a PSE located between MDIs is called a Mid-span PSE. Figure 17 illustrates the two power feed options allowed in the 802.3af/at standard for 10/100/1000M Ethernet systems (full duplex twisted pair data signaling is used in 1000M Ethernet).

In Alternative A, a PSE powers the end station by feeding current along the twisted pair cable used for the 10/100/1000M Ethernet signal via center taps on the Ethernet transformers. On the line side of the transformers for the PD, power is delivered through pins 1 and 2 and returned through pins 3 and 6.

In Alternative B, a PSE powers the end station by feeding power through pins 4, 5, 7and 8. In a 10/100/1000M system, this is done through the center taps of the Ethernet transformer. In a 10/100M system, power is applied directly to the spare cable pairs without using transformers.

The IEEE® Std. 802.3af/at standards are intended to be fully compliant with all existing non-powered Ethernet systems. As a result the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classify (optional in legacy 802.3af applications) the needed power prior to supplying it to the device. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

POE+: THE NEXT GENERATION

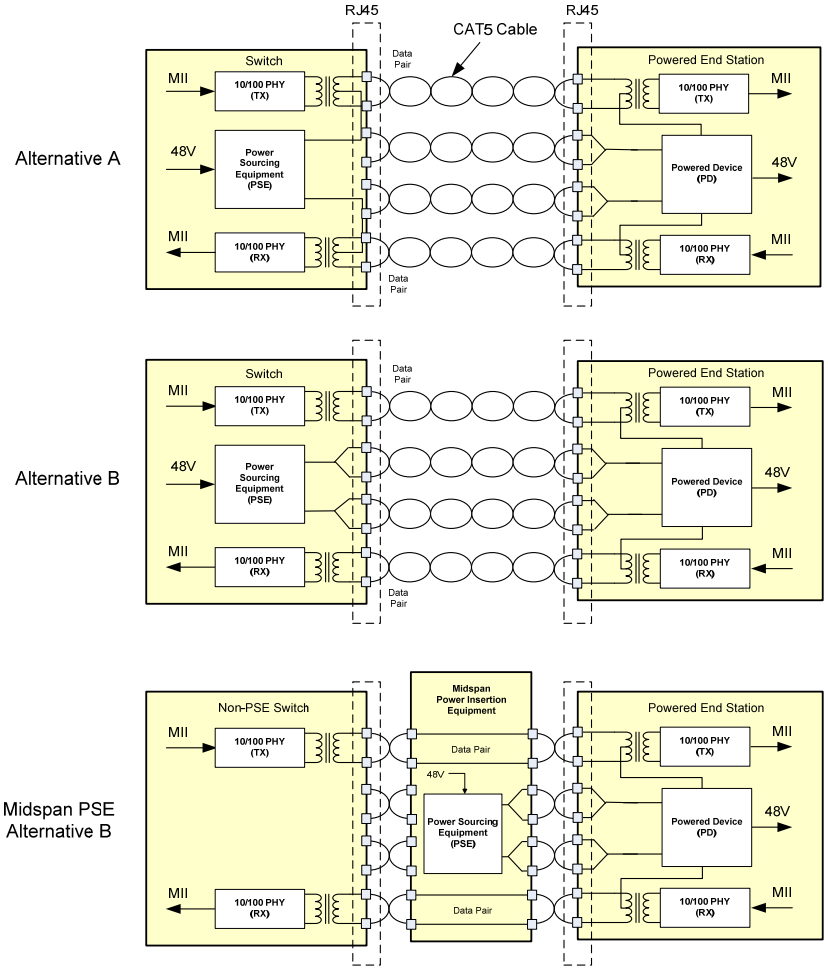
The AS1851A has been designed to be compatible with the IEEE 802.3at high power PoE standard. These devices are capable of providing the power needs of VoIP with video streaming, 802.11n multi-radio WAPs, and IP cameras with PTZ.

The AS1851A provides the normal signature resistance during detection phase for the PSE to recognize a PD. The device also supports the two-event classification method specified in the 802.3at standard (backward compatible to 802.3af classification modes) and can detect a Type 2 PSE. If the AS1851A detects a Type 2 PSE it will indicate this either on the AT_DET pin or in I^2C register 0A (hex) if in software mode. AT_DET pin is active high.

The AS1851A will issue the correct AT_DET state before PGOOD signal transitions to an “all good” state.

For a PD that is 802.3at compliant, Class must be set to Class 4 using appropriate RCLASS resistor.

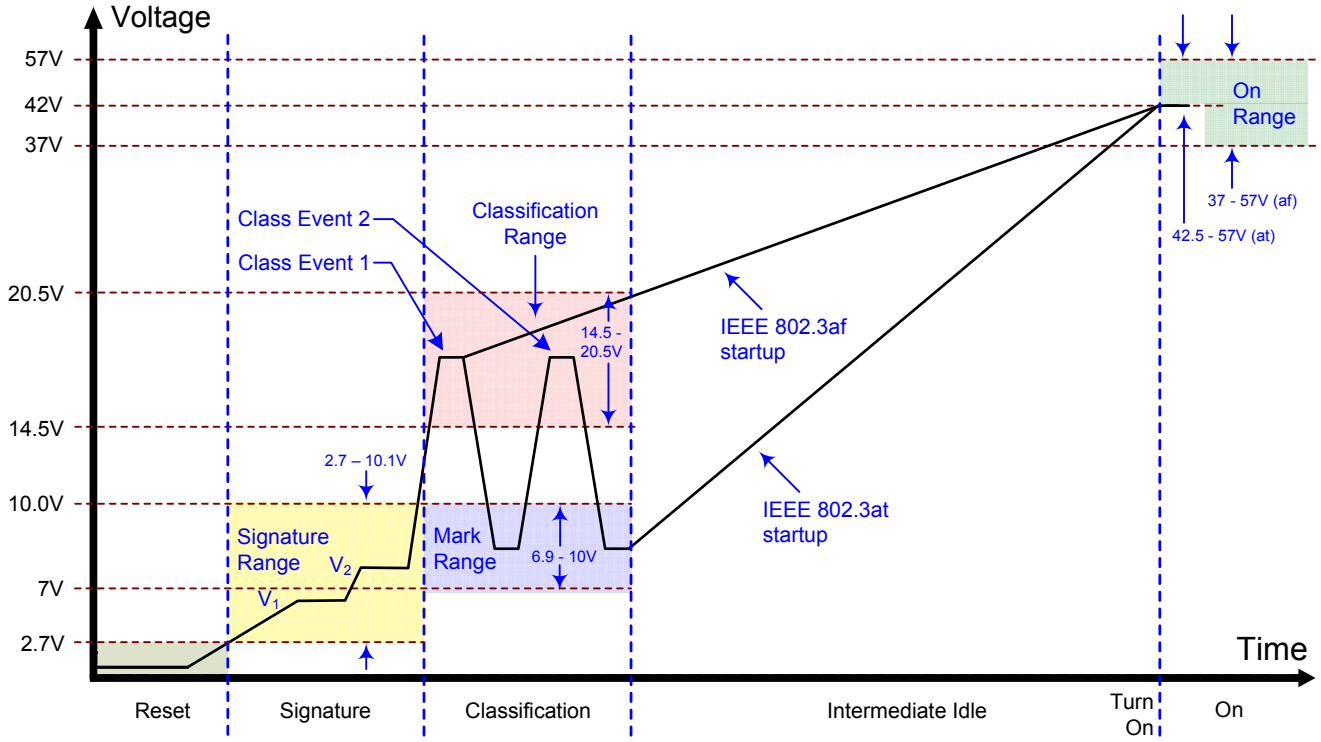
Figure 17 - IEEE® Std. 802.3af Power Feeding Schemes



POE POWER-ON SEQUENCE

The power-on sequence for PoE operation is shown in Figure 18. The waveform reflects typical voltages present at the PD during signature, classification and power-on.

Figure 18 - PoE Power-On Sequence Waveform

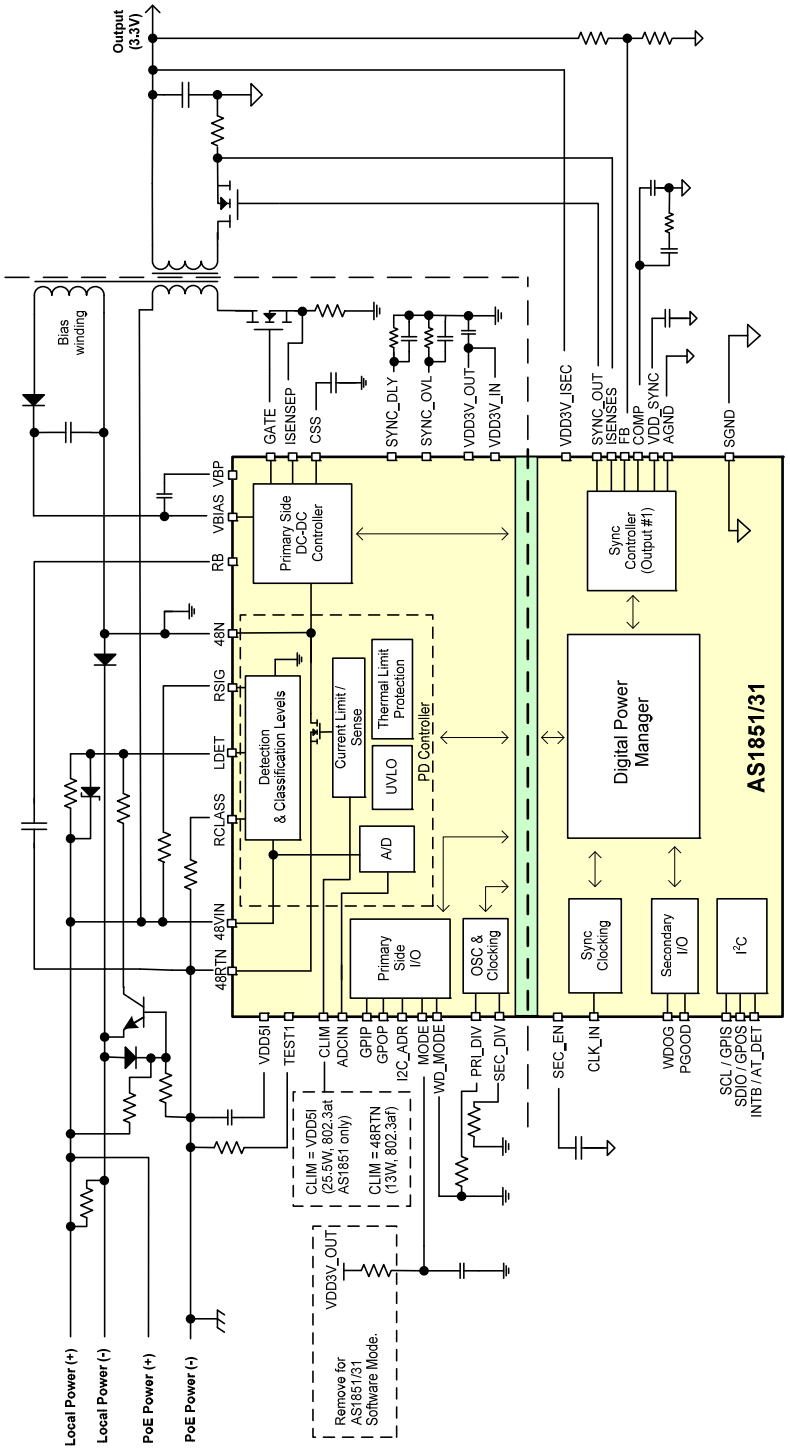


1. Voltages V1 and V2 are applied by the PSE to extract a signature value.

2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance connected to the RCLASS pin.

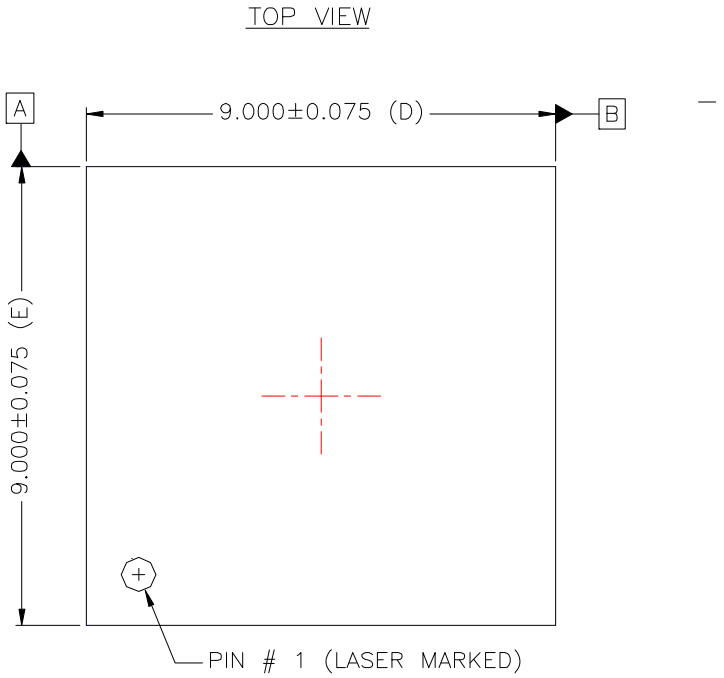
3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9-10V), followed by a second classification voltage. The PD responds by presenting a load current as determined by the resistor on the RCLASS pin. After the PSE measures the PD load current the second time and determines that is can deliver the requested power, it moves into the On state by raising the voltage to approximately 42V after which the PD operates over the On Range.

Figure 19 - Typical Isolated Synchronous Flyback Application

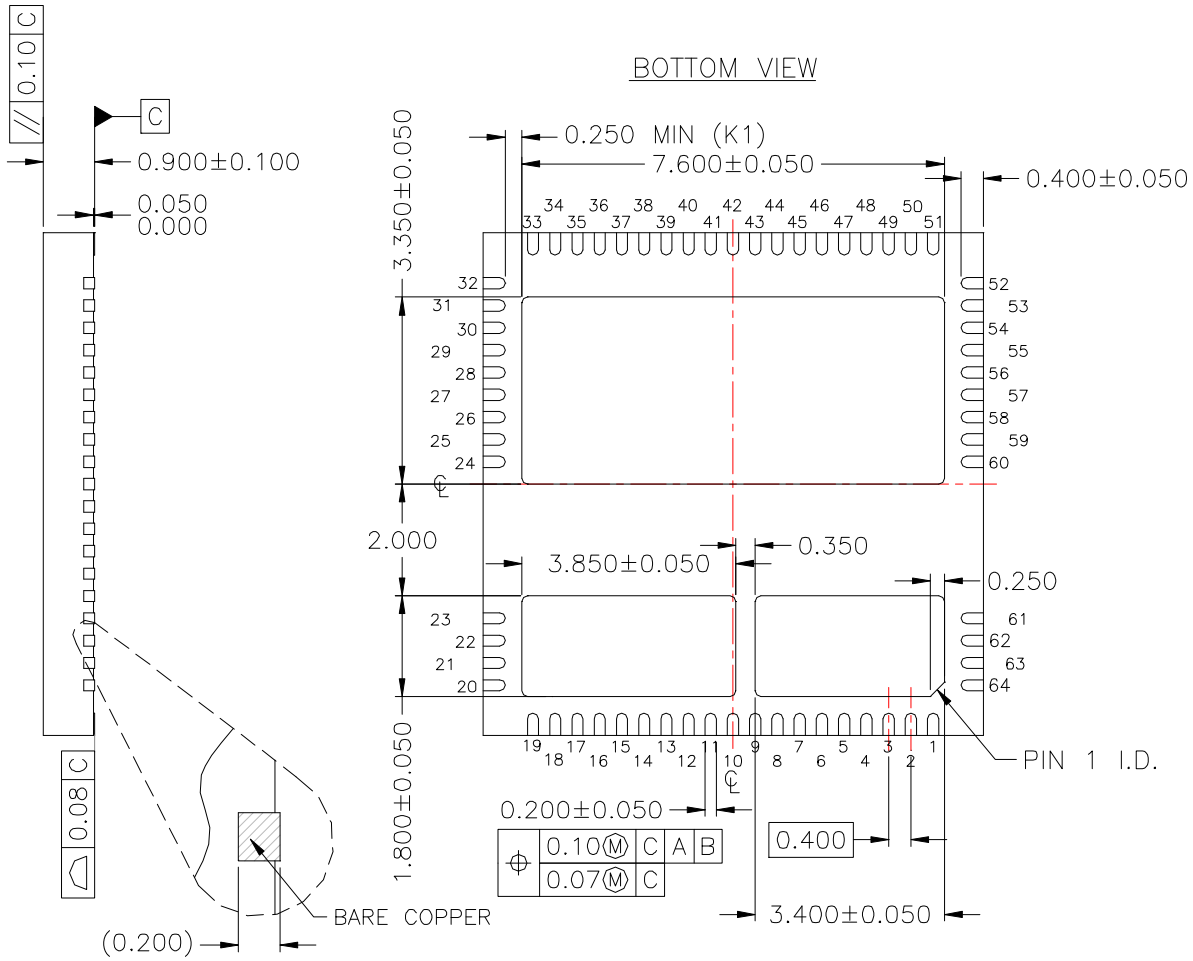


PACKAGE SPECIFICATIONS

Figure 20 - 64-Pin QFN Dimensions



NOTE :
1. Controlling Dimensions in mm.
2. REFER TO JEDEC MO-220 FOR DIMENSION NOT SHOWN HERE.
3. AVAILABLE LEADFRAME PART NUMBER : 16-064-374.


BOTTOM VIEW
0.10 C
C
0.900±0.100
0.050
0.000
0.08 C
(0.200)
BARE COPPER
0.250 MIN (K1)
7.600±0.050
0.400±0.050
3.350±0.050
2.000
3.850±0.050
0.350
0.250
1.800±0.050
0.200±0.050
0.10 M C A B
0.07 M C
0.400
3.400±0.050
PIN 1 I.D.

Contact Information

Akros Silicon, Inc.
6399 San Ignacio Avenue, Suite 250
San Jose, CA 95119
USA

Tel: (408) 746 9000
Fax: (408) 746-9391
Email inquiries: marcom@akrossilicon.com
Website: http://www.akrossilicon.com

Important Notices

Legal Notice

Reference Design Policy

This document is provided as a design reference and Akros Silicon assumes no responsibility or liability for the information contained in this document. Akros reserves the right to make corrections, modifications, enhancements, improvements and other changes to this reference design documentation without notice.

Reference designs are created using Akros Silicon's published specifications as well as the published specifications of other device manufacturers. This information may not be current at the time the reference design is built. Akros Silicon and/or its licensors do not warrant the accuracy or completeness of the specifications or any information contained therein.

Akros does not warrant that the designs are production worthy. Customer should completely validate and test the design implementation to confirm the system functionality for the end use application.

Akros Silicon provides its customers with limited product warranties, according to the standard Akros Silicon terms and conditions.

For the most current product information visit us at www.akrossilicon.com

Life Support Policy

LIFE SUPPORT: AKROS' PRODUCTS ARE NOT DESIGNED, INTENDED, OR AUTHORIZED FOR USE AS COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS. NO WARRANTY, EXPRESS OR IMPLIED, IS MADE FOR THIS USE. AUTHORIZATION FOR SUCH USE SHALL NOT BE GIVEN BY AKROS, AND THE PRODUCTS SHALL NOT BE USED IN SUCH DEVICES OR SYSTEMS, EXCEPT UPON THE WRITTEN APPROVAL OF THE PRESIDENT OF AKROS FOLLOWING A DETERMINATION BY AKROS THAT SUCH USE IS FEASIBLE. SUCH APPROVAL MAY BE WITHHELD FOR ANY OR NO REASON.

“Life support devices or systems” are devices or systems which (1) are intended for surgical implant into the human body, (2) support or sustain human life, or (3) monitor critical bodily functions including, but not limited to, cardiac, respirator, and neurological functions, and whose failure to perform can be reasonably expected to result in a significant bodily injury to the user. A “critical component” is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Substance Compliance

With respect to any representation by Akros Silicon that its products are compliant with RoHS, Akros Silicon complies with the Restriction of the use of Hazardous Substances Standard ("RoHS"), which is more formally known as Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. To the best of our knowledge the information is true and correct as of the date of the original publication of the information. Akros Silicon bears no responsibility to update such statements.

Revision:	Version 1.5
Release Date:	August 12, 2014