

# GaAs IC High Isolation Positive Control SPDT Switch DC–2.5 GHz

**iAlpha**

**AS148-24**

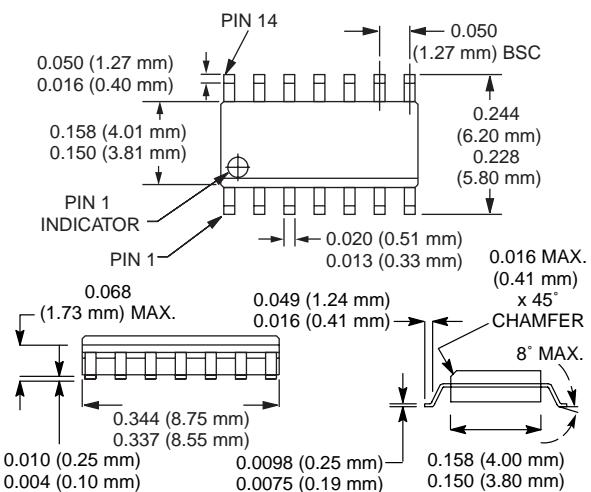
## Features

- Positive Voltage Control
- High Isolation (50 dB @ 0.9 GHz and 1.9 GHz)
- Low DC Power Consumption
- Base Station Synthesizer Switch

## Description

GaAs FET IC SPDT switch packaged in an SOIC-14 plastic package for low cost commercial applications. Ideal building block for base station dual band applications where synthesizer isolation is critical. Use in conjunction with the AS123-12 SPST switch to meet GSM synthesizer isolation requirement.

## SOIC-14



## Electrical Specifications at 25°C (0, +5 V)

Parameter <sup>1</sup>	Frequency <sup>2</sup>	Min.	Typ.	Max.	Unit
Insertion Loss <sup>3</sup>	DC–1.0 GHz DC–2.0 GHz DC–2.5 GHz	0.6 0.8 1.2	0.9 1.1 1.4		dB
Isolation	DC–1.0 GHz DC–2.0 GHz DC–2.5 GHz	44 45 32	50 50 42		dB
VSWR <sup>4</sup>	DC–2.0 GHz DC–2.5 GHz		1.3:1 1.5:1	1.5:1 1.8:1	

## Operating Characteristics at 25°C (0, +5 V)

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching Characteristics <sup>5</sup>	Rise, Fall (10/90% or 90/10% RF) On, Off (50% CTL to 90/10% RF) Video Feedthru			60 100 50		ns ns mV
Intermodulation Intercept Point (IP3)	Two-tone Input Power +10 dBm	0.5–2.0 GHz		+41		dBm
Control Voltages	$V_{Low} = 0$ to 0.2 V @ 20 $\mu$ A Max. $V_{High} = +5$ V @ 200 $\mu$ A Max. to +7 V @ 500 $\mu$ A Max. $V_S = V_{High} \pm 0.2$ V					

1. All measurements made in a 50  $\Omega$  system, unless otherwise specified.

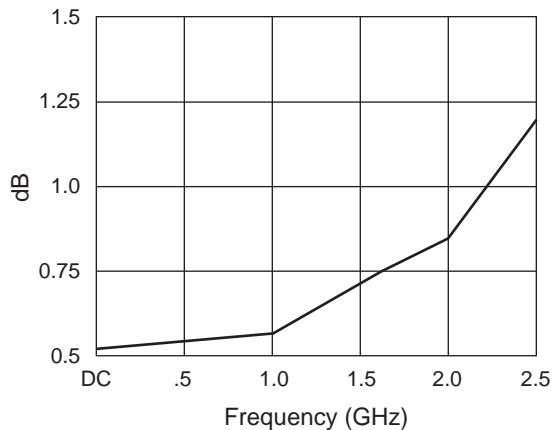
2. DC = 300 kHz.

3. Insertion loss changes by 0.003 dB/°C.

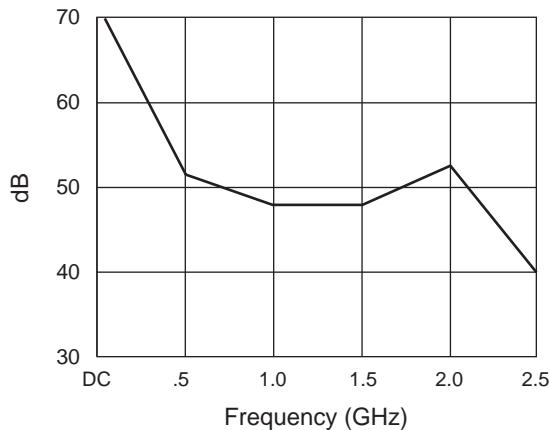
4. Insertion loss state.

5. Video feedthru measured with 1 ns risetime pulse and 500 MHz bandwidth.

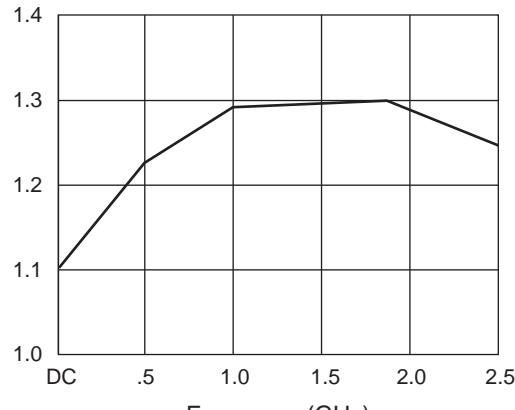
## Typical Performance Data (0, +5 V)



**Insertion Loss vs. Frequency**



**Isolation vs. Frequency**

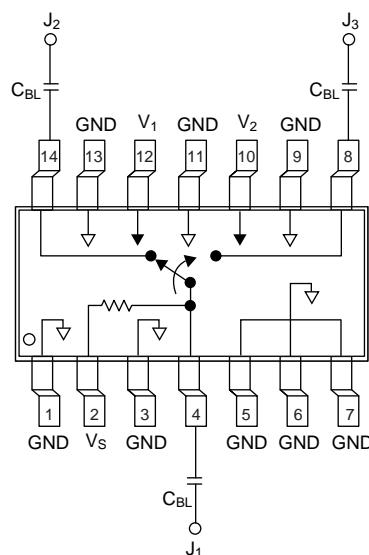


**VSWR vs. Frequency**

## Absolute Maximum Ratings

Characteristic	Value
RF Input Power	1 W Max. > 500 MHz 0/+8 V Control
Supply Voltage	+8 V
Control Voltage	-0.2 V, +8 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
$\Theta_{JC}$	25°C/W

## Pin Out



DC blocking capacitors ( $C_{BL}$ ) must be supplied externally.  
 $C_{BL} = 100 \text{ pF}$  for operation >500 MHz.

## Truth Table

$V_1$	$V_2$	$J_1-J_2$	$J_1-J_3$
$V_{High}$	0	Isolation	Insertion Loss
0	$V_{High}$	Insertion Loss	Isolation

$V_{High} = +5 \text{ to } +7 \text{ V}$  ( $V_S = V_{High} \pm 0.2 \text{ V}$ ).