AS1371

400mA, Low Input Voltage, Low Quiescent Current LDO

1 General Description

The AS1371 low input voltage, positive voltage regulator is designed to deliver up to 400mA while consuming typically only 15µA of quiescent current. The device operates from input voltages of 1.2V to 3.6V, and is available in fixed output voltages between 0.6V and 3.3V (programmable in 50mV steps).

Operation at the full 400mA load current is dependent upon the maximum power dissipation available from package and environment.

The low input voltage and ultra-low dropout voltage (20mV @ 100mA load and 80mV @ 400mA load) supports single primary cell operation in small applications, when operated with minimum input-to-output voltage differentials. In addition, the regulator provides a power management life extension by operating from pre-existing 1.8V and 2.5V outputs to provide low output voltages for new generation portable processor cores.

The device features stable output voltage with ceramic capacitors down to a value of 1µF, strict output voltage regulation tolerances (±1%), and good line- and load-regulation.

The AS1371 is available in a 6-pin 2x2 TDFN package and is qualified for -40°C to +85°C operation.

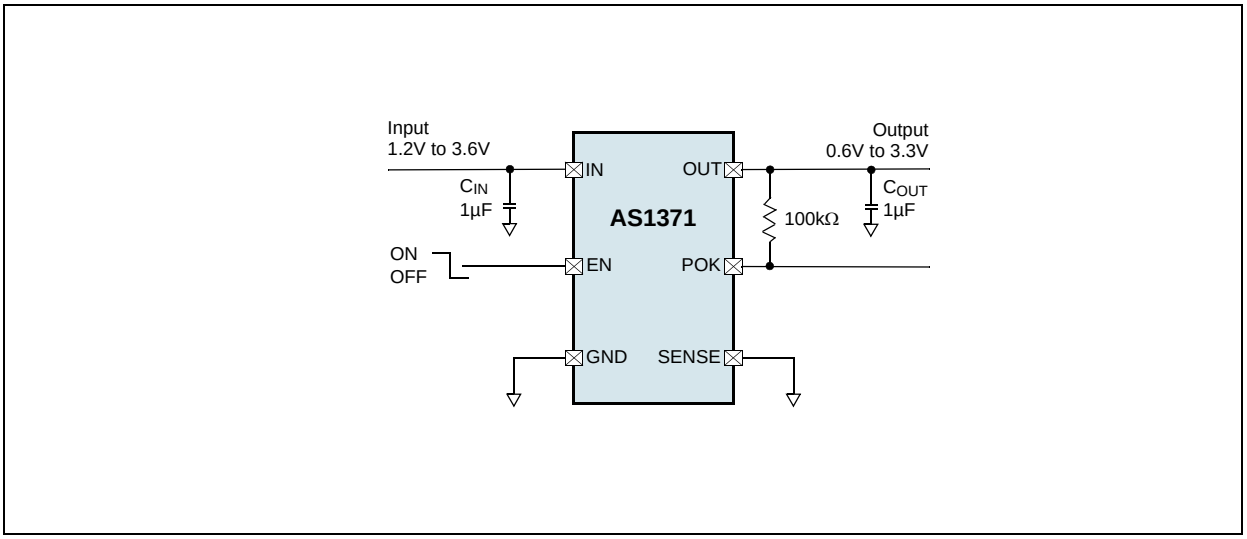
2 Key Features

- Ultra-Low Dropout Voltage: 20mV @ 100mA load
- Operating Input Voltage Range: 1.2V to 3.6V
- Output Voltages: 0.6V to 3.3V in 50mV steps
- Max. Output Current: 400mA
- Output Voltage Accuracy: ±1%
- Low Shutdown Current: 10nA
- Low Quiescent Current: 50µA @ max load
- Integrated Overtemperature/Overcurrent Protection
- Under-Voltage Lockout Feature
- Chip Enable Input
- Power-OK and Low Battery Detection
- Sense Input Option
- Minimal External Components Required
- Operating Temperature Range: -40°C to +85°C
- 6-pin 2x2 TDFN Package

3 Applications

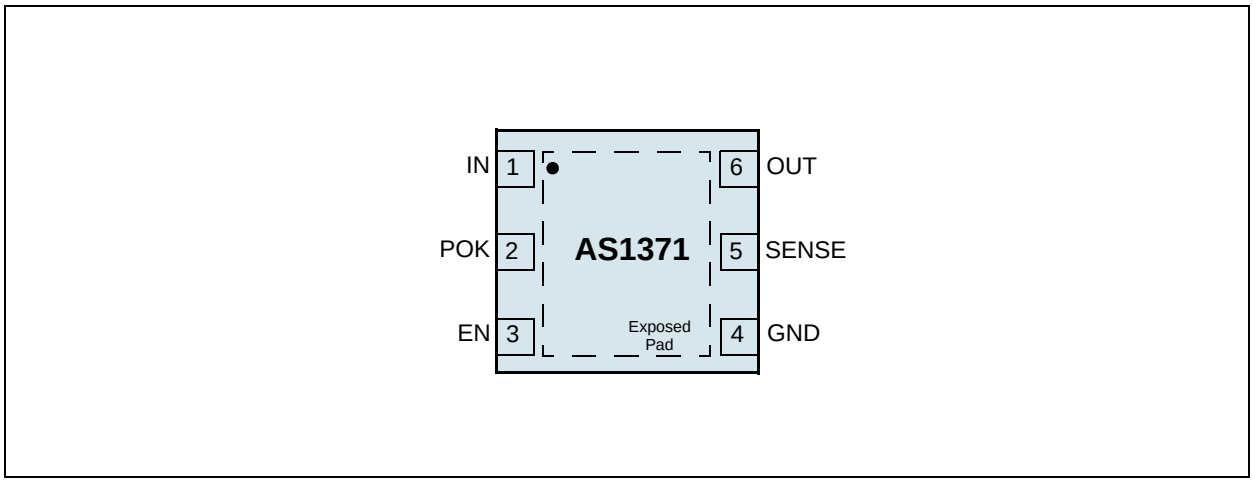
The devices are ideal for powering cordless and mobile phones, MP3 players, CD and DVD players, PDAs, hand-held computers, digital cameras, and any other hand-held and/or battery-powered device.

Figure 1. AS1371 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
IN	1	**LDO Input**. Input voltage range: 1.2V to 3.6V. Bypass with 1µF to GND.
POK	2	**Power-OK Output.** Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100kΩ pull-up resistor to pin OUT for logic levels. Leave this pin unconnected if the Power-OK feature is not used.
EN	3	**Active-High Enable Input.** A logic low reduces the supply current to < 1µA. Connect to pin IN for normal operation.
GND	4	**Ground.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.
SENSE	5	**Sense Input.** Represents the input for the Power-OK behaviour. If connected to GND the POK output is related to OUT.
OUT	6	**LDO Output.** Bypass with 1µF to GND.
GND	Exposed Pad	**Exposed Pad.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation. Internally it is connected GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
IN and EN to GND	-0.3	+5.0	V	
POK and OUT to GND	-0.3	V_{IN} + 0.3	V	
Output Short-Circuit Duration	Indefinite		V	
Thermal Resistance θ_{JA}	+78.6		ºC/W	
Junction Temperature T_J	+150		ºC	Internally limited
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature	+260		ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

V_{IN} = V_{OUT} (Nominal) + 0.5V, EN = IN, C_{IN} = C_{OUT} = 1µF, T_{AMB} = -40°C to +85ºC (unless otherwise specified). Typical Values are at T_{AMB} = +25ºC.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		1.2		3.6	V
V_{OUT}	Output Voltage	Available in 50mV steps, see Ordering Information on page 13	0.6		3.3	V
	Output Voltage Accuracy	T_{AMB} = +25ºC, I_{OUT} = 1mA, V_{OUT} > 1V	-1		+1	%
		T_{AMB} = -40 to +85ºC, I_{OUT} = 1mA, V_{OUT} > 1V	-2.7		+2.7	
I_{OUT}	Maximum Output Current		400			mA
I_{LIM}	Current Limit			650		mA
I_Q	Quiescent Current	I_{OUT} = 0mA		15	20	µA
		I_{OUT} = 400mA		50		
V_{IN}-V_{OUT}	Dropout Voltage[1]	I_{OUT} = 100mA		20	50	mV
		I_{OUT} = 400mA		80		
ΔV_{LNR}	Line Regulation	I_{OUT} = 1mA	-15	0	+15	mV
ΔV_{LDR}	Load Regulation	I_{OUT} = 1mA to 400mA		0.003		%/mA
	Output Voltage Noise	f = 10Hz to 100kHz, I_{OUT} = 10mA		100		μV_{RMS}
PSRR	Output Voltage AC Power-Supply Rejection Ratio	f = 10kHz, I_{OUT} = 10mA		50		dB
Shutdown[2]						
t_{ON}	Exit Delay from Shutdown[3,4]			90	150	µs
I_{OFF}	Enable Supply Current	EN = GND, T_{AMB} = +25ºC		0.01	1	µA
		EN = GND, T_{AMB} = +85ºC		0.04		
V_{IH}	Enable Input Threshold		1.0			V
V_{IL}					0.4	
I_{EN}	Enable Input Bias Current	EN = IN or GND, T_{AMB} = +25ºC		0.03	100	nA
		EN = IN or GND, T_{AMB} = +85ºC		0.2		
Power-OK Output						
V_{POK}	Power-OK Voltage Threshold[5]	SENSE = GND, $V_{POKFALLING}$	90	94	97	% V_{OUT}
		SENSE = GND, Hysteresis		1		
V_{SENSE}	Power-OK Sense Voltage Threshold	V_{OUT} = 1.05V, V_{SENSE} falling	650	800	950	mV
		Hysteresis		50		
V_{OL}	POK Output Voltage Low	I_{SINK} = 100µA			0.4	V
I_{POK}	POK Output Leakage Current	0 ≤ V_{POK} ≤ 3.6V, T_{AMB} = +25ºC, V_{OUT} in regulation			1	µA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Thermal Protection						
T_{SHDN}	Thermal Shutdown Temperature			150		ºC
ΔT_{SHDN}	Thermal Shutdown Hysteresis			15		ºC

1. Dropout voltage = V_{IN} - V_{OUT} when V_{OUT} is 100mV < V_{OUT} for V_{IN} = $V_{OUT(NOM)}$ +0.5V (applies only to output voltages ≥ 1.3V).
2. The rise and fall time of the shutdown signal must not exceed 1ms.
3. The delay time is defined as time required to set V_{OUT} to 95% of its final nominal value.
4. Guaranteed by design.
5. The functionality is proven by production test, limits are guaranteed by design.

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics

V_{OUT} = 1.8V, V_{IN} = *2.3V,* I_{OUT} = 1mA, T_{AMB} = +25°C (unless otherwise specified).

Figure 3. Output Voltage vs. Temperature

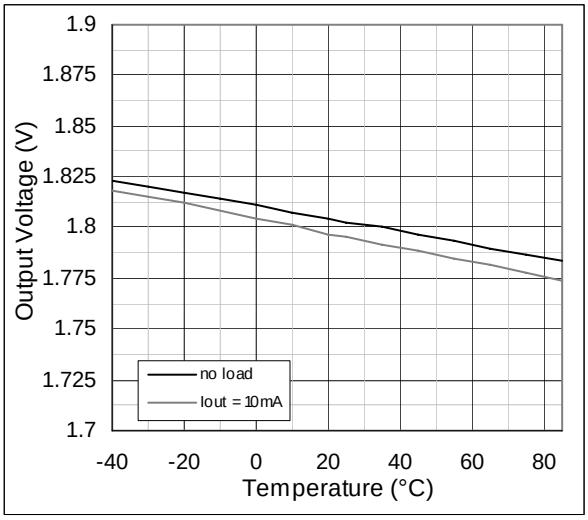


Figure 4. Line Regulation, V_{OUT} vs. V_{IN};

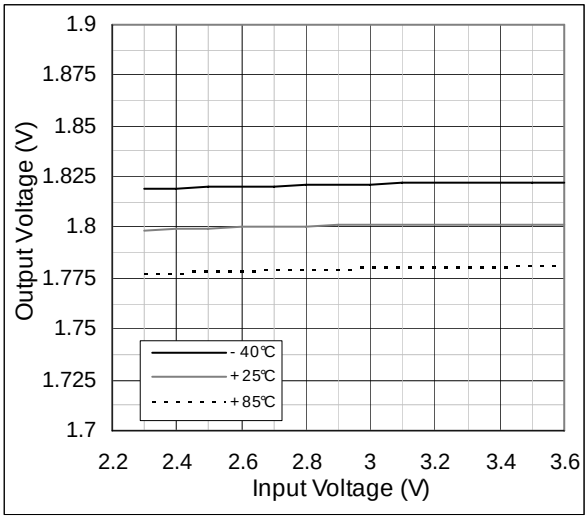


Figure 5. Load Regulation, V_{OUT} vs. I_{OUT};

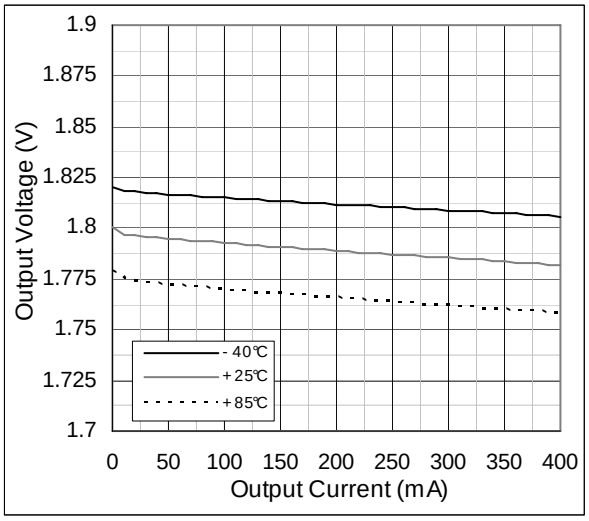


Figure 6. Quiescent Current vs. Input Voltage

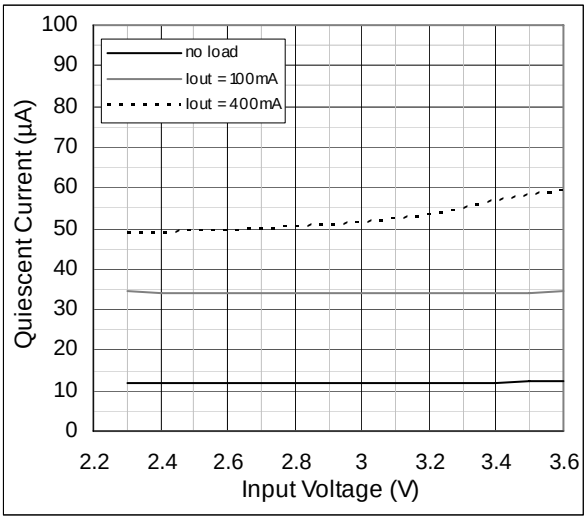


Figure 7. POK Voltage Threshold vs. Temperature

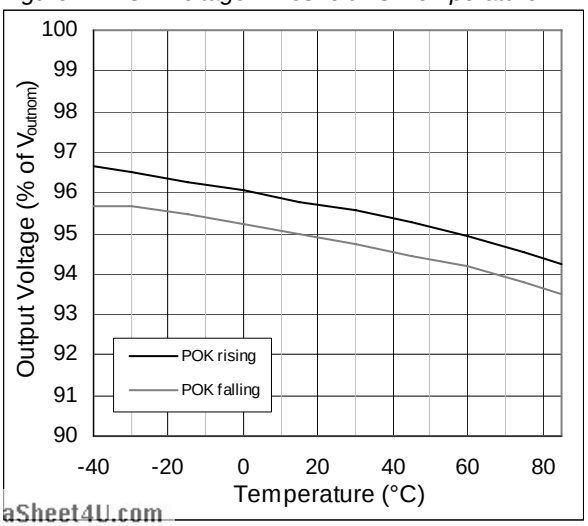


Figure 8. Dropout Voltage vs. Output Current

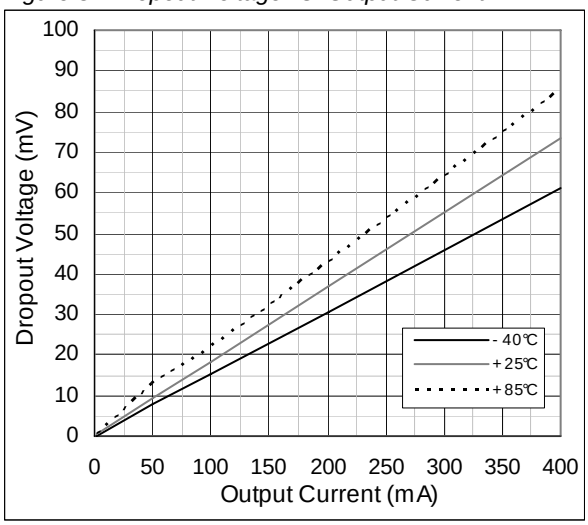


Figure 9. Line Transient Response; V_{IN} = 2.3V to 2.8V, no load

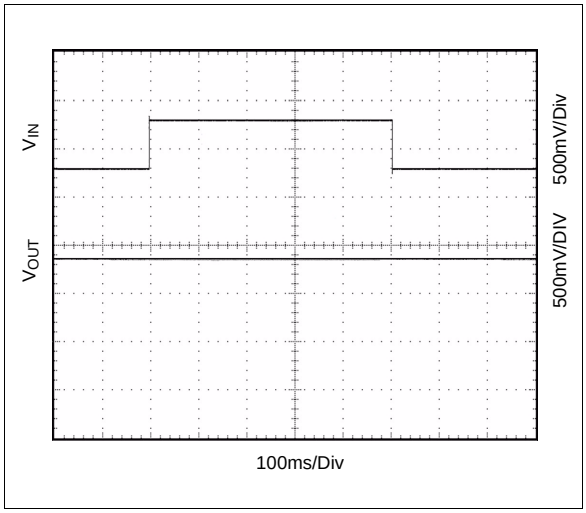


Figure 10. Load Transient Response; I_{OUT} = 0mA to 100mA

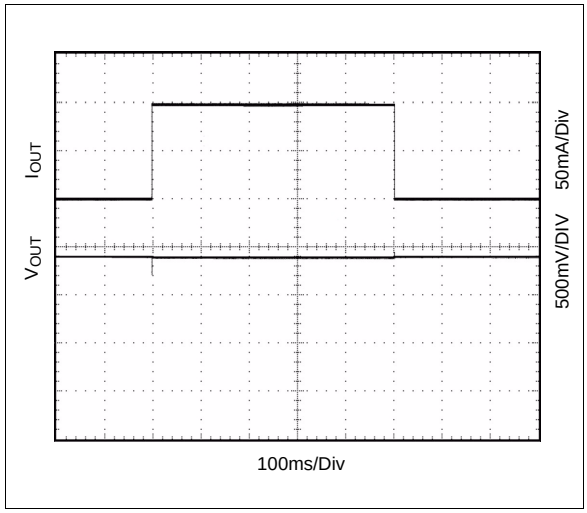


Figure 11. Turn ON

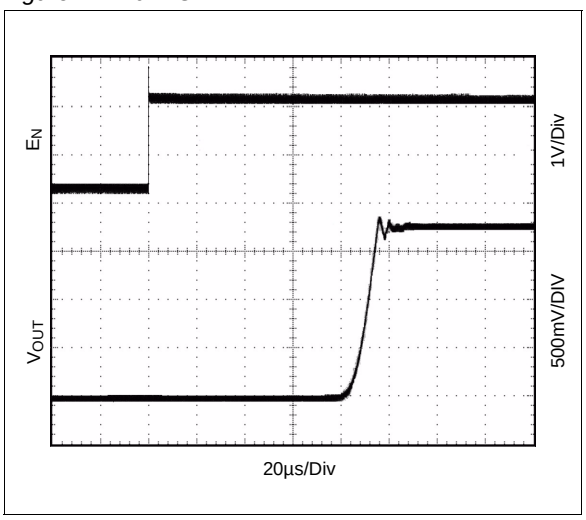
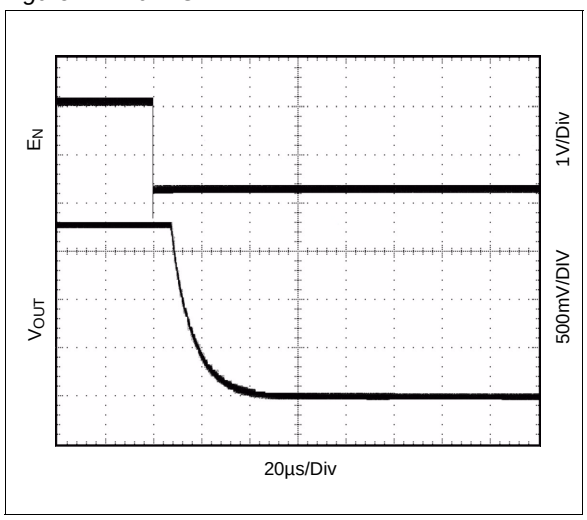


Figure 12. Turn OFF



8 Detailed Description

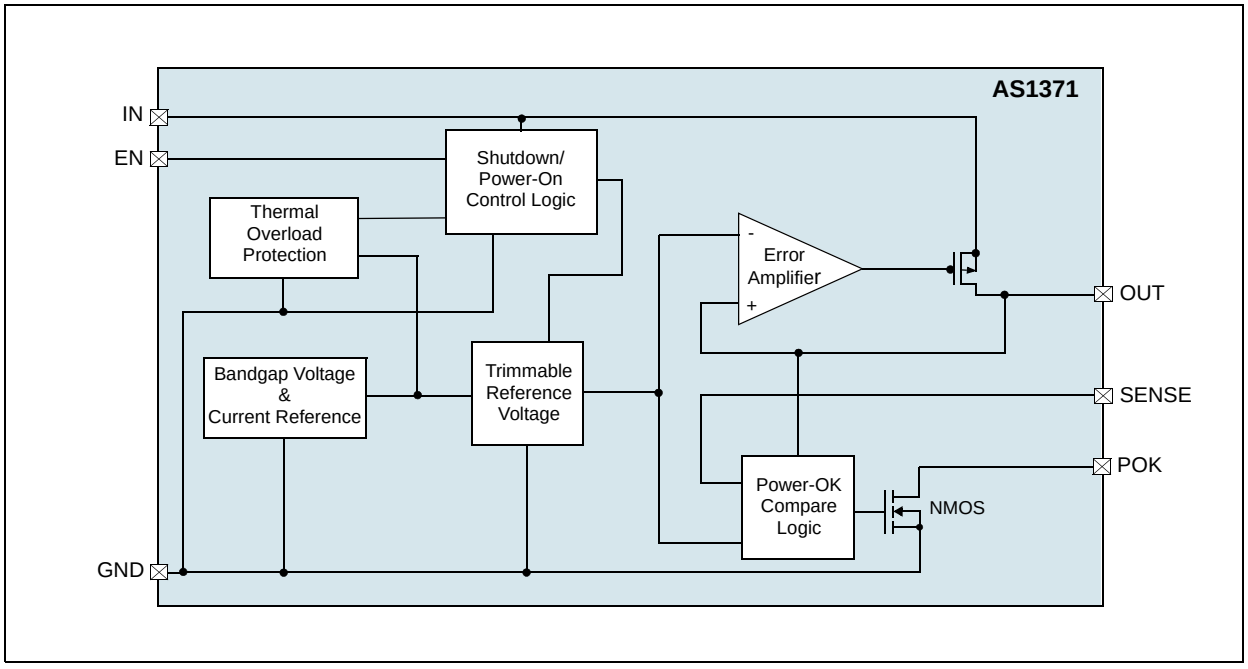
The AS1371 is a low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 400mA. All devices come with fixed output voltage from 0.6V to 3.3V. (see Ordering Information on page 13).

The AS1371 also features a Power-OK output to indicate when the output is within 10% (max) of final value, and also an Enable pin. Shutdown current for the whole regulator is typically 10nA. The device features integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 150°C. This is a useful protection when the device is under sustained short circuit conditions.

As illustrated in Figure 13, the devices comprise voltage reference, error amplifier, P-channel MOSFET pass transistor, Power-OK detect logic, internal voltage divider, current limiter, thermal sensor and shutdown logic.

The bandgap reference is connected to the inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the P-channel MOSFET gate is pulled lower, allowing more current to pass to the output, and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. The output voltage feeds back through an internal resistor voltage divider connected to pin OUT.

Figure 13. AS1371 - Block Diagram



Output Voltages

Standard products are factory-set with output voltages from 0.6V to 3.3V. A two-digit suffix of the part number identifies the nominal output (see Ordering Information on page 13). Non-standard devices are available.

For more information contact: http://www.austriamicrosystems.com/contact-us

Power-OK and Low-Battery-Detect Functionality

The AS1371's power-ok or low-battery-detect circuitry is built around an N-channel MOSFET. The circuitry monitors the voltage on pin SENSE and if the voltage goes out of regulation (e.g. during dropout, current limit or thermal shutdown) the pin POK goes low. The pin SENSE can be connected to a resistive-divider to monitor a particular definable voltage and compare it with an internal voltage reference. If the SENSE pin is connected to GND an internal resistive-divider is activated and connected to the output. Therefore, the Power-OK functionality can be realised with no additional external components.

The Power-OK feature is not active during shutdown and provides a power-on-reset function that can operate down to V_{IN} = 1.2V. A capacitor to GND may be added to generate a power-on-reset delay. To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help to minimize current consumption; a 100kΩ resistor is perfect for most applications (see Figure 1 on page 1).

For the circuit shown in the left of Figure 14 on page 11, the input bias current into SENSE is very low, permitting large-value resistor-divider networks while maintaining accuracy. Place the resistor-divider network as close to the device as possible. Use a defined resistor for R_2 and then calculate R_1 as:

$$R_1 = R_2 \times \left(\frac{V_{IN}}{V_{SENSE}} - 1 \right) \quad \text{(EQ 1)}$$

Where:

V_{SENSE} .... Is the internal sense reference voltage. For values see Table 3 on page 4.

R_2 .... Is the predefined resistor in the resistor divider.

In case of the SENSE pin is connected to GND, an internal resistor-divider network is activated and compares the output voltage with a 94% (typ.) voltage threshold. For this particular Power-OK application, no external resistive components are necessary.

Current Limiting

The AS1371 include current limiting circuitry to protect against short-circuit conditions. The circuitry monitors and controls the gate voltage of the P-channel MOSFET, limiting the output current to 400mA. The P-channel MOSFET output can be shorted to ground for an indefinite period of time without damaging the device.

Thermal-Overload Protection

The devices are protected against thermal runaway conditions by the integrated thermal sensor circuitry. Thermal shutdown is an effective instrument to prevent die overheating since the power transistor is the principle heat source in the device.

If the junction temperature exceeds 150ºC with 15ºC hysteresis, the thermal sensor starts the shutdown logic, at which point the P-channel MOSFET is switched off. After the device temperature has dropped by approximately 15ºC, the thermal sensor will turn the P-channel MOSFET on again. Note that this will be exhibited as a pulsed output under continuous thermal-overload conditions.

Note: The absolute maximum junction-temperature of +150ºC should not be exceeding during continual operation.

Operating Region and Power Dissipation

Maximum power dissipation is determined by the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation of the device is calculated by:

$$P = I_{OUT} \times (V_{IN} - V_{OUT}) \quad \textit{(EQ 2)}$$

Maximum power dissipation is calculated by:

$$P_{MAX} = \frac{T_J - T_{AMB}}{\theta_{JB} + \theta_{JA}} \quad \textit{(EQ 3)}$$

Where:

T_J - T_{AMB} is the temperature difference between the device die junction and the surrounding air.

θ_{JB} is the thermal resistance of the package.

θ_{JA} is the thermal resistance through the circuit board, copper traces, and other materials to the surrounding.

Note: Pin GND is a multi-function pin providing a connection to the system ground and acting as a heat sink. This pin should be connected to the system ground using a large pad or a ground plane.

9 Application Information

Capacitor Selection and Regulator Stability

Ceramic capacitors are highly recommended as they offer distinct advantages over their tantalum and aluminum electrolytic components. For stable operation with load currents up to 400mA over the entire device temperature range, use a 1µF (min) ceramic output capacitor with an ESR <0.2Ω. Use large output capacitor values (e.g. 10µF) to reduce noise and improve load transient-response, stability and power-supply rejection.

Note: Some ceramic capacitors exhibit large capacitance and ESR variations with variations in temperature.

Power Supply Rejection Ratio

The AS1371 is designed to deliver low dropout voltages and low quiescent currents. Power-supply rejection is typically 50dB at 10kHz. To improve power supply-noise rejection and transient response, increase the values of the input and output bypass capacitors, which are shown in Figure 14.

The Section 6 Electrical Characteristics on page 4 show also the device line- and load-transient responses.

Dropout Voltage

For standard products with output voltage greater than the minimum V_{IN} (1.2V), the minimum input-output voltage differential (dropout voltage) determines the lowest usable supply voltage. This determines the useful end-of-life battery voltage in battery-powered systems. The dropout voltage is a function of the P-MOSFET drain-to-source on-resistance multiplied by the load current, and is calculated by:

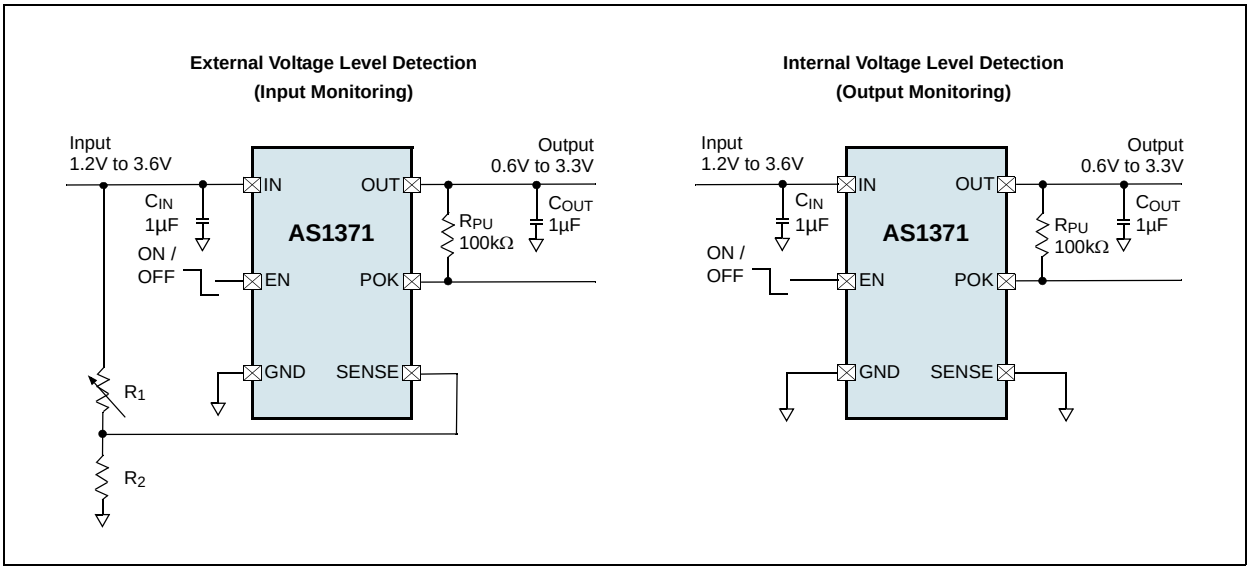
$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT} \quad \textit{(EQ 4)}$$

Where:

$R_{DS(ON)}$ is the drain-to-source on -resistance.

I_{OUT} is the output current.

Figure 14. Application Diagrams



10 Package Drawings and Markings

The device is available in a 6-pin 2x2 TDFN package.

Figure 15. 6-pin 2x2 TDFN package Diagram

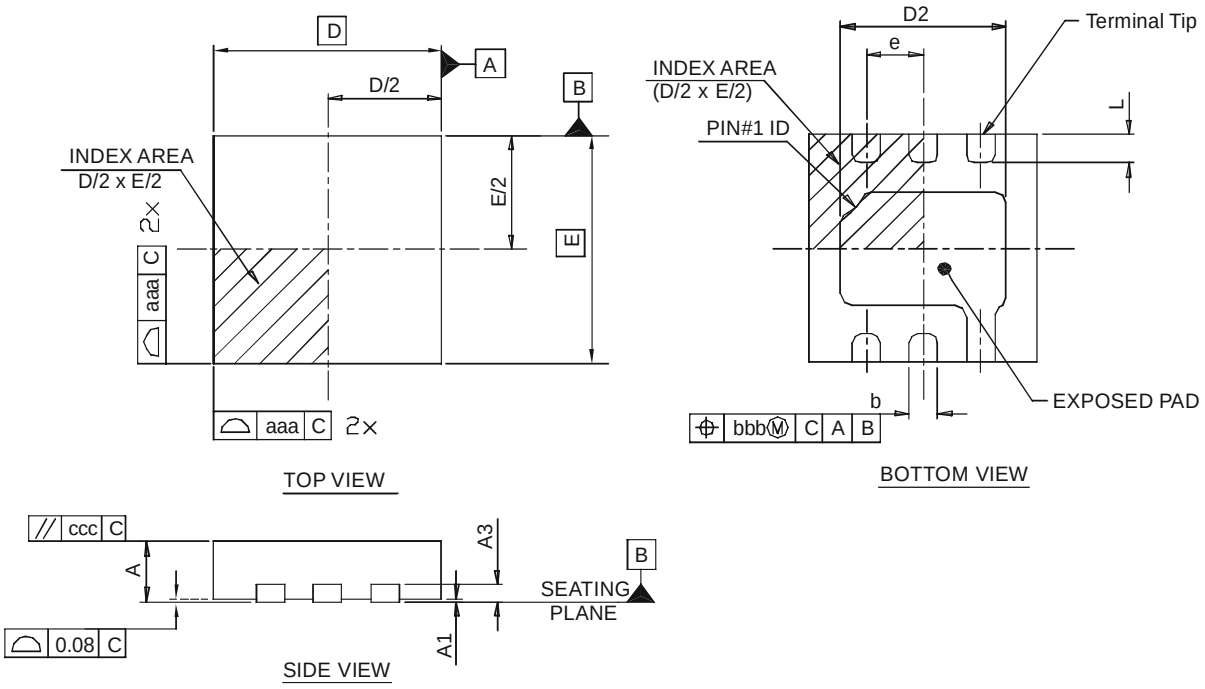


Table 4. 6-pin 2x2 TDFN package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.51	0.55	0.60	D2	1.30	1.45	1.55
A1	0.00	0.02	0.05	E2	0.85	1.00	1.10
A3		0.15 ref		L	0.15	0.25	0.35
aaa		0.15		N		6	
bbb		0.10		ND		3	
ccc		0.10		NE		3	
D	1.95	2.00	2.05	e		0.50	
E	1.95	2.00	2.05	b	0.20	0.25	0.32

Note:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminal.
4. ND and NE refers to the number of terminals on each side respectively.
5. Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the area indicated. The terminal #1 identifier may be either a mold, embedded metal or mark feature.
6. Dimension **b** applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.
7. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

11 Ordering Information

The device is available as the standard products listed in Table 5.

Table 5. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1371-BTDT-105	AT	1.05V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-12*	AM	1.2V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-15*	AN	1.5V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-18*	AO	1.8V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-20*	AP	2.0V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-25*	AQ	2.5V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN
AS1371-BTDT-30*	AR	3.0V	400mA, Low Input Voltage, Low Quiescent Current LDO	Tape and Reel	6-pin 2x2 TDFN

*) on request

Non-standard devices from 0.6V to 3.3V are available in 50mV steps. For more information and inquiries contact http://www.austriamicrosystems.com/contact

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

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